A Discrete-Time Audio ΔΣ Modulator Using Dynamic Amplifier With Speed Enhancement and Flicker Noise Reduction Techniques

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***Abstract*— This article presents a discrete-time second-order ΔΣ modulator for the audio applications. In this modulator, a novel dynamic amplifier is proposed to realize the switched-capacitor (SC) integrators. To eliminate the common-mode (CM) voltage drop in a closed-loop dynamic amplifier during the integration phase, without the use of additional load capacitance, the reset method for the amplifier is modified. Two auxiliary branches are introduced to enhance the settling speed of the integrator. Two different flicker noise reduction techniques (FNRTs) are developed to improve the signal-to-noise-and-distortion ratio (SNDR) (about 2 dB in the audio bandwidth). The prototype modulator is fabricated in 65-nm CMOS technology with a 0.12-mm^2 core area, which achieves a dynamic range (DR) of 91 dB and a peak SNDR of 89.6 dB in the 24-kHz signal bandwidth. It consumes only 49-μW power from a 0.8-V supply, translating into a Schreier figure of merit (FoM) of 176.5 dB.**

***Index Terms*— Delta sigma, dynamic amplifier, flicker noise reduction, integrator, low power, speed enhancement.**

I. Introduction

UBIQUITOUS smart devices have created a continually growing demand for the small-area and energy-efficient electronic systems, as the Internet of Things (IoT) prevails [1]–[3]. In a highly integrated CMOS system-on-chip (SoC), the digital part can achieve a high-speed and low-power performance, benefiting from the ongoing technology scaling. Conversely, the analog design is becoming increasingly challenging due to the reduced voltage headroom and shrunken transistor dimensions. This dilemma is prevalent in the analog-to-digital converters (ADCs).

Manuscript received January 2, 2019; revised May 31, 2019 and August 20, 2019; accepted September 7, 2019. This article was approved by Associate Editor Jeffrey Gealow. This work was supported in part by the National Key Research and Development Program of China under Grant 2016YFA0202200, in part by the Major Projects of the Ministry Science and Technology of China under Grant 2016ZX03001002-002, in part by the Beijing Municipal Science and Technology Project under Grant Z181100008918009, in part by the Youth Innovation Promotion Association Program, Chinese Academy of Sciences, under Grant 2016107, and in part by the National Natural Science Foundation of China under Grant 61874107. *(Corresponding author: Liyuan Liu.)*

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Digital Object Identifier 10.1109/JSSC.2019.2941540

Delta–sigma modulator (DSM)-based ADCs dominate the low-bandwidth signal acquisition applications, where high resolution is pursued. During the past several years, a very few innovations on discrete-time (DT) modulators have been reported on the top-class publications compared with their continuous-time (CT) counterparts [4]–[7]. However, switched-capacitor (SC) circuits have better tolerances for voltage and process variations and clock jitters [8]. Moreover, they are more compatible with the digital-oriented manufacturing, which implies the potential to regain the attention from the designer community. In conventional DT DSMs, most of the power is typically dissipated by the operational transconductance amplifier (OTA)-based integrators. This has led toward efforts to improve the SC integrators' energy efficiency. For example, comparator-based-SC circuits and an inverter-based integrator were presented in [9] and [10], respectively. Much earlier, a passive integrator proposed in [11] saved power significantly at the expense of a degradation in performance.

Devices with time-varying operating conditions can be utilized to devise dynamic circuits that can save power. For instance, to avoid the static power consumption, a dynamic amplifier was applied to achieve the sensing amplification in memory readout circuits [12]; moreover, it was used in a dynamic comparator as a preamplifier to improve the noise performance [13].

In this article, we present a novel integrator based on a dynamic amplifier. We eliminate the additional large capacitance load through the dedicated timing design. Two auxiliary branches are added to speed up the settling of the integrator, which can meanwhile maintain the common-mode (CM) characteristic. Furthermore, two flicker noise reduction techniques (FNRTs) are developed to improve the signal-to-noise-and-distortion ratio (SNDR). A single-loop second-order DT DSM is designed, employing the cascade-of-integrators feedforward (CIFF) topology with a 4-bit asynchronous SAR quantizer. Feedforward paths and a multi-bit quantizer can ensure that the integrators only process the small quantization noise, which can relax their design. The fabricated prototype achieves a peak SNDR of 89.6 dB and a dynamic range (DR) of 91 dB in the 24-kHz signal bandwidth and consumes 49 μW of power from the 0.8-V supply with an active area of 0.12 mm^2.

The remainder of this article is organized as follows. Section II reviews the use of dynamic amplifiers in ADCs.

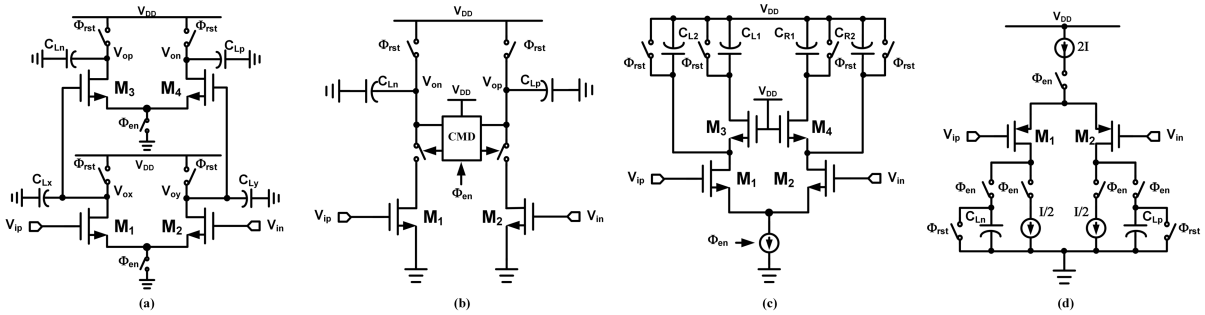

Fig. 1. Several implementations of dynamic amplifiers from previous studies. (a) Two-stage amplifier in [14]. (b) Amplifier with a CM detector in [15]. (c) Stacking amplifier in [16]. (d) Gain-boosting amplifier using two additional paths in [20].

Section III discusses the design of a dynamic amplifier-based integrator. The implementation details of the prototype DSM are provided in Section IV, followed by the measurement results in Section V. Finally, Section VI concludes this article.

II. Review of the Dynamic Amplifiers in ADCs

A dynamic amplifier can be used as an inter-stage block in a pipelined ADC in accordance with supply voltage scaling [14]–[18] or as a low-power OTA in the oversampling SARs [19], [20]. Fig. 1 shows several designs of dynamic amplifiers from the previous studies. A charge-steering amplifier was identified in [14], transformed from traditional current-steering ones. In this case, a two-stage configuration was applied to obtain a steady output voltage. Differently, [15] used a CM detector to realize this in a single-stage way. Voltage gain boosting was achieved by using a stacking structure in [16] and two additional paths in [20], respectively. Furthermore, linearity enhancement and PVT stabilization techniques for dynamic amplifiers were presented in [17]–[19].

Fig. 1(b) can be used to compute the small-signal voltage gain of a dynamic amplifier. For simplicity, the transconductance and output resistance are modeled using their average values $g_{m1,2}$ and $r_{o1,2}$ under a varying MOS drain voltage. Easily, the gain can be derived as

$$\text{Gain} = g_{m1,2} r_{o1,2} (1 - e^{-t/\tau}) \tag{1}$$

where $\tau = r_{o1,2} C_{Lp,n}$, denotes the time constant of this single-pole system. Equation (1) can be approximated into two different forms when two different conditions are of interest

$$\text{Gain} \approx \frac{g_{m1,2}}{C_{Lp,n}} t, \quad \text{for } t \ll \tau \tag{2}$$

and

$$\text{Gain} \approx g_{m1,2} r_{o1,2}, \quad \text{for } t \gg \tau. \tag{3}$$

Note that (1)–(3) reveal the dynamic nature of this kind of amplifier. Initially, the voltage gain linearly evolves with time based on (2); then, it complies with the exponential law in (1) and eventually reaches its final value in (3). The dynamic property can also be interpreted from the perspective of power consumption.

During the amplification phase, the CM output voltage declines from $V_{\rm DD}$, and its terminated value can be set at half of $V_{\rm DD}$ to obtain a wide swing. Assuming that reset and amplification divide the whole period equally, the power consumption of a dynamic amplifier can be expressed as

$$\begin{aligned} P_{dy} &= 2 \cdot V_{\rm DD} \overline{I_D} = 2 \cdot V_{\rm DD} \cdot \frac{1}{2} V_{\rm DD} \cdot C_{Ln,p} \cdot \frac{1}{T} \\ &= \frac{1}{2} {V_{\rm DD}}^2 C_{\rm tot} \cdot f \end{aligned} \tag{4}$$

where $C_{\rm tot} = C_{L,p} + C_{L,n}$. Hence, a dynamic amplifier's power consumption can be translated into a digital circuit with the same capacitor load size under an activation factor of 1/2.

When used in high-speed pipelined ADCs, a dynamic amplifier is often configured in an open-loop form, behaving like a voltage integrator during a short integration time interval as (2) indicates. Therefore, the voltage gain is typically limited to below 10. In fact, the SCs serve as dynamic resistors valued at $(C_L f)^{-1}$, which will also lead to (2).

III. Proposed Integrator Based on a Dynamic Amplifier

According to (3), when used in low-speed applications, a dynamic amplifier would exhibit a commensurate voltage gain to a conventional one. The difference is that a dynamic amplifier has a varying CM output voltage instead of a constant value in the conventional amplifiers. Actually, a dynamic amplifier can produce normal amplification as long as the terminated value of the CM output voltage is not as low as to cause the input MOSFETs to enter the linear regions.

A. Eliminating the Additional Capacitor Load

A dynamic amplifier's inherent DT property indicates its compatibility with SC circuits. Fig. 2(a) shows a parasitic-insensitive integrator incorporating a dynamic amplifier with a switched current tail clocked by $\Phi_{\rm en}$. Its timing diagram is shown in Fig. 2(b). During Φ_1, $C_{Sp,n}$ samples the input voltage, and the current tail is left open. When the reset signal $\Phi_{\rm rst}$ goes high, $V_{\rm op}$ and $V_{\rm ON}$ are pulled to $V_{\rm DD}$. Note that the enable signal $\Phi_{\rm en}$ coincides with the transferring clock Φ_2. When they turn high, the tail source begins to sink current from M1 and M2, causing the output nodes rolling from $V_{\rm DD}$. Meanwhile, the sampled charge is transferred into the integrating capacitors due to the establishment of feedback.

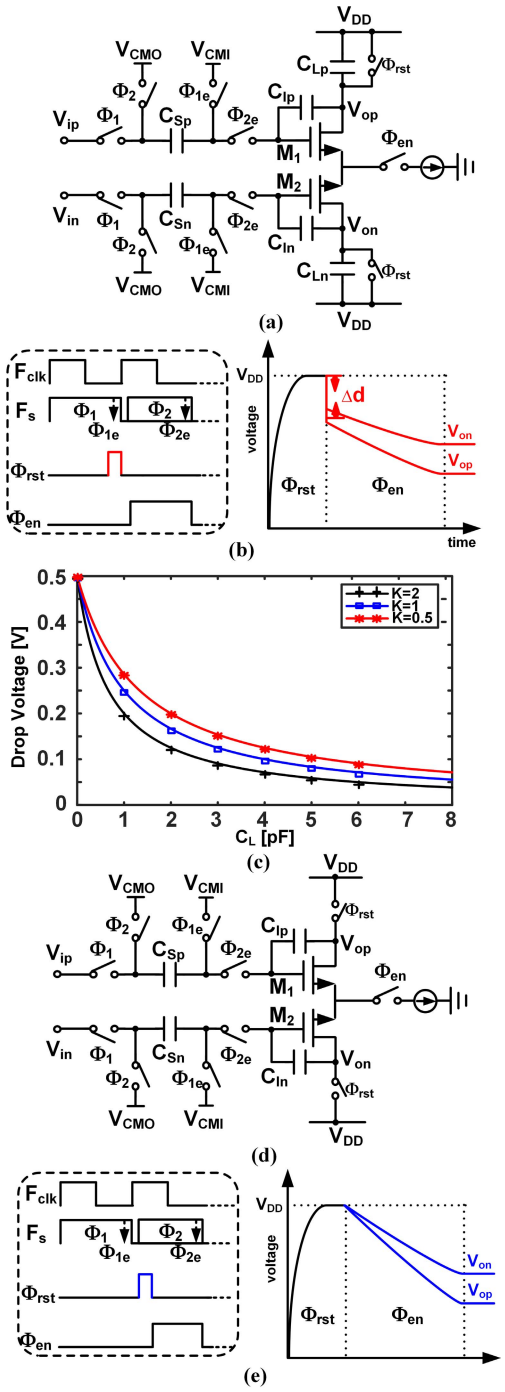

Fig. 2. SC integrators based on dynamic amplifiers with two different timing methods. (a) Schematic of an SC integrator with the additional capacitor load. (b) Timing method presented in [14] and [21] and associated CM voltage drop effect. (c) Simulated results versus expression (5). (d) Proposed integrator. (e) Modified timing method and the corresponding sketch map of the output voltage.

As shown in Fig. 2(b) and adopted in [14] and [21], the reset is arranged within the sampling phase. Unfortunately, in this case, the integrator would undergo an adverse phenomenon that we refer to as the CM voltage drop effect. It is illustrated in the right half of Fig. 2(b). The drop in voltage reduces the amplifier's output swing range available. If severe enough, the input MOS pairs would be brought out of the active regions, which are detrimental to the linearity, consequently, giving rise to unwanted distortions in the signal bandwidth.

Charge sharing accounts for the voltage drop effect. Based on the aforementioned working principle, the sampling capacitor $C_{Sp,n}$, integrating capacitor $C_{Ip,n}$, and load capacitor $C_{Lp,n}$ are serially connected between V_{CMO} and V_{DD} during Φ_2. At the beginning of this phase, charge sharing occurs, thus causing a CM voltage drop tagged by Δ_d

$$\Delta_d = \frac{C_{Sp,n} \cdot [(V_{\mathrm{DD}} - V_{\mathrm{CMI}}) + (V_{\mathrm{CM,in}} - V_{\mathrm{CMO}})]}{C_{Sp,n} + (K+1)C_{Lp,n}} \tag{5}$$

where $V_{\mathrm{CM,in}}$ denotes the CM input voltage and K is the integrator coefficient $C_{Sp,n}/C_{Ip,n}$. This equation excludes the parasitic capacitances on the gates and drains of the MOS pairs for conciseness. Generally, this simplification can be justified because large capacitors are often used in DSMs to reduce the thermal noise level. Besides, we suppose an initial voltage of zero across $C_{Ip,n}$ in (5). Assuming $V_{\mathrm{CM,in}}$, V_{CMI}, and V_{CMO} are all of $V_{\mathrm{DD}}/2$ and K is 1, $C_{Lp,n}$ should be chosen larger than $2C_{Sp,n}$ to ensure the dropped voltage below $0.1V_{\mathrm{DD}}$, as suggested in [21]. This implies that the one-side equivalent capacitance load would be increased from $1/2C_{Sp,n}$ to $5/2C_{Sp,n}$, which can cause a $4\times$ power waste according to (4). Fig. 2(c) shows the agreement of the simulated results with formula (5) under different K values. In this simulation, a 1-V supply and a 2-pF $C_{Sp,n}$ are chosen.

The voltage drop effect results in the unreasonable increase of $C_{Lp,n}$ to suppress the nonlinearity of a dynamic amplifier, which can cause a remarkable waste of power inevitably. To realize a low-power design, the additional large $C_{Lp,n}$ is eliminated in our proposed integrator shown in Fig. 2(d), for which we used the rearranged timing strategy demonstrated in Fig. 2(e). In this approach, the reset is contained within the transferring phase; that is, when Φ_2 and Φ_{rst} arrive, $C_{Sp,n}$ and $C_{Ip,n}$ are connected together with a constant output voltage (i.e., V_{DD}). To this end, the voltage drop can be circumvented because charge sharing occurs without affecting the output voltage but drawing some charge from the supply. Accordingly, there is no significant immediate CM voltage drop at the start of the enable phase in Fig. 2(e). Therefore, the output voltage can evolve from V_{DD} instead of a decreased value.

The proposed timing method works well because two basic principles of an SC integrator still hold: the charge conservation on high-resistance nodes (here are gates of MOS pairs) and the existence of feedback to force the charge to redistribute between different capacitors. In this article, we choose a switched current tail rather than a capacitor or a direct switch used in previous dynamic amplifiers. First, this can avoid the sensitivity of transconductance to the input CM level. Second, a fixed tail current can help to define the output CM voltage, which is important for the succeeding stage.

It is meaningful to assess the proposed dynamic amplifier-based integrator by comparing it with those based on switched-opamp, such as in [22] and [23]. While both integrators rely on powering down the amplifier during one of the two non-overlapping phases to save power, the proposed structure

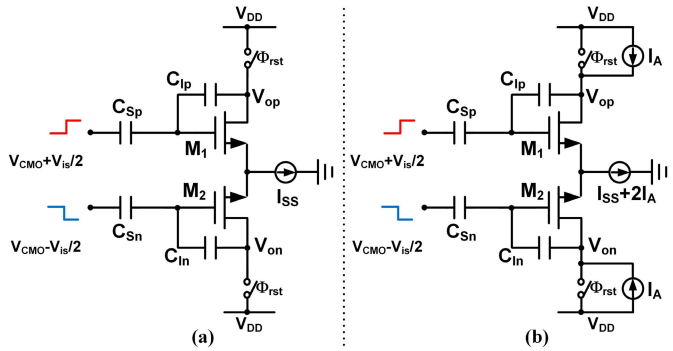

Fig. 3. Proposed dynamic amplifier during the transferring phase. (a) Without speeding up. (b) With the proposed speed enhancement branches.

has certain advantages. First, in a dynamic amplifier, there is no PMOS current source load and the corresponding CMFB circuits as in a normal differential amplifier, which can favor both the noise and power performance. Furthermore, the elimination of PMOS load makes a dynamic amplifier more suitable for a low-voltage supply. Interestingly, the amplifier's voltage gain also can be increased by about two times to reach the intrinsic level of an NMOS. In addition, under the aid of reset mechanism, the drains of the input pairs would not converge to ground when they are powered down, which is beneficial for a faster recovery from the off region.

B. Common and Differential Mode Decoupling

Fig. 3(a) shows the proposed SC integrator during the transferring stage with a step voltage input. Its differential mode (DM) small-signal analysis leads to

$$V_O \approx V_{O,\text{init}} + V_{\text{is}} \cdot \frac{C_{S_{p,n}}}{C_{I_{p,n}}} \left(1 - \frac{1}{A_0 \beta}\right) \cdot (1 - e^{-t/\tau_c}) \quad (6)$$

where $\beta = C_{Ip,n}/(C_{Ip,n} + C_{Sp,n})$ denotes the feedback factor and $V_{O,\text{init}}$ denotes the initial differential voltage across $C_{Ip,n}$. A_0 can be expressed by (3), and τ_c denotes the time constant of this closed-loop circuit

$$\tau_c = \frac{1}{\beta \cdot \text{GBW}} = \frac{C_{\text{eq}}}{\beta \cdot g_{m1,2}} \quad (7)$$

where C_{eq} is the equivalent capacitance load

$$C_{\text{eq}} = \frac{C_{S_{p,n}} \cdot C_{I_{p,n}}}{C_{I_{p,n}} + C_{S_{p,n}}} \quad (8)$$

and

$$g_{m1,2} = \frac{I_{\text{SS}}}{V_{\text{OV}}} \quad (9)$$

where V_{OV} denotes the overdrive voltage of input pairs. According to (6), the accuracy loss of an SC integrator comprises two parts: the gain and settling errors. In this sense, (6) can be rewritten as

$$V_O = V_{O,\text{init}} + V_{is} \cdot \frac{C_{S_{p,n}}}{C_{I_{p,n}}} (1 - \varepsilon_{\text{gain}}) \cdot (1 - \varepsilon_{\text{settle}}) \quad (10)$$

where $\varepsilon_{\text{gain}}$ and $\varepsilon_{\text{settle}}$ represent the gain and settling error, respectively. The gain error comes from the finite voltage gain, while the settling error exists due to the finite bandwidth.

Assume a large enough voltage gain of the amplifier in an integrator. To reach the N-bit settling accuracy during the transferring stage with a period of Δ_T, the settling error should satisfy

$$\varepsilon_{\text{settle}} = e^{-\Delta_T/\tau_c} < 2^{-(N+1)} \quad (11)$$

that is

$$\frac{\Delta_T}{\tau_c} > (N+1) \ln 2. \quad (12)$$

For instance, if $N = 15$, (12) requires $\Delta_T > 11\tau_c$, which can be realized by increasing the tail current to reduce τ_c according to (7) and (9) for a conventional amplifier. Its CM output voltage can be defined by the CMFB circuits at a constant value irrespective of I_{SS}. However, the CM output voltage of a dynamic amplifier is determined by the sinking current plus a certain time period; hence, I_{SS} cannot be arbitrarily increased. In this regime, the DM settling behavior couples with the CM output voltage. This phenomenon can be referred to as the CM-DM coupling effect of a dynamic amplifier.

The decrease of the CM output voltage during a time period Δ_T can be represented as

$$\Delta_{\text{VCM}} = \frac{I_{\text{SS}} \cdot \Delta_T}{2C_{\text{eq}}}. \quad (13)$$

Combining with (7) and (9), we can obtain

$$\frac{\Delta_T}{\tau_c} = 2\beta \frac{\Delta_{\text{VCM}}}{V_{\text{OV}}}. \quad (14)$$

In high-precision DSMs, capacitors are always sized by the thermal noise level, while I_{SS} (and hence $g_{m1,2}$) would be confined by Δ_{VCM} according to (13) and eventually by the supply voltage. This coupling effect determines the settling accuracy limit for a dynamic amplifier-based integrator under a certain supply. Considering a 1-V supply, if $\beta = 1/2$, $V_{\text{OV}} = 0.1$ V, and $\Delta_{\text{VCM}} = 0.5$ V, we have $\Delta_T = 5\tau_c$, which is insufficient for a 15-bit settling accuracy. This issue of incomplete settling would become more severe under a lower voltage supply.

The CM-DM coupling effect can be addressed using the proposed method, as shown in Fig. 3(b). Two speed enhancement branches I_A are added between V_{DD} and the output nodes, and the tail current is increased by $2I_A$. Hence, $g_{m1,2}$ turns into

$$(g_{m1,2})_A = \frac{I_{\text{SS}} + 2I_A}{V_{\text{OV}}}. \quad (15)$$

Therefore, one additional degree of freedom is achieved. This allows independently increasing the transconductance to enhance the settling of the integrator without affecting its CM characteristic since the equivalent sinking current, I_{SS}, remains the same as Fig. 3(a). Now, the ratio in (14) is increased to

$$\left(\frac{\Delta_T}{\tau_c}\right)_A = 2\beta \frac{\Delta_{\text{VCM}}}{V_{\text{OV}}} \left(1 + \frac{2I_A}{I_{\text{SS}}}\right). \quad (16)$$

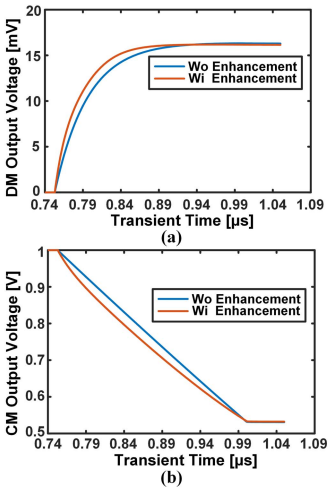

Fig. 4. Integrator's settling behaviors with and without proposed accelerating method under a step input. (a) DM settling. (b) CM settling.

Fig. 4 shows the DM settling improvement effect of this method by transient simulation with $\beta = 1/2$. The terminated CM output voltages show no difference between two cases. Note that the inserted I_A can decrease the dc voltage gain of the amplifier because of the finite output resistance of the inserted current source, and the gain decline would impede the integrator's performance in return. To mitigate this issue, the speedup branches can be added to the cascode structure, which will be explicitly elaborated in Section IV-A.

C. Thermal Noise Analysis and Flicker Noise Reduction

Performing the exhaustive noise analysis for dynamic circuits is difficult due to their large signal behaviors, for which device parameters vary with time. This varying nature precludes the use of ordinary steady-state analysis that is performed for the linear time-invariant systems. In fact, the noise process in a periodically ON-and-OFF switched circuit is cyclostationary [24]; moreover, it is more convenient to exploit it in the time domain [25], [26]. To explore the thermal noise effect in SC circuits, a design-oriented estimation was provided in [27].

In this article, the developed SC integrator has three working phases: sampling, reset, and transferring. During the sampling stage, thermal noise of sampling switches is the well-known KT/C noise; its effect can be estimated using [27, eq. (18)]

$$\overline{V^2_{\text{ni,sam(sw)}}} = \frac{kT}{C_{S_{p,n}}}. \tag{17}$$

During the transferring phase, the thermal noise attributed by the transferring switches [controlled by $\phi_{2(e)}$ in Fig. 2(d)] can be computed in [27, eq. (21)]. The following noise calculation assumes a sufficiently small switch conducting resistance R_{ON} (hence, $x = g_{m1,2}R_{\text{ON}}$ in [27, eq. (21)] approaches 0), which is often realized by a designer in practice. Hence, the noise of transferring switches can be obtained

$$\overline{V^2_{\text{ni,tra(sw)}}} = \frac{kT}{C_{S_{p,n}}}\left(\frac{x}{1+x}\right) \approx 0. \tag{18}$$

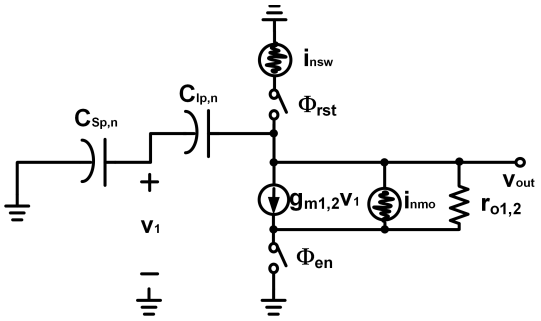

Fig. 5. Thermal noise analysis for the integrator during the reset and transferring phases.

Fig. 5 is used to explore thermal noise during the reset and transferring phases. In the reset stage, the noise of the reset switch represented as i_{nsw} introduces an initial KT/C noise across the capacitor load. Thereafter, this initial value would decay with time due to the finite output resistance [14]

$$\overline{V^2_{\text{no,rst(sw)}}} = \frac{kT}{C_{\text{eq}}}\text{e}^{-2t/\tau_0} \tag{19}$$

where C_{eq} fits (8), τ_0 equals $R_{\text{eq}}C_{\text{eq}}$, and R_{eq} denotes the equivalent output resistance

$$\frac{1}{R_{\text{eq}}} = \frac{1}{r_{o1,2}} + \beta g_{m1,2}. \tag{20}$$

During the transferring phase, the noise of the input pairs, denoted by i_{nmo}, performs its dynamic settling as

$$\overline{V^2_{\text{no,tra(mos)}}} = \frac{2kT\gamma\, g_{m1,2}R_{\text{eq}}}{C_{\text{eq}}}(1-\text{e}^{-2t/\tau_0}) \tag{21}$$

where the noise current of an MOSFET is considered with a one-side spectrum $4\text{kT}\gamma\, g_{m1,2}$ and γ is a technology coefficient.

The complete input-referred thermal noise voltage of the integrator based on a dynamic amplifier can be derived as

$$\overline{V^2_{\text{ni,tot}}} = \overline{V^2_{\text{ni,sam(sw)}}} + \overline{V^2_{\text{ni,tra(sw)}}} + \beta^2 \cdot \left(\overline{V^2_{\text{no,rst(sw)}}} + \overline{V^2_{\text{no,tra(mos)}}}\right). \tag{22}$$

Equations (17)–(22) can be used to compare the thermal noise of a dynamic amplifier-based integrator with a conventional one. The sampling thermal noise has no difference. MOSFETs and the reset noise exhibit an exponential evolution feature. In an actual low-speed case, MOSFET's noise can reach its ultimate value and the reset noise decays to zero via a sufficiently long time period. Finally, a multiplying factor $2\times$ should be included for a differential implementation.

As far as flicker noise is concerned, while some methods are documented in the previous literatures, such as [26] and [28], it is still problematic to obtain a closed-form formula that is not very tedious for design. Generally, chopper stabilization (CHS) is used in DSMs to remove the flicker noise. Unfortunately, it was still visible in the measured output spectrum of our previous work, as shown in [21, Fig. 8] although CHS was already applied.

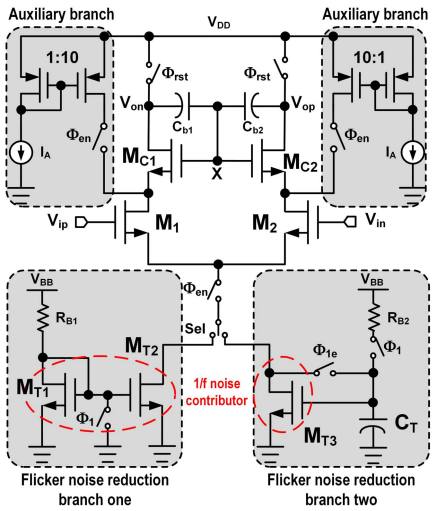

Fig. 6. Proposed dynamic amplifier.

For a conventional OTA-based integrator, only the flicker noise of the input MOS pairs is considered. The tail current source is excluded unhesitatingly because of the high CMRR of a differential structure. However, it is different for an integrator using a dynamic amplifier. Because of the reset mechanism, the input pairs are imbalanced during the transferring phase, i.e., when $\Phi_{\rm rst}$ comes, the accumulated charge on the integrating capacitor causes a differential voltage on the gates of the input pairs. The additional noise effect due to this disparity is estimated in [29] as

$$\Delta I_{D1} - \Delta I_{D2} = g_{m0}\left(1 + \frac{I_n}{2I_{\rm SS}}\right)\Delta V_g \tag{23}$$

where g_{m0} denotes the transconductance of a noiseless MOSFET, I_n denotes the noise current of the tail source $I_{\rm SS}$, and ΔV_g denotes the imbalanced differential voltage at the input pairs. In this, the flicker noise of the tail MOSFET can appear at the output nodes. Hence, it should be treated deliberately.

We implemented two techniques in this article to reduce $1/f$ noise of the tail, as shown in Fig. 6. The first branch uses the switching method presented in [30]. The dc voltage generated by R_{B1} and M_{T1} only needs to be accessible during Φ_2; hence, M_{T1} is switched into the cutoff region during Φ_1. The second branch utilizes an auto-zeroing technique that is commonly used in SC circuits. During Φ_1, M_{T3} is configured in the diode mode and the dc biasing voltage along with the equivalent $1/f$ noise voltage is sampled by C_T. During the following transferring phase, the held voltage across C_T generates the tail current in M_{T3}, and the flicker noise is cancelled because of its low-frequency nature. In Section V, measurement results for our proposed FNRTs can be found.

IV. Prototype Implementation

A. Schematic of the Proposed Dynamic Amplifier

Fig. 6 shows the overall design of our proposed dynamic amplifier. To boost the voltage gain, a cascode structure is adopted (40 dB is achieved in this design). Because the drain voltage varies from $V_{\rm DD}$ to $V_{\rm DD}/2$, it is more appropriate to bias M_{C1} and M_{C2} dynamically, preventing them from entering the linear regions. For this purpose, a bootstrapped voltage can be generated from the common sources of M_1 and M_2 by using a diode-connected NMOS. Briefly, this article uses two small mimcaps C_{b1} and C_{b2} (with the value of 250 and 100 fF in the first- and second-stage integrators, respectively). M_{C1} and M_{C2} are realized by low-threshold transistors and they have tens of nano-amperes drain–gate leakage currents when their drain–gate voltages are $V_{\rm DD}$. If X has an initial voltage of 0, M_{C1} and M_{C2} will be in the cutoff regions. When $V_{\rm op}$ and $V_{\rm ON}$ are reset to $V_{\rm DD}$, the drain–gate leakage currents of $M_{C1,2}$ will charge X slowly to open $M_{C1,2}$, and hence, the output nodes can be pulled down. Thereafter, X can be lifted near to $V_{\rm DD}$ at the very beginning of $\phi_{\rm rst}$, while $V_{\rm op}$ and $V_{\rm ON}$ are reset due to the much smaller parasitic capacitance on it compared with $C_{b1,2}$.

Two speed-enhancing branches are introduced to address the CM-DM coupling effect described in Section III-B. By inserting them at a low-impedance node, their impact on the voltage gain could be neglected. Moreover, to save the power of auxiliary branches, the current mirror is designed with a $10\times$ gain. When the proposed dynamic amplifier is used in a DSM, the equivalent capacitance is often of several picofarads. Even though the introduction of the speed-up branches will increase the parasitic capacitances on the cascode nodes, they are far less than the load capacitor yet. And hence, the accelerating branches will not cause the issue of stability, and the amplifier can still behave as a single-pole system.

We develop two different tail branches to perform the flicker noise reduction, while a control signal *Sel* is used for the selection. In the first branch, M_{T1} is cycled between the strong-inversion and cutoff regions, which can reduce flicker noise from its physical root. In the other branch, C_T (realized by PMOS) is used to store the dc biasing and flicker noise voltage, and its value is big enough (about 8 pF) to ensure a low-level KT/C noise stemming from its sampling mechanism. Moreover, an earlier version of Φ_1 is used to mitigate the charge-injection effect of the two switches in the second branch. Interestingly, the added speed-up branches are also favorable to the flicker noise reduction according to (23) because the tail current is increased by $2I_A$.

It is useful to point out that the reset noise on the load capacitance (including C_{b1} and C_{b2}) would decay toward zero by the law of (19), which can hardly have an impact on the integrator characteristics. Besides, when the imbalance in the circuit is considered, the low-frequency components of such KT/C noise can be chopped out, as they can be equivalent to the input offset.

B. Architecture and Circuit Descriptions of the Designed DSM

To verify the proposed integrator, we have designed a single-loop second-order SC DSM. Fig. 7 shows its circuit details and timing diagram. Coefficients of the DSM are taken from [21], achieving an excellent and a robust NTF.

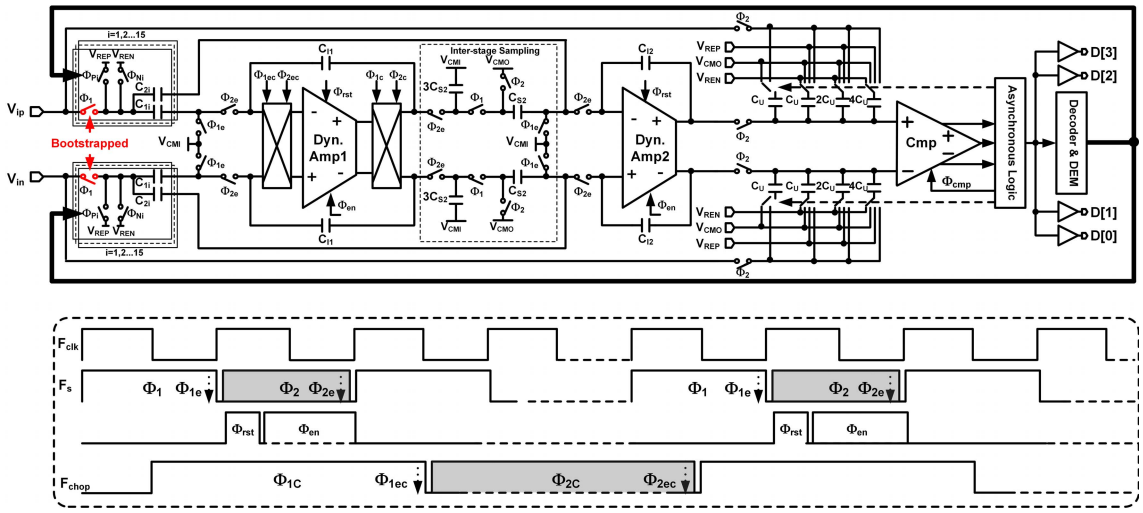

Fig. 7. Schematic details and timing diagram of this design.

This design simplifies the five-bit asynchronous SAR quantizier in [21] into a four-bit one to cut down the digital part power, which is ensured by the realization of a higher voltage gain of the proposed dynamic amplifier. To achieve signal summing, a low-power passive method from [31] that can avoid signal attenuation is used. Moreover, sampling switches are locally bootstrapped to improve the linearity. For the same purpose, a simple multi-bit dynamic element matching (DEM) algorithm is adopted to alleviate mismatches among the sampling capacitor units. CHS technique is used in the first-stage integrator to improve its low-frequency performance, and the chopping frequency is set at a half of the sampling frequency according to [32]. The inter-stage passive sampling network is marked by the dashed line in Fig. 7. During the sampling phase (Φ_1 for both integrators), the dynamic amplifier in the first-stage integrator is disabled, and sampling of the next stage is achieved by charge sharing over the passive capacitor network. Meanwhile, charge sharing is utilized to achieve the integrating coefficient (3/4) of the second stage. The comparator in the SAR is based on the widely used double-tail structure in ADCs [13].

The first-stage integrator is designed with the sampling capacitance of around 7.92 pF (the sum of C_{1i}, $i = 1, 2 \times 15$) and the integrating capacitance of 12.29 pF (the value of C_{I1}). C_{S2} and C_{I2} in the second-stage integrator are both relaxed to 0.27 pF under the help of a high gain of the first stage. The value of the feedback capacitor of the second-stage integrator is around 0.23 pF (the sum of C_{2i}, $i = 1, 2, \ldots, 15$). The unit capacitor in the SAR is implemented by mom capacitance with the value of 5.5 fF. The sampling frequency of this design is chosen to be 3.072 MHz to obtain a 64× oversampling ratio (OSR) for a 24-kHz signal bandwidth.

Finally, (17)–(22) can be used to calculate the expected in-band thermal noise. Assuming a large enough loop gain (i.e., $\beta g_{m1,2} r_{o1,2} \gg 1$), R_{eq} in (20) approximates $1/\beta g_{m1,2}$. Hence, the upper limit of the in-band thermal noise expressed by (22) is

$$\overline{V_{n,\text{th(in-band)}}^2} = \frac{2}{\text{OSR}} \frac{kT}{C_{S_{p,n}}} (1 + 2\gamma). \tag{24}$$

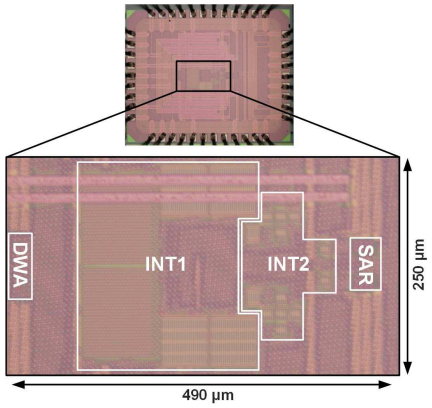

Fig. 8. Chip microphotograph of the fabricated DSM in 65-nm CMOS.

Applying the aforementioned implementation values and assuming $\gamma = 2.5$, the in-band thermal noise is about −95 dBFS with T of 300 K.

V. Experimental Results

The prototype modulator is fabricated in a 65-nm 1P9M CMOS process. Its core area is 0.12 mm^2 (490 μm × 250 μm), as shown in Fig. 8. The modulator draws 61 μA of current in total from two 0.8-V supplies formed by two separated off-chip regulators, which corresponds to 49 μW of power consumption. The analog (including Int1, Int2, and comparator) and digital (including SAR logic, DWA, and clock generating circuits) parts consume 56% and 44% of the total power, respectively. Besides, four references (denoted by V_{CMI}, V_{CMO}, V_{REP}, and V_{REN} in Fig. 7) are all realized off-chip and totally consume 11-μW power.

Fig. 9 shows the measured output spectrum with a −5.3-dBFS sinusoidal input at 1.07813 kHz. The flicker noise is reduced using CHS and the proposed FNRTs, making the spectrum in the low-frequency region nearly flat. The most visible distortion at the third harmonic is −104.3 dBFS, resulting in an SFDR of 99 dB. Fig. 10 shows the measured

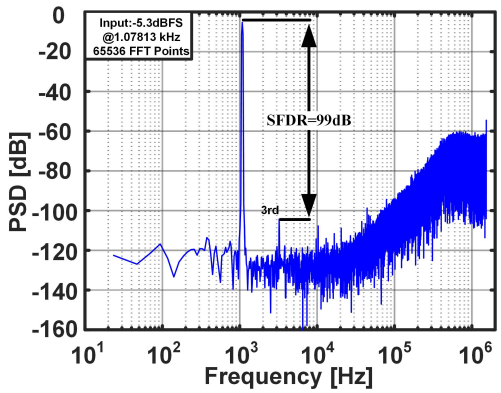

Fig. 9. Measured output spectrum for a 1.07813-kHz input signal.

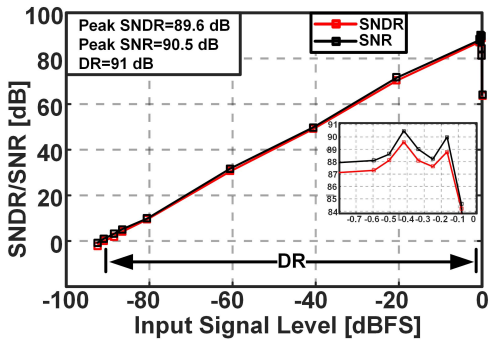

Fig. 10. Measured SNDR/SNR versus the input signal level.

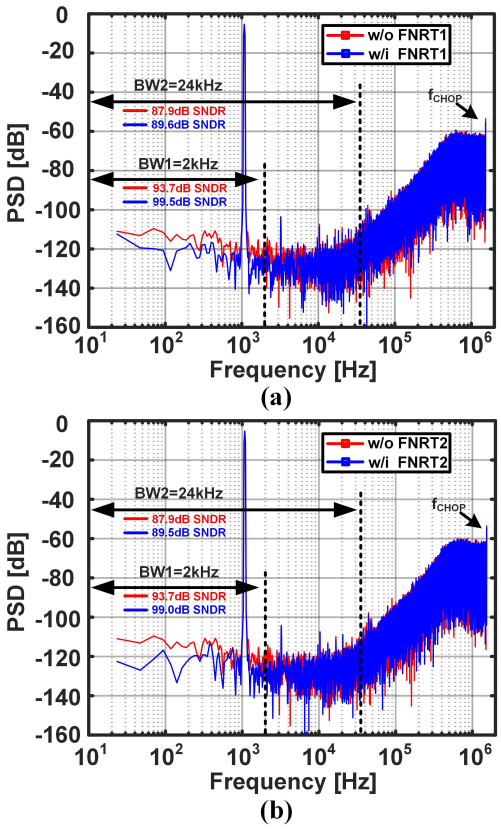

Fig. 11. Output spectrum with and without FNRTs. (a) With and without FNRT1. (b) With and without FNRT2.

TABLE I
MEASUREMENTS OVER FIVE SAMPLES

	Peak SNDR [dB]	Total Power [μw]	SNDR Improvement using FNRT1 [dB]	SNDR Improvement using FNRT2 [dB]
Sample1	89.6	49	1.7	1.6
Sample2	88.2	48	1.8	1.7
Sample3	87.7	44	2.0	1.7
Sample4	88.3	52	1.9	2.2
Sample5	87.3	49	2.1	1.8

[1] The SNDR improvement is calculated in the 24-kHz bandwidth.

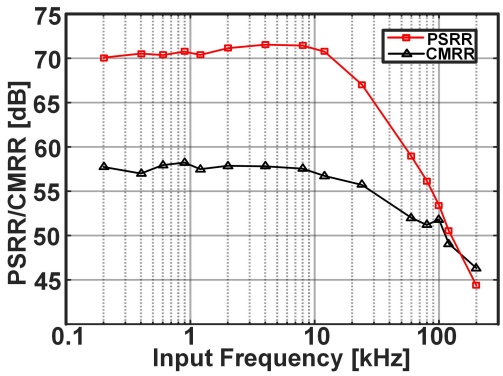

Fig. 12. Measured PSRR and CMRR.

SNDR and SNR versus the sinusoid input signal level. The designed modulator achieves a peak SNDR of 89.6 dB and a peak SNR of 90.5 dB in the 24-kHz bandwidth, and the DR is 91 dB.

Fig. 11 shows the improvements in the SNDR of our proposed FNRTs. Clearly, both FNRTs can flatten the spectrum. To illustrate the validity of the FNRTs, SNDR over two different bandwidths, i.e., BW1 (2 kHz) and BW2 (24 kHz), is calculated. The measured results demonstrate that both techniques can achieve an improvement in the SNDR of about 2 dB in BW2 and 5.5 dB in BW1, respectively. Note that FNRT1 uses switching to reduce the $1/f$ noise but it cannot eliminate it completely [30]; FNRT2 uses the auto-zeroing technique, but it is limited by the amplifier's finite voltage gain (the amplifier is M_{T3} with load R_{B2} here).

To demonstrate the SNDR and power variations over different chips and to verify the effectiveness of the proposed FNRTs credibly, we have tested five samples. Table I lists the measurement results. It can be noticed from the table that all samples can achieve an SNDR of over 87 dB, and the average power consumption is below 50 μW. Both FNRTs can realize an improvement in the SNDR of about 2 dB in the audio bandwidth.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORK

	This Work	Jang [4] JSSC'19		Cardes [2] JSSC'18	Gönen [33] JSSC'17	Billa [5] JSSC'17	Grassi [34] ESS-CIRC'16	Leow [6] JSSC'16	Zhang [21] ASSCC'16	Wang [7] JSSC'15
Type	**DT**	CT	CT	CT	DT	CT	DT	CT	DT	CT
Technology[nm]	**65**	65	65	130	160	180	180	65	65	28
Supply[V]	**0.8**	1.2	1.2	1.8	1.8	1.8	1.8	1	1	3.3/1
BW[kHz]	**24**	24	20	20	20	24	20	25	24	24
F_S[MHz]	**3.072**	6.144	8	20	11.29	6.144	2.4	6.4	3.072	24
$SNDR_{Peak}$[dB]	**89.6**	94.1	88.5	76.6	103	98.5	80	95.2	91.2	98.5
SNR_{Peak}[dB]	**90.5**	94.8	90.1	-	106	99.3	-	100.1	91.9	100.6
DR[dB]	**91**	98.2	93.1	98.5	109	103.6	96	103	93	100.6
Power[μW]	**49/60***	68	55	560	1120	280	730	800	94	1130
$Area_{Core}$[mm^2]	**0.12**	0.14	0.27	0.04	0.16	-	0.4	0.256	0.11	0.022
FOM_S [dB]	**176.5/175.6***	179.5	174.1	152.1	175.5	177.8	154.3	170.1	175.2	171.8
FOM_{DR} [dB]	**178/177***	183.6	178.7	174	181.5	182.9	170.4	177.9	177	173.8
FOM_W[fJ/Step]	**41.4/50.6***	34.2	63.1	2533	242.5	85	223.2	340	66.2	342.3

$FOM_S[dB] = SNDR + 10\log(BW/Power)$
$FOM_{DR}[dB] = DR + 10\log(BW/Power)$
$FOM_W[fJ/Step] = Power/(2 \cdot BW \cdot 2^{\frac{SNDR-1.76}{6.02}})$

[1] * includes the references power.

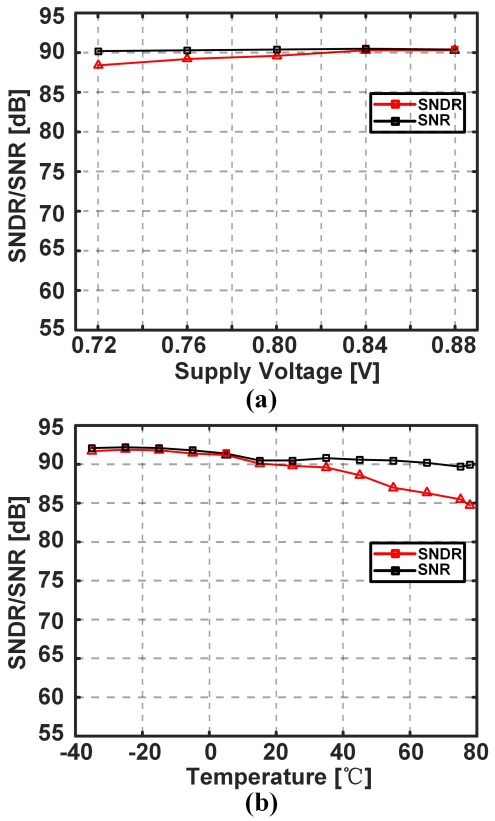

Fig. 13. Measured peak SNDR and SNR versus (a) voltage and (b) temperature.

Fig. 12 shows the PSRR and CMRR of the designed DSM, and they are measured under a 50-mV sinusoid input both. The PSRR is about 70 dB at low frequency. In the entire audio bandwidth, the CMRR and PSRR are above 55 and 65 dB, respectively. The result is comparable to the previous low-power designs [35]. To investigate its robustness to voltage and temperature fluctuations, the modulator has been tested with the supply ranging from 0.72 to 0.88 V (±10% deviation of 0.8 V) and temperature from −35 °C to 80 °C (at a fixed supply of 0.8 V). According to Fig. 13, the SNDR variation is less than 1 dB over the supply range and the SNR variation is less than 0.5 dB. SNDR and SNR both increase slightly when the temperature drops, and the SNDR loss at the high-temperature end is 5 dB. A performance summary of the proposed DSM and a complete comparison with some other modulators designed for the audio applications is shown in Table II. Three popular figure of merits (FoMs) are included.

According to Table II, the DSM in this article achieves a near 90-dB SNDR under the lowest supply voltage and consumes the least power. SNDR and SNR are worse than the calculated value by (24). This is because the residual $1/f$ noise in the signal bandwidth degrades the measured values and distortions, and spurs also cause the degradation of SNDR. To further improve the SNDR under the same-sized sampling capacitances, the amplifier's thermal noise can be reduced by means of a switched tail capacitor instead of a current source in this article. In this way, the integrator will settle progressively slower during the whole transferring period and eventually halt, which can achieve noise reduction, as explained in [36]. Moreover, slew limit in a current tailed amplifier will also vanish.

VI. CONCLUSION

In this article, a low-power audio DT-DSM fabricated in a 65-nm CMOS process is presented. The proposed modulator employs a dynamic amplifier-based SC integrator, and a low-power timing method is proposed to eliminate the additional load capacitor of the dynamic amplifier. Two speed-up branches are used to accelerate the settling of the integrator. This article also presents two FNRTs to achieve about 2-dB SNDR improvement in the audio bandwidth.

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