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QUASI-ONE-DIMENSIONAL ELECTRON STATES IN A SPLIT-GATE GaAs/AlGaAs HETEROSTRUCTURE

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Self-consistent solutions for quasi-one-dimensional electron states in a narrow inversion layer channel at a GaAs/AlGaAs heterointerface have been obtained for a structure with a split gate. A simple model for fixed charge at the exposed surface in the gate opening has been used in the calculation. Energy levels for lateral motion are separated by ~ 1–5 meV for the example considered, with a 0.4 μm gate opening.

1. Introduction

Structures intended to achieve reduced dimensionality of carriers in semiconductors are now being made in many laboratories. There are already several calculations of the energy levels or charge density in such structures [1–8], involving various degrees of approximation. In this paper we use the self-consistent scheme developed for calculating two-dimensional quantization effects in a gated Si structure [5] to study the charge and potential distributions and the electron energy levels of a gated GaAs/AlGaAs heterostructure.

2. Description of the calculation

The structure we consider, illustrated in fig. 1, has a split gate over a conventional GaAs-based heterostructure, as used for example in the work of Thornton et al. [9] and Zheng et al. [10]. The device parameters used in our calculation lead to a channel electron density of 4.4×10^{11} cm^{-2} in the absence of a gate. The exposed surface in the gate opening introduces a new element not present in the Si calculation, because exposed GaAs surfaces have Fermi level pinning near midgap [11]. AlGaAs surfaces can be expected to show similar behavior [12].

To find the surface charge density associated with the Fermi level pinning, a calculation was first carried out using MONTE [13], a conventional drift-diffu-

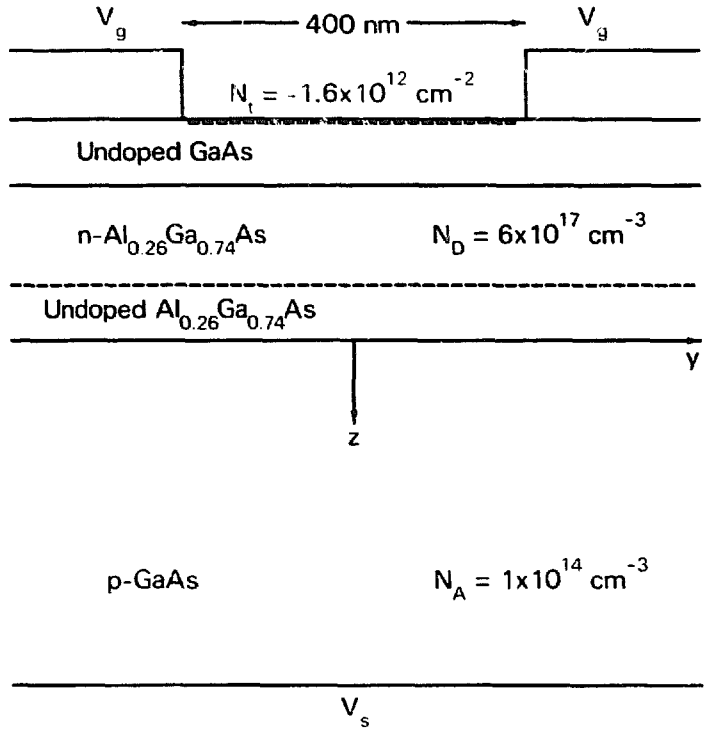

Fig. 1. Device geometry considered in this work. The layer thicknesses are 24 nm for the undoped GaAs top layer, 36 nm for the doped AlGaAs layer, 10 nm for the undoped AlGaAs spacer layer and 6 μm for the GaAs substrate. The donor binding energy and heterojunction conduction band offset are taken to be 0.05 and 0.2 eV, respectively. The calculation assumes a uniform surface charge density in the gate opening, ignoring a region of positive surface charge near the edge of the gate.

sion device model without quantum effects but with provision for current flow, to find the steady-state values of surface charge density for various gate voltages and temperatures. That model assumed that there are 3×10^{12} donor and acceptor states per cm^2 at the surface, both lying at an energy 0.7 eV below the conduction band edge. We found that the surface charge density was only weakly temperature dependent and was approximately constant except near the edges of the gate, where there was a reversal of the surface charge density over a region of order 20 nm, whose width increased with increasing magnitude of the gate voltage. Since this transition layer width was at most 10% of the width of the gate opening in the example we considered, we ignored it in the self-consistent calculations. Including it would shift the value of gate voltages by about -0.15 V for the same channel charge density, but would not change other results of our calculations significantly.

In our calculation we assume that the surface charge density present at temperatures of order 100–200 K is frozen in as the sample cools to the helium temperature range for which the self-consistent calculations are carried out. This assumption yields a surface charge density of -1.6×10^{12} charges per cm^2 under the conditions of the calculation. We treat this charge as constant over the entire width of the gate

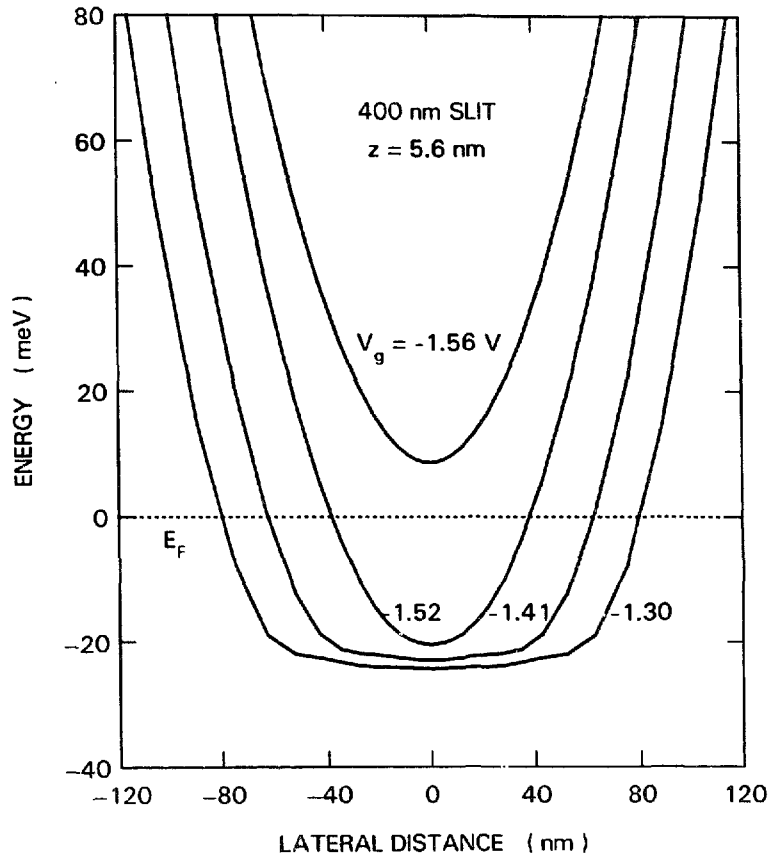

Fig. 2. Calculated lateral potential profiles at 4.2 K along a line 5.6 nm from the GaAs/AlGaAs interface, near the mean of the vertical electron charge distribution, for four values of gate voltage.

opening, ignoring the charge reversal at the edge of the gate, as mentioned above. An implicit assumption underlying this picture is that there is little or no conduction along the surface. If surface conduction were significant, the surface states could equilibrate with the gate. Then the exposed surface would effectively be part of a continuous gate and would prevent a channel from forming under the gate opening. We take the experimental findings on such structures [9,10,14], which show that a laterally confined channel forms, as qualitative support for our assumption of fixed surface charge, although the correct quantitative description could differ from the one used here.

We solve the Schrödinger and Poisson equations self-consistently, ignoring image and exchange–correlation effects, which are expected to change our results only slightly. The Lanczos method is used, as in ref. [5], to find eigenvalues for the first few iterations, but we then iterate to convergence using a Rayleigh quotient iteration method [15], which results in faster execution time. Other steps to speed the calculation have also been implemented, and results are obtained in approximately 2 min of CPU time per voltage point on an IBM 3090 with vector attachment. About 80% of the CPU time is spent in vector mode.

3. Results and discussion

Preliminary calculations were carried out for structures like the one illustrated in fig. 1, for a range of gate openings. We found that the electron density under the gate can be extinguished with suitable negative voltages on the gate, and that the channel under the gate opening can also be turned off provided the gate opening is less than 0.5 μm wide. We therefore show results for a 0.4 μm gate opening to illustrate a case in which the channel can be turned off.

Fig. 2 shows lateral potential profiles sampled at the average distance of the electron charge distribution from the GaAs/AlGaAs interface. As in previous calculations, the potential is nearly parabolic when there is little or no charge in the channel, but approximates a truncated parabola with a flat bottom as charge accumulates in the well.

Calculated energies for the first five subbands are shown in fig. 3. The level spacings range from about 5 meV near threshold to about 1 meV in the gate voltage range considered here. The level spacing decreases as the effective channel width increases, as expected. The one-dimensional regime, with little or no charge in the second subband, has a maximum charge density of about 10^6 electrons per cm, about half the value found in the Si structure considered previously. In both cases, narrower structures would increase the charge possible in the one-dimensional regime.

Charge densities sampled at the average distance of the electrons from the

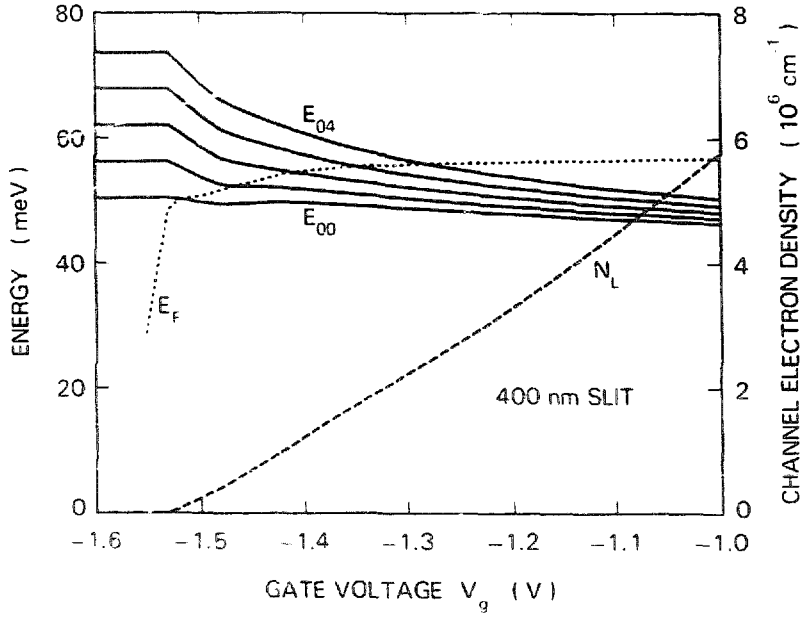

Fig. 3. The five lowest subband energies, the Fermi energy (dotted curve) and the integrated charge per unit length in the channel (dashed curve) versus gate voltage.

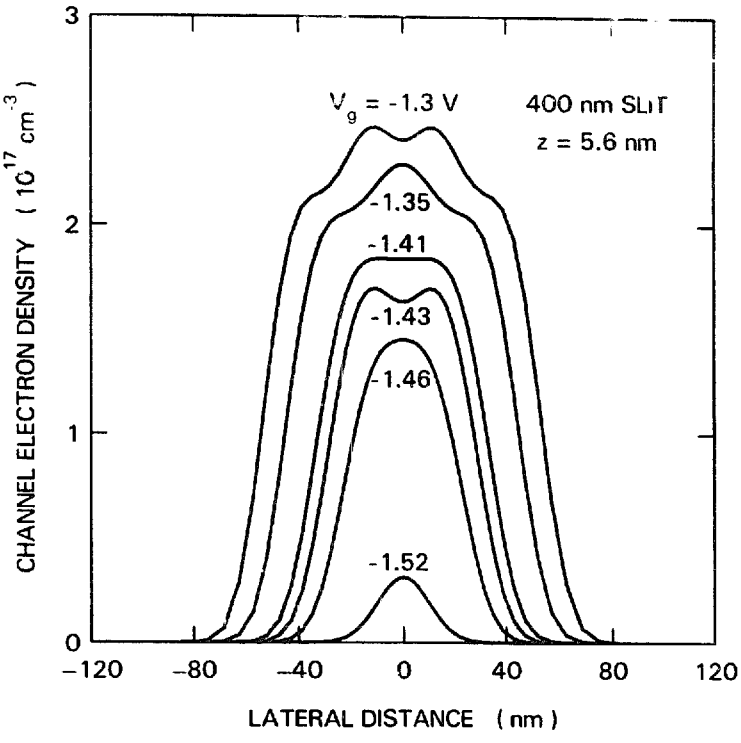

Fig. 4. Density of electrons, sampled along the same line as in fig. 2, for six gate voltages.

GaAs/AlGaAs interface are shown in fig. 4 for several gate voltages. The distinctive shapes arise as successive subbands contribute to the channel charge density.

The results presented here apply to a particular device geometry. Many other calculations suggest themselves, including the dependence of the energy levels on gate opening, channel density, and other device parameters. Calculations are also indicated for etched mesas and periodic structures. Hansen et al. [16] have obtained spectra for a structure with a grating superimposed on a heterostructure, in which spatially separated narrow channels can be induced. To compare the experimentally observed spectral features and the one-electron energy levels obtained in calculations like the one described here it will be necessary to calculate corrections that may be produced by depolarization and excitonic effects. In two-dimensional silicon inversion layers, those corrections are of opposite sign and tend to cancel each other [17].

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