



ALTERNATING SPACE-CHARGE-LIMITED CURRENTS IN HYDROGENATED AMORPHOUS SILICON

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Space-charge-limited currents in $n^+ - i - n^+$ sandwich samples of hydrogenated amorphous silicon have been investigated under alternating current (AC) conditions. When the voltage sweeping rate exceeds the release rate of carriers from deep traps, the AC current-voltage characteristics differ markedly from the direct current (DC) characteristics. This is attributed to the remaining space charge in the samples which acts as a potential barrier and reduces the current. A simple model is proposed to describe the time-dependence of this injection-induced barrier.

1. Introduction

In several recent papers the observation of space-charge-limited currents (SCLC) in hydrogenated amorphous silicon (a-Si:H) has been reported, either in forward biased Schottky diodes^{1,2} or in $n^+ - i - n^+$ sandwich devices^{3,4,5} and in a lateral configuration⁶. SCLC measurements provide information on the density and distribution of gap states^{7,8}. Densities of states near midgap between 10^{16} and $10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ have been deduced from SCLC experiments on a-Si:H $n^+ - i - n^+$ devices^{3,4,5}.

In this paper we present the current-voltage characteristics of $n^+ - i - n^+$ devices at AC conditions and propose a model to explain the large discrepancy between AC and DC characteristics.

2. Experimental

The a-Si:H films have been produced by rf glow discharge decomposition of silane at a substrate temperature of 275 °C. For the n^+ contact layers, which had a thickness of 50 nm, a mixture of 1% phosphine in silane was used. Glass plates with evaporated chromium stripes have been used as substrates. As upper electrodes chromium stripes were evaporated perpendicular to the lower electrodes, the overlapping area (1 or 4 mm²) defining the device.

Chromium-coated single-crystal silicon has also been used as a substrate. In this case chromium dots with an area of 0.5 or 10 mm² provided the upper contact.

3. The Model

A triangular sweep voltage with amplitude V_0 is applied to the $n^+ - i - n^+$ sandwich device in the SCLC regime. The injected charge is, in a first approximation, homogeneously distributed through the film and resides predominantly in deep traps³. First, we consider the hypothetical situation that the release time of carriers from traps is infinite. Then the space charge per unit area in the sample is constant, Q_0 :

$$Q_0 = \frac{2\epsilon_s V_0}{L} \tag{1}$$

where ϵ_s is the semiconductor permittivity and L the undoped layer thickness. Q_0 is related to the trap distribution $N_t(E)$ by

$$Q_0 \approx eL \int_{E_{F0}}^{E_{Fn1}} N_t(E) dE \tag{2}$$

where E_{F0} and E_{Fn1} are the equilibrium Fermi-level and the quasi-Fermi level at applied bias V_0 respectively. The energy band profiles at different voltages can be deduced from Poisson's equation and are shown in figure 1. At a bias V with $|V| < V_0$ a potential barrier U_{max} is located at

$$x_{max} = \frac{V_0 + V}{2V_0} L \tag{3}$$

with

$$U_{max} = \frac{(V_0 - |V|)^2}{4V_0} \tag{4}$$

In a practical device carriers are released from traps and U_{max} decreases with time. The realistic energy band profile lies between the dashed curve, which represents the steady-state profile at bias V, and curve 2 in figure 1. The traps are refilled again up to E_{Fn1} after application of the peak bias $+V_0$ or $-V_0$.

The release time $\tau(E)$ of a trap located at energy E is given by

$$\tag{5}$$

where E_c is the energy level of the conduction band edge and the preexponential factor A is assumed constant. When the voltage is reduced from V_0 to V at a rate much faster than the release

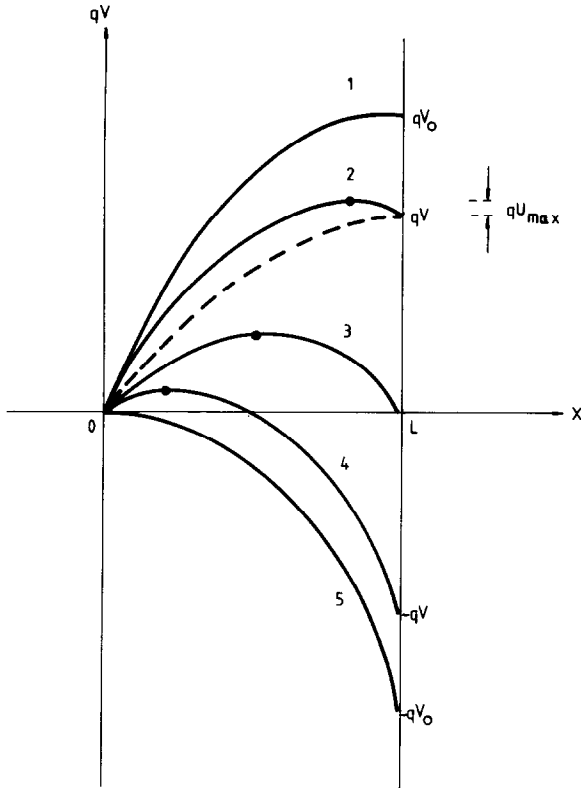


Figure 1. Energy band profiles at different voltages and with constant space charge. The dashed line is the steady state profile at bias V.

rate of electrons from traps, the excess density of occupied traps $N(E,t)$ is given by

$$N(E,t) = N_t(E) \exp\left(\frac{-t}{\tau(E)}\right) \left(\frac{1}{1 + \exp\left(\frac{E - E_{Fn1}}{kT}\right)} - \frac{1}{1 + \exp\left(\frac{E - E_{Fn2}}{kT}\right)} \right) \tag{6}$$

Here t is the time elapsed since the last peak bias has been applied and E_{Fn2} is the quasi-Fermi level at bias V .

When retrapping effects are neglected, the charge per unit area evolves in time as

$$Q(t) = \frac{2\epsilon_s V}{L} + Q'(t) \tag{7}$$

with

$$Q'(t) = eL \int N(E,t) dE \tag{8}$$

The time dependence of U_{max} is then obtained by replacing V_0 in equation (4) by

$$|V| + LQ'(t)/2\epsilon_s$$

and given by

$$U_{max}(t) = \frac{(LQ'(t)/2\epsilon_s)^2}{4(|V| + LQ'(t)/2\epsilon_s)} \tag{9}$$

The AC current i at voltage V is related to the barrier height by

$$i = C \exp\left(-\frac{eU_{max}(t)}{kT}\right) \tag{10}$$

Under the condition that the energy band profile is only slightly different from the steady-state profile, i.e. $U_{max}(t) \ll V$, the constant C can, in a first approximation, be taken equal to i_0 , the steady-state current at applied bias V . Then,

$$i = i_0 \exp\left(-\frac{eU_{max}(t)}{kT}\right) \tag{11}$$

The model predicts that the potential barrier decay time depends on $E_c - E_{F0} = E_a$, the conductivity activation energy, for fixed $N_t(E)$, V_0 , V and L , since for increasing E_a the quasi-Fermi levels lie also deeper in the gap and hence the release time from traps between E_{Fn1} and E_{Fn2} increases.

4. Results and Discussion

In figure 2 a current-voltage-oscillogram of a $n^+ - i - n^+$ device is shown. The ramp voltage

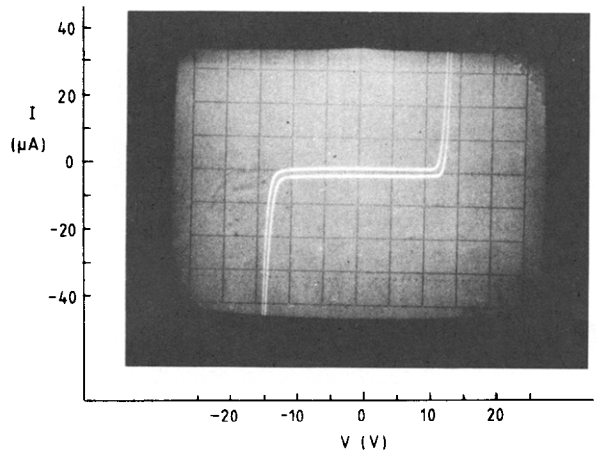


Figure 2. Current-voltage oscillogram of a $n^+ - i - n^+$ device at a frequency of 500 Hz and an amplitude of 15 V.

had a frequency of 500 Hz and an amplitude of 15 V. The area of the device was 0.5 mm^2 and the thickness L of the undoped layer $1.5 \text{ }\mu\text{m}$. The hysteresis in the high current region is due to the difference in elapsed time, defined in the previous section, for the curves with increasing and decreasing bias. In the low bias region the device acts as a capacitor and the hysteresis in this region is due to displacement currents. In figure 3 the comparison is shown between the DC characteristic and the AC characteristic at a frequency of 1 kHz and an amplitude of 15 V. In figure 4 the same data are plotted on a double-logarithmic scale. For the AC characteristic the transition to the high current regime is much sharper and occurs at a higher voltage. The voltage for onset of high current at

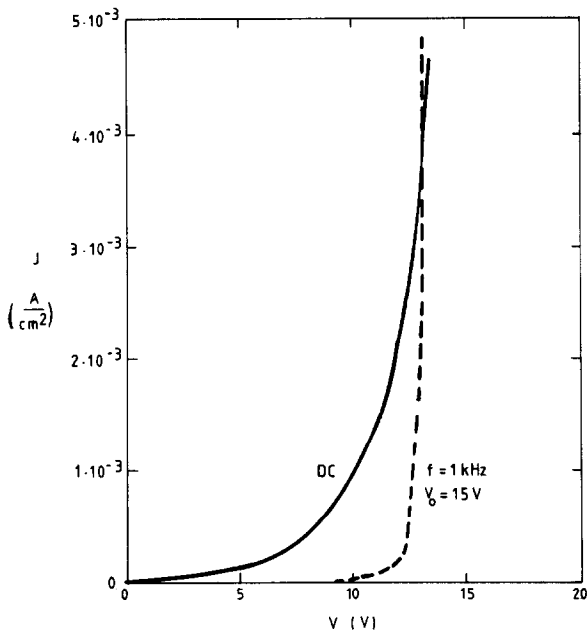


Figure 3. DC and AC characteristics on a linear scale for a device with $L=1.5 \mu\text{m}$.

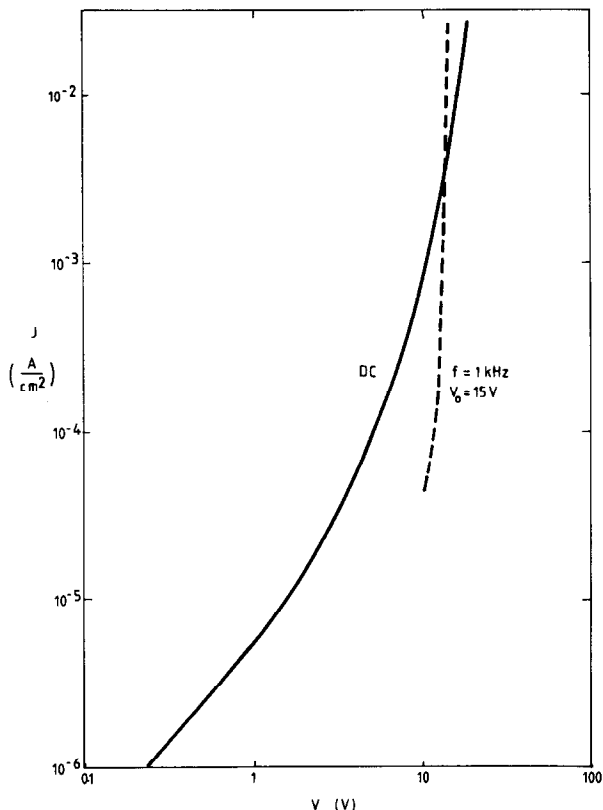


Figure 4. DC and AC characteristics on a double-logarithmic scale for a device with $L=1.5 \mu\text{m}$.

fixed $f=1\text{kHz}$ increases with increasing amplitude V_0 , from 4 V at $V_0=5$ V to 12 V at $V_0=15$ V, in accordance with the model.

With increasing voltage the AC characteristic approaches and crosses the DC characteristic. Beyond the crossing point the AC current exceeds the steady-state current. This can be attributed to transient currents which occur before the establishment of a new quasi-Fermi level. They are considerably larger than the steady-state current due to the progressive thermalization of trapped electrons. This thermalization process is also responsible for dispersive transport in disordered semiconductors⁹.

The large variation of the current-voltage characteristics with frequency and amplitude is observed in many samples with different values of L and E_a . The frequency at which deviations from the DC characteristic start, depends on E_a as predicted by the model. Even on one sample E_a can be modified by the Staebler-Wronski-effect¹⁰.

We compared the characteristics of a sample in the light-soaked state ($E_a=0.61$ eV) with those of the same sample in the annealed state ($E_a=0.51$ eV). The current is restored to i_0 on a time scale of minutes and seconds respectively, in qualitative agreement with the model.

To check the consistency of the model more quantitatively we have measured the response of the current to a voltage step from V_0 to V and compared the results with numerical calculations using equations (2), (5), (6), (8), (9) and (11). The ratio i/i_0 is plotted in figure 5 as a function of elapsed time t for a device with $L = 1.5 \mu\text{m}$ and $E_c - E_{F0} = 0.7$ eV. The solid and dashed lines represent the measured and calculated results respectively for $V_0 = 16$ V and $V = 6.8$ and 10 V. For the calculations the preexponential factor A in equation (5) was taken equal to 10^{-11} sec⁷. $N_t(E)$ was determined from the DC current-voltage characteristic by the method described in our previous paper³ and was found to be equal to $7 \cdot 10^{16}$ eV⁻¹cm⁻³, independent of energy, in the range of interest between E_{F0} and E_{Fn1} .

The shape of the measured curves and their dependence on V agrees well with the calculated results. However, slight modifications in the values of E_{F0} , $N_t(E)$ and temperature result in large changes of the time scale for the calculated curves, without changing their shape. Since E_{F0} and $N_t(E)$ are not known with great accuracy (e.g. an error of a factor 2 is possible in $N_t(E)$ ³), the good quantitative agreement between calculated and measured results in figure 5 is not very significant.

In summary, we have shown that alternating space-charge-limited currents can be considerably smaller than the DC current at the same applied voltage. The experimental results are qualitatively explained by a model in which the AC current is reduced by a potential barrier which is due to the remaining space charge in the sample. The charge storage effects are indicative of deep traps with a density $10^{16} - 10^{17}$ eV⁻¹cm⁻³, in agreement with steady-state SCLC measurements.

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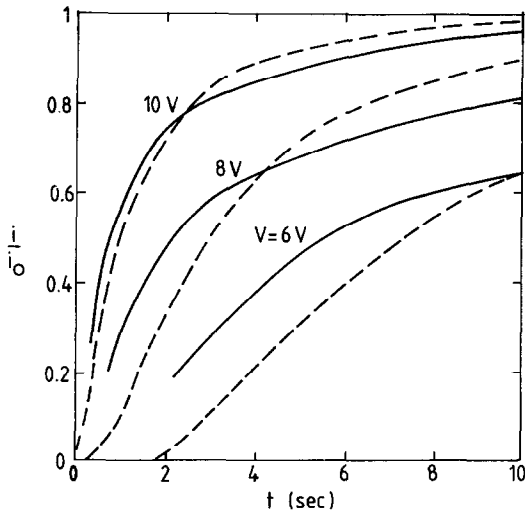


Figure 5. The response of the current on a voltage step from $V_0 = 16$ V to $V = 6, 8$ or 10 V. The solid and dashed lines represent the measured and calculated results, respectively.

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