A Critical Review of VLSI Die-Attachment in High Reliability Applications

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VLSI die bonding materials and processes for VLSI die-attachment are reviewed, including the bonding mechanism, metallurgy, process variables, and limitations of solders, organic adhesives, and glass adhesives. The common die bond related problems, disbonding, and die cracking are examined from a fundamental viewpoint as is the role of wafer backside in obtaining reliable die bonding. It is concluded that two technologies—eutectic and glass die bonding—are well suited to deal with large die sizes for VLSI applications in hermetic packages.

ONE OF THE FIRST OPERATIONS in assembly, after a silicon wafer has been sawed into individual components (chips), is chip-attachment (die bonding) to a substrate. With the emergence of VLSI technology, the chip size has grown steadily, placing rather stringent demands on the processing and reliability of die bonding. It has been well recognized by the industry that die bonding technology for large VLSI devices (5 mm by 5 mm or greater) requires special considerations, primarily due to stress management and thermal dissipation issues. The purpose of this article is to examine die bonding materials and processes from a fundamental viewpoint in order to determine if large VLSI chip attachment requires new die bonding materials, or merely more stringent process controls with the existing die bonding technologies.

First, the various die bonding materials used in the industry are examined with a discussion of their properties and limitations. Next the primary reliability concerns associated with VLSI die bond processes are examined. A thorough discussion of the metallurgy of the gold-silicon (Au-Si) eutectic die bond process (the industry standard) follows and includes a discussion of the bonding mechanism, bonding process variables, and thin film metallurgy associated with such a process. The use of organic adhesives for VLSI die bonding is reviewed next. Finally there is a discussion of the emerging glass die bond technology, followed by a look into the future of VLSI die bonding.

Die Bonding Materials

The die bonding process includes a large choice of materials, which may be broadly classified into the three categories below.

Solders

These include single, binary, and ternary metallic compositions and may be further classified into two subgroups—hard and soft solders. Hard solders (Au-Si, Au-Sn, Au-Ge) have rather high flow stresses (onset of plastic flow) and thereby offer excellent fatigue and creep resistance. The disadvantage of using hard solders is primarily due to their lack of plastic flow which leads to high stresses in the silicon chip due to the thermal expansion mismatch between the die and the substrate.

The soft solders are low melting temperature binaries and ternaries (e.g., Pb-Ag-In and Pb-Sn compositions) which have a high degree of plastic strain capability. This allows for a reduction of the thermal stresses on the chip, but makes the solders prone to fatigue and creep-rupture failures at the device operating temperature [1, 2]. Thus, in spite of the low die-stress advantage, the soft solders have failed to emerge as a popular group of useful die bonding materials.

Organic Adhesives

Epoxies and polyimides filled with precious metals have found widespread acceptance as die bond materials in low cost packaging schemes (plastic packages) [3, 4]. They offer the advantage of lowest processing temperatures and lower cost compared to the gold based hard solders. Numerous papers have claimed the lowering of thermal stresses in silicon by the use of organic adhesives [5–7].

These adhesives are filled with a metal to provide the thermal and electrical conductivity required in most applications (silver being the most common filler). However, the use of organic adhesives in high reliability packages (hermetically sealed) has been slow in acceptance due to the poor thermal stability of these materials, especially when filled with silver [8]. Furthermore, due to the high amounts of solvents and binders used in these adhesive pastes for processing purposes, it is extremely difficult to obtain a die bond area free of any voids, leading to poor thermal dissipation and other reliability concerns [9]. The poor thermal stability coupled with the outgassing of entrapped solvents and other gaseous species remains a challenge in the application of these materials to high reliability VLSI applications.

Glass Adhesives

Silver filled specialty glass materials have emerged in the past few years as a serious contender in VLSI die bond applications [10]. These materials offer the possibility of a void-free die bond interface with excellent thermal stability [8]. However, the currently available materials require high processing temperatures (>400 °C) and *oxidizing ambients* for optimum adhesion creating some special processing concerns. In addition, the glass die bond materials also need solvents and binders for processing purposes leading to the problem of complete solvent removal similar to the case of organic adhesives.

Die Bond Reliability Issues

VLSI die bond materials and process selection are based upon the nature of the reliability issues involved. In a non-hermetic package, die corrosion may become an overriding factor in materials selection [5]. For high power dissipation devices, heat dissipation and elimination of hot spots becomes a key issue [11]. In spite of such specialized considerations, the common concerns with die bond reliability are primarily two-fold: disbonding failures (interfacial rupture) and die cracking (silicon fracture). The following discussion of these two failure mechanisms will highlight the key materials science principles which can be used for process optimization.

Disbonding

Disbonding failures which lead to a total separation of the chip from the substrate are most commonly observed during the centrifuge testing of the finished packages.

A quick calculation using the 30K g acceleration typically used in industry shows that for a 100% bonded die (no interfacial voids) the tensile stress on the die is about 200 psi. This value is far below the ultimate tensile strength of most solders and adhesives and implies that the cohesive failure of the die bond materials is most unlikely. Thus, in case of a failure due to disbonding, either there is a high degree of voiding under the die, or the interface between the solder/die or solder/substrate is not chemically bonded. An examination of the failed interface becomes necessary to identify the source of the problem. Various causes of chip disbonding are:

1. Solder and/or die backside oxidation [12],
2. Non bonding impurities on the solder surface [13],
3. Formation of brittle intermetallic phases [14],
4. Substrate metallization adhesion failure [15, 16],
5. Solder fatigue or creep rupture [2],
6. Insufficient amount of adhesive or solder,
7. Extensive voiding under the die [9].

Die Cracking

Die cracking has emerged primarily as a large die VLSI problem and has been the focus of several key papers in the past [17–21]. This problem is more insidious compared to disbonding since the crack propagation may be delayed until a sufficient number of thermal cycles have been experienced by the system. This represents a serious reliability hazard since the power cycling of devices in field applications results in thermal cycling. Three key features of this failure mechanism are [6, 20, 21]:

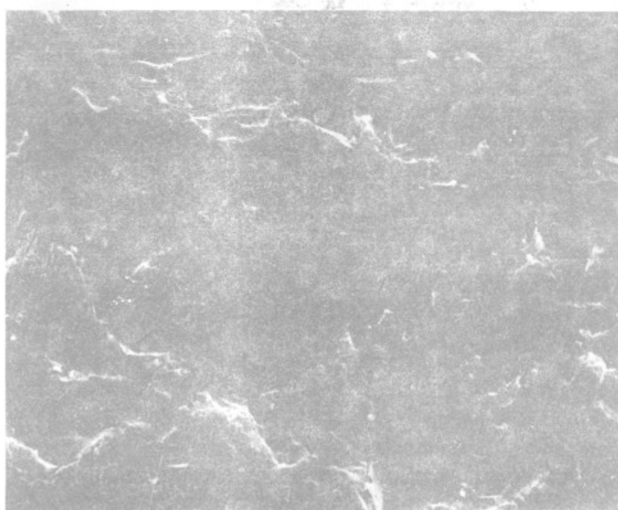
1. The cracks usually show up after temperature excursions (thermal shocks, thermal cycling, etc.)
2. The crack typically emanates from the bottom of the silicon chip near the die edges and corners.
3. Two types of cracks are observed, vertical and horizontal.

The die cracking problem can be analyzed based upon the basic fracture mechanics principles. Thus, silicon failure can be described as:

$$\text{microcrack (flaw) in Si} + \text{stress} \rightarrow \text{fracture}$$

i.e., since silicon is brittle, its fracture usually requires stress assisted crack propagation initiated at a pre-existing flaw, or microcrack, on the external silicon surfaces.

The microcracks in silicon arise as a natural consequence of damage to the silicon surface during wafer backside preparation and wafer sawing [21]. In most applications, an ohmic contact from the die backside to the substrate is needed for proper operation of the device. This requires removal of the process contaminants from the backside as well as removal of any diodes formed inadvertently on the backside during the device fabrication process. In order to



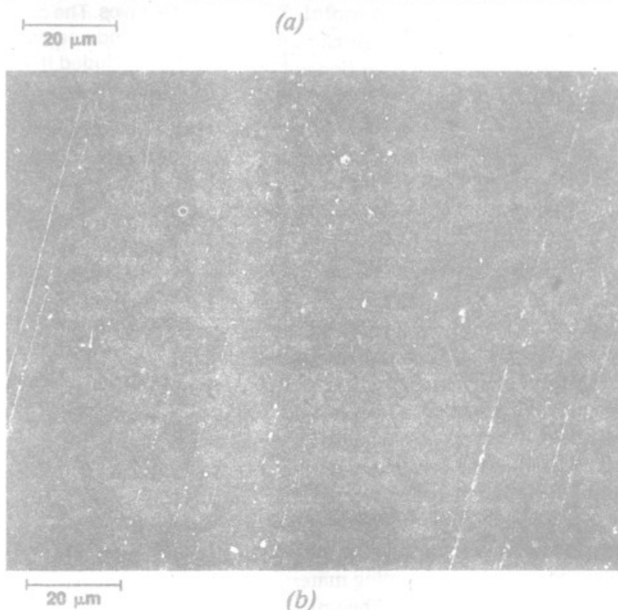


Fig. 1—SEM micrograph of the die backside after removal of some silicon by (a) sandblasting with Alumina (SWAM machine) and (b) Mechanical grinding with diamond impregnated wheels (DISCO grinder).

achieve this, the wafer backside has to be abraded or mechanically polished to remove about 20 to 50 μm of silicon after the IC fabrication has been completed, resulting in mechanical damage of the die backside and introducing microcracks in silicon.

Figure 1 compares the SEM micrographs of die backsides subjected to sandblasting and mechanical grinding to remove a layer of silicon. The figure clearly indicates that the former is worse from the viewpoint of creating microcracks on the die backside and increasing the die cracking jeopardy.

The occurrence of horizontal cracks in the silicon has been attributed to the high shear stresses near the die edges when bonded to a substrate with higher thermal expansion coefficient relative to silicon [21]. The thermal stress of a bonded joint is highly dependent upon the bond line thickness for shear constrained systems [22]. This implies that the shear stresses in silicon are going to be dependent upon the adhesive or solder bond thickness. The experimental data of Hund and Burchett on Au-Si eutectic [21] and of Van Kessel, et al., on adhesive bonded silicon [6] clearly demonstrate

the validity of this argument. For reliable VLSI die attachment, this implies that the bond line thickness needs to be optimized for individual bond materials.

Fracture propagation vertically from the die backside requires a tensile stress field to be present in silicon near the microcracks. The primary stresses in silicon arise from the thermal expansion mismatch between the die and the substrate. The stress analysis of a die bonded to various substrates has been reported in many papers [20–25]. If a perfect die bond is assumed (no voids or nonuniformities), basic stress analysis calculations show that the silicon backside goes into compression upon cooling from the die attachment temperature. Since the compressive strength of silicon is extremely high, vertical die cracking of perfectly bonded devices is most unlikely. In order to explain the vertical die cracking behavior observed, the secondary stresses due to the presence of voids in the die bond region have to be accounted for.

Many authors have qualitatively described the stress intensification mechanism due to the voids at the die bond interface [5, 6]. Finite element stress analysis has been used by Chiang and Shukla [20] to show that the presence of voids at the die bond interface does create significant secondary stresses in silicon. In particular, the presence of voids due to unbonded die edges or corners (open or edge voids) exerts a tensile field in the bonded regions of silicon near the bonded/unbonded discontinuity causing a crack to propagate upwards, away from the free edges. Their model also indicates that a fully enclosed void (closed void) of a relatively small size (10 mils wide) under the die is less likely to cause the die cracking. The die cracking model in Fig. 2 represents pictorially the essence of such stress analysis, and has been experimentally confirmed.

Hund and Burchett [21] have measured the creep rate for Au-Si eutectic and shown substantial stress relief occurring above 150 °C. This implies that the residual stresses in silicon will depend upon the package cooling rate after die bonding. In the worst case of a fast cooldown (no stress relief), Hund and Burchett's stress calculations for a void free die bond indicate substantial tensile stress components near the die edges which could lead to die fracture. However, their failure analysis of the cracked devices does not mention any occurrence of voiding at the die bond interface, which would act as stress raisers if present. The vertical failure mode described by them is very similar to the failures associated with the occurrence of edge voids.

Based upon the die cracking model described above, it is obvious that a good VLSI die attach process will require a void free, uniform die bond. In the case of gold-silicon die bonding, it is very common to have some regions of die left unbonded, especially at the edges, with the problem getting worse as the die size increases. In order to understand the reasons underlying this behavior and determine how to alleviate the problem, the metallurgical principles of soldering have to be discussed. Although the following discussion is based upon the Au-Si metallurgy, the principles involved can be applied to other solder die bond metallurgies as well.

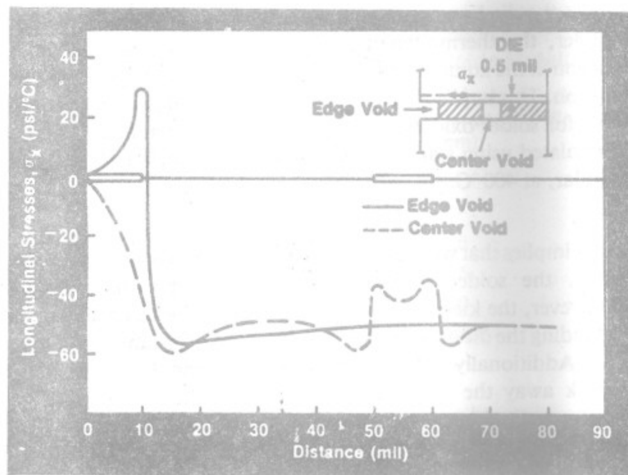


Fig. 2—Finite element stress calculation results showing the longitudinal stress, σ_x, in silicon 0.5 mil away from the die bond line as a function of die bond void locations (Edge vs. Center) [20].

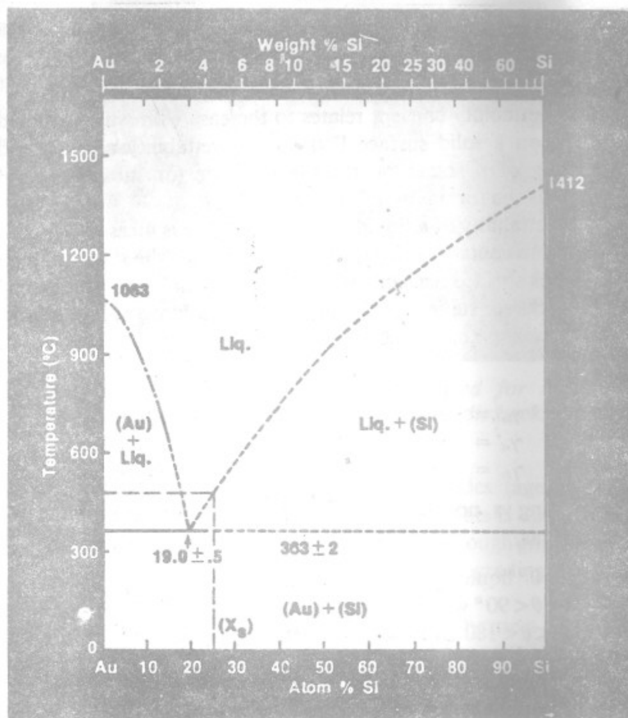


Fig. 3—Au-Si phase diagram showing the silicon saturation composition (X_s) achieved at a die bond temperature of 500 °C.

Eutectic Die Bonding

Bonding Mechanism

Figure 3 shows the phase diagram for the Au-Si binary system. The die bonding process is carried out at temperatures above the eutectic temperature (363 °C). Typically, the reaction is initiated by using an Au-Si preform of composition close to the eutectic composition although pure gold preforms are used in the industry as well. In the case of pure gold preforms, the silicon from the die backside reacts with gold at the die bond temperatures to initiate the eutectic liquid formation. In either case, at the bonding temperature (typically > 400 °C), the liquid solder continues to consume the silicon from the die backside and gold from the substrate (if available) in order to achieve equilibrium. Since the silicon supply is virtually unlimited, silicon from the die backside dissolves into the solder until the liquid reaches a saturation composition (X_s, see Fig. 3). From the viewpoint of such a bonding process, it is imperative that the supply of silicon from the die backside be unimpeded in order to obtain a good diffusional bond.

Upon cooling, the bond consists of Au-Si hypereutectic phases (Si rich eutectic microstructure) and represents a typical diffusional bond. The equilibrium phase diagram in Fig. 3 shows no detectable solubility of gold and silicon into each other below the eutectic temperature but metastable gold silicides are known to exist [26, 27]. Thus, although the microstructure observed (Fig. 4) indicates some mechanical interlocking of gold and silicon phases, it is very likely that some degree of chemical bonding also exists.

Solder Oxidation

At the die bond temperature, when silicon saturates the liquid solder, the thermodynamic activity (chemical potential) of the silicon in the liquid solder phase is equal to the activity of pure solid silicon. This implies that the equilibrium partial pressure of oxygen P_{O2} for solder oxidation at a given die attach temperature can be calculated using standard thermodynamic principles [28]. In particular, at 400 °C, the calculation gives:

$$P_{O2} \simeq 10^{-67} \text{ Atm.}$$

This implies that when the Au-Si eutectic system is used for die bonding, the solder oxidation is virtually impossible to avoid. However, the kinetics of such oxidation can be controlled by surrounding the die attachment area with copious amounts of an inert gas. Additionally, any 'scrubbing' done during the die bonding to break away the oxide layers is helpful. The use of pure gold preforms (in situ eutectic formation) minimizes this problem significantly, and its use for large VLSI devices becomes mandatory.

The above discussion has highlighted the oxidation problem of eutectic solder involving an easily oxidizable component. The use of soft solders is likely to cause a similar or worse problem since the soft solders are made from easily oxidized base metals. In order to understand exactly how the oxidation of solder affects die bond reliability, the following discussion of the theory of adhesion becomes necessary.

Theory of Adhesion (Wettability, Contact Angle)

The wettability concept relates to the ease with which a liquid spreads on a solid surface [29]. Good wettability allows rapid spreading of a solder on the die backside (or substrate), and minimizes the formation of voids.

The wettability of a liquid on a solid surface is measured by the equilibrium contact angle, θ, which is defined by the static balance of various surface tension forces as depicted in Fig. 5. Balancing these forces for static equilibrium of the liquid drop in Fig. 5 leads to the familiar Young's equation:

$$\gamma_{sv} - \gamma_{sl} = \gamma_{lv} \cos \theta$$

where, γ_{sv} = surface energy of solid-vapor interface
γ_{sl} = surface energy of solid-liquid interface
γ_{lv} = surface energy of liquid-vapor interface

The wetting vs. non-wetting conditions are defined (somewhat arbitrarily) as,

$\theta = 0°$ liquid spreads spontaneously
$0° < \theta < 90°$ wetting behavior (partial spreading)
$90° < \theta < 180°$ non-wetting behavior (liquid beads up)

The contact angles described above become modified for real, atomically non-planar surfaces. Surface area increases with increasing surface roughness further degrading wettability if the contact angle for idealized planar surface is greater than 90°. Conversely, the wettability is improved for a real surface if θ is less than 90° for the idealized case [30].

Thermodynamic considerations of the solid-liquid-vapor system described in Fig. 5 can be used to quantify the adhesion of the liquid to the solid [30]. This is defined by the reversible "work of adhesion,", W_a, and is given by the surface energy balance from the first law of thermodynamics:

$$W_a = \gamma_{sv} + \gamma_{lv} - \gamma_{sl}$$

or, combining the above equation with Young's equation, one obtains (Young-Dupree equation):

$$W_a = \gamma_{lv}(1 + \cos \theta)$$

From the above equation, it is obvious that good wetting ($\theta < 90°$) and high liquid surface tension are necessary (but not sufficient) conditions for good adhesion of the solder to the solid surface. For real surfaces, the equation for the work of adhesion has to be modified to take into account the surface roughness, as well as the strain energy associated with the interface upon cooling down to room temperatures. The modified phenomenological equation is [30]:

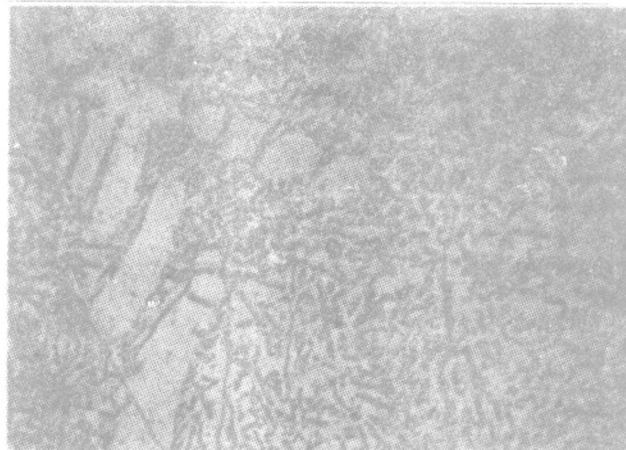


Fig. 4—Microstructure of Au-Si eutectic bond showing highly interlaced network of Au (bright areas) and Si (dark areas).

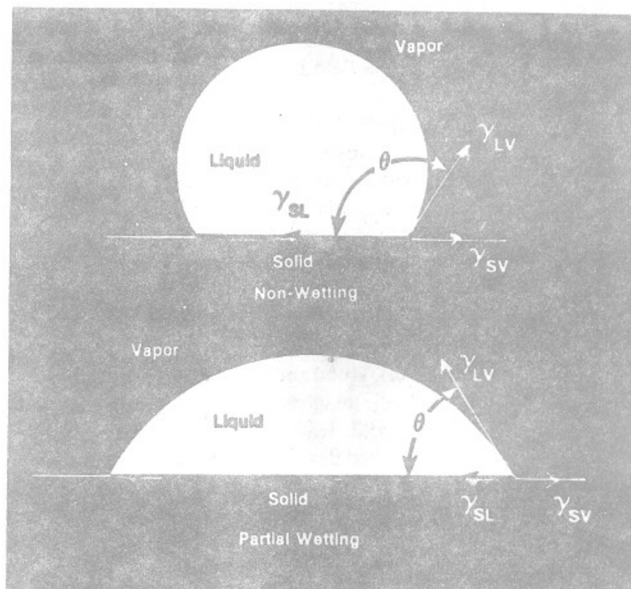


Fig. 5—Equilibrium for a small liquid drop on a solid surface, showing the three interfacial tension forces involved in defining the equilibrium contact angle.

$$W_a = k[\gamma_{lv}(1 + \cos \theta) - \gamma']$$

where k = contact coefficient (a function of surface roughness), and γ' = strain energy due to cooldown to room temperature.

Since the strain energy is rather low for hard solders, the adhesion of Au based solders to a Si surface is expected to be higher compared to the soft solders. More importantly, the above equations also show that the adhesion and wettability are aided by high energy solid and liquid surfaces.

In order to get optimum die bonding, it is thus crucial to provide a low contact angle during soldering by presenting a high energy

solid surface to the liquid. Herein lies the basis for good processing controls and also defines the thick/thin film metallurgy of the silicon backside and the package substrate.

High and Low Energy Surfaces

The energy of solid and liquid surfaces depends primarily upon the nature of bonding [31]. Clean metallic solid and liquid surfaces have high surface energies associated with them. This makes such surfaces prone to adsorption of organics, oxidation, etc., in order to lower their surface energies. The oxides, in general, have lower surface energies than nascent metal surfaces while most organic polymers with poor crystallinity and low melting point have the lowest surface energies. This implies that the presence of oxides or adsorbed organics will greatly reduce the wettability. In addition, silicon has rather high surface energy associated with it due to its covalent bond nature. Therefore, if left bare, it will lower its surface energy by oxidation leading to low wettability.

This discussion emphasizes the importance of mechanical scrubbing done during eutectic die bonding. Scrubbing causes the surface energy lowering oxides and other contaminants to be displaced from the interface, exposing a high energy silicon (native) surface during the die bonding process. This also explains the underlying reasons why the die bond problems with the large area VLSI devices are aggravated. If the die backside (or, to a lesser degree, the substrate surface) is oxidized, the solder liquid 'dewets' the oxidized areas. A typical die bond process involves the initial solder placement in the substrate center. The solder spreading, if hindered, will leave the die corners or edges unattached (edge voids). The probability of this increasing with the die size makes the die cracking potential more severe for the large devices.

Die Backside Metallurgy

Die Backside Requirements

Based upon the discussions above, the die backside requirements for good die bonding are:

1. It must react (supply silicon) readily with the Au based solder.
2. It must be highly wettable by the solder (low contact angle).
3. Its wettability should not degrade with time (i.e., no aging at room temperatures).

The native silicon surface does not meet the last requirement (it readily adsorbs oxygen and other impurities to lower the surface energy and degrade solderability). In order to meet these requirements, the die backside has to be coated with appropriate metallic thin films. Various thin film metallurgies have been used in the industry to fulfill this purpose and are listed in Table I.

Die Backside Evaluations

In order to evaluate the quality of various backside preparation techniques and thin film metallurgy options, contact angle measurements have been performed using pure gold preforms in a high vacuum apparatus (Fig. 6). The use of pure gold preforms is necessary in order to allow in situ formation of Au-Si liquid, since the Au-2 wt% Si preforms do not melt uniformly due to the preoxidized condition and other contaminants (Fig. 7).

The data from the contact angle measurements are summarized in Table II. From this table, it can be concluded that:

1. The sandblasted silicon surface with high roughness ($R_a \simeq 10$ μm) has very poor wettability. The mechanically polished surface ($R_a \simeq 0.3$ μm) exhibits superior wettability. It is very difficult to provide a conformal coating of appropriate thin films on a wafer backside with a high degree of asperity (as is the case with the sandblasted surface), which causes the surface to become rich in silicon oxide by aging. This leads to high contact angles.

Table I—Currently Used Silicon Backside Metallurgies[a]

Final Metal	Nominal Thickness (nm)	Barrier Metal	Nominal Thickness (nm)	Surface[b] Roughness R_a (μm)
Au	100	none	–	10.0
Au	100	none	–	0.3
Au	150	Cr	25	10.0
Au	150	Cr	25	0.3
Au	100	Ti	30	0.3
Au	50	Ti/Ni	150/50	1.0
none	–	none	–	0.3–10[c]

[a] Data obtained by analysis of die backside from various IC manufacturers from U.S. and Japan.
[b] Artifact of methods used for backside silicon removal.
[c] Dependent upon backside removal technique.

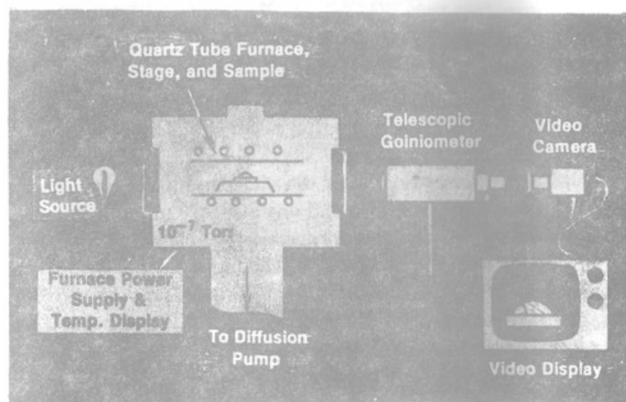


Fig. 6—Schematic of the apparatus used for contact angle measurements of Au-Si liquid drop on the die backside.

2. A gold coated silicon backside degrades (ages) with time, reflected by increased contact angles. This is due to the rapid room temperature diffusion of silicon through gold [32] causing silicon oxide to appear on the surface degrading bonding and wettability.
3. The use of refractory metal diffusion barriers (Ti, Cr, etc.) results in improved solderability and prevents room temperature aging. These diffusion barriers prevent the formation of silicon oxide on the backside at room temperatures, but allow the silicon to diffuse at the die bonding temperature to react with the solder.

Although the use of refractory metals as Si diffusion barriers at room temperatures is useful to prevent aging, secondary problems have to be accounted for. Cr is known to diffuse through the gold grain boundaries and oxidize causing solderability degradation [33, 34]. Thus a careful control of Cr and Au thicknesses becomes very important in practice [35]. Secondly, Cr can become an almost "perfect" diffusion barrier at elevated temperatures (die bonding temperature) if any oxygen is incorporated in it during the film deposition. The incorporation of any nitrogen in Ti leads to a similar phenomenon. This would prevent diffusional mixing of the solder with the silicon backside leading to poor adhesion. The mechanism of such phenomena can be explained based upon the concept of "stuffed" grain boundary barriers [36]. This highlights the need for good vacuum practices during the deposition of barrier films on the wafer backside in order to obtain optimum backside characteristics.

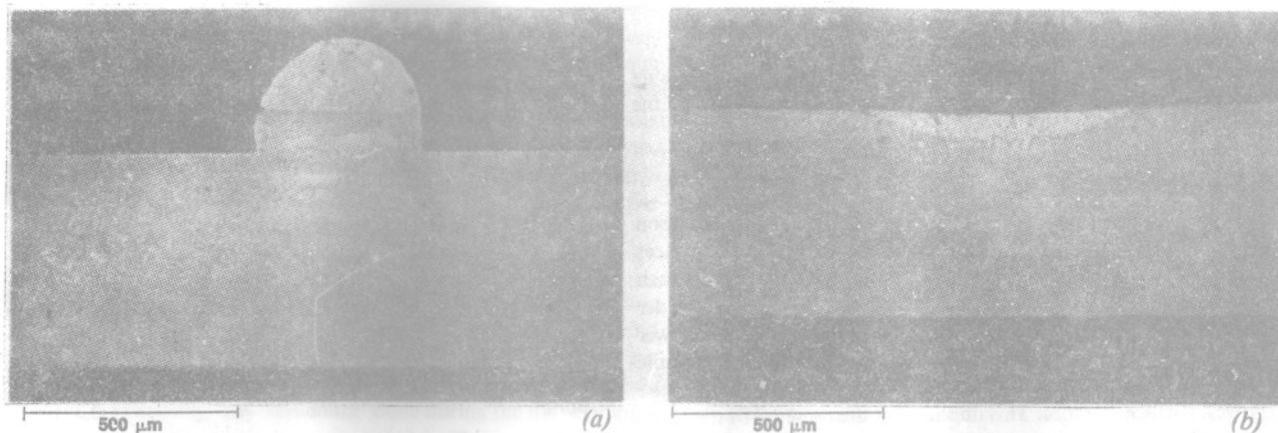


Fig. 7—Optical micrographs of samples from contact angle measurements, (a) bare Si backside (DISCO grind) showing $\theta = 90°$, (b) same backside with Cr/Au deposited thin films showing complete spreading ($\theta = 0°$).

Adhesive Die Bonding

Bonding Mechanism

The adhesion of epoxies and polyimides to silicon and metallic substrates is primarily due to Lewis acid-base (charge transfer) interactions. In addition, the use of silane coupling agents may be made to enhance the bonding to silicon surfaces. From the bonding mechanism, it is obvious that the rougher surfaces will provide higher degrees of adhesion, and any surface contamination with non-polar organics will severely degrade adhesion. Such considerations imply that the wafer backside requirements for organic adhesives are very different compared to the eutectic bonding. Native oxide on the die backside or coating with amphoteric metals is expected to lead to the highest possible adhesion.

Processing Considerations for Adhesives

There are two major issues with the use of organic adhesives in high reliability VLSI applications. The limited thermal stability of adhesives is well established [8, 9]. Weight loss studies of completely cured epoxies also indicate a finite weight loss at elevated temperatures [9]. The outgassed products from epoxies are generally corrosive in nature and present a fundamental problem in high reliability applications. The polyimides have better thermal stability compared to the epoxies but they are known to absorb moisture, which may be subsequently released in the hermetic package cavity and cause moisture related failures.

The other concern with the use of adhesives for large die bonding arises from the fact that it is very difficult to remove completely all the solvents from the adhesive without leaving behind voids at the die bond interface. Estes has shown the degradation in mechanical, thermal and electrical properties of conductive epoxies due to voids formation during the processing [9].

Fortunately, it is possible to design epoxies with practically 100% solids, but the low glass transition temperatures for such epoxies may pose problems in HTB (High Temperature Bake) testing, if the test temperature goes above the glass transition temperature. Bolger and Mooney [5] have reviewed the evolution of epoxies for die bonding purposes and point out that the glass transition temperature has to be maintained above 150 °C in order to reduce the failure due to the rapid expansion of the adhesive above the glass transition temperature. However since the epoxies are more compliant above the glass transition temperature, it is not clear that the rapid thermal expansion would be a major problem. Clearly more work is needed in this area.

It has been shown earlier that the thermal stresses in silicon are aggravated by the presence of voids at the die bond line and also when the bond thickness is reduced. The control of adhesive processing to provide a void free, controlled thickness bond for large VLSI devices remains a challenge.

Glass Die Bonding

The glass die bonding materials have been a recent addition to the multitude of die bond material choices [8, 10]. The approach

Table II—Contact Angle Data for Various Silicon Backsides

Silicon Removal Method	Average Surface Roughness R_a (μm)	Metallization Layers [c]	Metallization Thickness (nm)	θ Pre-Aging	θ Post-Aging [d]
Alumina Sandblasting [a]	7.0	Au	150	$83 \pm 7°$	– [e]
Diamond Grinding [b]	0.3	Au	150	$3 \pm 3°$	– [e]
Sandblasting [a]	7.0	Au/Cr	150/20	$83 \pm 7°$	90°
Grinding [b]	0.3	Au/Cr	150/20	$3 \pm 3°$	$3 \pm 3°$
Grinding [b]	0.3	Au/Ti	150/30	$3 \pm 3°$	$3 \pm 3°$

[a] Semiconductor Wafer Abrading Machine (SWAM)
[b] Disco grinder
[c] First layer is the outermost layer
[d] 168 hrs at 85 °C, 85% RH
[e] θ could not be measured due to the lack of reaction with pure gold

used above for discussing the eutectic and adhesive die bond processes is also applicable in this instance.

Bonding Mechanism

Glass die bonding is obtained by using special glass compositions which have relatively low glass-transition and working temperatures (lead borate based glasses). This is necessary to allow the molten glass to bond to silicon die by an "oxide bond" at processing temperatures close to the eutectic Au-Si bonding. These glasses are generally filled with silver to enhance the electrical and thermal conductivity of the material. After complete thermal treatment, the bond microstructure consists of an interlaced network of silver in a sintered, glassy matrix [8].

The low temperature glasses used for sealing and adhesion purposes have been recently reviewed [37]. A consequence of the low processing temperature requirement is poor thermal stability of such glasses in reducing or inert atmospheres. The lead oxide based glasses reduce to metallic lead at relatively low temperatures in a reducing atmosphere which interferes with the oxide bond mechanism. Thus it becomes mandatory to process the glass die bonding in oxidizing ambients. As shall be seen in sections below, this requirement poses a serious reliability concern, when Ni/Au plated ceramic laminated packages are used.

Die Backside Requirements

Since the bonding mechanism involves silicon availability on the die backside, bare silicon backside is optimum. In fact, the native oxide on the die backside will only aid in the bonding process. However, if any thin film metallurgy has to be used for process compatibility purposes, it should be kept in mind that the use of any diffusion barriers (unintentional) which prevent silicon from diffusing out would degrade the adhesion. In one example, a CVD nitride film left on the die backside unintentionally severely degraded the die adhesion [38]. On the other hand, Moghadam [8] reported excellent adhesion obtained for die backside coated with aluminum, which is a good oxide bond former and also allows rapid silicon diffusion at elevated temperatures.

A review of the die backside requirements for solder vs. glass die bonding indicates that although the requirements are different, the optimum backside features required for the eutectic bonding are fully compatible with the glass die bonding process, due to the requirement of silicon availability for bonding at elevated temperature. This would be a very important consideration in manufacturing for process flexibility.

Glass Bonding Process Considerations for VLSI Devices

1. Bond-Line Thickness Control: Since the glass material is inherently brittle, a reduction in the bond thickness reduces the bond strength. The adhesion vs. bond thickness data on one particular glass die bond system indicate a minimum of 2 mil thickness for good adhesion [38]. This is one of the major differences between the solder vs. glass systems. In eutectic soldering, the surface tensions during cooldown from die bond temperatures virtually self-control the die bond thickness and uniformity, leading to 0.3–0.5 mil as a typical thickness. In the case of glass die bonding, control of bond layer thickness to >2 mils with thickness uniformity control for a large VLSI chip becomes a major manufacturing issue analogous to the solvent based organic adhesives.
2. Solvent and Binder Evaporation: As the die size increases, the evaporation of entrapped solvents and binders underneath the die becomes very difficult since void elimination and complete solvent loss require prolonged time-temperature bakes. This greatly impacts the throughput time of the process.
3. Processing in Laminated Ceramic Packages: This is a special concern for VLSI devices, since the large die size and high pin counts make ceramic packages the only package choice available for many of these devices. The glass die bonding materials currently available require processing at 400–450 °C in oxidizing atmospheres for prolonged times (several minutes and longer). Experiments have shown that heating the laminated side brazed ceramic packages in such an oxidizing ambient can lead to Ni/W diffusion through the gold plating and subsequent oxidation [39]. The presence of Ni and W oxides on the surface of the seal ring causes a serious hermeticity reliability problem (Au-Sn solder sealed packages).

The diffusion and subsequent oxidation of Ni through gold layers has been studied by many researches [40, 41], but the diffusion coefficients are not well known and are highly dependent upon the quality of plated films. However, it is possible to do rough calculations for experimental designs based upon the data accumulated on eutectic die bonding.

This is feasible since the Au-Ni thick films on ceramic packages do experience high temperature in air during the eutectic die bond process (only the die bond area is flooded with inert gas), exposing the seal ring to some air. Knowing the time-temperature of exposure at eutectic die bonding temperatures (known to be reliable from a hermetic seal viewpoint), comparison of equivalent diffusion lengths to other time and temperatures is possible provided the activation energy for Ni diffusion is known.

Such calculations have shown that it is feasible to process glass die bonding at elevated temperatures in air without degrading the seal quality and reliability, provided that certain time/temperature limits are not exceeded [39]. However, the exact time/temperature limits for this process are highly dependent upon the nature and quality of the metallization on the ceramic. For example, tangible differences in seal quality after glass die bonding are observed among various vendors [38], since the Ni plating varies from being a single layer to dual electroless/electroplated layers, which greatly modify the Ni and W diffusion properties.

Future Perspective

The die bonding technologies for VLSI large devices are at an interesting juncture. One school of thought maintains (and it is also the opinion of the authors) that the Au-Si eutectic die bonding will remain as the workhorse for VLSI devices. However, reliability requirements do indicate that the automated die bonding will require a very careful control and characterization of die backside quality since pure gold preforms, which become a must in large VLSI applications, rely upon a clean backside to provide the silicon for bonding and wettability. With the use of a silicon backside optimized for bonding and wettability, pure gold preforms and controlled inert atmosphere at die bonding, the eutectic process does not present a theoretical limitation with respect to the increasing VLSI die size.

The use of organic adhesives is bound to increase, especially in plastic packaging. However, they are far from achieving the stringent long-term reliability goals from the outgassing of contaminants viewpoint. In addition, the thermal stability limitations with organic adhesives will continue to preclude them from reliable applications in hermetic packages. The significantly lower cost of the organic adhesives over the other die bonding materials is a tremendous advantage which cannot be overlooked, and further research needs to continue in this area to enhance the product base for organic adhesives.

The advent of glass die bonding has been considered by the industry as a possible panacea for the eutectic bond stress related problems. The stress problems with eutectic die bonding are much

better understood today than a few years back, reducing the sense of urgency to change the die bonding processes. The glass die bonding material offers a significant cost advantage over the Au-Si system, and if the processing concerns with large die in ceramic packages are resolved, it will become a serious contender. Further research by the material suppliers towards reducing the glass processing temperatures by modifying the glass composition should aid tremendously in coping with some of the processing problems associated with this material. Due to the manufacturing difficulties associated with the bond line thickness control and voids elimination in solvent based die attach materials, B-staging of adhesives (thick film deposition and sintering on the wafer backside) offers significant promise and is worthy of further investigation.

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