

## EFFICIENT GaAs/Ge/Si SOLAR CELLS

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### ABSTRACT

Epitaxial GaAs layers with a reduced dislocation density have been grown on Ge-coated Si substrates by using a new technique involving multiple growth interrupts and thermal cycles. The open-circuit voltage of shallow-homojunction solar cells fabricated in these GaAs layers was found to increase with the number of interrupts and thermal cycles. Small-area cells with conversion efficiencies up to 14% (AM1) have been obtained. In addition, monolithic tandem cells composed of a GaAs top cell and a Si bottom cell that are connected by a thin epitaxial Ge layer have been fabricated.

### INTRODUCTION

Shallow-homojunction  $n^+/p/p^+$  GaAs solar cells with conversion efficiencies exceeding 20% (AM1) have been fabricated on GaAs (1) and Ge (2) substrates. With the objective of reducing the cost of such cells, we have been investigating the use of Si as a substrate material. We previously reported (3,4) the fabrication of shallow-homojunction cells with conversion efficiency of 12% (AM1) on Ge-coated  $p^+$  Si substrates. In this paper we report recent advances in GaAs/Ge/Si material preparation that have resulted in an improvement in cell performance. Small-area cells with conversion efficiencies up to 14% have been achieved. We also describe the fabrication of tandem cells composed of a shallow-homojunction GaAs top cell and a Si bottom cell that are connected by a thin epitaxial Ge layer. These are the first monolithic tandem cells in which Si is used as the low bandgap material. The cells exhibit open-circuit voltages of  $\sim 1.2$  V and good fill factors (0.75-0.8), but the photocurrent density is limited because the difference in bandgap between Si and GaAs is too small. This result suggests the possibility of developing low-cost, high-efficiency monolithic tandem cells that utilize Si for the bottom cell and a material with a higher bandgap than GaAs for the top cell.

### MATERIAL PREPARATION

To form the GaAs/Ge/Si structures, the Si substrate is first coated with a Ge epilayer deposited by e-beam evaporation (5), and GaAs epilayers are then grown by chemical vapor

deposition (CVD) in an  $\text{AsCl}_3\text{-GaAs-H}_2$  system. The surface morphology and crystal quality of the epilayers have been significantly improved by using several new growth procedures.

### Surface Morphology

As described previously (3,4), mirror-smooth GaAs epilayers have been grown on Ge-coated Si substrates oriented  $2^\circ$  off (100) toward (011). If (100)-oriented Si substrates are used, the GaAs layers display irregular surface morphology, as shown in Fig. 1a, due to the formation of

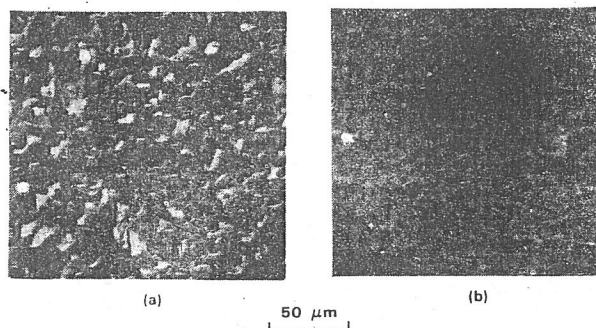


Fig. 1. Optical micrographs showing (a) antiphase domains in GaAs layer on Ge-coated Si (100) substrate and (b) domain-free GaAs layer grown on Ge-coated Si substrate oriented  $2^\circ$  off (100) toward (011).

antiphase domains. These domains, which have also been observed in layers of GaP on Si and GaAs on Ge (6), result from the symmetry difference between the GaAs and Ge lattices. Nucleation of GaAs on (100) Ge may occur in either of two orientations, (100) or (100), which are not equivalent for GaAs because of its polar nature. GaAs epilayers without domains have been grown on Ge-coated Si substrates oriented  $2\text{-}3^\circ$  off (100), toward either (011) or (111). The surface morphology of such a domain-free layer is shown in Fig. 1b.

Although the surfaces of domain-free GaAs layers are specular over most of their area, both hillocks and pits are observed. These defects originate from small pits, 1-10  $\mu\text{m}$  in diameter, that are present in the underlying Ge layers.

These pits can cause faceting of the GaAs layer, which results in hillock formation (Fig. 2a), or by exposing the Si substrate they can inhibit GaAs nucleation and therefore produce pits (Fig. 2b).

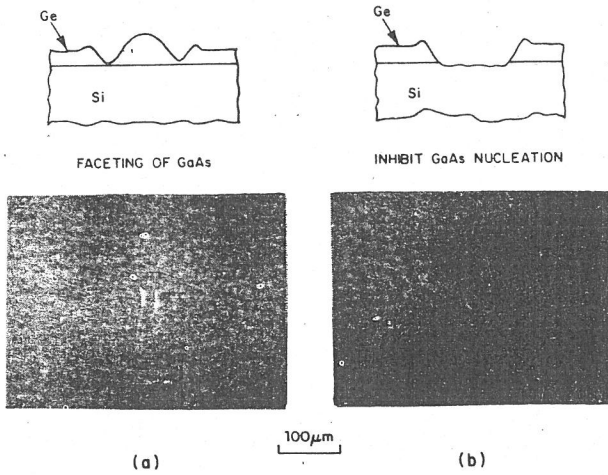


Fig. 2. Optical micrographs of GaAs layers grown on Ge/Si substrates that have micropits in the Ge layers. The micropits can (a) produce GaAs faceting, causing hillock formation or (b) inhibit GaAs nucleation, causing pit formation.

The Ge pits result from spitting of the Ge source during e-beam evaporation. Spitting can be greatly reduced by decreasing the beam power, which also reduces the Ge deposition rate. By using a rate of  $\sim 100$  Å/min the Ge surface pit density has been reduced to less than  $10$  cm $^{-2}$ , compared to  $\sim 10^4$  cm $^{-2}$  for the rate of  $\sim 600$  Å/min used in previous experiments (5).

Reducing the Ge pit density has two important benefits for the GaAs layers: (1) reduction of cracks and (2) reduction of autodoping. Since these layers are under a large tensile stress due to differential thermal contraction between GaAs and Si, they have a tendency to crack. Cracking frequently originates from hillocks, where the material is fragile and the local stress is large. By reducing hillock density, decreasing the pit density in the Ge layers therefore reduces cracking in the GaAs layers.

During the growth of GaAs layers on Ge/Si substrates, they are doped with Si and Ge donors, which compensate the p and p $^+$  layers of the solar cell structure. If a sufficient area of the Si substrate is exposed by pits in the Ge layer, the donor concentration may reach  $10^{17}$ - $10^{18}$  cm $^{-3}$ , resulting in carrier lifetime degradation and poor junction characteristics. For the Ge layers with low pit densities autodoping is limited to  $2$ - $5 \times 10^{16}$  cm $^{-3}$ , which is low enough for the growth of efficient n $^+$ /p/p $^+$  shallow-homojunction structures.

## Dislocations

The GaAs layers previously grown on Ge/Si substrates contain a high density ( $> 10^7$  cm $^{-2}$ ) of dislocations (3,4). These dislocations originate from the Ge epilayers, which contain more than  $10^9$  cm $^{-2}$  dislocations due to the large lattice mismatch ( $\sim 4\%$ ) between Ge and Si. The high dislocation density in the GaAs results in a high junction leakage current and hence significant reduction of open-circuit voltage of solar cells. We have investigated a new growth technique for GaAs that greatly reduces the propagation of dislocations into the junction region and therefore produces a marked increase in open-circuit voltage.

The basic principle of the new growth technique is illustrated in Fig. 3. In the

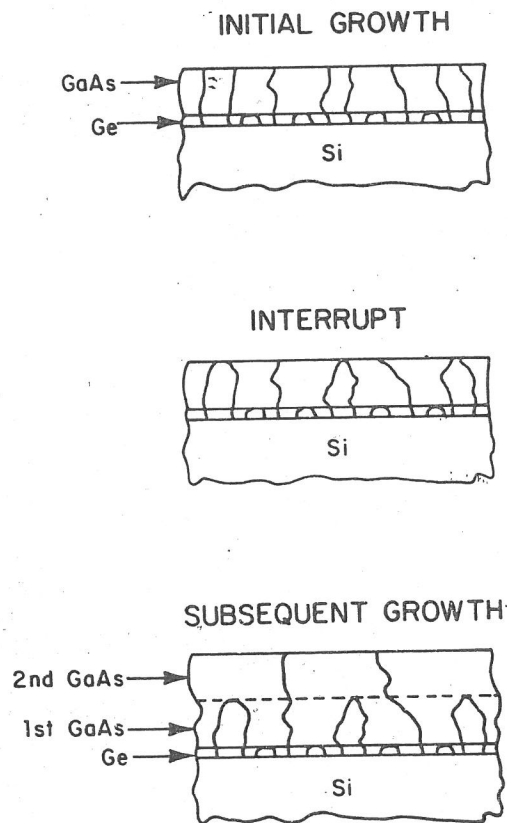


Fig. 3. Schematic diagram showing the use of growth interrupt and thermal cycling technique to reduce dislocation density in GaAs layers grown on Ge/Si substrates.

initial GaAs growth many dislocations threading from the Ge layer are incorporated into the GaAs layer. After the GaAs layer becomes  $\sim 0.1$   $\mu$ m thick, growth is interrupted and the sample is cooled from the growth temperature of  $\sim 700^\circ$ C to about room temperature. During cooling, since the

GaAs layer is subjected to a large thermal stress the dislocations tend to move and interact with each other to form loops and networks. When growth is resumed, the loops and networks reduce the dislocations available for threading into the next GaAs layer. If the sequence of interrupted growth and thermal cycling is repeated, the process of dislocation interaction can lead to a progressively lower dislocation density in the successive GaAs layers. Figure 4 is a

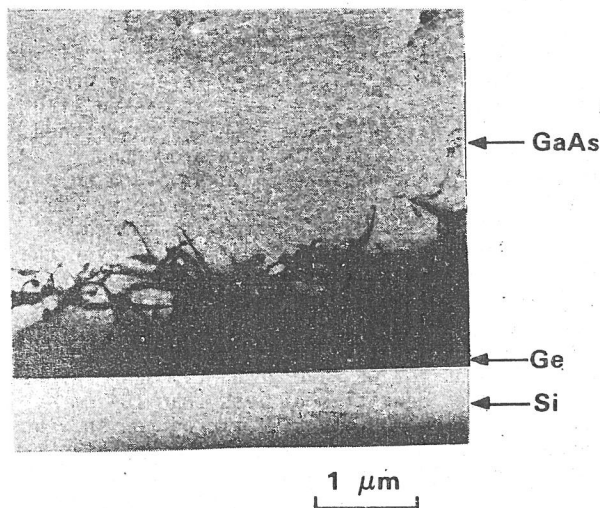


Fig. 4. Cross-section TEM micrograph of a GaAs layer grown on Ge/Si substrate with 10 growth interrupts and thermal cycles.

cross-section micrograph, obtained by transmission electron microscopy (TEM), of a GaAs sample deposited on a Ge/Si substrate with ten growth interrupts and thermal cycles. The dislocation density in the final GaAs layer is estimated to be one to two orders of magnitude lower than this density in samples grown without interruption.

In a number of runs for preparing GaAs n<sup>+</sup>/p/p<sup>+</sup> solar cell structures on Ge/Si substrates, we have grown the p<sup>+</sup> region by the new technique, using up to 20 growth interrupts and thermal cycles per run. In any one run, the individual p<sup>+</sup> layers were of the same thickness, which was chosen to make the total thickness of the p<sup>+</sup> layer region about 4 μm. The p and n<sup>+</sup> layers, which were grown without interruption, were 4.0 and 0.15 μm thick, respectively.

#### SOLAR CELL CHARACTERISTICS

Small-area solar cells 0.6 mm in diameter have been fabricated from the GaAs structures by procedures similar to those used for cells on bulk single-crystal GaAs or Ge substrates (1,2). For cells without an antireflection (AR) coating, the short-circuit current density J<sub>sc</sub> is ~ 14 mA/cm<sup>2</sup>. Figure 5 shows the open-circuit voltage V<sub>oc</sub> of these cells as a function of the number of p<sup>+</sup> growth interrupts. Each data point represents an

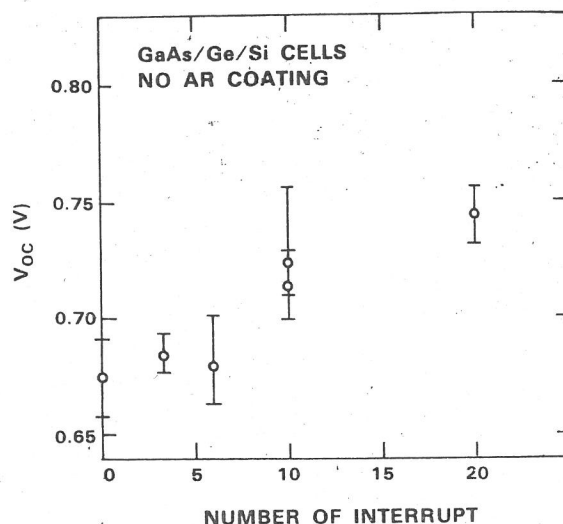
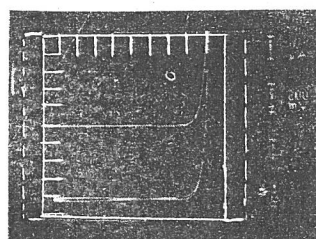


Fig. 5. Open-circuit voltage V<sub>oc</sub> as a function of number of GaAs growth interrupts for solar cells fabricated in GaAs layers grown on Ge/Si substrates.

average of values measured for more than 50 devices, and the error bars indicate the range of measured values. The value of V<sub>oc</sub> increases from ~ 0.67 V with no interrupt to ~ 0.75 V with 20 interrupts. After the n<sup>+</sup> layer is thinned to 500-600 Å by anodization and stripping and the cells are AR coated by anodization, J<sub>sc</sub> increases to ~ 24 mA/cm<sup>2</sup>, close to that of single-crystal GaAs cells, and the V<sub>oc</sub> values each increase by ~ 0.05 V. Figure 6 shows the I-V characteristics



V<sub>oc</sub> = 0.79 V  
 ff = 0.75  
 J<sub>sc</sub> = 24 mA/cm<sup>2</sup>  
 η ~ 14 %  
 AM1

Fig. 6. I-V characteristics (at AM1) of small-area GaAs/Ge/Si solar cell fabricated in GaAs layer with 10 growth interrupts.

under AM1, one-sun illumination of a typical AR-coated cell that was fabricated from a GaAs structure with 10 p<sup>+</sup> growth interrupts. The cell has V<sub>oc</sub> = 0.79 V, J<sub>sc</sub> = 24 mA/cm<sup>2</sup> and fill factor of ff = 0.75, giving an efficiency of ~ 14%.

#### OTHER METHODS FOR REDUCING DISLOCATIONS IN GaAs

In addition to the growth interrupt and thermal cycling technique, we have investigated

two other possible methods for reducing the dislocation density in GaAs layers grown on Ge/Si substrates: (1) multiple heterostructure growth and (2) lateral epitaxial overgrowth.

The possibility of using multiple heterostructures to suppress dislocation propagation was suggested by the multilayer studies of Matthews and Blakeslee (7). In an initial investigation of the distribution of dislocations in such a structure, we have prepared the sample shown schematically in Fig. 7, which

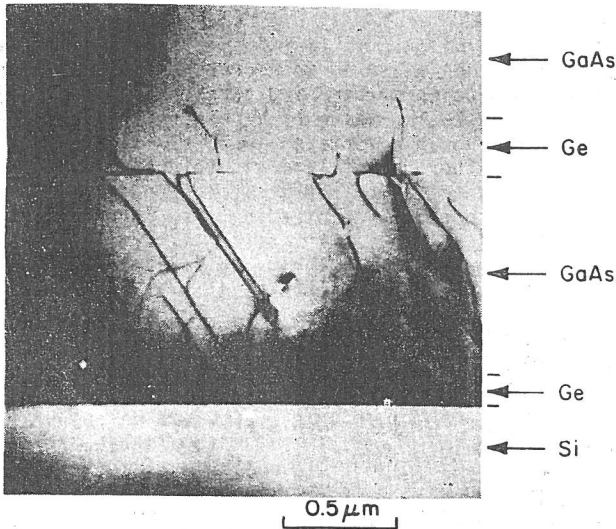
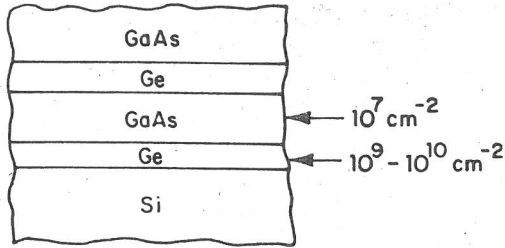


Fig. 7. Schematic diagram and cross-section TEM micrograph showing the use of alternating GaAs and Ge layers to reduce dislocation propagation.

consists of the Ge/Si substrate, a 1- $\mu\text{m}$ -thick GaAs layer, a 0.3- $\mu\text{m}$  Ge layer, and a 2- $\mu\text{m}$  GaAs top layer. The GaAs and Ge layers were deposited in separate systems, so that some contamination may be present at the interfaces between these layers. As shown in the cross-section TEM micrograph of Fig. 7, the first GaAs layer contains the expected high density of dislocations. Some of these dislocations terminate or bend over at the interface between this GaAs layer and the following Ge layer. Consequently, this Ge layer and the top GaAs layer have much lower dislocation counts. The dislocation density in the top GaAs layer is estimated to be  $\sim 10^6 \text{ cm}^{-2}$ . The

dislocation density should be further reduced by growth of additional Ge and GaAs layers.

Another promising method for reducing dislocation densities in GaAs layers on Ge/Si substrates is the lateral epitaxial overgrowth technique. The overgrowth technique was developed for growth on reusable substrates by means of the CLEFT (cleavage of lateral epitaxial films for transfer) process (8). The principle of this technique is illustrated by the top portion of Fig. 8, which is a schematic cross-sectional diagram of a sample at an intermediate stage of overgrowth. After an initial GaAs layer is grown on the Ge/Si substrate, this layer is masked with a film of  $\text{SiO}_2$ , narrow stripe openings are etched in the  $\text{SiO}_2$  film, and GaAs is then grown under conditions such that nucleation takes place only on the regions of the first layer exposed by the openings. The epitaxial GaAs deposits formed on these exposed regions seed lateral growth over the  $\text{SiO}_2$ . If this growth is allowed to proceed for a sufficient time, the growth fronts from adjacent openings merge to form a continuous GaAs layer with the same orientation as the Si substrate. By using this technique we have grown (9) GaAs layers with dislocation densities of less than  $10^4 \text{ cm}^{-2}$ . Figure 8 is a cross-section TEM micrograph showing a typical laterally overgrown region. In this region, there are no dislocations in the overgrown

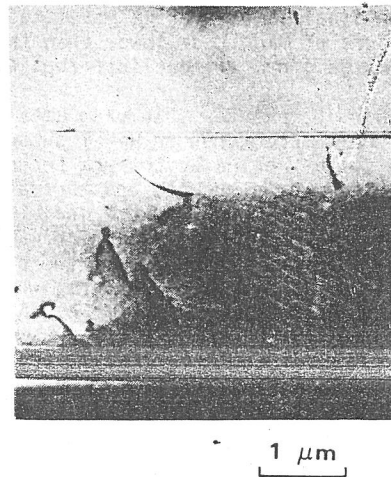
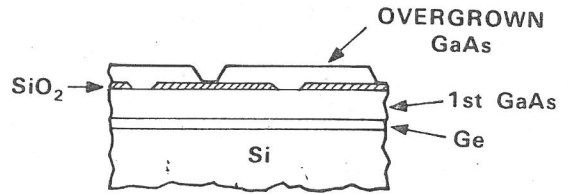


Fig. 8. Schematic diagram and cross-section TEM micrograph showing the lateral overgrowth technique used to produce low-dislocation-density GaAs layers.

GaAs layer, although as usual the layer grown directly on the Ge/Si substrate contains a high density of dislocations. In fact, the only

dislocations that we have observed in the overgrown layers are a small number that originate within the stripe openings but quickly bend over and do not propagate. Initial experiments (9) indicate that the electrical properties of the laterally overgrown layers are comparable to those of conventional GaAs epilayers grown on single-crystal GaAs substrates.

#### GaAs-Si MONOLITHIC TANDEM CELLS

In a few experiments, GaAs  $n^+/p/p^+$  structures were grown with 10  $p^+$  growth interrupts on Ge-coated Si substrates that were lightly doped ( $0.1-1 \Omega \text{ cm } p\text{-type}$ ). An  $n-p$  junction was formed in the vicinity of the Ge/Si interface as a result of As diffusion through the Ge layer during GaAs growth. The presence of this junction is indicated by the photovoltaic response shown at the lower left of Fig. 9, which was obtained for a cell that was fabricated in the Ge/Si substrate after etching away the GaAs layers. A  $V_{OC}$  value of 0.45-0.5 V is observed. The I-V characteristics of a typical small-area (0.6 mm in diameter) GaAs-Si monolithic tandem cell are shown at the lower right of Fig. 9. Although the tandem cells have relatively low values of  $J_{SC}$  ( $\sim 7 \text{ mA/cm}^2$ , without AR coating), they exhibit a  $V_{OC}$  of 1.2 V and good fill factors (0.75-0.8), indicating

#### GaAs-Si MONOLITHIC CELL

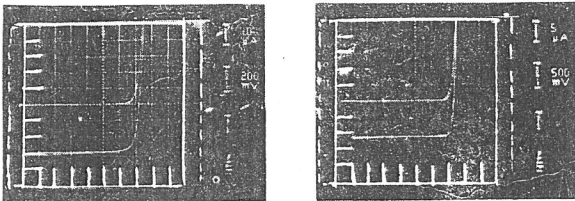


Fig. 9. Schematic cell structure and I-V characteristics for monolithic GaAs-Si tandem cells.

that the Ge layer forms a low-resistance interconnect between the  $p^+$ -GaAs and  $n^+$ -Si. The mechanism for the formation of such an interconnect is not clear. The thin Ge layer, which contains a high dislocation density and is heavily doped with As, may form good tunneling junctions with both the GaAs and Si.

The current density of the tandem cells is limited by the photocurrent generated in the

bottom Si cell. In the GaAs-Si monolithic structure this photocurrent is small because only a small fraction of the solar spectrum lies between the bandgaps of GaAs and Si. It should be possible to increase the photocurrent in such a current-mismatched tandem cells by etching openings in the top GaAs cell to expose the bottom Si cell, as shown schematically in Fig. 10. Since

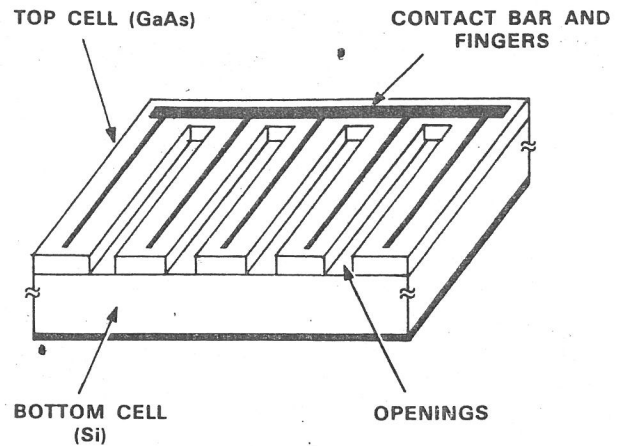


Fig. 10. Schematic diagram showing a GaAs-Si monolithic tandem cell with openings etched in the GaAs layers.

the exposed Si can generate 3-4 times more photocurrent per unit area than the unexposed Si, the net photocurrent of the cell is increased despite the reduction in area of the GaAs cell. A simple analysis (10) predicts that optimum performance will be achieved by exposing  $\sim 30\%$  of the Si area, which will increase the photocurrent by 90%. Monolithic tandem cells utilizing Si as the base material should be advantageous because the use of Si would not only reduce the material cost but also add a new degree of freedom for increasing the efficiency. For example, it should be possible to use the GaAs/Ge/Si structure as the substrate for the growth of AlGaAs to form the monolithic AlGaAs-GaAs-Si tandem cell, which has a theoretical efficiency of 40% (AM1). If AlGaAs could be grown directly on Ge/Si substrates, it would be possible to fabricate monolithic AlGaAs-Si tandem cells. A theoretical efficiency of 36% (AM1) is expected for this nearly optimum material system.

#### CONCLUSION

We have used several techniques to improve the quality of GaAs epilayers grown on Ge-coated Si substrates. Much better surface morphology and lower autodoping are achieved by decreasing the density of pits in the Ge coating layer. The growth interrupt and thermal cycling technique causes the dislocations in the initial GaAs layer to form loops and networks that reduce the propagation of dislocations into the junction region. Methods utilizing multiple

heterostructures and lateral overgrowth are also quite effective in reducing the dislocation density of the GaAs layers. Small-area solar cells with conversion efficiency of ~ 14% (AM1) have been obtained by using the growth interrupt and thermal cycling technique. Further improvement in cell performance should be achieved by further reducing the GaAs dislocation density. We have fabricated monolithic tandem cells that are composed of a GaAs top cell and a Si bottom cell connected by a thin epitaxial Ge layer. The characteristics of these cells justify further development of monolithic multiple junction cells using Si as the low bandgap material.

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