Conservative Optical Logic Devices: COLD

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I. INTRODUCTION

This chapter covers the union of two fields that seldom touch each other—optical devices and Boolean logic. The history of that interaction between those fields is traced below, and we will attempt to make the text readable to those active in one field but not the other. The "bottom line" of this chapter is easy to summarize: there is a new kind of optical logic device with very exciting features and capabilities. It can be

- Programmed to perform any of the 16 Boolean logic functions
- Built into a silicon chip along with the electronics needed to program it
- Operated at any bandwidth at which optical signals can be produced and read
- Made to consume no energy in so doing.

Many of those strange and wonderful properties were presaged by much earlier and still ongoing work on "conservative logic"—logic that does not dissipate any information and so is reversible.

Much of the work in this field has been done at the two universities with which the authors of this chapter are affiliated. This chapter is designed to provide interested readers an overview of that ongoing work.

II. A SHORT OVERVIEW OF CONSERVATIVE LOGIC

This chapter is concerned with the familiar Boolean logic operations and a type of variant that can accomplish the same things in a quite different manner. That variant is called *conservative logic*.

Boolean logic is, by and large, performed using physical devices called Boolean logic gates. The names of some of these gates are familiar to all readers: AND, OR, NOR, and so forth. The computer used to type this chapter operates with Boolean logic gates. They are small, integratable, fast, cheap, and accurate—and they are continuing to improve rapidly in all of those characteristics. There is a strong burden of proof on any serious developer of optical logic devices. Why bother with them, since electronics is wonderful, ubiquitous, and the incumbent? Many works on optical logic shirk their burden of proof that they are even potentially superior to electronics in at least

TABLE I
COMMON BOOLEAN GATES

A	B	AND (A, B)
0	0	0
0	1	0
1	0	0
1	1	1

A	B	OR (A, B)
0	0	0
0	1	1
1	0	1
1	1	1

A	B	NOR (A, B)
0	0	1
0	1	0
1	0	0
1	1	0

The truth tables for three common Boolean gates: AND, OR, and NOR. Altogether, there are $2^4 = 16$ such gates.

some conceivable circumstance. We will try to be somewhat more responsible in that regard herein.

By design, a Boolean logic gate has two binary inputs and one binary output. Given the two inputs, each gate has a special defining output. Most often, the lookup table defining the gate (called a truth table) is the easiest way to specify such a gate. Table 1 shows the truth tables of some familiar gates.

A striking aspect of these gates is that they destroy information. Two input bits result in one output bit. As a result, these gates are generally irreversible. If it is known that AND(A, B) $=$ 0, there is no way to determine the A and B values that led to that output. Such gates dissipate information. Since information, entropy, and energy are closely coupled in physics, the gates also dissipate energy. The energy required to destroy one bit of information at temperature T is $kT \ln 2$, where k is Boltzmann's constant. This might seem a trivial energy price to pay, as kT is unimaginably small at room temperature. The problem is that at high speed, billions of bits per second are destroyed and thus the power that needs to be removed can be very great. Furthermore, electronic computer chips do not operate near kT. More typically, they dissipate $\sim 10^9 kT$ per operation. Therefore computers need cooling—a lot of it. They are major energy consumers. This physics-of-computer insight is due to Landauer (1961).

Perhaps the high energy price could be avoided if no information were destroyed. The resulting "conservative logic gate" would have no physics-imposed minimum energy. This concept was explored by Bennett (1962) and Bennett and Landauer (1985), but two questions are raised. First, it is hard to believe that a conservative logic gate that makes no decision can accomplish anything useful. Are there conservative logic devices that can do useful things? The answer is yes. The first and still most widely studied conservative logic gates were due to Fredkin and Toffoli (1982). Although those gates and their uses are fascinating, they are not discussed here to keep the chapter focused and reasonably compact.

Second, barely touched by the early theorists of conservative logic was the quantum mechanical uncertainty relationship between energy and time. It says, effectively, that the less energy you use, the slower you must go. That relationship is probably more intuitive if stated in the other direction: the faster you go, the more energy you need. But what if a conservative optical logic gate can be operated at zero energy? Will that require infinite energy or no energy? These questions are addressed in the tale related below.

A. The Morphology and History of Optical Logic

Almost half a century of research in optical logic has led to some brilliant successes and more than a few widely publicized failures. This section provides a short account of that history. The trend in refereed publications in the field is on a dramatic upswing. The doubling time for publication rate is only twice that for Moore's law (Schaller, 1997)—the field is booming. This trend makes now an appropriate time to ask the question: How can we improve on the rather unspecific term *optical logic*? Can we find a simple way to assign any optical logic device to a well-defined and highly meaningful niche within the very broad field of optical logic? That points to the need for a morphological analysis of optical logic that is revealing in itself and provides a way to characterize the type of optical logic described later.

The universal genius Johann Wolfgang von Goethe wrote in 1795 that "morphology may be viewed as a theory in and of itself" and that "morphology may be said to include the principles of structured form" (Miller, 1995). Goethe explicitly dismissed "number and quantity" and chose to pursue qualitative statements. The modern use of the term *morphological analysis* is employed here in Zwicky's sense (Zwicky, 1969). Most publications using the phrase *morphological analysis* deal with lexical or grammatical morphologies or physical morphologies of biological entities; however, the idea is quite general. Morphological spaces (in the simplest instances) can be viewed as hyperspaces of many dimensions. Each of the mutually orthogonal morphological axes is quantized into two (usually) or more disjoint regions. This defines hyper-rectangular parallelepipeds that we call *morphological niches*. Once the morphological niches are defined, we find that each example occupies one and only one niche. It now becomes possible to determine the occupation level of each niche. In so doing, much can be learned about the field, and advances can be made by contemplating why some niches are empty or nearly so while others are heavily occupied.

Our use of morphological analysis is only very distantly related to the image processing method called *morphological processing* (Dougherty and Lotufo, 2003).

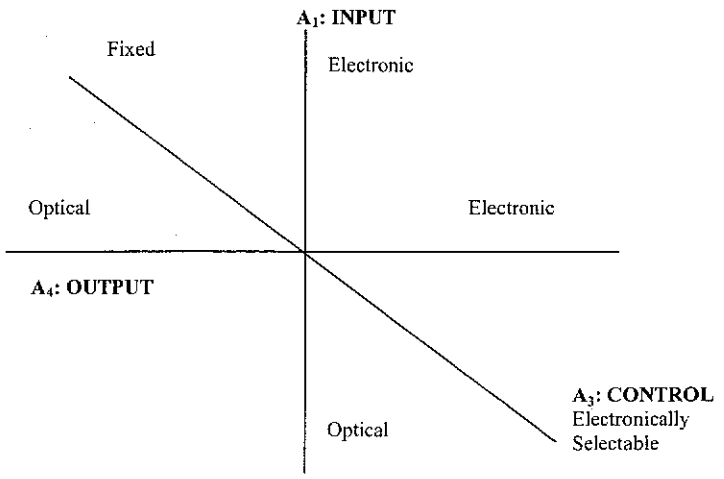

FIGURE 1. This diagram illustrates the optical logic morphological space but only at the expense of suppressing two axes and ignoring some possibilities along the axes illustrated. In this simplified case, there are $2^3 = 8$ morphological niches.

B. Morphological Axes

We consider a hyperspace with the following morphological axes:

- A_1: Input modality (Electronic, E; Optical, O, or Electronically modulated optics, EO)
- A_2: Operational principle (E; O; EO, Optical interaction with materials; Mechanical, M; Passive, P)
- A_3: Control of functionality (None—fixed functions, F; E; or O)
- A_4: Output modality (E or O)
- A_5: Input/output encoding (Same, S, or different, D)

A morphological niche for a logic device (electronic or optical) is specified by the vector

$$\mathbf{A}^T = (A_1, A_2, A_3, A_4, A_5).$$

Because complex five-dimensional spaces are difficult to visualize, a three-dimensional (3D) simplified morphology is shown in Figure 1.

C. Cascadability

Cascadability is possible (but not assured) when $A_1 = A_4$ and $A_5 = S$. Essentially all electronic logic devices are cascadable, but few optical logic

devices are. There are many devices for which $A_1 = O$ and $A_4 = O$, but $A_5 = D$. This observation is inserted to illustrate the utility of morphological analysis in discussing logic devices.

D. Electronic Logic Devices

Electronics occupies several niches.

$(E, E, F, E, S)^T$ is the most common. It is a simple fixed-function gate. It is cascadable.

$(E, E, E, E, S)^T$ is also widely used. Field programmable gate arrays (FPGAs) are an example.

E. The A_1 Axis in Optical Logic

O. A beam of light that is input into an optical logic device may already be modulated by amplitude, phase, polarization, and so on. For instance, it may arrive as a signal carrying information in and by that modulation.

E. It is quite common in optical logic to input the variables to be processed electronically and use optics to read the result. Much of the work reported here uses this approach.

EO. Some of the earliest optical logic gates used the nonlinearity of electrically driven lasers to achieve the desired nonlinearities.

F. The A_2 Axis in Optical Logic

Nearly all cases of optical logic have $A_2 = O$ or $A_2 = EO$. To most people, this is what defines *optical logic*.

G. The A_3 Axis in Optical Logic

Nearly all optical logic devices are fixed function, that is, in almost every instance the $A_3 = F$. We have introduced a new kind of optical logic for which the A_2 axis in optical logic $= E$. We have called these *universal logic gates*, because they can be switched electronically among any of the 16 Boolean logic gates.

H. The A_4 Axis in Optical Logic

In every case of optical logic gates known to us, $A_4 = O$. This (apparently) is the de facto definition of optical logic, as it is the only fixed morphological axis.

I. The A_5 Axis in Optical Logic

Sadly in view of the need for $A_5 = S$ for cascadability, all optical logic devices known to us exhibit $A_5 = D$.

J. A Short History of Optical Logic

While we have made a serious attempt to produce an unbiased bibliography of optical computing (see below), we cannot produce an unbiased history of the field. There must be editorial judgment on what is and is not important to include, so we make no apology for this.

We perceive the field as having progressed through multiple cycles of hope and hype followed by depression and inactivity. Here are the primary cycles we have observed.

1. *Cycle 1: Initial Enthusiasm Brought to a Crashing End*

> "If the only tool you have is a hammer, you tend to see every problem as a nail."—Abraham H. Maslow

Lasers, holograms, and nonlinear optics reawakened optics in the late 1960s and early 1970s. Suddenly physical optics became more important than geometric optics in terms of excitement generated. Nonlinearities had to be useful for something. But what? Logic seemed an obvious answer. Every form of nonlinearity from lasers to photorefractives was explored. Claims were made that were embarrassing to some of us even then about the future of "all-optical computers." At the heart of all computers is the logic, so optical logic was to be the way to keep Moore's law forces going.

This phase crashed twenty years ago when IBM physicist Robert Keyes published a paper entitled "Optical Logic in the Light of Computer Technology" (Keyes, 1985). It caused an instant furor in the fledgling optical logic community.

The Keyes paper was narrowly focused on the use of nonlinear optical devices to replace transistors as the logic components of a general purpose computer. To our knowledge, no one now seriously proposes such a thing, so obviously Keyes was right. So why revisit the paper now? Our reason is that

most of his arguments apply to optical logic broadly—not just for that narrow purpose.

The arguments that seem peculiar to the general purpose computer (cascadability, low cost, reliability, small size, low power, uniform and controllable fanout, and so forth) still apply to the more limited applications for optical logic practiced and contemplated today. If that is so, then optical logic devices failing those tests dramatically have an extra burden of proof if their inventors seriously propose that their devices be used.

Keyes remarked, "Attempts to introduce new technologies for logic gates often fail because a focus on device speed diverts attention from other factors." This statement is a cautionary warning readers (and perhaps even referees) in the field might attend. We have experiments involving thousands of dollars worth of equipment filling an optical table that achieve some logic operations at almost the speed of the transistors in the PC. Surely, the authors of such papers should offer us the readers some hope that these huge limitations might someday be overcome.

Elsewhere Keyes notes, "Circuits designed for widespread use and mass production must take into account the variability of device characteristics and operating conditions." Just because a doctoral student can make one at the end of an arduous thesis effort does not mean that it can be produced.

There is a tempting error that optical logic papers sometimes commit and is not new. Keyes saw it even two decades ago and warned against it. Sadly, his warning is often ignored. He said, "One must also avoid the error of comparing laboratory experiments with contemporary commercial technology, rather than with the advanced technologies that will be available when the laboratory results have been reduced to practice." Moore's law shows no sign of failure.

Keyes advanced specific criticisms against logic based on nonlinear optics. They concern size, reliability, and cascadability.

On size, he stated "Digital optical devices tend to be large, with dimensions in the ten to several hundred micrometer range." That tendency has changed only slightly, and submicron optical devices seem problematical even in principle.

The reliability requirement (in terms of fractions of operations of any logic element that are likely to fail) depends on the number of devices, how many operations per unit time are required of them, and mean time between failure for the system (as Keyes detailed in his paper). He concluded 20 years ago that a failure rate of 10^{-10} per hour or better was needed then. Twenty years of Moore's inexorable law make the current needs much more severe.

Cascadability is vital to digital computing. The problems concerning different input and output encryption and unknown and variable fanout have already been noted. Keyes also pointed out that connection reliability was

critical. He also noted that discrete component connections system fare poorly compared with integrated circuit connections. Level control (0s being real 0s and 1s being a predictable fixed value) also seemed easier in electronics than in optics.

It should be evident that Keyes' concerns are still valid. Making a full all-optical computer seems highly unlikely. However, the smaller lessons he sought to teach us are still often neglected.

We believe the following two rules would help the field if, as is unlikely, they were widely followed.

- Not everything that can be done optically should be done optically. Optical logic devices that cannot be defended as even potentially useful should be treated with caution or indifference.
- Authors should attend to the critical issues of size, reliability, and cascadability.

2. *Cycle 2: Specific Devices Reawaken Hope*

Four independent devices/systems appeared more or less simultaneously. Each was said to solve the problems. At least two of them were the subject of massive publicity efforts that led to even greater depression when the grandiose claims failed to be demonstrated. The devices were (in no particular order):

- A shadow casting system for optical parallel array logic systems (OPALS)
- Logic devices based on a multiple quantum well–type of device called a SEED
- Optical programmable logic arrays
- A technique based on pattern recognition and look up tables (a kind of two-dimensional [2D] cellular array processor) called *symbolic substitution*

All of these were much closer to the goal of practicality than the concepts for the first cycle. Unfortunately, the combination of hype and failure effectively killed the field.

3. *Cycle 3: The Era of the Semiconductor Optical Amplifier (SOA)*

Here, at last, optical logic became practical and useful. Perhaps the key change was the realization that (as Keyes was trying to indicate), the all-optical computer is not a feasible or even desirable goal. Optical logic must be a niche technology that is suitable for only some, not all, purposes. The niche filled by the SOA-based logic devices is signal processing in infrared communication. They are tremendously fast and practical for this purpose, and they can avoid costly optical-to-electronic-to-optical conversions. This cycle is still ongoing and has restored the credibility of the words *optical logic*.

4. *Cycle 4: COLD: Conservative Optical Logic Devices*

COLD aims at satisfying needs in other niche markets. Where it is applicable, it has uniquely wonderful properties. For many applications, however, it is not applicable. This (COLD) field is the topic of this chapter.

5. *Cycle 5: Integrated Silicon COLD*

Recently many integrated optical devices on silicon substrates have been developed and many more are being developed that combine small optical components on the same substrate as the electronics that operate them—a kind of "best of both worlds" approach. Those devices can be used for COLD.

6. *Cycle 6: The Golden Age?*

Optical logic suffers from its own problems (some of which are discussed here) and from competition with a far better-developed field of electronic logic and its inexorable rapid improvement (Moore's law in its various forms). Now it appears that trends in electronics that have been exhibited for the past 50 years may soon introduce expanded niches for optical logic. Here is a brief discussion of a subject whose details carry far beyond the scope of this chapter.

1. Accelerating charges in electronic logic circuits produce radiating electromagnetic fields, additional to low-range reactive electromagnetic fields.
2. Radiated power is proportional to the frequencies of several harmonics of the processor clock frequency.
3. Converting that into the current terms of Moore's law, the amount of power radiated doubles every 18 months.
4. To avoid evanescent leakage between components and "wires," they must be spaced several wavelengths apart.
5. The antenna mismatch between wavelength and component sizes may be improved somewhat, avoiding resonances.
6. At 10 GHz, the wavelength is about 0.5 cm in silicon surface waveguide. At 100 GHz (where Moore's law predicts we will be in 2013), the wavelength is still big: 0.5 mm.
7. Therefore, ultra-high clock cycle rates will require very large spacing of components to avoid major crosstalk problems. This suggests that the 50-year trend in electronics of simultaneous and proportional increase in speed and decrease in size can no longer occur. Increasing speed will require increasing size.
8. The optical wavelength of interest remains fixed at about 1.5 μm. Thus, optical components working at very high clock rates can be put much closer together than can electronic components.

9. It seems likely that on-chip optics will be important for ultra-high-speed chips.
10. Once a signal is in the optical domain, doing logic on it optically makes sense.
11. Optical logic could become ubiquitous in future computer chips.
12. That is especially the case if, as is the case, the optical logic elements can change functionality rapidly under user control.

III. Logics for Optics

For the most part, the history of optical logic has involved searching for ways for optical elements to implement familiar logical systems. Thus, the overwhelming majority of work has concentrated on implementing some form of Boolean logic in much the same way that electronics does. Although such an approach may seem obvious, it is not the only possible one. Recently work has begun to formulate new systems of logic that are particularly amenable to optical implementation. This section surveys three of these logics: logical digraphs, vector logic, and complex logic. Logical digraphs and vector logic are innovations in logical syntax. They both use a diagrammatic syntax that is easily implementable in optics. In addition, vector logic promises to be readily extendable to fuzzy logic. Complex logic extends traditional semantic systems to the complex plane. This yields a logical system that is more compatible with the wave equations typically used in optics.

A. Logic Digraphs for Optical Logic

A *directed graph* (*digraph*) is a mathematical object called a graph with directed edges. A *graph* is a network of nodes, called vertices, and line segments, called edges, between one or more pairs of vertices. A *directed edge* is an edge that comes out of a vertex and goes into a vertex in one direction only. Graphs can be diagrammed topologically as well as symbolized set-theoretically and algebraically. *Logic digraphs* are digraphs used in a diagrammatic logic to represent propositions and arguments for both the logic of terms and the logic of propositions. Such a diagrammatic logic is called digraph logic. Pioneering work in digraph logic has been done by Gardner, Mes, and Harary (Gardner, 1983: Mes's unpublished work is mentioned in the Appendix of Gardner and Harary, 1988). McCurdy and Westphal (2005) have enhanced and extended the work of Harary and Gardner.

Digraph theory is a part of combinatorial topology. *Topology* is the study of those properties of geometric objects that are invariant under continuous deformation. *Combinatorics* is the study of ways and numbers of ways

that discrete objects can be combined. Since digraphs are constructed by combining vertices and directed edges, they can be analyzed and explicated both combinatorially and topologically (Boltyanskii and Efremovich, 2001).

B. The Syntax of Logic Digraphs

The space of logic digraphs is n-dimensional, topological space. Syntactically, vertices may be placed in that space anywhere short of losing numeric identity, and edges may be inscribed as any continuous curve of any length greater than zero. However, pragmatically, it is convenient to place the vertices in the plane. When diagrammed, vertices are nodes labeled either P_i or $\overline{P}_i$, where $1 \leq i \leq m$ or $P, Q, R, \ldots, \overline{P}, \overline{Q}, \overline{R}, \ldots$ when the number of vertices is small. Another diagrammatic convention places the respective P_i and $\overline{P}_i$ at diametrically opposite locations on a circle. One further convention is that directed edges are to be straight lines except when diagramming edges in cycles. If labels for edges are needed, $\mathbf{e}_1, \mathbf{e}_2, \ldots, \mathbf{e}_n$ are used.

A well-formed logic digraph (*wfld* pronounced "woofled") includes any vertex and its label inscribed in the plane, any digraph in which a directed edge is drawn out of a vertex into a vertex, any digraph in which the direction of any edge has been reversed, any digraph in which the tail of a directed edge is detached from a vertex and then reattached to a vertex, and finally, any digraph in which a directed edge has been erased.

The mathematics of graph theory can be used to analyze and construct logical digraphs. One such mathematical notion that plays a major role in digraph logic is transitive closure of a digraph (Gross and Yellen, 2004) (Figure 2). Figure 2(a) is a digraph of a directed sequence of directed edges beginning out of vertex A via vertex B ending into vertex C. In such cases, the application of transitive closure permits a directed edge out of vertex A directly into vertex C [Figure 2(b)].

The result is an acyclic digraph called a *transitive graph*. Transitive closure is, obviously crucial for the semantics of arguments, but also, somewhat

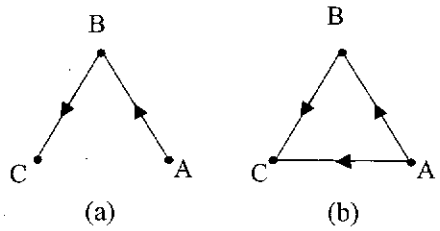

FIGURE 2. Illustrative directed graphs (digraphs). Figure 2(b) is derived from Figure (a) by a process called transitive closure that is important to the logic developed here.

surprisingly, for the semantics of conjunctional propositions. Two other mathematical notions are those of connected and disconnected digraphs. If F and G are digraphs and the labeled vertices of F are included in the vertices of G and, further, the edges of F are included in the edges of G, then F is a subgraph of G. A digraph is connected if there is an edge-vertex sequence, ignoring direction, between any two vertices in that digraph. Otherwise, a digraph is disconnected. The maximal connected subgraphs of a digraph are called *components* (Gross and Tucker, 1987).

C. *The Semantics of Logic Digraphs*

Digraphs can be used to represent propositions and arguments.

Propositions. Single propositions, $\mathbf{P}_i$, are directed edges into vertices $\mathbf{P}_i$, where $1 \leq i \leq m$. Typically, they are directed edges out of $\mathbf{P}_i$ [Figure 3(a)]. In such cases the logical negation of these propositions, $\sim\mathbf{P}_i$, are directed edges out of vertices $\mathbf{P}_i$ into vertices $\mathbf{P}_i$ respectively, that is, with edges reversed [Figure 3(b)].

Compound propositions are logic digraphs consisting of two or more directed edges. They are either connected digraphs, in which case they are conjunctional propositions, or they are disconnected digraphs, that is, they have two or more components, in which case they are alternational propositions. Connectedness and disconnectedness are topologically invariant properties of that digraph. Thus, in digraph logic the logical distinction between conjunctional and alternational propositions is displayed by the topological distinction between connected digraphs and disconnected digraphs. For example, conjunctional propositions of two conjuncts, $\mathbf{p} \wedge \mathbf{q}$, and an alternational proposition of two alternates, $\mathbf{p} \vee \mathbf{q}$, are diagrammed as shown in Figures 4(a) and 4(b).

Figure 4(a) consists of two edges as a single component, ignoring isolated vertices, and, hence, is a conjunctional proposition. Figure 4(b) also consists of two edges, each of which is a separate component and, hence, is an alternational proposition. The conditional proposition, $\mathbf{p} \rightarrow \mathbf{q}$, is diagrammed in Figure 4(c). Note that the same diagram also represents logically equivalent contrapositive of $\mathbf{p} \rightarrow \mathbf{q}$, $\sim\mathbf{q} \rightarrow \sim\mathbf{p}$. It, too, is not a conjunctional proposition since $\mathbf{p} \rightarrow \mathbf{q}$ is equivalent to $\sim(\mathbf{p} \wedge \sim\mathbf{q})$, but rather it is an alternational proposition since it is equivalent to $\sim\mathbf{p} \vee \mathbf{q}$.

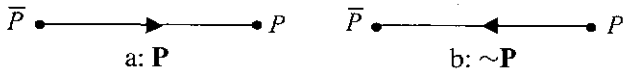

FIGURE 3. These simple digraphs show the distinction between $\mathbf{P}$ and $\sim\mathbf{P}$.

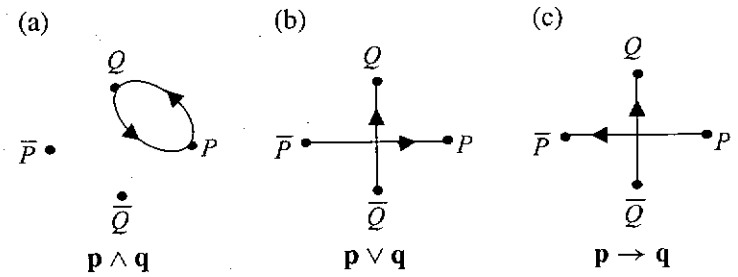

FIGURE 4. The relationships among propositions **p** and **q**.

Arguments. Propositions represented by directed edges can be combined in the same logical digraph to represent the premises of arguments. Applying transitive closure to such logical digraphs, directed edges for conclusions can be drawn literally and logically. The result is a digraph representing an argument. For example, Figure 5(a) is the logical digraph for the argument of affirming the antecedent and Figure 5(b) is the logical digraph for the argument of hypothetical syllogism.

D. Incidence Matrices for Logic Digraphs

In graph theory matrices can be used to represent digraphs algebraically. The incidence matrix **M** for a logic digraph has m rows, one for each vertex, and n columns, one for each edge. An entry m_{ij} in the i-th row and the j-th column of **M**, where $1 \leq i \leq m$ and $1 \leq j \leq n$ is

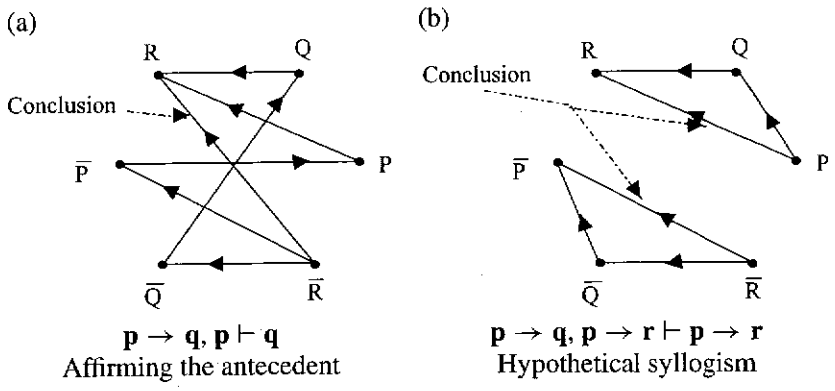

FIGURE 5. In Figure 5(a), transitive closure was applied once to draw the directed edge out of **Q** directly into **Q** representing the conclusion **q**. In Figure 5(b), transitive closure was applied twice to yield the directed edges that represent the conclusion **p** → **r**.

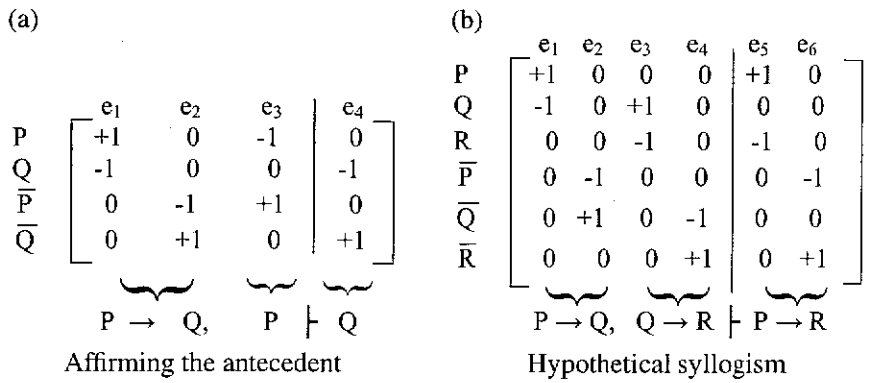

FIGURE 6. (a) The edge-columns for the premises, $\mathbf{e}_1$, $\mathbf{e}_2$, and $\mathbf{e}_3$, sum to the edge-column for the conclusion $\mathbf{e}_4$. Thus, transitive closure is captured algebraically by a kind of vector addition. (b) The edge-columns for premise $\mathbf{p} \rightarrow \mathbf{q}$, $\mathbf{e}_1$ and $\mathbf{e}_2$, and the edge-columns for premise $\mathbf{q} \rightarrow \mathbf{r}$, $\mathbf{e}_3$ and $\mathbf{e}_4$, require two separate applications of transitive closure, namely, $\mathbf{e}_5 = \mathbf{e}_1 + \mathbf{e}_3$ and $\mathbf{e}_6 = \mathbf{e}_2 + \mathbf{e}_4$ to yield the two edge-columns for the conclusion $\mathbf{p} \rightarrow \mathbf{r}$.

$+1$, if the j-th edge is incident out of the i-th vertex;

-1, if the j-th edge is incident into the i-th vertex; and

0, if the j-th edge is neither incident out of nor into the i-th vertex

(Swamy and Thulasiramin, 1981).

Thus, the vertex out of which a directed edge is incident is a logical source, whereas the vertex into which a directed edge is incident is a logical sink.

Incidence matrices can symbolize both digraphs for propositions and for arguments. In incidence matrices for arguments, the edge-columns for premises are all to be placed to the left of the edge-columns for the conclusion. A vertical partition line is inserted between the last of the premise edge-columns and the first of the conclusion edge-columns. For example, the incidence matrices of the digraphs for affirming the antecedent and hypothetical syllogism are shown in Figure 6.

E. Optical Digraph Logic

Digraph logic can be implemented optically with directed edges as conduits for light and vertices as entrance and exit ports. Networks of these would be passive means for doing logic. They would also be conservative in the sense that for all combinations of inputs where the presence of light represents 1 and the absence of light represents 0, the number of 1s and 0s in the inputs would equal the number of 1s and 0s in the outputs. Finally, every logical digraph

has a corresponding inverse digraph. For example, the inverse of the logical digraph for $\mathbf{p} \wedge \mathbf{q}$ is the digraph for $\mathbf{q} \wedge \mathbf{p}$. The reason for the invertibility of all logical digraphs is that they are permutation functions. All permutation functions are invertible. Logic can be done by *permuting* channels of light.

F. On the Way to Vector Logic

The space of vector logic is an n-dimensional space with a quasi-Cartesian coordinate system. Within that space vectors representing propositions have fixed locations, fixed directions, fixed lengths, and therefore fixed points of origination and termination. Digraph logic is a kind of relative vector logic with directed edges of no fixed location, no fixed length, with only relative directions and relative points of origination and termination. If, however, we wish to make certain spatial operations part of the syntax of our diagrammatic logic, then metric and projective properties must be imposed on the space of logical digraphs to provide the means for performing such logical operations as negation and contraposition. These types of imposition eventually induce a fixed point in that space which it is natural to treat as an origin. Some of the laws governing these spatial operations are those of the dihedral group $\mathbf{D}_4$, the group of the reflections of the square.

G. Vector Logic

Vector logic treats propositions as vectors in logical space. Logical space is an n-dimensional space whose axes are determined by the variables under consideration. Within this space, vectors represent propositions. Because we are concerned with Boolean logic, we take the space to be discrete, specifically the n-th power of $\{-1, 0, 1\}$ where -1 on an axis represents the negation of the variable associated with that axis. This chapter concentrates on two dimensions, p and q, but we have shown elsewhere (Westphal and Hardy, 2005) that the logic is easily extended to n dimensions.

Consider then a 2D space in which the axes are labeled by propositional variables. Two-dimensional space is used here for expositional reasons, but (Westphal and Hardy, 2005) the results also hold for n-dimensional space. To model Boolean logic, we consider only that discrete subspace in which the points have integer values between -1 and 1, understanding -1 to represent a value of "false" for the relevant variable. The resulting space is shown in Figure 7.

Within this space vectors represent propositions. For example, the vector from the origin to (p, q) represents "P $\vee$ Q." Translating this vector from the origin to (−p), yields (−p) $\rightarrow$ (q), which is naturally interpreted as

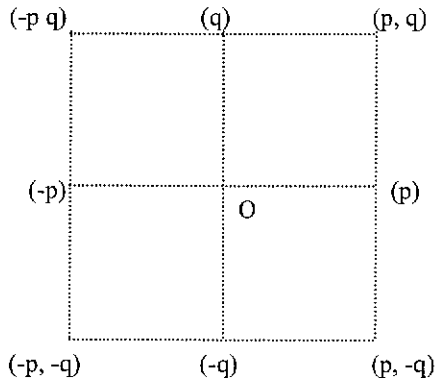

FIGURE 7. The 2D vector space for premises p and q and their negations. Propositions and theorems relating p and q can be worked out in this space to draw valid conclusions.

"$\sim P \rightarrow Q$." It is important that these two propositions are equivalent. Vector translation typically preserves propositional content with one interesting exception. Vectors that end at the origin are considered to be bound and express the conjunction of the literals at their starting point. As conjunctions they are not equivalent to any free vector. Figure 8 illustrates the interpretation.

Even at this stage of the exposition, some interesting logical relationships become apparent. For example, reversing any vector produces its dual. An important point is that since P is self-dual, it can be expressed both by the vector O $\rightarrow$ (p) and by (p) $\rightarrow$ O. Sliding a vector lengthwise through the origin produces a vector that expresses the negation of the original.

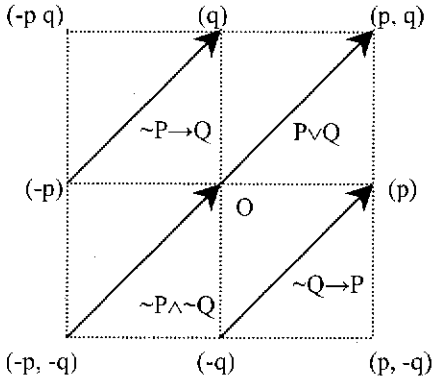

FIGURE 8. Vectors directed toward the origin and translations of those vectors have unique interpretations as shown. They are ANDs, not ORs, as are vectors pointing away from the origin.

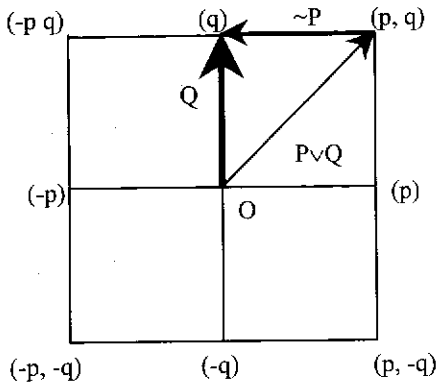

FIGURE 9. This figure shows how vector logic can draw the correct conclusion (q) from the two propositions P ∨ Q and ~P.

The real power of the system lies in the ability to model inference by vector addition. Provided the vectors involved are either all free or all bound, the proposition expressed by the sum of a set of vectors will be a logical consequence of the propositions expressed by the vectors in the set. Figure 9 illustrates this property with regard to disjunctive syllogism (P ∨ Q, ~P therefore Q), with the bold arrow representing the conclusion. The requirement that all vectors be free in this case constrains the interpretation of the top vector to ~P rather than P.

This allows us to express any proposition that is equivalent to either a disjunction of literals or a conjunction of literals and perform logical operations on them. We have suggested elsewhere (Westphal *et al.*, 2005) how such operations can be computed optically with simple Fourier optics. Similar results can be achieved using tunable prism deflectors (article forthcoming).

To achieve expressive completeness (the ability to express every function of Boolean logic), we introduce the notion of a system of vectors. A *system of vectors* is a set of vectors that jointly expresses a single proposition. We require that systems of vectors contain either only bound vectors or only free vectors. A system of bound vectors expresses the disjunction of what each of the vectors expresses individually, whereas a system of free vectors expresses the conjunction of what the vectors express individually. This provides the ability to express any proposition that can be expressed in either conjunctive or disjunctive normal form. Of course, as every Boolean proposition can be expressed in each of these forms, this yields expressive completeness. Figure 10 shows (P ∧ Q) ∨ (~P ∧ ~Q) as expressed by a system of free vectors.

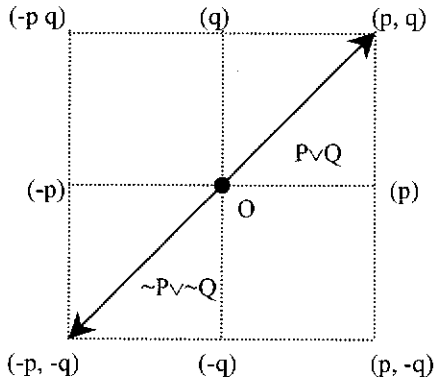

FIGURE 10. $(P \vee Q) \wedge (\sim P \vee \sim Q)$.

Further rules, such as those for combining systems of vectors, are presented in logic as a vector system (Westphal and Hardy, 2005). Clearly, much of Boolean logic can be accomplished vectorially. As we have shown, such representations are far easier to implement optically than are their binary counterparts. Whether all of Boolean logic can be captured in vector logic remains an open question.

H. Complex Logic

Boolean logic only allows two values, 1 and 0. There have been many extensions to Boolean logic based on allowing more values. For example, Łukasiewicz (1920) (in French, translation by McCall, 1967) suggested a logic with three values, and Post (1921) (reprinted by Van Heijenoort, 1967) offers logics with integer-many values. Fuzzy logic further extends Boolean logic by allowing all real values between 1 and 0 inclusive. Complex logic extends each of these logics (including Boolean) by allowing variables to take complex values. The value of a function in complex logic is thus a pair of numbers, one real and the other imaginary. We concentrate on the complex logic initially developed by Ramot *et al.* (2002, 2003), although we note an earlier formulation by Mizraji (1992).

The promise of complex logic with respect to optical implementation is that the logic will more easily mesh with the complex values used in waveform equations and still yield results that are interpretable within the context of Boolean and/or fuzzy logic. Again, in our approach, we try to adapt the logic to an optical implementation rather than conversely.

Just as fuzzy logic reduces to Boolean logic when the values are restricted to {0, 1}, complex logic should reduce to its base logic when the imaginary

components are 0. However, the inclusion of phase information allows propositions to "interfere" in much the same way that coherent beams of light can interfere with each other.

Although much work remains to be done both on complex logic itself and any potential optical implementation, early results are promising. For example, a central function in Ramot *et al.*'s presentation is *vector aggregation*. Vector aggregation allows multiple complex fuzzy sets to be summarized by a single one. Given a collection of sets $A_1, A_2, \ldots, A_n$, vector aggregation produces a set A such that for any x, the grade of membership of x in A is the weighted sum of the grade of membership of x in $A_1, A_2, \ldots, A_n$. If the weights are assumed to be equal, then the membership grade of x in A is given by the formula

$$\mu_A = \frac{1}{n} \cdot \sum_{i=1}^{n} \mu_{A_i}(x),$$

where the membership grades are complex. Electronically this function is nontrivial to compute. However, optics can compute it very easily. If we take each μ_{A_i} to be encoded as intensity and phase of mutually coherent beams of light, then μ_A is encoded by the intensity and phase of their superposition. In the case of two beams, this function can be implemented by adjusting the phase of one beam by $\pi/2$ and joining the beams with a beamsplitter. One output of the beamsplitter yields μ_A yields its complement. As with Fourier transform, we have a function that is easy to compute optically but difficult to compute electronically. However, in this case the function is part of logic.

Vector aggregation is not the only piece of complex logic that has a relatively simple optical implementation.

Clearly more research is needed—both on the development of complex logic and on its optical implementation. The same holds true of logical digraphs and vector logic. However, in each case clear advances are seen by focusing on matching logic to optics rather than the more traditional method of trying to mimic electronic logic with optics.

IV. Interferometers for Special Conservative Optical Logic Operations

Interferometry is key to much that follows. As some readers may not understand interferometry, a brief review is provided here. The illustrative example will be a Mach-Zehnder interferometer, but almost any interferometer can be used. Figure 11 shows a Mach-Zehnder interferometer.

Assume a beamsplitter takes two inputs from left and bottom (Figure 12). If it is necessary, a phase shifter may be inserted to one of the inputs to make

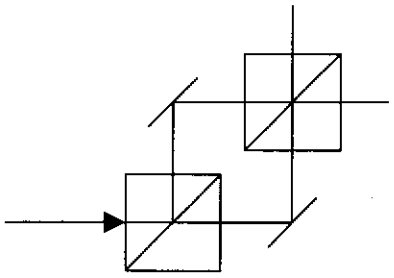

FIGURE 11. A simple Mach-Zehnder interferometer. The laser light enters from the bottom left (arrow). It is split into two beams by the first beamsplitter. A second beamsplitter combines the two beams into two distinct mixtures of the beams produced by the first beamsplitter.

two input beams interfere properly. Then the beamsplitter can be viewed as a pair of logic gates with inputs A and B and outputs C and D.

An interferometer can be interpreted as different logic gates with a different encoding method. There exist at least two classes of encoding for inputs: amplitude encoding and phase encoding.

For amplitude encoding, 0 is represented by no energy and 1 is represented by a fixed level of energy. If both A and B are 1, then they are mutually coherent. The interferometer is adjusted such that if both A and B are 1, then they offset in D output and all energy goes out from C. The results are shown in Table 2.

It is obvious that the output D can be interpreted to an XOR gate. Output C can be thresholded at either level ½ or 2. If ½ is the threshold, then the output C is an OR gate. On the other hand, if 2 is the threshold, then the output C can be interpreted as an AND gate.

In phase encoding, the amplitudes and polarizations of both inputs are fixed but the phases corresponding to Boolean values 0 and 1 differ by π. We

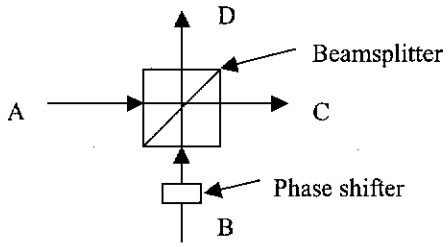

FIGURE 12. A beamsplitter with two inputs and two outputs; a phase controller in one beam is the basic unit studied. A and B are mutually coherent inputs to the beamsplitter leading to two mixed output beams C and D. The phase shifter affects how the beams are mixed.

TABLE 2
AMPLITUDE ENCODING

Input A	Input B	|Output C|²*	|Output D|²
0	0	0	0
0	1	½	½
1	0	½	½
1	1	2	0

* The detected outputs have patterns that can be used (after thresholding) to implement OR and XOR gates.

assume that the phase of input B is shifted by $\pi/2$. The response table for this case is shown in Table 3.

For inputs, we assume that $-1/\sqrt{2}$ is interpreted by 0 and $1/\sqrt{2}$ is interpreted by 1. In this coding schema, the output C can be viewed as an XOR gate and the output D can be viewed as a COINC logic gate after detection. However, inputs $(-1/\sqrt{2}, -1/\sqrt{2})$ vs. $(1/\sqrt{2}, 1/\sqrt{2})$ and inputs $(-1/\sqrt{2}, 1/\sqrt{2})$ vs. $(1/\sqrt{2}, -1/\sqrt{2})$ are distinguishable before detection. In other words, this pair of gates is reversible before detection.

Having constructed XOR/COINC logic gates with Mach–Zehnder interferometers, it is natural to ask what kinds of logic gates will be obtained if more than one beamsplitter and phase shifter are cascaded when if a certain kind of coding schema is used—say, phase coding. For example, can we construct the AND, OR, NAND, and NOR gates. Surprisingly, we can prove that logic gates that can be constructed by beamsplitters and phase shifters, or even any linear devices, are very limited if inputs are encoded by phases.

Conservative optical devices must obey the energy conservation law. Thus, the output energy should be same as the input energy. Conversely, all conservative optical devices are reversible. That means, if the relationship between

TABLE 3
PHASE ENCODING

Input A	Input B	Output C	Output D	|Output C|²	|Output D|²
$-1/\sqrt{2}$	$-1/\sqrt{2}$	0	$-i$	0	1
$-1/\sqrt{2}$	$1/\sqrt{2}$	-1	0	1	0
$1/\sqrt{2}$	$-1/\sqrt{2}$	1	0	1	0
$1/\sqrt{2}$	$1/\sqrt{2}$	0	i	0	1

The prediction signals from a phase-modulated two-input interferometer produce two outputs that are clearly reversible (conservative).

TABLE 4
ACHIEVABLE INPUT–OUTPUT PAIRS

A	B	C_1	D_1	C_2	D_2	C_3	D_3	C_4	D_4
0	0	0	1	0	1	0	1	½	½
0	1	0	1	0	1	0	1	½	½
1	0	0	1	0	1	1	0	½	½
1	1	0	1	1	0	1	0	½	½

A and B are inputs, and C_i and D_i are pairs of possible outputs. It is assumed that 0 and 1 values of A and B represent physical inputs $-1/\sqrt{2}$ and $1/\sqrt{2}$, respectively; 0 or 1 Outputs represent $|\text{output}|^2$ is 0 or 1.

input and output is expressed as a function $\mathbf{O} = \mathbf{f}(\mathbf{I})$, where $\mathbf{I} = (I_1, \ldots, I_n)$ and $\mathbf{O} = (O_1, \ldots, O_n)$, then the function $\mathbf{f}$ is a reversible function. In other words, given any $(O_1, \ldots, O_n)$, there is a *unique* $(I_1, \ldots, I_n)$ such that $(O_1, \ldots, O_n) = \mathbf{f}(I_1, \ldots, I_n)$. These two conditions can help rule out many logic gates (Table 4).

Because phase coding schema is being used, all possible inputs have the same energy. So if outputs are encoded by the energy after detection, then one output is 0 if and only if the other output is 1.

The gates represented by C_1 and D_1 are **0** and **1**. We will show that cascading simple gates, or furthermore, *any* linear optical logic gate, cannot produce these.

The gates represented by C_2 and D_2 are very desirable. They are AND and NAND. The former is useful in many cases, but the latter is more important, as all of the other 15 Boolean gates can be built from NAND gates.

The gates represented by C_3 and D_3 are not very interesting, but they are not precluded by energy conservation.

The gates represented by C_4 and D_4 are not Boolean functions if energy 1 is interpreted as 1 and energy 0 is interpreted as 0. However, it also represents the function **1** if we interpret energy ½ outputs as 1 and energy 0 outputs as 0. It is clear that more restrictions are needed to narrow which gates are achievable in the manner.

The reversible argument can be used to exclude some possible outputs. That argument states that the outputs must be distinct and uniquely determined for each input pair. So if all nonzero outputs have the same phases, then all the above pairs of outputs are not possible. If phases of nonzero outputs can have two possible values (e.g., 1 and -1 or i and $-$i) before detection, then C_1/D_1 and C_2/D_2 can be excluded by the pigeon-hole principle. (The pigeon-hole principle asserts that if we have fewer pigeon holes than pigeons and we put every pigeon in a pigeon hole, then there must result at least one pigeon hole

with more than one pigeon.) However, C_3/D_3 and C_4/D_4 cannot be excluded. Actually, the trivial direct output will generate C_4/D_4.

This output is not a very surprising or profound result, but it serves as a good introduction to the more general and interesting methods and results. We can prove the following theorem.

Theorem 1. *For a linear two-inputs, two-outputs optical logical system, if Boolean* 0 *and* 1 *are interpreted by beams with equal energy but opposite phases, then the only possible outputs are XOR/COINC or* **0/1** *if at most two possible outputs are allowed (that means no thresholding is allowed).*

Proof. A simple Mach–Zehnder gate produces XOR/COINC output, and a trivial direct output (that means two outputs are just two inputs) will produce **1** function after detection. Therefore, we just have to prove that these two pairs of functions are the only two pairs of functions we can get for linear optical logical gates.

Assume we encode 0 and 1 by the input $-\alpha$ and α, respectively. So the inputs $(-\alpha, -\alpha)$ and (α, α) are encoded by $(0, 0)$ and $(1, 1)$ respectively. Note that $(c\alpha, c\alpha) = (-\alpha, -\alpha)$, where $c = -1$. So if $f(\mathrm{a}, \mathrm{b})$ is a linear function, then $f(-\alpha, -\alpha) = -f(\alpha, \alpha)$. That means, the outputs of $(0, 0)$ and $(1, 1)$ have the same energy but with opposite phases. Thus, after detection the outputs of $(0, 0)$ and $(1, 1)$ are the same. Similarly, we can prove that the output of $(0, 1)$ has the same energy as the output of $(1, 0)$. Thus the only possible output functions are the four functions shown in Table 5.

By energy conservation requirement, if one output is XOR or COINC (after detection), then the other one must be COINC or XOR, respectively. If one output is **0**, then the other one must be **1**. If one output is **1**, the other one can be either **0** or **1**. So the only pair that must be excluded is **0/1**.

Toward contradiction, we assume that there is an optical linear gate that can generate **0/1** pair. Let the output function for **1** output be f and assume $f(\alpha, \alpha) = \boldsymbol{\beta}$ and $f(-\alpha, \alpha) = \boldsymbol{\gamma}$. Then $f(-\alpha, -\alpha) = -\boldsymbol{\beta}$ and $f(\alpha, -\alpha) = -\boldsymbol{\gamma}$. Besides, $|\boldsymbol{\beta}| = |\boldsymbol{\gamma}| = \sqrt{2}|\alpha|$. We assume $c = \boldsymbol{\gamma}/\boldsymbol{\beta}$. So $|c| = 1$ and $\boldsymbol{\gamma} = c\boldsymbol{\beta}$.

TABLE 5
THE ONLY PAIRS OF LOGIC OPERATORS THAT CAN BE IMPLEMENTED INTERFEROMETRICALLY AND REVERSIBLY

Input A	Input B	XOR	COINC	0	1
0	0	0	1	0	1
0	1	1	0	0	1
1	0	1	0	0	1
1	1	0	1	0	1

By the linearity of the function, $f(c\alpha, c\alpha) = cf(\alpha, \alpha) = c\beta = \gamma = f(-\alpha, \alpha)$. Besides, if $(c\alpha, c\alpha)$ are two inputs for the gate, then the output for the other output is $c0 = 0$. So $(c\alpha, c\alpha)$ generates exactly the same outputs as $(-\alpha, \alpha)$. Since an optical logic gate is reversible, $-\alpha = c\alpha$ and $\alpha = c\alpha$. So $c = -1$ and $c = 1$, which is a contradiction. This proves that **0/1** is *not* a possible output. □

Another output coding schema is analyzed in the following theorem. We proved that if phase coding is also used for output, then virtually nothing of interest is gained.

Theorem. *If both inputs and outputs are encoded by equal-energy opposite-phase beams, then the only two inputs/two outputs Boolean functions that can generate are* $f(A, B) = A$, $f(A, B) = \sim A$, $f(A, B) = B$ *and* $f(A, B) = \sim B$.

Proof. Assume that $-\alpha$ is used to encode 0 and α is used to encode 1 for inputs. Let f be an output function, $f(-\alpha, -\alpha) = \beta$ and $f(-\alpha, \alpha) = \gamma$. By the linearity, $f(\alpha, \alpha) = -\beta$. Since it is assumed that the output function is a Boolean function, there are just two possible values for all possible inputs: either $\gamma = \beta$ or $\gamma = -\beta$. If it is the former case, then $f(-\alpha, \alpha) = f(\alpha, \alpha)$ and $f(\alpha, -\alpha) = f(-\alpha, -\alpha)$. If the output β is interpreted by 0 and $-\gamma$ is interpreted by 1, then the corresponding Boolean function f is exactly the function $f(A, B) = B$. If the output β is interpreted by 1, then $f(A, B) = \sim B$. If $\gamma = -\beta$, then $f(-\alpha, \alpha) = f(-\alpha, -\alpha)$ and $f(\alpha, -\alpha) = f(\alpha, \alpha)$. If β is interpreted by 0, then $f(A, B) = A$; otherwise $f(A, B) = B$. This finishes the proof. □

In addition, we can also prove that it is not possible to construct a Fredkin gate only by linear devices.

A Fredkin gate (Fredkin and Toffoli, 1982) is a reversible logic gate with three inputs and three outputs. It is very important because it is the first reversible logic function that can generate all Boolean logic functions. A Fredkin gate has three inputs a, b, c, and three outputs a′, b′, and c′ such that c′ = c and if c = 0, a′ = a, b′ = b; if c = 1, a′ = b and b′ = a. It is natural to ask whether it is possible to construct a conservative interferometric Fredkin gate. Here, we prove that it is not possible under certain restrictions.

Theorem. *It is not possible to construct a linear optical Fredkin gate if equal-energy opposite phases are used to encode* 0 *and* 1 *for inputs and equal-energy opposite phases or energy after detection are used to encode* 0 *and* 1.

TABLE 6
INPUT/OUTPUT COMPLEX VALUES PRODUCED BY A SIMPLE INTERFEROMETER

Input A	Input B	Output C	Output D
$-1/\sqrt{2}$	$-1/\sqrt{2}$	-1	0
$-1/\sqrt{2}$	$1/\sqrt{2}$	0	$-i$
$1/\sqrt{2}$	$-1/\sqrt{2}$	0	i
$1/\sqrt{2}$	$1/\sqrt{2}$	1	0

Proof. Assume such a linear optical gate can be constructed and input $-\alpha$ is interpreted as 0 and α is interpreted as 1.

If the outputs are encoded by equal-energy opposite phases, then consider inputs for $(-\alpha, \alpha, -\alpha)$ and $(\alpha, -\alpha, \alpha)$. These two inputs are opposite each other, so all three of their outputs have the same energy but with opposite phases by the linearity. Therefore, their outputs should have different values for all a′, b′, and c′. However, these two inputs should be interpreted as (0, 1, 0) and (1, 0, 1), respectively, and their outputs should be interpreted as (0, 1, 0) and (0, 1, 1), respectively, by the definition of Fredkin gate. Thus the output a′ should be the same for both inputs, which is a contradiction.

Suppose the outputs are encoded by different energy levels. Then consider the inputs $(-\alpha, -\alpha, -\alpha)$ and (α, α, α). By the linearity, all three of their outputs have the same energy but opposite phases. That means three outputs have the same value after detection. However, these two inputs are interpreted as (0, 0, 0) and (1, 1, 1) and their outputs are the same as their inputs, which are different. That is also a contradiction. This finishes the proof of the theorem. □

Even though the possible logic gates constructed by linear devices are limited, outputs of interferometers can carry more information before detection.

TABLE 7
INPUTS ARRANGED IN GRAY CODE FASHION*

Input A	Input B	Output C	Output D
$-1/\sqrt{2}$	$-1/\sqrt{2}$	-1	0
$-1/\sqrt{2}$	$1/\sqrt{2}$	0	$-i$
$1/\sqrt{2}$	$1/\sqrt{2}$	1	0
$1/\sqrt{2}$	$-1/\sqrt{2}$	0	i

* This is Table 5 with the inputs arranged in Gray code fashion to illustrate some features of the transitions from one input to the next.

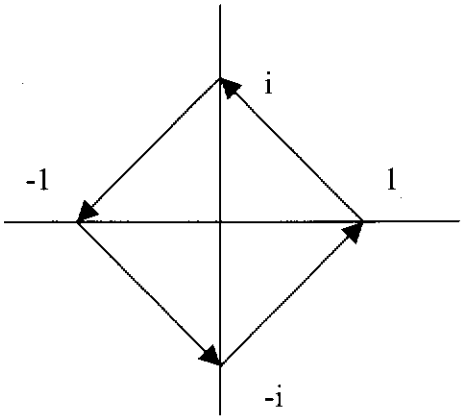

FIGURE 13. Nonzero outputs of the interferometer arranged in a Gray code.

Consider the simple construction described in Figure 12. Assume possible inputs of A and B are $1/\sqrt{2}$ or $-1/\sqrt{2}$. To make them interfere properly, a $\pi/2$ phase shift is needed in one arm. The resulting input/output pattern is shown in Table 6.

Obviously, this is reversible. Here, the input pairs are written in lexical Boolean order: (0, 0), (0, 1), (1, 0), and (1, 1). If a Gray code is used (a Gray code is an ordering of 2^n binary numbers such that only one bit changes from one entry to the next) for ordering, the results in Table 7 are obtained.

Figure 13 shows the nonzero outputs as they progress along the unit circle in the complex domain. The progression of nonzero outputs from a simple interferometric logic gate constitutes a Hamiltonian cycle. (A Hamiltonian path is a path that passes through every vertex of a graph exactly once.

TABLE 8
EFFECTS ACHIEVABLE BY PHASE SHIFT VALUES OTHER THAN $\pi/2$*

Input A	Input B	$c = 0$		$c = \pi/2$		$c = \pi$		$c = 3\pi/2$	
		C	D	C	D	C	D	C	D
$-1/\sqrt{2}$	$-1/\sqrt{2}$	$(-1-i)/2$	$(-1-i)/2$	0	$-i$	$(-1+i)/2$	$(1-i)/2$	-1	0
$-1/\sqrt{2}$	$1/\sqrt{2}$	$(-1+i)/2$	$(1-i)/2$	-1	0	$(-1-i)/2$	$(-1-i)/2$	0	$-i$
$1/\sqrt{2}$	$-1/\sqrt{2}$	$(1+i)/2$	$(1+i)/2$	0	i	$(1-i)/2$	$(-1+i)/2$	1	0
$1/\sqrt{2}$	$-1/\sqrt{2}$	$(1-i)/2$	$(-1+i)/2$	1	0	$(1+i)/2$	$(1+i)/2$	0	i

* The $\pi/2$ case is included for comparison. The table shows only some of the possible effects.

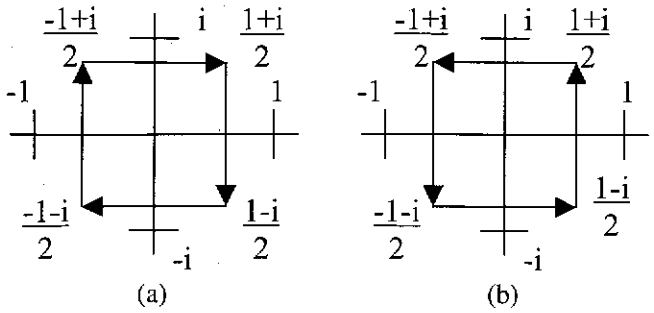

FIGURE 14. Outputs of a Mach-Zehnder interferometer with $c = 0$ ordered by a Gray code.

A Hamiltonian path that is also a loop is called a Hamilton [or Hamiltonian] cycle.)

However, if the phase shifter c changes the phase of input B by other values, then the following outputs before detection are obtained (Table 8).

The nonzero outputs for $c = 3\pi/2$ also constitute a Hamiltonian cycle but with the opposite direction. For $c = 0$ or $\pi/2$, four possible outputs ordered with a Gray code of input form a Hamiltonian cycle with a square shape as with the opposite direction. Figure 14 shows outputs C and D when $c = 0$.

V. TOWARD AN ALL-PASSIVE NOR GATE

In related designs, the relative phase between two laser beams at a beamsplitter is used to select the desired outputs. The calculations (see Figure 1) are based on the fact that the phase difference between the transmitted and reflected beams from a beamsplitter is $\pi/2$ (Traub, 1999) and that the change of phase between $\vec{S}$ and $\vec{P}$ polarized laser beams after reflection from a 45° mirror is π. We have verified this property experimentally. We assume that a polarizing beamsplitter introduces a phase shift of $\varphi + \pi/2$ when the $\vec{S}$ component of the laser beam is reflected, and a phase shift of φ when the $\vec{P}$ component of the laser beam is transmitted. φ is a phase dependent on the properties of the polarizing beamsplitter.

Figure 16 shows an all-passive XNOR or coincidence gate. The inputs are polarization dependent for fixed values of the phases of the inputs. The relative phase between inputs, as well as the angles of the half waveplates, are determined from the desired values of output 2. The logic state 0 is represented by the $\vec{P}$ polarized input beam, while the logic state 1 is represented by the $\vec{S}$ polarized input beam.

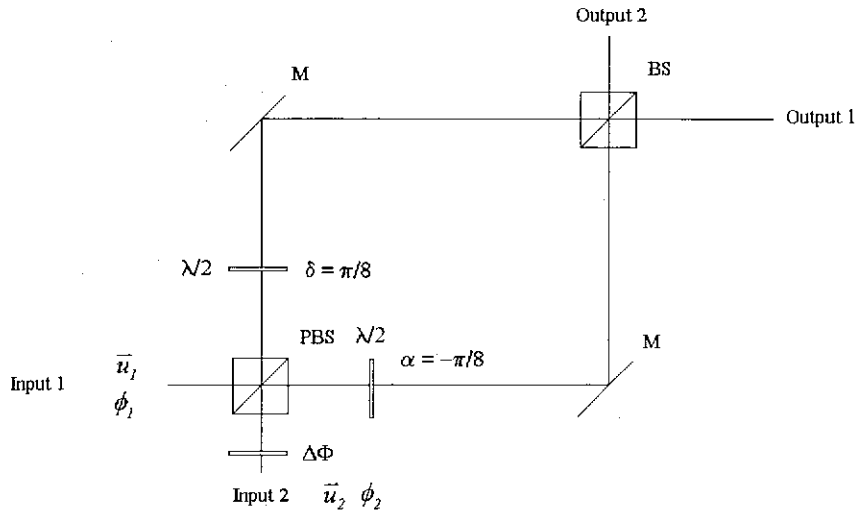

FIGURE 15. Optical layout; $\vec{u}_1$ and $\vec{u}_2$ are the inputs polarization vectors, respectively. BS, Beamsplitter; PBS, polarizing beamsplitter.

Table 9 shows the different polarizations and phases at output 2 for the different inputs. The phase difference between the two inputs chosen is $\Delta\phi = \phi_2 - \phi_1 = \pi/2$. The angles α and δ of the two half waveplates (Figure 15) are $-\pi/8$ and $\pi/8$, respectively, for the desired outputs. The intensity unit is I, and φ_0 is a constant phase. Table 10 shows the values of the polarizations, intensity, and phase at output 1.

When the polarizations of the input beams are different, the two input beams combine at the polarizing beamsplitter (PBS) and follow the same path, on which they interfere at one of the two half-waveplates. The emerging laser beam is then split at the beamsplitter, retaining its polarization.

When the two input beams have identical polarization, each beam travels a different path, and they interfere as they enter the final beamsplitter. A change

TABLE 9
POLARIZATIONS AND INTENSITIES AT OUTPUT 2 FOR DIFFERENT INPUTS. NOTE THE XOR AT OUTPUT 2

Inputs and intensity (I)	Output intensity (I)	Output polarization
(0, 0), 1	1	1
(1, 1), 1	1	1
(0, 1), 1	1	0
(1, 0), 1	1	0

TABLE 10
THE LOGIC STATES AT OUTPUT 1

Inputs and intensity (I)	Output intensity (I)	Output polarization
(0, 0), 1	1	0
(1, 1), 1	1	0
(0, 1), 1	1	0
(1, 0), 1	1	0

of phase is necessary for the (0, 0) input to modify the output 1 to a NOR gate.

We are currently in the process of testing the XNOR gate and are also working toward building a totally passive NOR gate based on related principles. At the same time, we are working on structurally identical gates whose inputs and outputs are phase dependent rather than polarization dependent.

VI. THE MACH-ZEHNDER INTERFEROMETER AS AN OPTICALLY CONTROLLABLE DIGITAL LIGHT DEFLECTOR

The most powerful COLD approach we have found to date involves a digital light deflector (DLD). We can make it conservative, because we can build the DLD out of conservative operations such as the Mach-Zehnder interferometer.

Analog light deflectors suffer from several problems. First, accuracy problems are inherent in any analog system. Second, none of them are random access. Third, mechanical scanners are slow (except for spinning mirrors or prisms or holograms), whereas electro-optic deflectors are faster but do not achieve high numbers of resolvable spots. Acousto-optic deflectors have many advantages but they tend to be low efficiency and to consume a large amount of power. Those shortcomings spurred the invention of the DLD (Kulcke *et al.*, 1964; Soref and McMahon, 1965; Nelson, 1964).

A DLD is an N-stage system wherein the path taken by the light is the cumulative effect of binary path choices made in all stages. Figure 16 shows a one-stage DLD and Figure 18 shows a two-stage DLD.

Now suppose single-stage DLDs are cascaded as shown in Figure 17. In general, N stage gives 2^N possible output positions. The output positions can be accessed randomly. The critical time is the switching time for each stage.

A Mach-Zehnder interferometer can easily be modified to look like a single-stage DLD as suggested in Figure 18.

The following unique properties make this DLD so important:

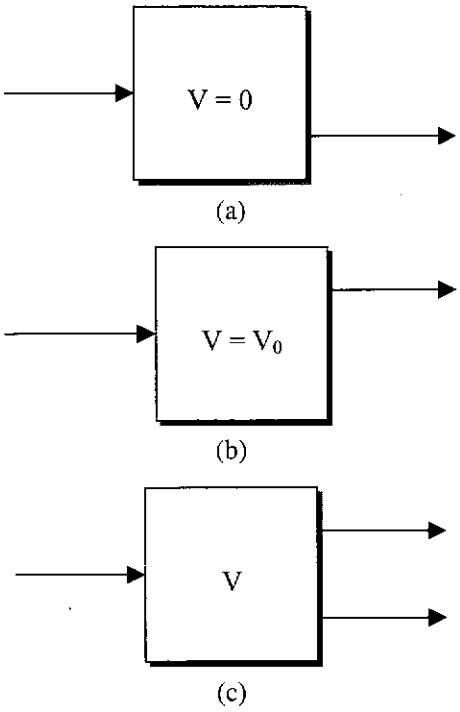

FIGURE 16. Suppose the light comes out the bottom when the applied voltage is 0 (a) and out the top when it is V_0 (b). Then the value of V_{in} determines the position of the exiting light. This is a single-stage DLD and represented here by (c).

1. It is all optical switching—light switching light. If the input control beam is phase modulated at any frequency, the DLD will keep pace with that modulation. It does not limit signal bandwidth.
2. Being passive, it costs no energy.
3. It is information conservative and hence fully reversible. We make use of the reversibility next.

Consider a two-stage DLD to take a single beam into one of four possible output positions depending on two control phases. It could be followed by a reversed two-stage DLD that takes whatever output position the first two stages produces and sends it into a single-output position, so long as its control signals match the control signals of the two-stage DLD. We call this second two-stage system a digital light combiner, (DLC). Figure 19 shows these two systems (DLD and DLC) working together.

Caulfield (2002) has explored the use of such complex do-nothing machines as a general paradigm for invention. By placing a controllable operator

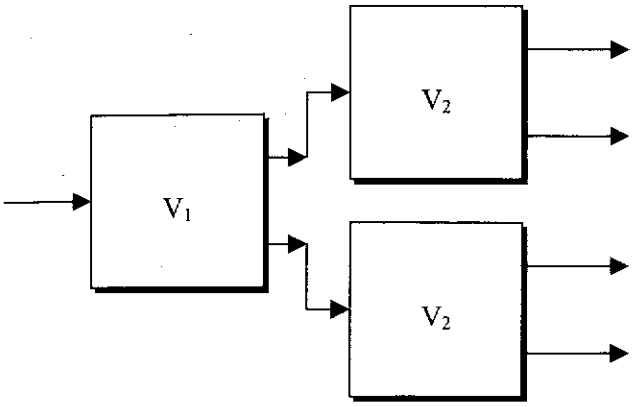

FIGURE 17. After two stages, there are four selectable output positions—one for every V_1-V_2 pair.

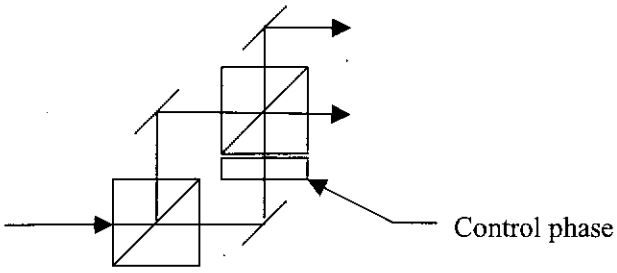

FIGURE 18. The entire energy of the input beam goes either to the top or bottom output depending on the phase of one beam relative to the other. A mirror is used to direct both output beams in the same direction. This is easily recognized as a single-stage DLD.

somewhere between the input and output, they often can perform useful functions, as shown in Figure 20.

A mask selects the positions (control signal pair) that will be allowed to pass. Each of the 16 possible mask functions corresponds to a unique one of the 16 Boolean logic gates.

Now, suppose the mask is not (as assumed above) a binary transmit or absorb function but a transmit or reflect function. The transmitted light corresponds to one Boolean function, and the reflected light (viewable using a beamsplitter in the input beam) is the complementary function. XOR and COINC are complementary. AND and NAND are complementary, and so forth.

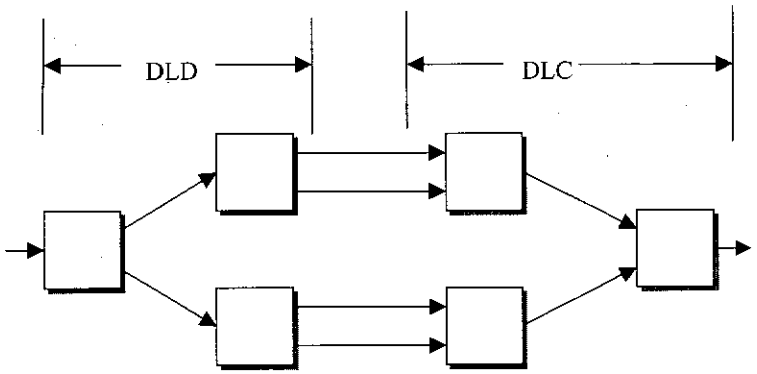

FIGURE 19. A DLD followed by a DLC is a very complex way of accomplishing nothing. The output beam is in the same place regardless of the controls on the DLD and DLC, so long as they match.

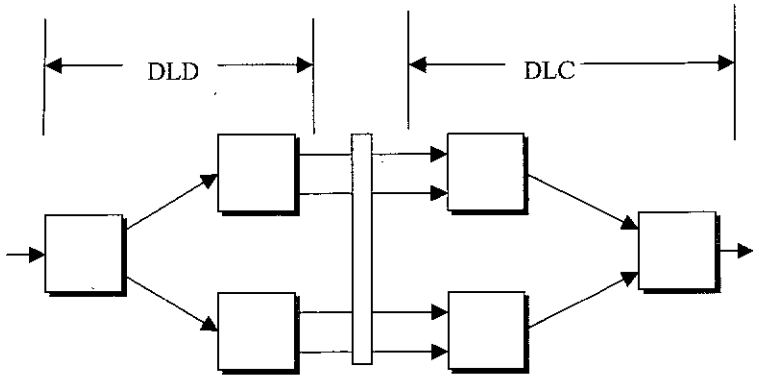

FIGURE 20. A DLD followed by a DLC with a mask between them embodies whichever Boolean function was used to design the mask. This is the basic concept of the DLD-based generalized logic device.

A. Morphology of the DLD-Based Logic Device

The morphologic axes are those of interest:

- A_1: Input modality (Electronic, E; Optical, O, or Electronically modulated optics, EO)—In this case the arguments of the function being evaluated are input as phases of the "control beam" relative to the signal beam. These may be "given" in the sense that the signals being processed may arrive phase

modulated. Alternatively, they can be set locally using a phase modulator that is electronically controlled. Thus there are two versions: O and E.

- A_2: Operational principle (E; O; EO, Optical interaction with materials; Mechanical, M; Passive, P)—This is strictly optical—O.
- A_3: Control of functionality (None—fixed functions, F; E; or O)—A mask must be set electronically, so this is E.
- A_4: Output modality (E or O)—The output is purely optical—O.
- A_5: Input/output encoding (Same, S, or different, D)—Unfortunately, the input and output encryption are different—D.

Thus we have (O, O, E, O, D) and (E, O, E, O, D) versions.

B. Integration of DLD Logic Onto a Silicon Chip

Silicon optics is increasing dramatically in terms of investment of government and private funds. For COLD, it raises the exciting possibility of optical logic devices that, compared with their bulk optical counterparts, have numerous potential advantages including the following:

- Small size (this applies laterally, where dimensions are several millimeters and vertically, where they are several microns). Small size also gives very low latency.
- Low operation voltages (volts, not kilovolts)
- Low cost (in production)
- Easy, fast operations (built-in electronics on the same chip, low voltages, etc.)
- No misalignment (they are built aligned and stay that way)
- Ruggedness. Neither integrated optics nor integrated electronics chips are likely to be injured by dropping or other mishandling that would surely destroy a bulk optical system.

All that is needed is an interferometer of some sort, and they abound. For example, Mach-Zehnder interferometers have been made in silicon, and Caulfield *et al.* (2005) suggest using one of the designs—resonant microring structures—for DLD logic. Figure 21 is a sketch of an integrated optical Mach-Zehnder interferometer drawn to resemble its bulk optical counterpart for reader convenience. It has two input and two output waveguides and a phase controller for electronic control.

The mask functions can be implemented by another such interferometer for each output. The unwanted light is removed from the beam by interferometry. Alternatively, and perhaps more simply, the light can be coupled into an adjacent waveguide by inducing the appropriate phase change along the coupling region.

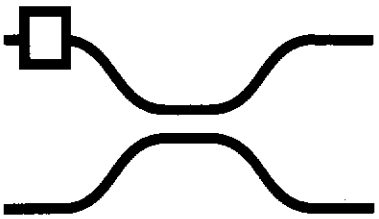

FIGURE 21. Construction of an integrated Mach-Zehnder interferometer (actually, just the beam combining beamsplitter section) is straightforward. By adjusting the phase with the modulator shown, all of the light from both input beams can go into either of the output beams. This is also a single-stage DLD.

VII. MULTIPLE COLD CHIPS

These new chips have new capabilities whose value cannot be estimated now. For instance, all current very high-speed parallel processes use single instruction multiple data (SIMD) systems, because there is no convenient rapidly reprogrammable general optical gate. The creation of those gates allows new approaches such as multiple instruction multiple data (MIMD) systems. Computer science has paid little attention to MIMD systems, because they are difficult to understand and not readily achievable in simple fast systems. Our work will change at least the second condition. Suitable devices will be easy to acquire. We imagine the FPGA controlling the gate functionality of a hybrid (electrooptic) MIMD system.

Crudely, the hybrid chip that is our ultimate goal would resemble Figure 22. This is a very flexible system. It goes beyond FPGAs and PLAs that have programmable interconnections to gates with programmable functionality interconnected in programmable fashion. Extending the Flynn notation (Flynn, 1995) somewhat, we can call this a flexible instruction/multiple data (FIMD) system. As yet, there is no general way to use the full power of a FIMD system. It is, however, readily reprogrammable into an SIMD system such as a PLA. The COLD gates perform AND functions. Connecting the output of one to the input of another produces an output that is the AND of both functions on their variables. Multiple strings of such COLD AND systems can generate multiple minterms of a logic gate with numerous variables. It is easy to OR the optical outputs of the various minterms simply by bringing them all together (e.g., with an integrated optics lens) onto a single detector and thresholding the detected signal.

VIII. ADVANTAGES ACHIEVED BY COLD

1. COLD does not limit the system bandwidth. It can perform logic operations at any bandwidth at which the input optics can be modulated.

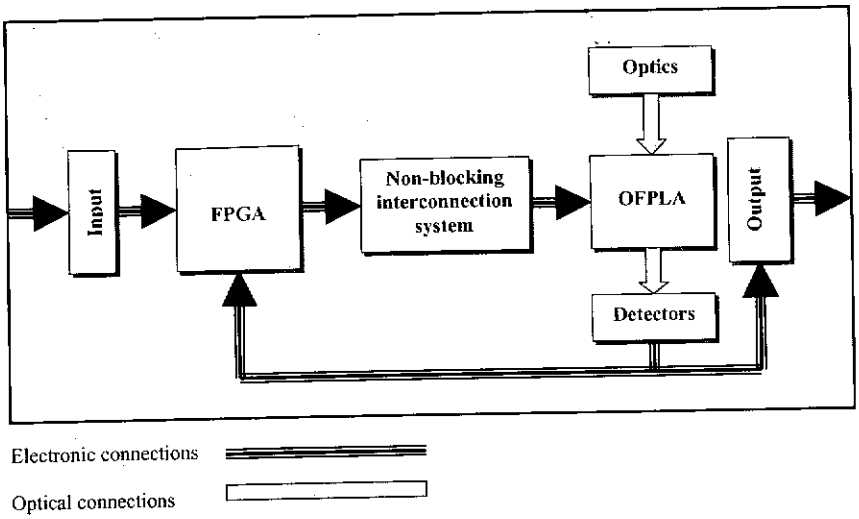

FIGURE 22. A Field generalized optical logic element (GOLE) array with an FPGA providing flexible interconnections for the flexible GOLEs.

2. COLD costs no energy. Optical signals at high bandwidth are to be processed. Because they have no intrinsic speed limit, a conventional Boolean logic device switching at the minimum energy of $\delta E = kT \ln 2$ must take a time of at least $\delta \geq \hbar/(kT \ln 2) \approx 0.366$ milliseconds according to the uncertainty principle. To go faster, more energy must be expended. Remember that current electronic devices spend around $10^{10}kT$ per binary operation, so they can achieve their high speed. However, going to a conservative logic gate that is fully passive drives both δE and δt to zero simultaneously.
3. COLD can be reprogrammed, making them the most flexible logic gates ever.
4. COLD can be integrated onto silicon and operated with silicon voltages to help solve the looming problem with ultra high speed electronics noted earlier.
5. Multiple COLDs on a chip constitute a FIMD system of enormous but largely unexplored flexibility and computational power.

IX. CONCLUSIONS

This chapter has been only a preliminary analysis of a totally new approach to optical logic that seems to hold great promise. We have done a great deal of work not reported here on applications, on fuzzifying the logic, and on finding

non-Boolean logics more amenable to COLD. The objective of this chapter is to provide a simple but complete introduction to COLD.

ACKNOWLEDGMENT

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APPENDIX A

Recent Selected Bibliography on Optical Logic

We have compiled about 850 journal titles in optical logic. The selection excludes quantum, molecular, and fuzzy logic. However, if an area, such as header recognition includes an optical logic gate, the article is included. The selection method started with covering all relevant journals. Later cross-referencing and Internet-based search engines directed us to additional important articles in less popular journals. Since subject index search in optical logic was not found reliable, we manually searched through all the titles of the articles for selections. Some articles provided no clue of optical logic or gate in the title, key words, or abstract but they were full of logic and gates in the remainder of the manuscript. The collection is still revised and updated but it represents the subject matter very well now. This appendix lists articles since 2000.

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