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Improved Electrical Performance and Thermal Stability of HfO_2/Al_2O_3 Bilayer over HfO_2 Gate Dielectric AlGaN/GaN MIS–HFETs

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AlGaN/GaN metal–insulator–semiconductor heterostructure field-effect transistors (MIS–HFETs) with a HfO_2/Al_2O_3 bilayer gate dielectric have been fabricated, characterized, and compared with HfO_2 gate dielectric MIS–HFETs. Physical and electrical characterizations have revealed the enhanced properties of the HfO_2/Al_2O_3 bilayer dielectric over that of the single HfO_2 layer. As a result, the fabricated HfO_2/Al_2O_3 MIS–HFETs exhibit better electrical performance and thermal stability than the HfO_2 transistors. The maximum drain current of the HfO_2/Al_2O_3 MIS–HFETs has increased by ~8.5%, while the off-state drain current has reduced by nearly 1 order of magnitude than that of the HfO_2 MIS–HFETs. After the thermal stress at elevated temperatures (400 and 500°C) for a prolonged duration up to 500 min, the irreversible device performance degradation, including drain current, peak transconductance, threshold voltage, and gate leakage current for the HfO_2/Al_2O_3 MIS–HFETs, is substantially less than that for the HfO_2 MIS–HFETs. A longer lifetime of $\sim 4 \times 10^6$ h at 150°C has also been estimated for the former, compared to that of the latter of $\sim 2 \times 10^5$ h.
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AlGaN/GaN heterostructure field-effect transistors (HFETs) have great potential as high power, high frequency, and high temperature devices owing to their excellent material characteristics.[1-3] Unfortunately, the Schottky gate (SG) leakage current is a major problem, which can lead to increased subthreshold current, higher power consumption, reduced breakdown voltage, and increased noise figure. An effective way to solve this predicament is by introducing a dielectric layer on the surface of the substrate as the gate insulator to form the metal–insulator–semiconductor (MIS)–HFETs. In addition, this dielectric can be used to passivate the surface traps, thus minimizing the current collapse problem. To date, various dielectrics,[4-15] such as SiO_2, Si_3N_4, AlN, Ga_2O_3, Al_2O_3, Sc_2O_3, HfO_2, ZrO_2, HfAlO, and Pr_2O_3, and dielectric stacks,[16,17] such as an Al_2O_3/Si_3N_4 bilayer and an Al_2O_3–HfO_2 laminated layer, have been explored as the gate insulators. Their corresponding MIS–HFETs have reported enhanced performance in terms of higher saturation drain current, higher breakdown voltage, lower gate leakage, and lower off-state drain current in comparison to corresponding unpassivated SG–HFETs, generally at the expense of a decrease in the device transconductance and a negative shift in the threshold voltage.[6,8-10,13-17] Therefore, the use of dielectrics with high dielectric constant (high-k) has been suggested[8-15,17] to mitigate these issues.

Owing to its high dielectric constant (20–25), HfO_2, deposited by various methods,[9-12] has recently attracted much attention as the gate dielectric for GaN-based devices. However, it tends to change from the amorphous to the polycrystalline state at 500°C, which may increase the grain boundary leakage and thereby pose thermal stability concerns for the devices. Moreover, it has a relatively small bandgap (5.6 eV).[18] On the contrary, Al_2O_3, which has a lower dielectric constant (9), has a larger bandgap (8.8 eV) and better thermal stability (can remain amorphous up to 1000°C) and has also shown a good passivation effect on GaN.[6,7] To reap the collective advantages of both dielectrics, Park et al.[17] proposed the use of an Al_2O_3–HfO_2 laminated layer as the gate dielectric on AlGaN/GaN HFETs, and Yue et al.[19] reported the usage of the stack gate dielectric HfO_2/Al_2O_3. However, their studies are limited to demonstrating the effectiveness of the hybrid dielectric as a gate insulator as well as a surface passivation layer. In this work, we systematically investigate not only the electrical performance of the HfO_2/Al_2O_3 bilayer gate dielectric MIS–HFETs, but also their thermal stability and in comparison to those of HfO_2 MIS–HFETs. In our experiments, both Al_2O_3 and HfO_2 are grown by a pulsed laser deposition (PLD) technique.

Experimental

The AlGaN/GaN epilayer was grown by metalorganic chemical vapor deposition on a sapphire substrate with the scheme of (from the top) GaN (2 nm)/$Al_{0.23}Ga_{0.77}N$ (20 nm)/GaN (above 2000 nm)/AlN buffer layer. All the (Al)GaN layers were unintentionally doped. Mesa isolation was realized using Cl_2/BCl_3 plasma by inductively coupled plasma. Then, a surface treatment was carried out, including an ultrasonic bath in acetone and followed by 2-propanol for 5 min each, boiling in an acid solution of HCl:deionized (DI) water (1:1) for 10 min, and, finally, a DI water rinse. Source/drain ohmic contacts were formed by depositing Ti/Al/Ni/Au (25/200/40/100 nm) using an electron-beam (E-beam) evaporator and followed by annealing at 900°C for 60 s in vacuum. The specific contact resistance (ρ_C) was measured as 9×10^{-6} Ω cm^2 using the transmission line method at room temperature. The spacing between the source and drain electrodes was 20 μm. The oxide layer was deposited between the source and drain region before the gate metal deposition. Two types of insulators, HfO_2 (~20 nm) and HfO_2/Al_2O_3 (~10/ ~ 10 nm), were deposited by the PLD technique. The film thickness was estimated by measuring the thickness of reference samples, which were grown under the same conditions using an atomic force microscope. Subsequently, the HfO_2 film was annealed at 300°C for 10 min in N_2 to improve the dielectric quality. Hall measurements revealed that this thermal treatment helped improve the AlGaN/GaN heterostructure two-dimensional electron gas (2DEG) conductivity ($n_s \times \mu$) by ~2.3% [from 1.28×10^{16} (V s)$^{-1}$ for the as-deposited film to 1.31×10^{16} (V s)$^{-1}$]. In addition, the X-ray diffraction (XRD) measurement (not shown) has confirmed that the annealed HfO_2 film remains amorphous, which is preferable because the polycrystalline gate dielectric could present issues of structural anisotropy and large leakage current through grain boundaries.[20] The HfO_2/Al_2O_3 bilayer insulator was given a postdeposition thermal treatment at 600°C for 10 min in N_2 to induce an inclusion of Al atoms into HfO_2 film, which has been reported to improve the dielectric characteristics,[21,22] and as the intermixing reaction of HfO_2 and Al_2O_3 was reported to occur around 600°C.[21] An enhanced 2DEG conductivity of ~2.26% [from 1.33×10^{16} (V s)$^{-1}$ for the as-deposited film to 1.36×10^{16} (V s)$^{-1}$] was measured. Finally, the E-beam evaporated Ni/Au (30/80 nm) gate electrode with a dimension of 10×100 μm^2 was defined by optical lithography.

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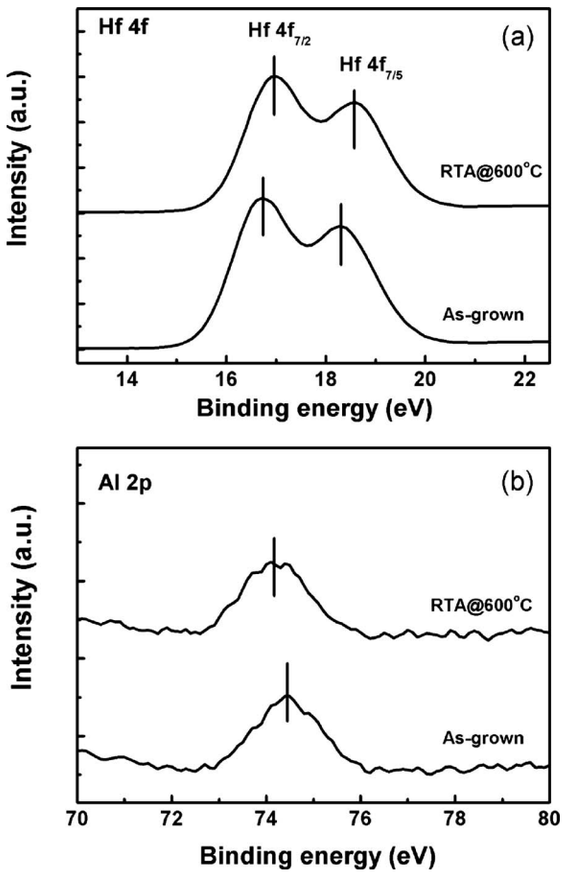

Figure 1. XPS spectra of (a) Hf 4f and (b) Al 2p core levels for the HfO_2/Al_2O_3 bilayer dielectric before and after annealing at 600°C for 10 min in N_2.

X-ray photoelectron spectroscopy (XPS) was performed to analyze the element interaction in the dielectrics. Capacitance–voltage (*C-V*) measurements at 100 kHz were used to determine the films properties. DC performance of the fabricated HFETs was obtained from an HP4156A semiconductor parameter analyzer for the current–voltage (*I-V*) characterization.

Results and Discussion

Physical and electrical characteristics of HfO_2 and HfO_2/Al_2O_3 dielectrics.— Figure 1a and b shows the XPS spectra of Hf 4f and Al 2p core levels, respectively, of the HfO_2/Al_2O_3 bilayer dielectric film. After annealing at 600°C, the peak position of Hf 4f shifts to a higher binding energy compared to that of the as-deposited film, indicating the intermixing of HfO_2 and Al_2O_3. The higher binding energy shifts are caused by the lower electronegativity of Hf (1.23) relative to that of Al (1.47).[21] In the case of Al 2p spectra, the binding energy for the samples annealed at 600°C shifts to the lower binding energy, again confirming the occurrence of an interaction between Hf and Al atoms in the bilayer dielectric.

C-V measurements at 100 kHz, as shown in Fig. 2, were conducted to examine the quality of the two types of dielectrics. During the measurements, the source and drain electrodes of the fabricated HFETs were shorted. At 2DEG accumulation, the total capacitance can be expressed as $1/C_{tot} = 1/C_{dielectric} + 1/C_{HFET}$. The estimated C_{HFET} is 3.5 pF ($\varepsilon_{GaN} = 8.5$, $\varepsilon_{Al_{0.23}Ga_{0.77}N} = 8.81$). From the measured values of C_{tot} for the two types of MIS–HFETs, 2.5 pF for HfO_2 and 2.1 pF for HfO_2/Al_2O_3 passivated devices, the capacitance values of the two types of dielectrics are calculated to be 8.8 pF for HfO_2 and 5.3 pF for HfO_2/Al_2O_3. Thus, the dielectric constant of HfO_2 is ~20, which is a typical value as reported,[9,10] while the effective dielectric constant for the bilayer HfO_2/Al_2O_3 film is estimated to be ~12, a value intermediate to that of pure Al_2O_3 film of ~9 and pure HfO_2 film of ~20. Compared to the dielectric constant of the Hf–Al–O film (16.6),[23] the value of our bilayer structure is lower, which is suspected to be caused by the incomplete interaction between HfO_2 and Al_2O_3. Coupled with the XPS results shown in Fig. 1, which has confirmed the interaction between HfO_2 and Al_2O_3, we suggest that there is only a partial interaction between Al_2O_3 with HfO_2 in the bilayer film to form the Hf–Al–O structure, while the remaining Al_2O_3 is intact. The effect of the two series capacitances, i.e., Hf–Al–O and Al_2O_3 layers, results in a smaller effective dielectric constant. In addition, a sharper transition from depletion to accumulation is observed for the *C-V* curves of HfO_2/Al_2O_3, relative to that of HfO_2, indicating a better interfacial property of the former.[6]

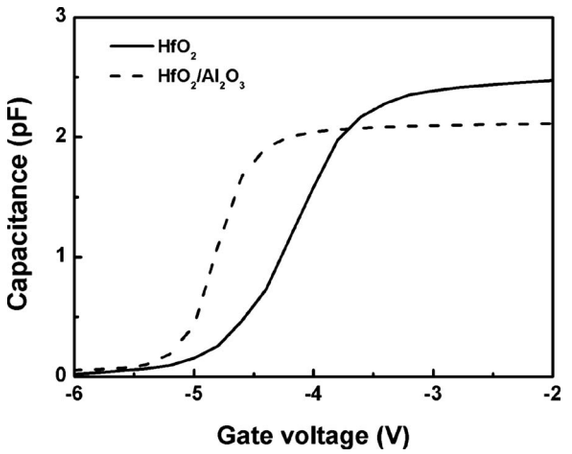

Figure 2. *C-V* curves of the HfO_2 and HfO_2/Al_2O_3 gate dielectric MIS–HFETs measured at 100 kHz. The gate length and width are 10 and 100 μm, respectively. Source and drain electrodes were externally connected during the *C-V* measurements.

From the X-ray reflectivity (XRR) fringe pattern (not shown) of the annealed dielectrics, the interfacial roughness values of 1.2 and 0.5 nm were measured for the HfO_2/GaN and Al_2O_3/GaN interfaces, respectively. The relatively rough interface of the former could be related to the broad shoulder observed in the XRD spectra of the annealed HfO_2 film (not present in that of the Al_2O_3 film), which may signify the existence of partial polycrystalline particles[24] in the film.

Room-temperature Hall effect measurements using van der Pauw contacts were performed. The 2DEG conductivity ($n_s \times \mu$) of the unpassivated AlGaN/GaN heterostructure is 1.25×10^{16} $(V\ s)^{-1}$. After adding the passivation layer of HfO_2, this value increases by ~4.8% [to 1.31×10^{16} $(V\ s)^{-1}$], suggesting a decrease in the electron trapping caused by surface states.[25] With the HfO_2/Al_2O_3 bilayer passivation, $n_s \times \mu$ is further enhanced and increases by ~8.8% [to 1.36×10^{16} $(V\ s)^{-1}$] with respect to the unpassivated structure. As a result, the sheet resistance decreases by 3.2% for HfO_2, while it decreases by 5.8% for the HfO_2/Al_2O_3 passivation. All these results suggest the improved HFET structure after a surface passivation. More importantly, the passivation effect is further enhanced using the HfO_2/Al_2O_3 bilayer dielectric.

I-V characteristics of MIS–HFETs with HfO_2 and HfO_2/Al_2O_3 dielectrics.— Figure 3a and b shows the typical *I-V* characteristics of the HfO_2 and HfO_2/Al_2O_3 gate dielectric MIS–HFETs, respectively. For comparison, the *I-V* curves of unpassivated SG–HFETs are also shown in Fig. 3c. Both types of MIS–HFETs exhibit good saturation and pinch-off properties without any abnormal kink ef-

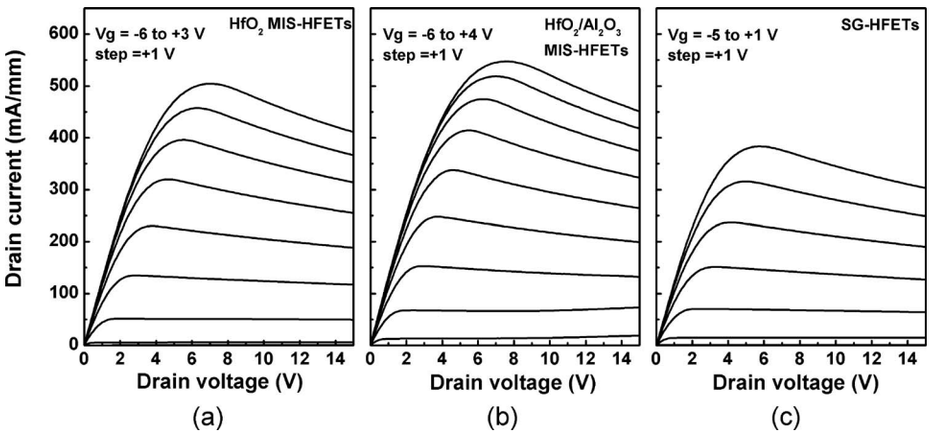

Figure 3. Typical *I-V* characteristics of (a) HfO_2 MIS–HFETs, (b) HfO_2/Al_2O_3 MIS–HFETs, and (c) SG–HFETs.

fect, indicative of the good quality of both types of dielectrics grown by PLD. The self-heating effect, observed in all the transistors, is caused by the poor thermal conductivity of the sapphire substrate. For SG–HFETs, the gate voltage (V_g) can only be biased up to $V_g = +1$ V without a noticeable gate leakage. However, the HfO_2 MIS–HFETs can be biased up to $V_g = +3$ V, while the HfO_2/Al_2O_3 MIS–HFETs show an even better gate controllability of up to $V_g = +4$ V. As a result, a larger maximum drain current by ~8.5% can be achieved for the bilayer HfO_2/Al_2O_3 MIS–HFETs compared to the HfO_2 passivated devices. Even at $V_g = +3$ V, the maximum operative gate voltage for the HfO_2 MIS–HFETs, the HfO_2/Al_2O_3 MIS–HFETs also exhibit a drain current higher by ~3% than that of the HfO_2 MIS–HFETs. This may be attributed to the better interfacial quality of Al_2O_3/substrate than HfO_2/substrate, as suggested from the *C-V* measurements (see Fig. 2). The larger reduction in surface defects caused by the better Al_2O_3/GaN interface, compared to HfO_2/GaN, could have led to a larger increase in the 2DEG conductivity, thereby an enhancement of the drain current. In addition, the values of on-resistance (R_{on}) extracted from the linear region of the *I-V* curves ($V_g = 0$ V) are estimated to be 10.3 and 9.8 Ω mm, respectively, for the HfO_2 and HfO_2/Al_2O_3 MIS–HFETs. The smaller R_{on} of the latter corresponds well to its larger 2DEG conductivity, as indicated by Hall measurements. The reduced R_{on} of the HfO_2/Al_2O_3 MIS–HFETs makes them more attractive for power switching application.[26]

Figure 4 shows the transfer characteristics of the SG–HFETs, HfO_2 MIS–HFETs, and HfO_2/Al_2O_3 MIS–HFETs. Both types of MIS–HFETs exhibit a slightly lower maximum transconductance ($g_{m,max}$) compared to the SG–HFETs. This is caused by the presence of the gate dielectric, which increases the separation from the gate to the 2DEG channel. However, due to the high dielectric constant of HfO_2, the decrease in $g_{m,max}$ is much smaller than that of MIS–HFETs using low-*k* dielectrics.[4-6] Similarly, the negative shift in V_{th} for both kinds of high-*k* MIS–HFETs, mainly caused by the increased gate-to-channel distance, is relatively small. Because the effective *k* value of the HfO_2/Al_2O_3 bilayer (~12) is lower than that of HfO_2 (~20), inevitably, the $g_{m,max}$ of the bilayer MIS–HFETs is smaller (by ~5.7%) than that of HfO_2 passivated devices. Also, a more negative shift (by approximately −0.3 V) in V_{th} can be observed in the former. Despite this shortcoming, more advantages may be achieved by the HfO_2/Al_2O_3 bilayer dielectric. The gate voltage swing (GVS), defined as the range of voltage for a 10% drop from $g_{m,max}$, is 2.95 V for SG–HFETs, 3.2 V for the HfO_2 MIS–HFETs, and 3.4 V for the bilayer HfO_2/Al_2O_3 MIS–HFETs. The larger GVS suggests a better linear behavior, from which a smaller intermodulation distortion, a smaller phase noise, and a larger dynamic range can be expected,[27] thus making the HfO_2/Al_2O_3 MIS–HFETs more desirable for practical amplifier applications. In addition, it is observed that both types of MIS–HFETs yield a lower off-state drain current than the SG–HFETs. For example, the off-state drain current of the HfO_2 MIS–HFETs is more than 1 order of magnitude lower than that of the SG–HFETs, while that for the HfO_2/Al_2O_3 MIS–HFETs is reduced by approximately 2 orders of magnitude, suggesting a higher breakdown voltage for the bilayer MIS–HFETs.

A gate leakage current comparison of the three types of HFETs is illustrated in Fig. 5. Both MIS–HFETs exhibit a lower gate leakage

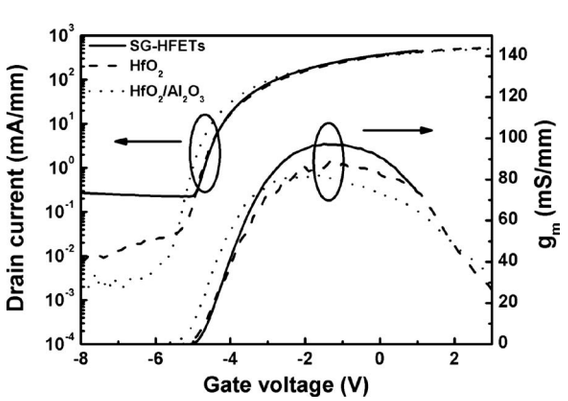

Figure 4. Transfer characteristics of HfO_2 and HfO_2/Al_2O_3 gate dielectric MIS–HFETs and unpassivated SG–HFETs. The measurements were conducted at 6 V drain-to-source bias.

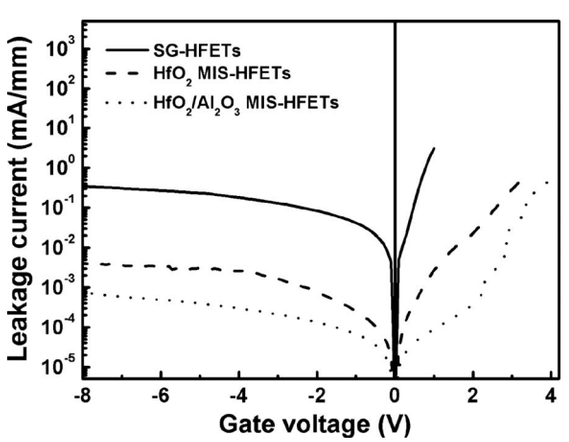

Figure 5. Gate leakage current comparison for HfO_2, HfO_2/Al_2O_3 gate dielectric MIS–HFETs, and unpassivated SG–HFETs.

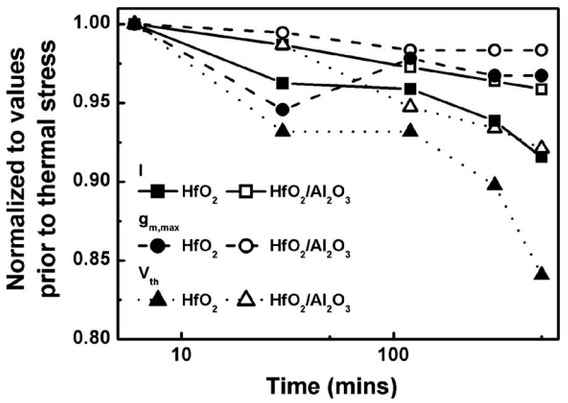

Figure 6. Variation in the maximum drain current (V_g = +3 V), $g_{m,max}$, and V_{th} as a function of thermal stress duration at 500°C for HfO_2 and HfO_2/Al_2O_3 MIS–HFETs.

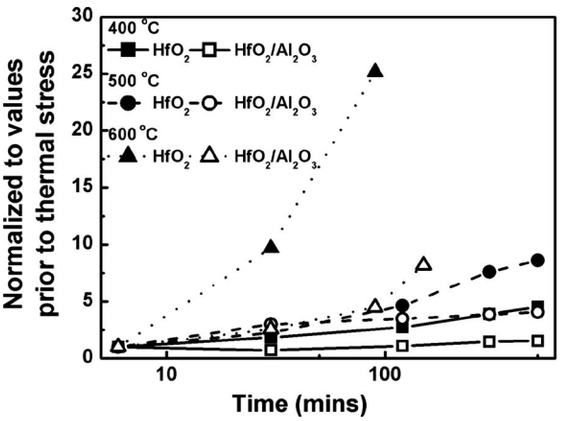

Figure 7. Variation in the gate leakage current as a function of thermal stress duration at 400, 500, and 600°C for HfO_2 and HfO_2/Al_2O_3 MIS–HFETs. The current was measured at −5 V gate-to-source bias.

than the SG–HFETs, also suggesting a higher breakdown voltage for the former. More specifically, when $V_{gs} = -5$ V, the leakage currents for the SG–HFETs, HfO_2, and HfO_2/Al_2O_3 MIS–HFETs are 2.3×10^{-1}, 3.0×10^{-3}, and 3.8×10^{-4} mA/mm, respectively. Clearly, HfO_2/Al_2O_3 MIS–HFETs exhibit the lowest leakage, which is on the one hand due to the larger conduction band offset between Al_2O_3 and the substrate (~2.6 eV) [4] compared to that of HfO_2 (~1.71 eV) [9] and on the other hand related to the better interfacial quality of Al_2O_3/substrate.[16]

Thermal stability of MIS–HFETs with HfO_2 and HfO_2/Al_2O_3 dielectrics.— For applications, such as in automobiles and for defense, the devices are required to operate at elevated temperatures. Accordingly, in this work, an elevated temperature thermal stress (at 400 and 500°C) was applied to the two types of MIS–HFETs to examine their high temperature performance and stability. *I-V* measurements were performed at room temperature intermittently after the stress temperature ramped down.

Figure 6 shows the changes in the maximum drain current (V_g = +3 V), peak transconductance, and threshold voltage for the two types of MIS–HFETs, normalized with respect to the corresponding values before thermal stress, as a function of thermal stress duration at 500°C. Those at 400°C depict the same trend, albeit to a lower degradation extent and, hence, are not shown. Both types of MIS–HFETs remain functional after thermal stress for a prolonged time, although irreversible degradation in the device performance is observed, which might be related to the reduced 2DEG conductivity in the HFET structure.[28] There is less degradation in the device performance for the HfO_2/Al_2O_3 MIS–HFETs than HfO_2 MIS–HFETs. For example, after thermal stress for 500 min, the drain current and $g_{m,max}$ of HfO_2 MIS–HFETs have dropped by 8.4 and 3.3%, respectively, while V_{th} has shifted positively by ~15.9%. As for HfO_2/Al_2O_3 MIS–HFETs, the degradation in the drain current and $g_{m,max}$ are lower at 4.1 and 1.6%, respectively; the change in V_{th} is also lower at 7.9%.

Figure 7 shows the change in the gate leakage current, with respect to the value before thermal stress, as a function of the thermal stress duration at different temperatures for HfO_2 and HfO_2/Al_2O_3 MIS–HFETs. The leakage current evolution at 600°C is also tracked and shown for the later device lifetime estimation. The leakage increases with thermal stress duration and temperature for both types of devices. At 600°C thermal stress, a large gate leakage occurs in HfO_2 MIS–HFETs, which on the one hand may be caused by the crystallization of HfO_2, thus providing the pathways for leakage, and on the other hand may be related to the in-diffusion of the gate metal into the underlying layers, hence degrading the device performance. Obviously, the HfO_2 MIS–HFETs exhibit more severe gate leakage degradation than the HfO_2/Al_2O_3 MIS–HFETs. For example, after thermal stress at 500°C for 500 min, the gate leakage has increased by ~8.6 times, relative to that before thermal stress, for the HfO_2 MIS–HFETs, while it increases only by ~4.1 times for the HfO_2/Al_2O_3 MIS–HFETs.

The lifetime of the two types of MIS–HFETs at 150°C, which is viewed as the starting point for high temperature operation,[29] is extracted using the Arrhenius equation: $t_f \sim A \exp(E_a/kT)$, where t_f is the time for the device to reach a failure criterion, E_a is the activation energy, k is the Boltzmannn's constant, T is the absolute temperature, and A is a constant. Because it takes a long time for the devices to degrade severely, and the purpose here is mainly to quantitatively compare the device stability, a moderate increase (4 times) in the device gate leakage is herein regarded as a failure criterion. The activation energies for HfO_2 and HfO_2/Al_2O_3 passivated devices are estimated to be 1.00 and 1.08 eV, respectively. The slightly higher E_a of the latter indicates the better thermal stability of the bilayer transistors and translates to a lifetime at 150°C of ~4×10^6 h, which is 20 times higher than that of HfO_2 MIS–HFETs at ~2×10^5 h.

Based on the preceding experimental observations and discussion, the enhanced electrical performance and thermal stability of the HfO_2/Al_2O_3 bilayer gate dielectric MIS–HFETs over the HfO_2 counterparts can be explained as follows. The incorporation of an amorphous Al_2O_3 interfacial layer into the gate dielectric leads to a smoother dielectric/substrate interface (XRR measurements) with an enhanced interfacial property (Fig. 2), which on the one hand improves the 2DEG conductivity of the heterostructure (Hall measurements) and increases the device current drive capability (Fig. 3) and on the other hand contributes to the reduced off-state drain current and gate leakage (Fig. 4 and 5). The improved thermal stability of the HfO_2/Al_2O_3 transistors, as shown in Fig. 6 and 7, can be attributed to both the formation of Hf–Al–O and the remaining nonreacted Al_2O_3 in the bilayer dielectric. The incorporation of Al into HfO_2 helps increase the dielectric crystallization temperature[22] by forming the Hf–Al–O structure (confirmed by XPS measurements), which remains amorphous under such high temperature thermal stress.[23] This, together with the remaining nonreacted amorphous Al_2O_3, can serve as an effective barrier layer to suppress the diffusion of oxygen or gate metals into the underlying substrate, thus reducing the formation of interfacial defects and enhancing the device thermal stability. Although the effective dielectric constant of the HfO_2/Al_2O_3 bilayer (~12) is lower than that of HfO_2 (~20), this predicament is expected to be mitigated by further optimizing the thickness ratio of HfO_2 and Al_2O_3, enhancing their interactions and forming more Hf–Al–O (16.6) in the bilayer film.

Conclusions

We have fabricated AlGaN/GaN MIS–HFETs with a HfO_2/Al_2O_3 bilayer, which has a relatively high-k ($\sim$12), as the gate dielectric and compared their performance with that of HfO_2 MIS–HFETs. The HfO_2/Al_2O_3 bilayer dielectric possesses a better interfacial quality than HfO_2 with the GaN substrate. As a result, fabricated HfO_2/Al_2O_3 MIS–HFETs exhibit better electrical characteristics than HfO_2 MIS–HFETs, such as a larger maximum drain current, smaller on-resistance, larger GVS, lower off-state drain current, and lower gate leakage. In addition, thermal stability experiments have shown that with the incorporation of the Al_2O_3 layer, the device performance degradation is suppressed, and this may be attributed to both the formation of the Hf–Al–O structure and the amorphous nature of the remaining Al_2O_3. Although the HfO_2/Al_2O_3 MIS–HFETs show a slightly lower transconductance and more negative V_{th} than HfO_2 MIS–HFETs, these trade-offs are balanced by the overall improvement in the device electrical performance and thermal stability. Therefore, HfO_2/Al_2O_3 bilayer stack should be a promising gate dielectric for high performance MIS–HFET fabrication.

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