High Performance and Highly Uniform Metal Hi-K Gate-All-Around Silicon Nanowire MOSFETs

J. W. Sleight, S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. C. M. Fuller, L. M. Gignac, S. Mittal, J. S. Newbury, T. Barwicz, M. M. Frank, and M. Guillorn
IBM T. J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY 10598
Phone: 914-945-1876; E-mail: sleight@us.ibm.com

We demonstrate undoped-body, metal hi-k gate-all-around (GAA) Si nanowire (NW) MOSFETs with excellent electrostatic scaling. These NW devices, with a TaN/Hf-based gate stack, have high drive-current performance with NFET/PFET IDSAT = 825/950 µA/µm (circumference-normalized) or 2592/2985 µA/µm (diameter-normalized) at supply voltage VDD = 1 V and off-current IOFF = 15 nA/µm. Superior NW uniformity is obtained through the use of a combined hydrogen annealing and oxidation process. For the first time, a clear dependency of short-channel effects versus wire size is observed. Additionally, we demonstrate agglomeration-free epitaxial silicon growth on small-diameter NWs outside the gated region, lowering the extrinsic contact resistance to the device.

The initial definition of the NWs uses conventional ebeam lithography and RIE. After the H2 annealing and oxidation NWs well below 10 nm in diameter are reliably generated, with resulting LER at the level of our measurement limit (<0.8nm). During hydrogen annealing, Si redistributes and sharp corners are rounded and smoothened [1]. This results in NW cross-section reshaping (Fig. 1a inset and 1b) and also roughness reduction Fig. 1b shows a series of NWs with decreasing patterned width, at the same original height (same SOI thickness).

While the NW channel diameter needs to be small, the source/drain (S/D) extension regions must remain sufficiently thick to minimize series resistance and prevent silicide runaway [2]. Defect free selective Si epitaxy on sub-10 nm NW was performed without NW agglomeration by initiating growth at low temperature.

GAA NW FET devices were fabricated, incorporating the wire formation described above, through the first metal level. Structural images are shown in Fig. 2. The gate stack utilized a Hf based dielectric with a TaN metal capped with poly-Si. Inversion oxide thickness TINV was 1.7 nm. A NiPt silicide was used. Figs. 3 and 4 show selected electrical characteristics of our undoped-body, GAA NW devices. Mid-gap metal gates lead to normally-off FETs with centered threshold voltage. The excellent wire size control of our process enables reliable investigation of size scaling in undoped, GAA channels. Dependence of short-channel effects on NW size is shown in Fig. 3. Scaling the body dimensions of NW FETs clearly improves short-channel control, as is expected for fully-depleted (FD) undoped-body devices. These NW devices exhibit extremely high drive currents, as illustrated in Fig. 4. We observe similar or higher NW PFET drive currents over NFET, with the NW PFETs outperforming IBM's 45nm-technology partially depleted (PD) SOI PFETs with poly/SiON gate stack [3].

References:

[1] K. Sudoh et al., Jpn. J. Appl. Phys. 43, p. 5937, 2004.
[2] J. Appenzeller et al., IEDM Tech. Dig., p. 555, 2006.
[3] S. Narasimha et al., IEDM Tech. Dig., p. 689, 2006.

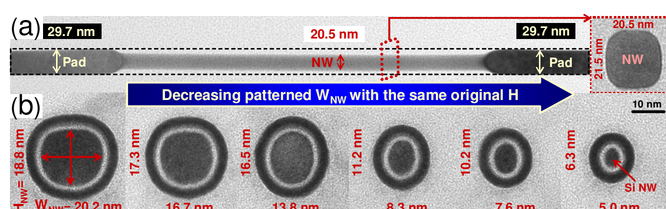

Fig. 1. Maskless NW thinning and reshaping by hydrogen annealing (a) after hydrogen annealing (and prior to oxidation): H_{NW} is reduced while the pad thickness remains constant due to Si migration. Current example shows a 2/3 height reduction, but further thinning and rounding by this maskless process can be obtained. (b) Dependency of NW's final cross-section on initial W_{NW} (varied) and H (same for all since sharing SOI). More thinning and rounding occurs with narrower NW due to enhanced Si migration at high-curvature surfaces. NWs in (b) have high-z elements coated to highlight the edges.

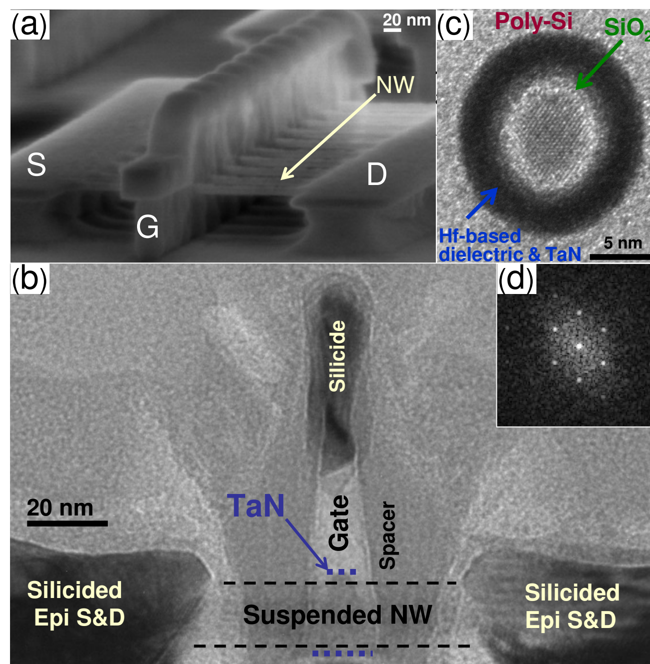

Fig. 2. Structural images of GAA NW FET. (a) SEM after gate etch (Fig. 5d) showing structural integrity of NWs outside the gate region. (b) TEM of the final, GAA NW FET along the NW channel with L_G ~ 15 nm. (c) Cross-sectional TEM of a NW inside the gate. NW dimension is 5.0 nm × 6.3 nm. (d) Diffractogram of the Si region in (c) showing a [110]-oriented NW.

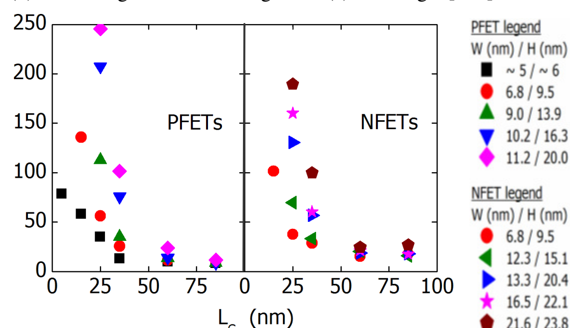

Fig. 3. Physical gate length L_G dependence of drain-induced barrier lowering (DIBL) of NW PFETs and NFETs. The width *W* and height *H* of the NWs are noted in the legend. DIBL is defined as $|V_{TLIN} - V_{TSAT}|$ / 0.95 V, where V_{TLIN} and V_{TSAT} are the threshold voltages at drin bias $|V_{DS}|$ = 0.05 and 1 V, respectively. Our undoped-body NW FETs have centered V_{TLIN} due to the use of mid-gap metal gates. The data also demonstrates that scaling the body dimensions of NW FETs leads to improved short-channel control.

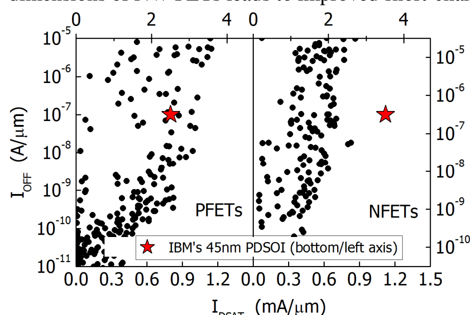

Fig. 4, On-current I_{DSAT} vs. off-current I_{OFF} of NW PFETs and NFETs with currents normalized by circumference (bottom/left axis) and by effective diameter (top/right axis). I_{OFF} and I_{DSAT} are extracted at drain bias $|V_{DS}|$ = 1 V, and gate voltage $|V_G|$ = 0 and 1 V, respectively. IBM's 45nm planar poly/SiON PDSOI data is shown for comparison [10].