INVITED SURVEY PAPER *Surveys on Image Processing Technologies—Algorithms, Sensors and Applications—*

Computational Sensors——Vision VLSI

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SUMMARY Computational sensor (smart sensor, vision chip in other words) is a very small integrated system, in which processing and sensing are unified on a single VLSI chip. It is designed for a specific targeted application. Research activities of computational sensor are described in this paper. There have been quite a few proposals and implementations in computational sensors. Firstly, their approaches are summarized from several points of view, such as advantage vs. disadvantage, neural vs. functional, architecture, analog vs. digital, local vs. global processing, imaging vs. processing, new processing paradigms. Then, several examples are introduced which are spatial processings, temporal processings, A/D conversions, programmable computational sensors. Finally, the paper is concluded.

key words: computational sensor, smart sensor, vision chip, intelligent sensor, CMOS sensor, silicon retina, image processing system, visual information processing system, vision system

1. Introduction

In biological vision, the retina is the imaging sensor. The retina not only detects image signals but also processes limited, low-level tasks, in order to enhance imaging performance and to preprocess tasks for later stages. Thus, given the precedent in biological vision, integration of processing and sensing is reasonable in order to augment sensing and processing performance.

Traditionally, a visual information processing system comprises discrete system modules; an image sensor (normally CCD camera), a A/D conversion and a digital processing system. Then, the combined system tends to be large and the image acquisition is limited only to that of NTSC standard spatio-temporal resolution. Development of VLSI technologies leads to producing a new generation of image sensors which integrate sensing and processing on a single chip, that we call a computational sensor, or a smart sensor, an intelligent sensor, a vision chip.

Computational sensors are designed for specific targeted applications. Circuits for both photodetection and processing co-exist on a single chip. Sensing and processing have interactions in a low level. The major advantages of computational sensor are "size" and "speed." Differing from the conventional visual processing systems which comprises module systems and follows the sense-read-processing paradigm, tight integration of sensing and processing realizes a very small integrated system on a chip. The speed is not restricted by the video rate any more.

The freedom from the restriction of video standard has a very significant impact on real time image processing. For example, let's take a look at motion estimation which is a heavy processing in the conventional framework in which the rate is limited by the video rate (30 Hz), that is the communication bottleneck between the sensor and the processor. Because the complexity of motion estimation is determined by the dimensions of the search space, faster frame rate can reduce the difficulty of the task. If the frame rate can be much faster than the video rate, the search area can be very small and the motion estimation can be much easier.

Fundamental device technology of image sensor is changing, too. So far, CCD sensors has been dominating, but CMOS active pixel sensors (CMOS sensor in short) is emerging as a competitive new image sensor technology. Although CMOS passive pixel sensor has been existing, CMOS active pixel sensor is relatively new [38], [39]. CMOS active pixel sensor has several transistors as an active amplifier in a pixel. Because of the CMOS process compatibility, CMOS sensor is easier to be integrated with additional circuits, and it can achieve functionality with lower power dissipation. CMOS sensor is attempted to be integrated with A/D conversion and timing control etc., which results in on-chip-digital-camera. The major advantage of the CMOS sensor is the functionality.

Most of the computational sensors have been made by ordinary CMOS process, and it can be viewed as a functional CMOS sensor. At present, CMOS sensor is being improved in its imaging quality, and in the near future its functionality will be more and more important. Then, interest of sensor device technology of CMOS sensor and interest of processing technology for computational sensors are overlapping. The sensor device technology and the processing applications are sharing the common field of research and development as shown in Fig. 1.

In this paper, computational sensor is described from several points of view. Some examples are described, and then the paper is concluded.

2. Computational Sensors

Computational sensor (or smart sensor, vision chip) is a

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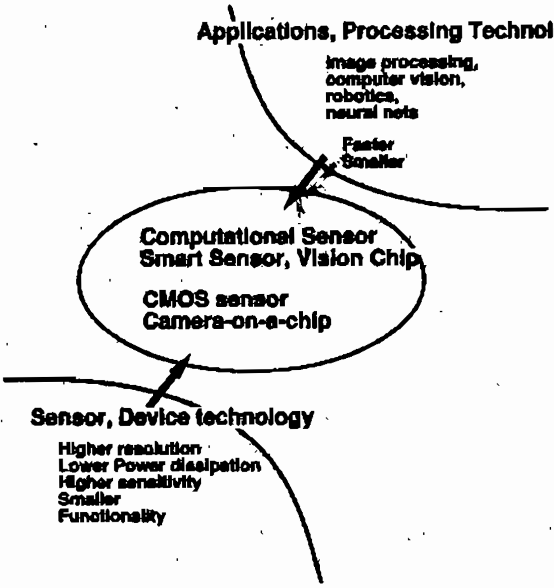


Fig. 1 Computational sensors and related fields.

small integrated system, in which processing and sensing are unified on a VLSI chip by co-existing circuits of photo-detection and processing. Computational sensors are designed for specific target applications.

In the early days, in order to make fast image processor, CCD technology was adopted for image processing. Convolution operation was implemented by CCD which divide and shift charge packets [6]. Pixel parallel focal plane processor was even made under CCD technology, and a generic focal plane architecture based on CCD was discussed in [7]. However, CCD is not easy to be integrated with CMOS computational circuits. Now, most of the computational sensors are made by ordinary CMOS process.

Various computational sensors have been made, and in this section they are surveyed from several points of view.

2.1 Advantages vs. Disadvantages

When compared to traditional module system based visual information processing systems, computational sensor has advantages and disadvantages which are listed below.

■ Advantages
(1) Size
(2) Speed
(3) Power dissipation
(4) Application specific image format
(5) Mutual interaction between sensing and processing

As noted in the introduction, small size and fast speed is the most advantageous in computational sensor. Compared to the conventional module processing system, power dissipation is also reduced by orders of magnitude. Image format is able to be optimized for the target application. An extreme example is a polar coordinate sensor [8], [9], in which the pixels are arranged in such a way that the density of the pixel changes high to low from the center to the peripheral (Fig. 2). Last but not the least, the mutual interaction between sensing and processing is the big advantage over the traditional systems. Computational sensor can handle analog data of the photo-detector so that it can feedback the results of the processing to parameters of sensing, or it can finish processing during integration.

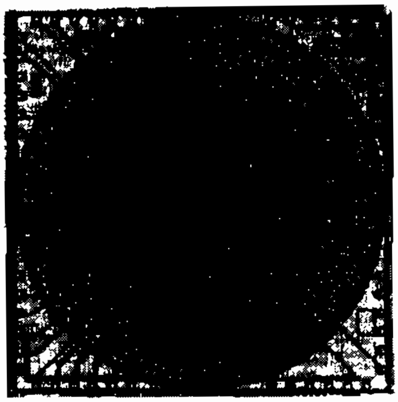


Fig. 2 Polar coordinate sensor: Photo detectors are arranged in concentric rings and with a size varying linearly with the distance from the geometric center [9].

■ Disadvatages
(1) Precision
(2) Resolution and fill factor
(3) Design difficulty
(4) Programmability

Computational sensor has disadvantages too, and they are listed above. The majority of the computational sensors utilizes analog processing circuit, and the precision should be accounted if they are enough for the target applications. Because of use of many analog circuits, the design is not easy. When each pixel contains processing circuits, the resolution and the fill factor is low, which results in poor imaging capability. Computational sensor is not general purpose. Architecture as well as processing scheme should be optimized to reduce the effects of those disadvantages.

2.2 Neural vs. Functional

Computational sensor becomes widely known by the work of silicon retina [3] which computes spatial and temporal derivatives of image projected onto its focal plane. In the human retina, the communication between neurons is based on the analog and graded poten-

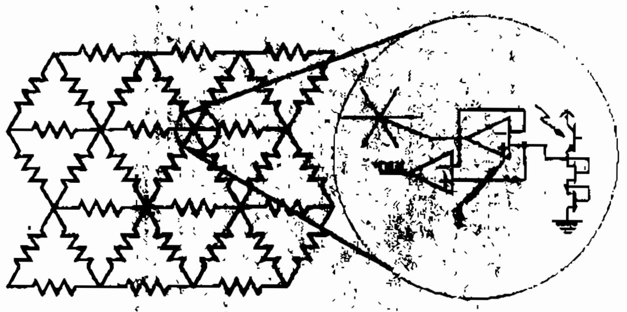


Fig. 3 Silicon retina by resistive network [1], [3].

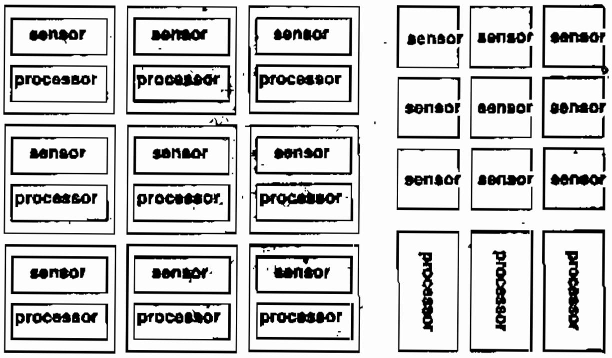
tials (not spikes). Thus, human retina is inherently well modeled by electronic circuit and has been attempted to be modeled by a resistive network and logarithmic photo-detector (Fig. 3). Some early vision tasks have been implemented. Using resistive networks, optical flow field computation edge detection etc. were implemented as a computational sensor [3]–[5], [25]. These works were rather focused on modeling biological neural systems. They suffer from low resolution and low precision. One of the interesting research activities developed from the neural nets based researches is artificial eye or visual prosthesis that could help a blind person obtain visual information [10].

On the other hand, many computational sensors are designed for specific target tasks such as compression [18], [19], [22], enhancement [23], multiresolution [14], moment computation [42], A/D conversion [33]–[37], range finding [40], [41] etc. Although some tasks are functionally similar to those of human retina, they are designed by special analog processing schemes which are very different from that of biological neural networks. Computational sensor, which makes use of very limited resources (area, power), does not necessarily follow biological computational principle. In the rest of the paper, we are apart from the neural network based approach and focus on the functional approach. In Sect. 3, some of the example will be introduced.

2.3 Architectures: Pixel Parallel vs. Column Parallel

There are two approaches to the parallel processing architecture on the focal plane, from the point of view of how to locate processing elements together with the photo-detector array. They are, as shown in Fig. 4, (1) pixel parallel architecture which has a processing element in each pixel, and (2) column parallel architecture which shares a processing element for pixels in a column.

The two have advantages and disadvantages. Parallelism is higher in the pixel parallel architecture, then the processing speed is fast, but it has lower fill factor, lower resolution, and higher power dissipation. Column parallel architecture has lower parallelism, but the photo-detector array can be almost the same as that of ordinary CMOS sensor, and it does not sacrifices the fill factor and resolution. The architecture should be chosen for the target application.



(a) pixel parallel (b) column parallel

Fig. 4 Pixel parallel and column parallel architectures for focal plane processing.

2.4 Analog vs. Digital

Computational sensors are designed for specific applications and most of them make use of analog processing which effectively use physical principle of a device to perform computation. Analog processing is fast and compact, and analog signal representation is efficient, but its precision is low. Analog processing also enables processing during integration.

However, there have been attempts towards programmable computational sensors based on digital processing, which enables several simple image processing operations. Implementations using both column parallel architecture [28], [29] and pixel parallel architecture [30]–[32] have been investigated, which are introduced in the next section.

2.5 Local Processing vs. Global Processing

Spatial processing on computational sensors requires connection between pixels. Local connection is easy, but global connection is not. Then, most of the tasks which were achieved by computational sensors are spatially local processing such as edge detection, filtering or temporal processing that does not need any inter-pixel connections. A global processing which cannot be achieved by spatially local processing, for example, finding the largest intensity in the image, need to handle the outputs of the local processings for the entire image.

2.6 Imaging vs. Processing

The resource of the focal plane is very limited. There is generally a trade off between "imaging capability" and "processing complexity." Processing complexity is related to some extent to the complexity of circuits. Higher complex processing needs higher complex circuit, which results in lower fill factor, lower resolution, higher power dissipation and higher noise. It may lead to significant degradation of imaging capability. Imaging capability of computational sensor should be concerned.

2.7 New Processing Paradigm

Traditional digital image processing system comprises a camera, A/D conversion and digital processing modules. It always uses normal NTSC video camera and their algorithms and performances for real time processing are rather optimized for the NTSC spatio-temporal resolution. Because of this fact, traditional image processing methods tend to get more complex in order to improve reliability. For example, in case of motion estimation, motion of only 30 frames per second of NTSC temporal resolution easily results in large displacements between frames which makes motion estimation harder. However, for example, if the temporal resolution is much higher, motion between frames is much smaller and its estimation task is much easier. Thus, advances in the sensor significantly change difficulties of the processing tasks.

Computational sensor also enables mutual interaction between the photo-detectors and the processors. The processing results can be feedbacked to photo-detectors to change imaging condition. The processing can also be done during integration. This is not possible in the traditional digital processing systems.

3. Examples for Computational Sensors

Recent examples of computational sensors are introduced in this section. They are chosen from those in categories of (1) spatial processing, (2) temporal processing (3) programmable computational sensor (4) A/D conversion on focal plane. (1) and (2) have features distinctive of analog processing on sensor focal plane.

3.1 Spatial Processing

3.1.1 Analog Filtering by Variable Sensitivity Photodetector (VSPD) Cells

Variable Sensitivity Photo-Detector (VSPD) cells was developed using special GaAs photo-detector pixel [11]. The interesting feature is that the output of the pixel depends on a sensitivity control voltage both in sign and magnitude. The control line is shared by pixels in a column. Thus, 1D analog filtering is easily achieved by appling the control signals to the pixels in a column and summing their outputs in current mode on a output line for the pixels in the column. 128 × 128 array was prototyped. The filtering operation is extended to 2 dimensional by adding the multiple output in a 1-D memory array [12] (Fig. 5).

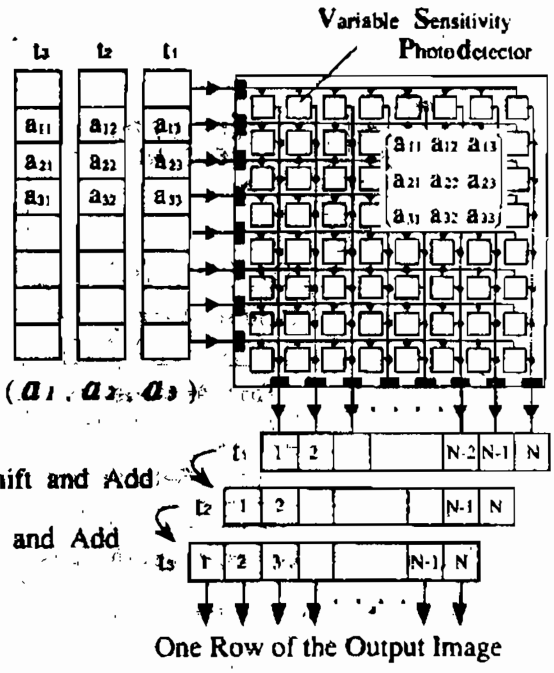


Fig. 5 Diagram of analog processing of VSPD pixel array [12].

n-MOS version of VSPD array was also developed by the same group. The n-MOS VSPD can control only the sign of the output of the pixel. Each pixel contains a PD and current direction conversion circuit of several transistors. 256 × 256 array, pixel of 35 × 26 μm^2 was developed under 2 μm n-MOS process.

3.1.2 Multiresolution Processing on Focal Plane

For variety of processing tasks, it is desirable to have image data available at varying resolutions to increase processing speed and efficiency. Multiresolution is a standard image processing methodology and it is usually generated by software based image pyramid approach.

A multiresolution CMOS sensor pixels was developed [14]. It is programmable to average and read out any size n × n block kernel region of pixels. The architecture is shown in Fig. 6. The prototyped sensor has 128 × 128 pixel array. At the bottom of each column, it has a network of switched capacitors to store signal levels of pixels. The column circuitry contains additional capacitors to perform averaging on any size of the kernel. Resolution is determined by the kernel. X-Y addressability of the sensor enables zoom into areas of interest.

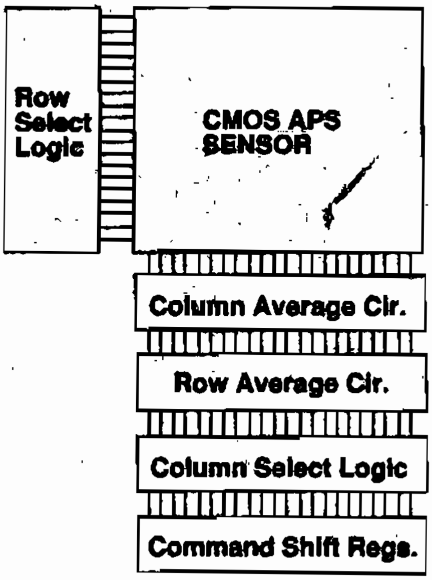


Fig. 6 Architecture of multiresolution CMOS sensor.

3.1.3 Spatially Variant Sampling Sensor

Biological vision has spatially variant sampling structure, which has high resolution in the fovea and sparse sampling in the periphery. Because of this structure, the region of interest is densely analyzed while sparsely keeping information of outside of the region. It is desirable to have such spatially variant sampling on the focal plane. It significantly reduces data and speed up entire processing.

One of such spatially variant sampling sensor is the polar coordinate sensor in Fig. 2, which has a fixed sampling structure. A spatially variant sampling sensor, in which sampling positions are programmable, was developed [15]. The architecture of the sensor is shown in Fig. 7. It has a CMOS pixel array and a memory array, each memory element of which corresponds to each pixel and contains a binary control data to determine that the corresponding pixel is read out. By using smart scanning shift register [18], selected pixels are read out in a compact sequence. Contrary to the random access CMOS sensor [17], the spatially variant sampling sensor reads out at high speed without need of pixel address for every access. Access to the memory array is separated, and rewriting the memory dynamically changes the sampling positions. A prototype of 64 × 64 pixels was developed.

A different approach was taken in [16], where pixels are scanned by quad-tree, and one quad-tree code determines a block of pixels to be read out. A prototype of 32 × 32 pixels were made.

3.2 Temporal Processing

Temporal processing can be very different between the computational sensor and the traditional digital processing system. Three examples are drawn in this section.

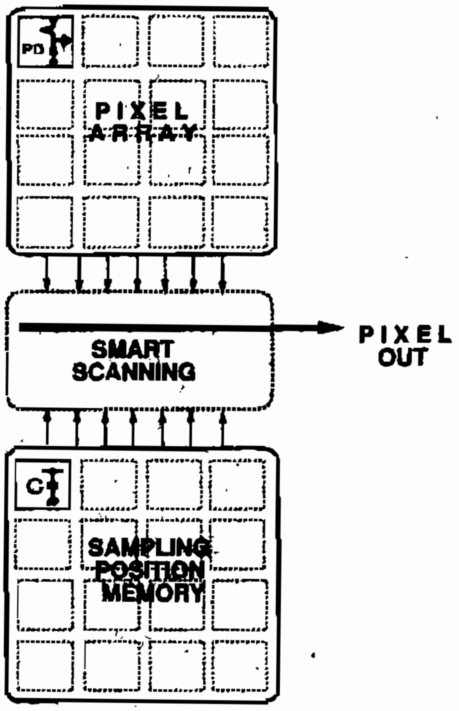


Fig. 7 Architecture of variable spatially sampling sensor.

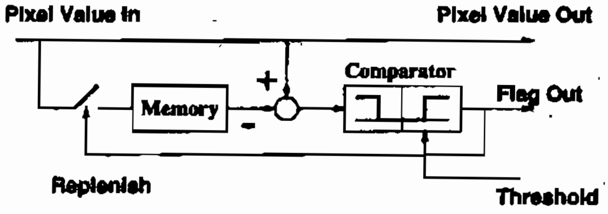


Fig. 8 Compression scheme of conditional replenishment.

3.2.1 Compression

Inherent difficulty of very fast image processing is transferring very high bandwidth image signal out of the sensor. Then, compression is one of the most desirable processing on focal plane. Compression integrated on focal plane overcomes the problem of high bandwidth, the fundamental limitation to the feasibility of high pixel-rate imaging such as high frame rate imaging.

Compression sensor integrated with analog compression using conditional replenishment was developed [18]–[21]. Figure 8 illustrates the scheme of conditional replenishment. Current pixel value is compared to the last replenished value stored in the memory, and the value and address of an activated pixel, for which the magnitude of the difference is greater than

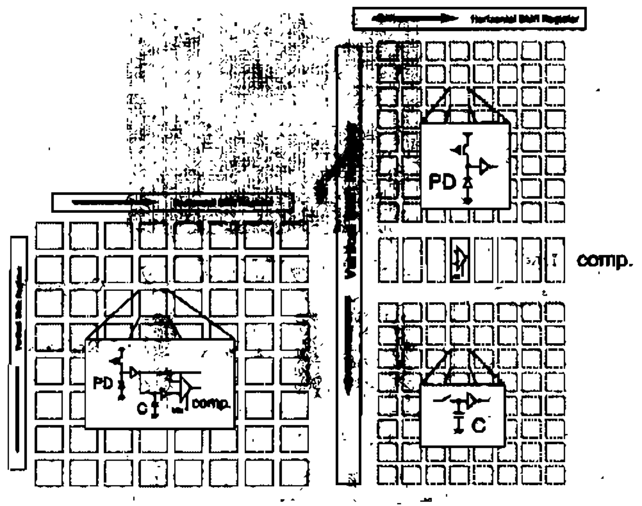


Fig. 9 Illustrations of compression sensors of pixel parallel architecture (left) and column parallel architecture (right).

the threshold, are extracted and output from the sensor. The value of the memory of the activated pixel is replenished by the current input value, and that of a non-activated pixel is kept unchanged. The conditional replenishment algorithm is not complex and lends itself easily to highly paralleled processing. This compression scheme gets more efficient at higher frame rate because motion is less at higher frame rate.

Compression sensors of both pixel parallel and column parallel architecture were developed. As shown in Fig. 9, in the pixel parallel approach [18], [19], each pixel contains photo-diode (PD), comparator and memory. Rate control for entire frame is also implemented on the focal plane in the pixel parallel prototype. The drawback is fill factor and power dissipation. The prototype of pixel parallel architecture, under 2 μm CMOS process has 32 × 32 pixels of 160 × 160 μm^2 pixel, and fill factor is 1.9%.

In order to improve the imaging performance, the column parallel architecture was also developed [20], [21]. The column parallel architecture has PD array, memory array and comparators shared by pixels in a column. Then, pixels in a row are processed in parallel. The PD array is almost ordinary CMOS sensor and the fill factor is very much improved (38.5% in 32 × 32 pixel prototype under 1 μm CMOS process). Because each comparator is shared by the pixels in a column, the total number of comparator is reduced and power dissipation is reduced. The operation speed is more than 15,000 frames per sec even in the column parallel prototype. The resolution of column parallel prototype is lately improved to 128 × 128 pixels [21].

As for compression, it is notable that a compression sensor with analog DCT transform on focal plane is also developed [22].

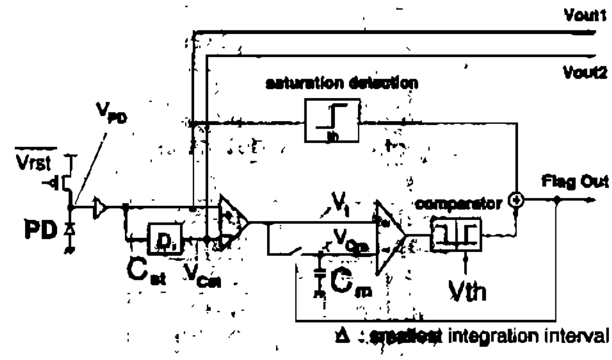


Fig. 10 Processing scheme for each pixel of adaptive sensor, in which integration time is adapted to motion and light.

3.2.2 Adaptive Sensor: Enhancement and Wide Dynamic Range

A computational sensor has been investigated, each pixel of which adapts its integration time to motion and light in such a way that the integration is finished if motion is detected or pixel intensity is saturated [23]. The pixel value is normalized after it is read out. Then, moving areas of pixels have shorter integration time with little motion blur, brighter areas have shorter integration without saturation, and darker areas have longer integration with better SNR. The pixel-wise adaptivity to motion and light improves intrascene temporal resolution and intrascene dynamic range. The processing scheme is illustrated in Fig. 10. A prototype of 32 × 32 pixels was developed, which uses column parallel processing architecture.

3.2.3 Motion Detection/Estimation

Motion detection scheme is rather different in computational sensor compared to ordinary digital processing scheme [24]. Motion detection on sensor focal plane ranges between change detection in a pixel, 1D motion direction detection, 1D motion vector (direction and magnitude) detection and 2D motion vector detection. Because of the limitation of spatial processing, typical approach to the motion detection on focal plane uses correlation between only adjacent pixels, as illustrated in Fig. 11. Temporal edge in each pixel or spatial edge is detected and the motion of the edge is measured using correlated information between adjacent pixels. For example, the time delay between the pulses is measured. In most cases, the motion detection of computational sensor is limited to one dimensional case. Review about motion processing is found in [24].

Differing from the above approach, optic flow scheme [3], [25] and block matching scheme [26] have been also investigated. In the former, motion field is computed by spatial gradient. In [25], formulation of optic flow is simplified and 2D motion vectors are com-

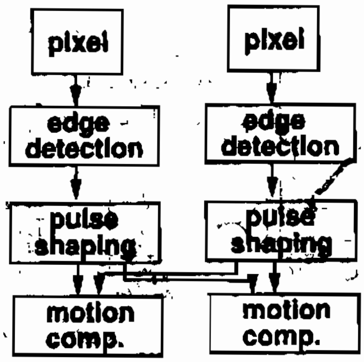


Fig. 11 Motion computation using correlation between adjacent pixels.

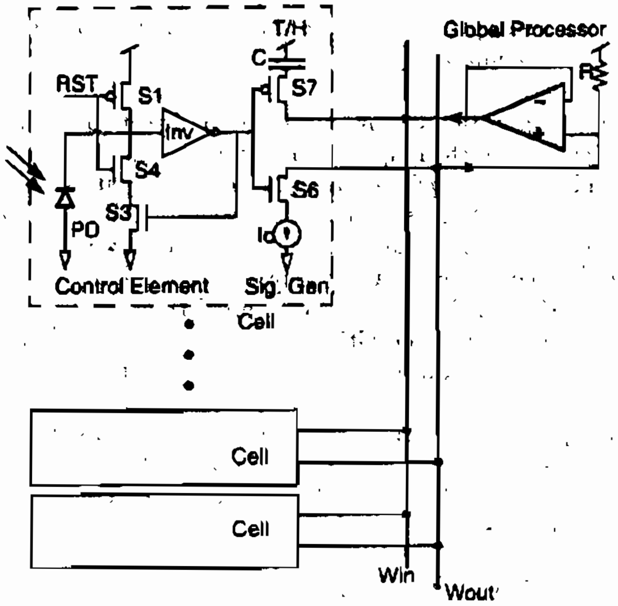


Fig. 12 Architecture of sorting sensor [27].

puted by pixel parallel processing. Block matching is also attempted in such a way that edges are detected first, and block matching of edges is performed, at very fast frame rate, in search area of ±1 pixels in both x and y direction. Matching is done in column parallel way [26].

3.2.4 Sorting Sensor

A computational sensor which sorts pixels by the magnitudes of their intensities and produce cumulative histogram was proposed. Finding the order is one of global operations that is not easy for computational sensors. In the sorting sensor shown in Fig. 12, each pixel contains an inverter, and intensity of pixels is observed by their response time. Temporal processing is efficiently applied to the task. The principle is as follows: when the inputs have different intensities, the responses are separated in time. A global processor (a single operational amplifier) survey the pixel array, aggregates triggers of pixels, and the voltage provided by the global processor to all pixels changes from high to low linearly to the number of accumulated number of triggered pixels. Each pixel has a memory which records the voltage of the global processor at the instance when the pixel is triggered. Then, the sorting order is in each memory of the pixel.

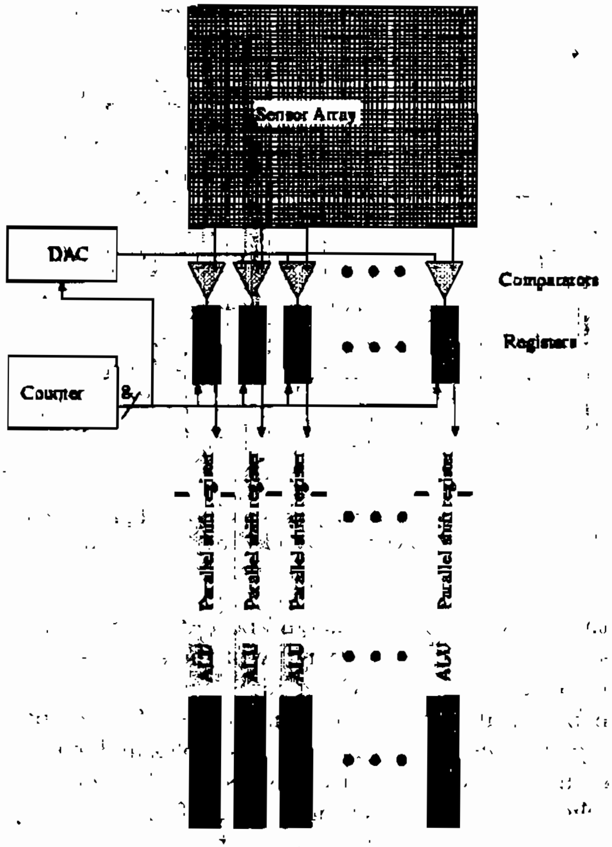


Fig. 13 Architecture of digital programmable computational sensor based on column parallel architecture [1], [28].

3.3 Programmable Computational Sensors

There have been attempts towards programmable computational sensors based on digital processing, which enables several simple image processing operations. Implementations using both column parallel architecture [28], [29] and pixel parallel architecture [30]–[32] have been investigated.

The column parallel architecture [28] has pixel array, and A/D conversion, register, ALU, memory for each column, which is shown in Fig. 13. Following this architecture, IVP developed and commercialized 256 × 256 pixel array with 8 bit A/D conversion [29]. This vision chip, for example, execute binary edge detection in 0.5 msec/frame and gray scale edge detection

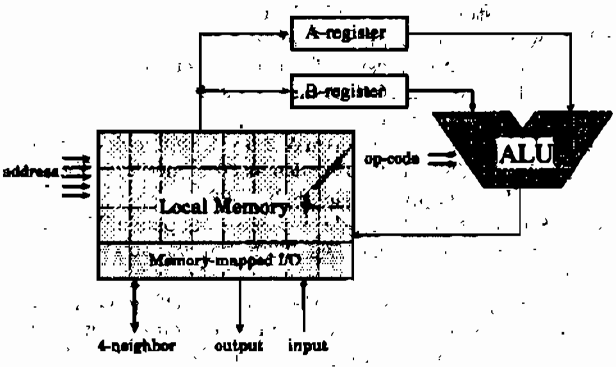


Fig. 14 Architecture of computational sensor based on pixel parallel digital approach [32].

in 10 msec/frame.

Pixel parallel digital approach is also investigated. Simple 2D boolean operation was achieved by pixel parallel fashion in [30]; the prototype contains 65×76 pixels with 1 bit pixel level digitization by thresholding, and executes, for example, edge detection in 5 μsec. Digital processing scheme based on efficient A/D conversion (named Near Sensor Image Processing, NSIP) was developed, in which the pixel intensity is represented by the time that it takes for the PD voltage from the precharged voltage to the reference voltage [31]. The prototype of 32 × 32 pixel arrays with processing circuit and A/D conversion for each pixel were implemented. The most straightforward approach in digital based pixel parallel scheme is [32], in which each pixel contains A/D conversion, ALU and local memory shown in Fig. 14. The processing speed is very fast, for example, edge detection is done in 1 μsec. The prototype of 8 × 8 pixel arrays were implemented. As mentioned in the introduction, the pixel parallel approach has disadvantage in fill factor and resolution. The fill factors for the above three are less or much less than 1%.

Apart from the specific computational sensor, CMOS sensor which is directed toward "camera-on-a-chip" also needs A/D conversion, timing control, gain control, white balance, interfaces etc. integrated together with pixel array. However, it may not need any parallel processing.

3.4 A/D Conversion (ADC)

ADC on focal plane is important especially for the "camera-on-a-chip" direction which requires higher precision for imaging quality. Various approaches were proposed, and parallelism differs among them. Single ADC integration (no parallelism), column parallel ADC and pixel parallel ADC have been investigated.

In case of single ADC integration, color CMOS sensors of 352 × 288 [33] and 306 × 244 pixels [34] integrated with flash ADC were developed. In the latter prototype, smoothing, edge detection, gain control, γ correction are carried out for the digitized image by digital processing, and finally DAC is performed, and analog video signal is output from the chip.

In case of the column parallel ADC integration, in which ADC can be much slower compared to the single ADC approach, single slope ADCs [28], [29] which is shown in Fig. 13 and successive approximation ADC [35] have been implemented on the focal plane. A commercial product of 512 × 384 pixels color CMOS sensor integrated with 8 bit column parallel ADC is in market [36]. Pixel parallel ADC is also investigated [37], in which $\Sigma - \Delta$ ADC is contained in each pixel.

4. Conclusion

Computational sensor is a very small integrated system, in which processing and sensing are unified on a single VLSI chip. It is designed for a specific targeted application. Research activities of computational sensor are summarized in this paper, along with examples of computational sensors of spatial processing, temporal processing, programmable computational sensors, and A/D conversion.

Integration of sensing and processing (or a part of processing) on a single chip is very challenging. The integrated system is quite different from the traditional module system which is limited to NTSC spatio-temporal resolution. Processing paradigm can quite differ from the digital processing framework.

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