Analytical models for amorphous-silicon and polysilicon thin-film transistors for high-definition-display technology

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Abstract — In just the last decade, the flat-panel-display industry has expanded into a multi-billion-dollar market, led primarily by color active-matrix liquid-crystal displays (AMLCDs). These displays use hydrogenated amorphous-silicon (a-Si:H) and polysilicon (poly-Si) thin-film transistors (TFTs) as the switching elements. Consequently, for display design, more sophisticated and accurate TFT models for circuit simulators are becoming essential. In this paper, we review the requirements of a-Si:H and poly-Si TFT technologies for use in AMLCDs and discuss two-dimensional device-simulation results, which allow us to examine phenomena caused by the high density of localized states in a-Si:H and poly-Si. With this understanding of both the material physics and the requirements for TFTs in AMLCD technology, we can develop suitable device models for circuit simulation and device design and characterization. Our physics-based analytical TFT models for both a-Si:H and poly-Si TFTs will be described. These models have been implemented in SPICE and accurately describe both the subthreshold and above threshold regimes.

Keywords — *Amorphous-silicon TFTs, polysilicon TFTs, thin-film transistors, AMLCDs.*

1 Introduction: TFT requirements for AMLCDs

The most important application of hydrogenated amorphous-silicon (a-Si:H) and polysilicon (poly-Si) thin-film transistors (TFTs) is in active-matrix liquid-crystal displays (AMLCDs). Just a decade ago, cathode-ray tubes completely dominated the display market, but the development of notebook PCs and high-definition TVs has created a demand for large-area flat-panel displays. In 1990, the market for LCDs worldwide reached $1.5 billion and is expected to grow to $10-15 billion by 1998. Accurate device models that reflect the critical parameters for AMLCD technology are necessary for circuit designers. In this paper, we will first review the requirements for TFTs in AMLCD technology in order to target the most important requirements for TFT modeling. In Sections 2 and 3, we discuss the physics and modeling of poly-Si and a-Si:H TFTs and present our TFT models for circuit simulation.

We will start from the discussion of the TFT parameters that are important for their applications in AMLCDs. The limitations in display performance may be caused by both the TFT characteristics and the resistance and capacitance of the metal gate lines. We will first examine the limitations caused by the TFTs, and then discuss those caused by the metal gate lines.

1.1 TFT performance limitations

A liquid crystal sandwiched between the pixel electrodes and the common bottom indium tin oxide (ITO) contact has a very large resistivity (on the order of 10^{12} Ω-cm), and each liquid-crystal cell can be represented by an equivalent nonlinear capacitance. The relative transmittance of the liquid-crystal cell varies with applied bias from nearly zero to a maximum, as shown in Fig. 1. Typically, $V_{90} \approx 2$ V and $V_{10} \approx 3.5$ V.[1] Hence, the cell switches from minimum to a maximum over a range of approximately 1.5–2 V.

Consider the operation of an AMLCD with N_{col} columns and N_{row} rows. In such a display, the pulse signal which turns the TFTs on is applied to all TFT gates in one row, then it is shifted to the next row, and so on. The gate pulse width, T_G, equals T_{frame}/N_{row}, where T_{frame} is the frame period. Typically, T_{frame} = 1/60 s = 16.7 ms. For N_{row} = 480, $T_G \approx 35$ μs. During each gate pulse, the video signal is applied to all the column electrodes. [Since liquid-crystal cells

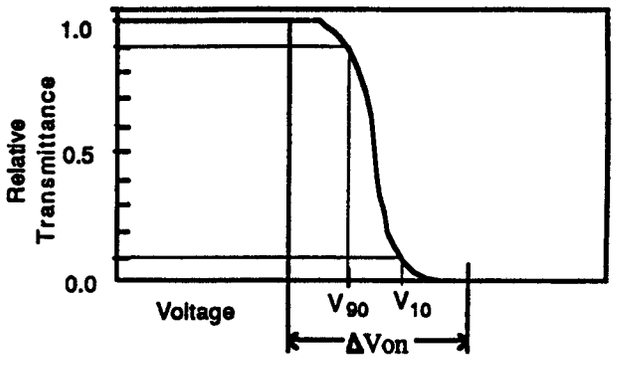

FIGURE 1 — Qualitative dependence of transmittance of a liquid-crystal cell on bias voltage.

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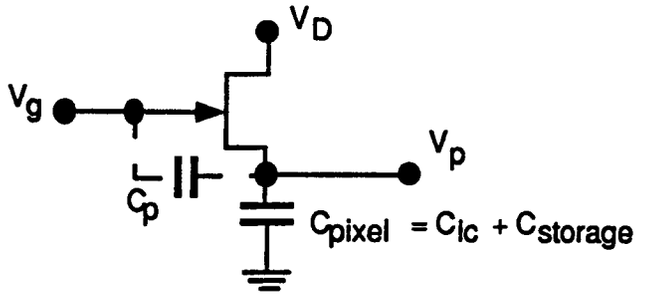

FIGURE 2 — Pixel driver circuit.

rapidly deteriorate at a dc bias and since the transmittance of the cells depends only on the voltage (electric field) magnitude and not on its polarity, the video signal polarity changes every frame cycle.] The video signal applied to a given column charges the liquid-crystal capacitance at the intersection of this column and the selected row of pixels. During this charging period, the TFT operates in the linear regime so that $V_{gs} - V_t > V_{ds}$, where V_{gs} is the gate-to-source voltage, V_t is the threshold voltage, and V_{ds} is the drain-to-source voltage. The on-current should be high enough to charge the pixel capacitance, C_{pixel} (which often includes an additional storage capacitance parallel to the pixel capacitance for better charge retention). Figure 2 shows the equivalent circuit for a pixel driver. Figure 3 shows the voltage waveforms obtained from a SPICE simulation with a feedthrough capacitance, C_p, of 0.2 pF and a pixel capacitance of 1 pF.

The on-current required to charge the pixel capacitance has to fulfill the following requirement:

$$I_{on} \geq \frac{6C_{pixel}V_{on}}{T_G} = \frac{6C_{pixel}V_{on}N_{row}}{T_{frame}}, \qquad (1)$$

where V_{on} is the gate voltage swing of the TFT in the on-state. The factor of 6 in Eq. (1) follows from the requirement that the pixel be fully charged and was estimated from SPICE simulations (see Fig. 3). The maximum loss in the pixel charge, ΔQ, tolerable while still preserving the gray scale is given by

$$\Delta Q = \frac{C_{pixel}\Delta V_{on}}{N_{gray}M}. \qquad (2)$$

This charge must be retained through T_{frame}. In Eq. (2), ΔV_{on} is the voltage switching the liquid crystal from the transparent to the opaque state, N_{gray} is the number of gray levels, and M is a safety margin coefficient ($M \approx 3$). Hence, the off-current should be less than

$$I_{off} \leq \frac{C_{pixel}\Delta V_{on}}{N_{gray}MT_{frame}} \qquad (3)$$

and the on-to-off ratio should be greater than

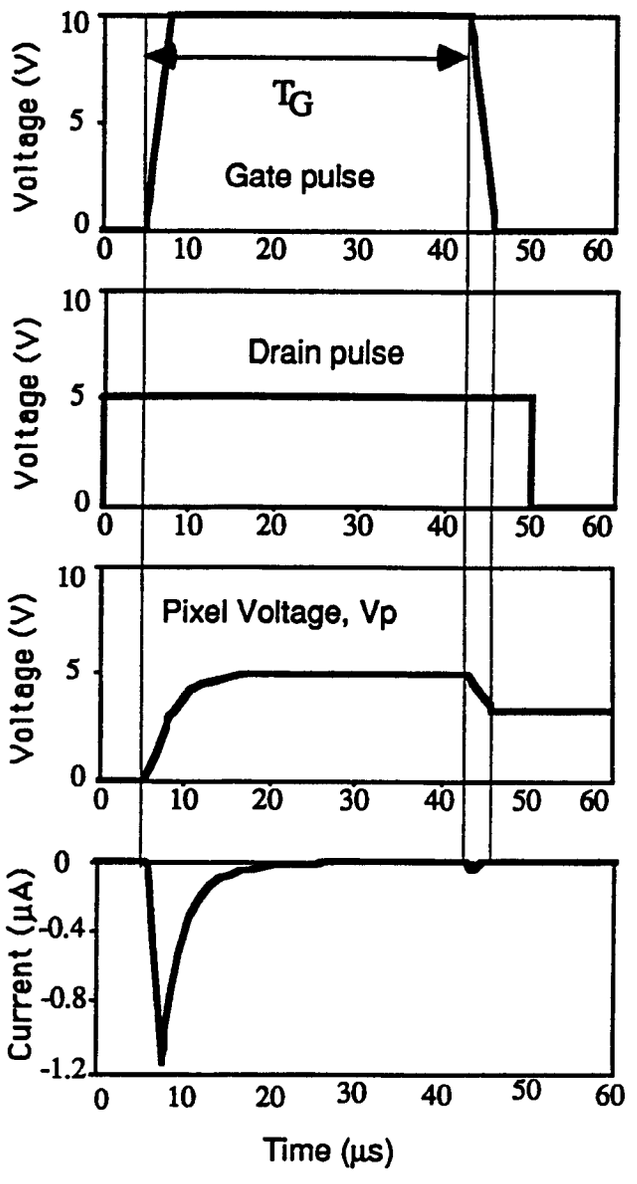

FIGURE 3 — Simulated voltage and drain-current waveforms for an a-Si:H TFT pixel driver. The feedthrough capacitance is 0.2 pF, the pixel capacitance is 1 pF, W/L is 35 μm/7 μm, V_{to} = 2 V, and $K_p = 2.3 \times 10^{-8}$ A/V^2.

$$\frac{I_{on}}{I_{off}} \geq \frac{6MN_{row}V_{on}N_{gray}}{\Delta V_{on}}. \qquad (4)$$

For $\Delta V_{on} \approx 1$ V, $V_{on} = 5$ V, $N_{gray} = 16$, and $N_{row} = 480$, we should have $I_{on}/I_{off} \geq 7 \times 10^5$. This estimate is in good agreement with the estimate of the on-to-off resistance ratio required for diodes used to drive LCDs.[2]

Generally speaking, a-Si:H TFTs meet this requirement at room temperature where an on-to-off ratio of 10^7 can be achieved even for zero gate voltage in the off-state. However, the off-current is temperature activated with an activation energy of the order of 0.7 eV.[2] Hence, the on-to-off ratio decreases with temperature, T, roughly as

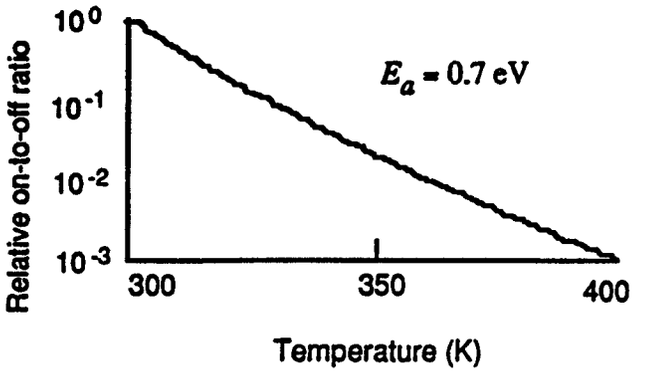

FIGURE 4 — Relative on-to-off current ratio as a function of temperature for an activation energy of 0.7 eV. Relative current ratio is defined as the current ratio at a temperature T divided by the room-temperature current ratio, which is ~10^7.

$$\frac{I_{on}}{I_{off}}(T) \approx \frac{I_{on}}{I_{off}}(T_0)\exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_0}-\frac{1}{T}\right)\right], \tag{5}$$

where k_B is Boltzmann's constant. Figure 4 shows the decrease in the relative on-to-off current ratio as a function of temperature assuming an activation energy of 0.7 eV. The relative current ratio is defined as the current ratio at a temperature T divided by the current ratio at room temperature (T_o). Because the room temperature ratio is ~10^7, and a minimum ratio of 10^5 is required, this figure indicates that a 480-row a-Si:H AMLCD could work reliably up to possibly 60°C. However, it may be very difficult to design such displays operating in a military range of temperatures (up to 125°C).

Another important limitation on the TFT follows from the voltage division between the TFT feedthrough gate-to-source capacitance, C_p, and the pixel capacitance in the on-state (which includes the storage capacitance) (see Fig. 2). When the gate bias is on ($V_g = V_{ghigh}$), the pixel capacitance stores charge $C_{pixel}V_D$ and the feedthrough capacitance stores charge $C_p(V_D - V_{ghigh})$. When the gate bias is brought to zero, these two charges combine, the resulting charge is shared between the two capacitances, and the pixel potential drops, as can be seen from Fig. 3 (see also Ref. 1, p. 104). To a first approximation

$$\begin{aligned} V_P &= \frac{C_P(V_D - V_{ghigh}) + C_{pixel}V_D}{C_{pixel} + C_P} \\ &= V_D\left(1 - \frac{C_P}{C_{pixel}+C_P}\frac{V_{ghigh}}{V_D}\right). \end{aligned} \tag{6}$$

The SPICE simulation of the pixel driver circuit shown in Fig. 2 for a typical a-Si:H TFT with a total pixel capacitance of 1 pF with and without the parasitic capacitance of 0.2 pF illustrates this effect.

It is very important, therefore, that C_p not be too large a fraction of the pixel capacitance. More importantly, C_p must not vary too much from one pixel to another. Uniformity of C_p is particularly important as the number of shades of gray increases and leads directly to a limitation on the TFT width, W, since C_p is proportional to W. If W is scaled down in order to keep C_p and ΔC_p small, then the gate length must be scaled down accordingly to keep the on-current high enough.

The transistor characteristics used in the pixel simulation shown in Fig. 3 (W = 35 μm, L_g = 7 μm, d_i = 0.3 μm, V_t = 2 V) are similar to those used in a 14.3-in. color display.[3] Since the gate pulse width used in this display is only 14.5 μs, the W/L ratio of 5 is probably close to the minimum possible value for this display. On the other hand, 7-μm-long a-Si:H TFTs may already exhibit short-channel effects, the most unpleasant of which is an increase in the leakage current.

Still another important problem is TFT stability[4] which is especially a concern for a-Si:H TFTs. A prolonged application of gate-to-drain dc bias causes a shift of the threshold voltage as well as large changes in the subthreshold and leakage currents[5,6]. Similar effects occur as a result of temperature increases to 160°C.[3] These effects are alleviated in the pixel driver circuits since, as mentioned above, the voltage polarities alternate each frame. Therefore, dc bias is never continually present at one side of the channel. This approach prevents the deterioration of the liquid crystal; nevertheless, the TFT stability is a concern, especially at elevated temperatures.

1.2 Metal-row-line performance limitations

Let us now examine the performance limitations presented by the metal gate (row) lines. When the voltage on the gate line changes, two issues must be considered: (i) the time delay imposed by the TFT gate capacitance alone, and (ii) the time delay associated with the metal-gate-line capacitance.

During a voltage transient, the TFT gate-capacitance charging time is on the order of the channel transit time, T_{tr}. Since the effective electron velocity $v \approx \mu_{FET}V_{ds}/L_{gate}$, then

$$T_{tr} \approx \frac{L_{gate}}{v} = \frac{L_{gate}^2}{\mu_{FET}V_{ds}}, \tag{7}$$

which is 0.2 μs for μ_{FET} = 1 cm^2/V-s, V_{ds} = 5 V, and L_{gate} = 10 μm. Since this is much smaller than the 10–40-μs gate pulse duration of a typical display, transit-time effects do not seem to present an important limitation.

During the same transient, the time constant due to the metal row line is $T_{RC} = 3R_sC_{line}$, where R_s is the series resistance of the gate line and C_{line} is the gate-line capacitance. The series resistance of the gate line is given by

$$R_s = \frac{\rho_{line}L_{line}}{S_{line}}, \tag{8}$$

where L_{line} is the length of the line (determined by the display size) and S_{line} is the line cross section. ρ_{line} is the line

resistivity, which varies from 2.5 to 200 μΩ-cm. A ρ_{line} of ~5 μΩ-cm is achievable for composite triple layer lines (see Ref. 1, p. 120). Assuming $S_{line} = 3L_{gate}d_{line}$, where d_{line} is the effective gate-line thickness and L_{gate} is the gate length (i.e., the row line is three times as wide as the TFT gate length), we find

$$T_{RC} = \frac{\rho_{line}L_{line}}{L_{gate}d_{line}} \frac{\varepsilon_i 3L_{gate}L_{line}}{d_i} = \frac{3\varepsilon_i\rho_{line}L_{line}^2}{d_{line}d_i}, \quad (9)$$

where ε_i and d_i are the gate dielectric permittivity and thickness, respectively. For $d_i = 0.3$ μm, $\varepsilon_i = 7 \times 10^{-11}$ F/m, $d_{line} = 0.2$ μm, and $\rho_{line} = 5$ μΩ-cm, we obtain $T_{RC}(\mu s) \approx 7 \times (L_{line}(\text{cm})/20)^2$. This is comparable to the gate pulse width, and, hence, the resistance of the gate lines may present a serious limitation to the increase in the display size.

The above discussions allow us to list the basic requirements for accurate TFT modeling. Analytical device models should be capable of describing (i) the device characteristics over many orders of magnitude of the device currents (to account for the large required on-to-off ratio), (ii) the device capacitance, and (iii) the proper scaling of characteristics with length and temperature. The models should also allow for routine automatic parameter extraction for use in quality control and assurance programs. This will permit statistical analysis of AMLCD data for improving yield. Finally, the models should guarantee excellent convergence and reasonable computation speed in the simulation of large TFT circuits. Current crystalline-silicon (c-Si) SPICE transistor models do not meet these requirements.

The remainder of this paper describes analytical models for both poly-Si and a-Si TFTs which meet these criteria.

2 Poly-Si TFT device models for circuit simulators

Poly-Si TFTs are very attractive for use in AMLCDs for several reasons. Larger displays can be realized by replacing a-Si:H TFTs as the pixel switching element. Also, replacing the c-Si devices currently used in peripheral circuitry allows virtually all of the display's circuitry to be integrated onto a single substrate, reducing manufacturing costs. In addition to display technology, poly-Si TFTs are already being implemented in analog and digital circuits for other large area applications.[7,8] Therefore, accurate circuit models are critical.

The main challenges in modeling poly-Si TFTs lie in their differences from c-Si devices: (i) subthreshold leakage caused by a high density of grain boundary traps in the bandgap; (ii) the "kink" effect, which results in an increase in output conductance in the saturation regime of operation; (iii) channel mobility, μ_{FET}, which increases with gate bias until it "saturates" at a high field value; (iv) low subthreshold slope, again due to the boundary traps; and (v) the discrepancies among the various methods of extracting threshold voltage.

2.1 Review of poly-Si TFT models

In 1986, Ahmed *et al.*[9] published a model for accumulation-mode poly-Si devices which was based on a one-dimensional solution of Poisson's equation and which included the effects of grain-boundary traps. However, the model's applicability to inversion mode devices was not clear because of a "reverse" charge shielding concept employed in its derivation. More importantly, for circuit simulators, their expression for drain current required iteration to first solve for surface potential.

A few years later, Lin *et al.* solved a quasi-two-dimensional Poisson's equation at a grain boundary of an enhancement-mode TFT.[10] This resulted in an expression for grain barrier height as a function of V_{gs} and lateral electric field (and therefore V_{ds}). The barrier height was then used in an expression for I_d above threshold. For small V_{ds}, the result was the same as for the linear region of a c-Si transistor with reduced mobility. For large V_{ds}, the expression for I_d was an integral equation which had to be evaluated numerically. In the saturation regime, I_d did not level off, but increased exponentially with V_{ds} due to drain-induced gate barrier lowering (DIGBL). This increase in I_d results directly from the dependence of barrier height on V_{ds}. Further insight relating TFT characteristics to the poly-Si material parameters was provided by Fortunato and Migliorato.[11]

Several examples of analog and digital circuit design[7,8] have been published which employ the circuit model originated by Izzard *et al.*[12] and expanded upon by Quinn *et al.*[13] Here, the authors adopted an "effective medium" approach which treated the non-uniform poly-Si sample with grain boundaries as some uniform effective medium with effective material properties.[14] The TFT's channel conductance was represented as a polynomial in V_{gs} and channel voltage. Expressing the conductance in this manner is likened to the method used by Shur *et al.*[15] for expressing a-Si:H TFT mobility. A significant difference, however, is that by expressing channel conductance (as opposed to mobility) as a polynomial, short-channel and temperature effects are essentially "buried" in the polynomial's coefficients.

Byun *et al.*[16] and Shur *et al.*[17] have also adopted the effective medium approach. This method is attractive because it allows the development of comparatively simple models with only a few easily extracted parameters which are well suited to circuit simulators such as SPICE. The drawback is that the circuit models cannot always be related to material properties as in Refs. 10 and 11.

The remainder of this section expands on the model presented in Ref. 17. Expressions will be presented for the subthreshold and above-threshold current, and subthreshold leakage current which will then be combined into a total drain current, I_d. The kink effect has not been included but will be added in the future.

2.2 Subthreshold and above-threshold currents

Subthreshold current in poly-Si TFTs is given by

$$I_{sub} = \mu_s C_{ox} \frac{W}{L} V_{sth}^2 \exp\left(\frac{V_{GT}}{V_{sth}}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right]. \quad (10)$$

Here, $V_{sth} = \eta kT/q$ is an extracted parameter and η is an ideality factor, $V_{GT} = V_{GS} - V_t$, μ_s is the effective subthreshold mobility, and the other symbols have their usual meaning. Equation (10) is very similar to the expression for subthreshold current in c-Si MOSFETs, which is dominated by the diffusion component of current.

The drain current above threshold is given by

$$I_a = \begin{cases} \mu_{FET} C_{ox} \dfrac{W}{L}\left(V_{GT}V_{DS} - \dfrac{V_{DS}^2}{2\alpha_{sat}}\right) & \text{for} \quad V_{DS} < \alpha_{sat} V_{GT} \\ \mu_{FET} C_{ox} \dfrac{W}{L} \dfrac{V_{GT}^2 \alpha_{sat}}{2} & \text{for} \quad V_{DS} \geq \alpha_{sat} V_{GT} \end{cases} \quad (11)$$

where the field-effect mobility, μ_{FET}, is given by

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_0} + \frac{1}{K_\mu |V_{GTE}|^m}. \quad (12)$$

In Eq. (12), $V_{GTE} \approx V_{GT}$ at large gate biases, and $V_{GTE} \approx 2V_{sth}$ for $V_{GT} \leq 0$ V.[18]

The field-effect mobility, μ_{FET}, given in Eq. (12) is quite different from its c-Si counterpart. In c-Si, mobility tends to decrease as V_{GT} increases.[19] In poly-Si TFTs, μ_{FET} increases with V_{GT} as the induced charge fills grain boundary traps, and a larger fraction of this induced charge resides in the conduction band and is mobile. For large V_{GT} the traps are filled, and the constant high field mobility, μ_0, dominates μ_{FET}, while at low V_{GT}, mobility is approximately proportional to $(V_{GT})^m$. K_μ and the exponent m are constants. Both measured and modeled field-effect mobility are plotted in Fig. 5 for a 50 × 50-μm² n-channel TFT.

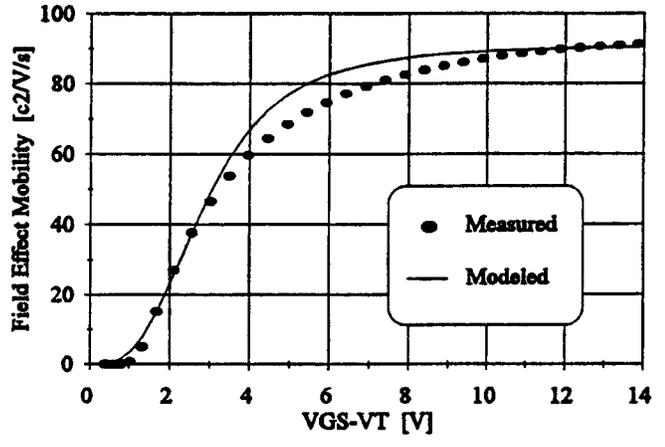

FIGURE 5 — Measured and modeled field-effect mobility for a 50 × 50-μm² n-channel poly-Si TFT.

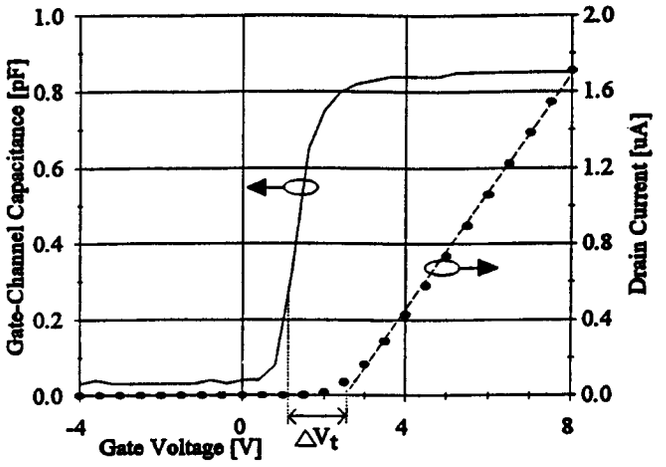

FIGURE 6 — N-channel TFT threshold voltage extraction from both I_d and C_{gc} data. The difference between the two methods, ΔV_t, is 1.5 V. For p-channel TFTs, ΔV_t can be as large as 5 V.

Because of this mobility behavior, it is important that the threshold voltage be defined in terms of the carrier density in the channel, and not simply extrapolated from $I_d - V_{GS}$ data. The V_t must be determined from C–V data since, unlike c-Si devices, it is very different from the apparent V_t deduced from the drain current data.[20] The shift in threshold voltage, ΔV_t, is shown in Fig. 6 to be 1.5 V for an n-channel TFT. ΔV_t can be as large as 5 V for p-channel devices.

Finally, note that instead of simply defining $V_{DS,SAT} = V_{GT}$, the saturation voltage is assumed to be proportional to V_{GT} with a constant of proportionality, α_{sat}. This is similar to an approximation made for c-Si devices to account for the variation of the depletion (bulk) charge across the channel.[21]

It should be pointed out that Eqs. (10) and (11) do not coincide at $V_{GS} = V_t$. Because of this, the subthreshold and above-threshold drain currents are combined to give the total drain current (excluding leakage) through

$$I'_d = \frac{I_{sub} I_a}{I_{sub} + I_a}. \quad (13)$$

Although somewhat arbitrary, Eq. (13) essentially picks the lesser of the two currents when deep in either the subthreshold or above-threshold regimes. It also provides a smooth transition between the regimes, which is very important for speedy convergence once the model is implemented in a circuit simulator.

All of the previous equations have been expressed in terms of the intrinsic voltages, V_{GS} and V_{DS}. However, series resistance in the source and drain terminals can be significant in poly-Si devices. The extrinsic voltages are the voltages that are actually applied during measurements of the device, and the intrinsic voltages are therefore defined as

$$\begin{aligned} V_{DS} &= V_{ds} - 2I_d(R_s + R_d) \\ V_{GS} &= V_{gs} - R_s I_d, \end{aligned} \quad (14)$$

where R_s and R_d are the source and drain resistances, respectively, and the lower-case subscript indicates an extrinsic volt-

TABLE 1 — Poly-Si TFT intrinsic model parameters.

Parameter	Description
V_t	Threshold voltage
C_{ox}	Gate insulator capacitance
V_{sth}	Sub-V_t thermal voltage fitting parameter
μ_s	Subthreshold mobility
α_{sat}	$V_{ds,sat}$ constant of proportionality
m	Low-field mobility exponential parameter
K_μ	Low-field mobility constant
μ_0	High-field mobility
A	I_{leak} electric-field constant
B	Drain-induced barrier-lowering term
C	I_{leak} constant of proportionality

age. For the devices presented here, $R_s = R_d$. R_s is comprised of the contact resistance plus the resistance associated with the sheet resistance of the source and drain regions. Although it is frequently approximated as a constant (as in Table 2), our data indicate that it is actually nonlinear. However, for long-channel devices such as those modeled in Table 2, the constant R_s is a reasonable approximation.

The parameters which must be extracted are summarized in Table 1. As previously mentioned, the goal is to extract parameters with little or no iteration, allowing convenient statistical analysis and rapid feedback in a fabrication facility. The following data are necessary to extract the parameters: (i) I_d *vs.* V_{gs} data for a low drain bias; (ii) I_d versus V_{ds} data for a large drain bias; and (iii) C_{gs}, the gate-to-source capacitance, as a function of V_{gs}. Since the components of R_s can be measured independently from test structures, series resistance can easily be included in the extraction procedure.

TABLE 2 — Parameters for TFTs shown in Figs. 7–14.

Parameter	*N*-ch 50 × 50 μm (Figs. 7 and 8)	*P*-ch 50 × 50 μm (Figs. 9 and 10)
R_S†	800 Ω	1500 Ω
V_t	1.157 V	−2.010 V
C_{ox}	32.8 nF/cm^2	32.8 nF/cm^2
V_{sth}	0.170 V	−0.261 V
μ_s	9.47×10^{-1} cm^2/V-s	9.03×10^{-3} cm^2/V-s
α_{sat}	0.9	0.6
m	3.06	2.68
K_μ	3.60	0.14
μ_0	91.3 cm^2/V/s	60.0 cm^2/V/s
A	5×10^4 cm^{-1}	5×10^4 cm^{-1}
B	5×10^{-5}	-2×10^{-5}
C	0.02 A	0.02 A

†R_S is an effective constant value (see text).

The above model has been applied to *n*- and *p*-channel TFTs as shown in Figs. 7–10. The extracted model parameters are listed in Table 2. Subthreshold leakage is considered next.

2.3 Subthreshold leakage current

As shown in Figs. 7 and 9, subthreshold leakage can be significant in both *n*- and *p*-channel devices for large drain bias. Several authors have proposed models for the leakage current, most of which are based on some sort of field emission. Fossum *et al.*[22] developed a model based purely on field emission through grain-boundary traps and achieved a good qualitative fit. A quantitative comparison of the theory with the data was not possible, however, because many of the material parameters were unknown.

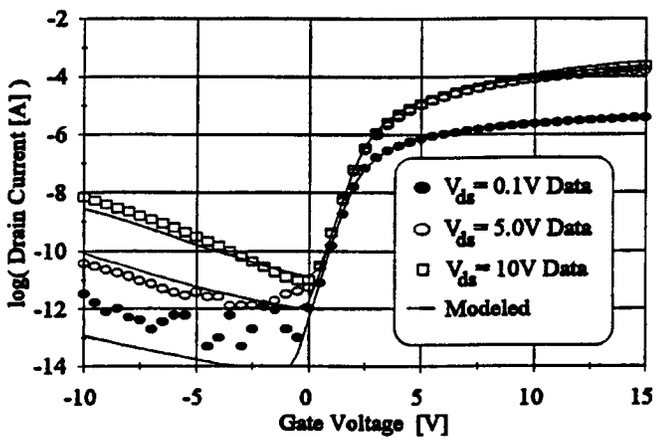

FIGURE 7 — *N*-channel 50 × 50-μm^2 poly-Si TFT subthreshold characteristic for drain biases of 0.1, 5.1, and 10.1 V.

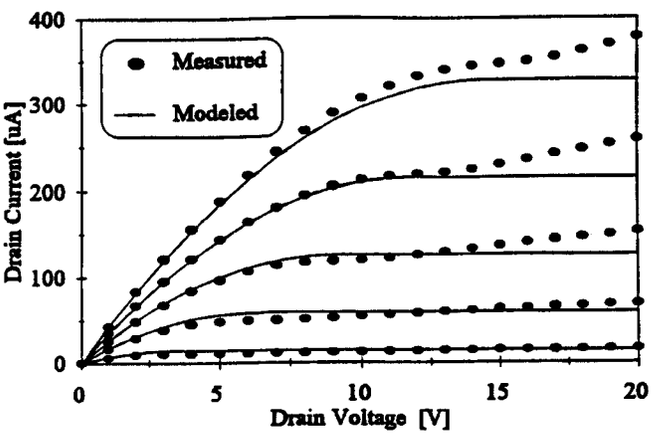

FIGURE 8 — *N*-channel 50 × 50-μm^2 poly-Si TFT above-threshold characteristic for gate biases of 5, 8, 11, 14, and 17 V.

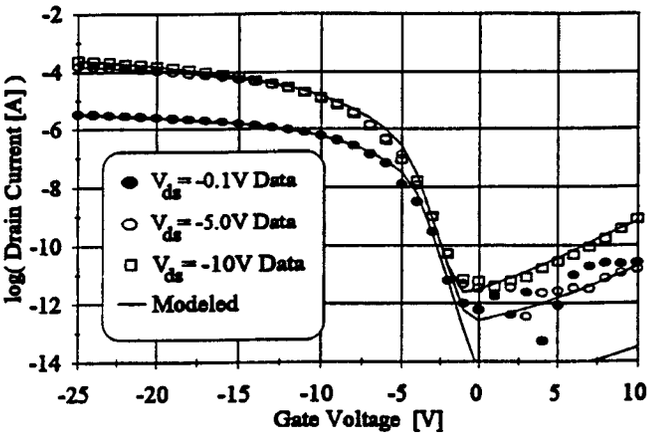

FIGURE 9 — *P*-channel 50 × 50-μm² poly-Si TFT subthreshold characteristic for drain biases of –0.1, –5.1, and –10.1 V.

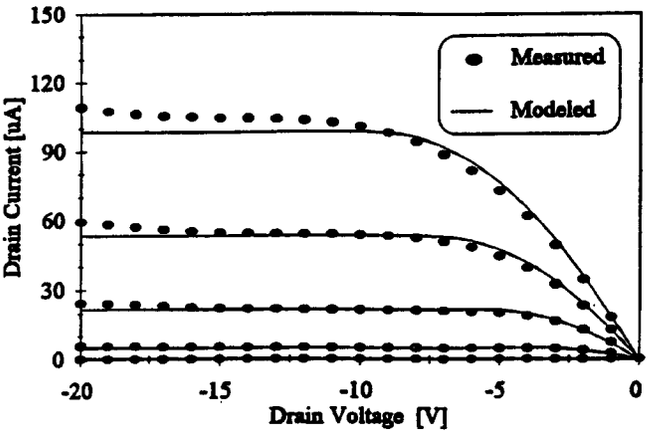

FIGURE 10 — *P*-channel 50 × 50-μm² poly-Si TFT above threshold characteristic for gate biases of –5, –8, –11, –14, and –17 V.

A more general model of thermionic field emission has recently been proposed in Refs. 23-26. The most comprehensive treatment is given by Bhattacharya *et al.*[26] where excellent quantitative agreement between theory and data is obtained while varying both gate bias and temperature. The leakage *vs.* drain bias characteristic was not examined, however.

Adan *et al.*[27] considered band-to-band tunneling and barrier lowering in addition to thermionic field emission in their treatment of the subject. Their results indicate that these other mechanisms should be included under certain circumstances (for example, with very high drain bias). Recently, the 2-D device simulations of Hack *et al.*[28] also suggest that barrier lowering at the source due to carrier generation at the drain may be important. Previously, the temperature dependence of the leakage was believed to rule out tunneling as a mechanism. However, their work shows that temperature-dependent barrier lowering near the source could account for the observed dependence, even if the leakage current originates as a tunneling current.

In all of the field-emission models mentioned, the exponential nature of the leakage with voltage is derived from the probability of tunneling through a triangular barrier.[29] This probability is an exponential function of both barrier height and electric field. Beyond this, there are essentially three complications. First, how should the electric field be calculated? The tunneling theory in Ref. 29 is one dimensional, but the fields produced by the gate and drain biases in a TFT are vertical and lateral, respectively. The models of Refs. 22, 26, and 27 all recognize the two-dimensional nature of the problem and make approximations to arrive at a net one-dimensional electric field.

The second complication is how the gate and drain biases effect the barrier height. Only Adan *et al.*[27] consider these effects, but they do show that barrier lowering may only be significant for large drain voltages.

The last complication involves calculating the volume near the drain in which these mechanisms occur. While most of the models assume that the leakage originates in the volume of the drain-depletion region, Bhattacharya *et al.*[26] point out that not even all of that volume is significant for thermionic field emission. This volume calculation is also a function of the two-dimensional electric field and structural parameters such as doping concentration.

We have modified the numerical model of Ref. 26 to more-accurately describe the drain bias dependence of the leakage current and expressed it in an analytical form more amenable for use in a circuit simulator. The details of the model will be published elsewhere. Here we state only the results with a brief description of each term.

The subthreshold leakage current is given by

$$I_{leak} = C\left[\exp\left(\frac{qBV_{DS}}{kT} - 1\right)\right](X_{TFE}(F) + X_{TE}) \qquad (15)$$
$$F = A(V_{DS} - V_{GS} + V_{FB}).$$

A, B, and C are constants; F is the maximum electric field near the drain; and the other symbols have their usual meanings. The constant B is related to the drain-induced barrier lowering and is expected to be a function of channel length for short-channel devices. C is proportional to the effective trap state density. X_{TFE} and X_{TE} describe the rates of thermionic field emission and thermionic-only emission of carriers from traps:

$$X_{TFE}(F) = \int_0^{W_C} \exp\left[-W - \frac{F_0}{F}(W_C - W)^{3/2}\right] dW$$

$$X_{TE} = \int_0^{W_C} \exp(-W)dW = \exp(W_C) \qquad (16)$$

$$F_o = (kT)^{3/2}\left(\frac{4}{3}\right)\frac{2\pi\sqrt{2m_e^*}}{qh}.$$

In Eq. (16), $W_C = (E_C - E_t)/(kT)$, E_t is the effective trap energy, and E_C is energy of the conduction band edge.

The total drain current is $I_d = I_d' + I_{leak}$, and is plotted in Figs. 7 and 9. The values used for the constants A, B, and C are listed in Table 2. An excellent fit is observed in all cases.

Still to be implemented are models for the "kink" effect at high drain bias, short-channel effects, and temperature effects.

3 a-Si:H TFT device model for circuit simulators

Hydrogenated amorphous-silicon (a-Si:H) is a direct-gap semiconductor with an energy gap close to 1.7 eV and electron and hole band mobilities on the order of 5–10 cm^2/V–s. The device characteristics of a-Si:H TFTs strongly depend on the density of the localized states. These states may vary depending on the deposition conditions, material quality, and the history of bias and/or thermal stress for a given sample. Two-dimensional numerical device modeling has allowed the investigation of the capture and emission of carriers from these traps and the resulting effects on device characteristics.[30-32] From this analysis, the trap state profile shown in Fig. 11 has been determined. As shown in the figure, the density of the localized states can be roughly modeled by exponential distributions of deep and tail states with possible peaks induced by the voltage and/or bias stress. The localized states in the upper half of the energy gap (closer to the bottom of the conduction band) behave as acceptor-like states, while the states in the bottom half of the energy gap behave as donor-like states. Donor-like states are positively charged when empty and neutral when filled; acceptor-like states are neutral when empty and negatively charged when filled.

The distribution of the localized states is not symmetrical, since there are more donor-like states than acceptor-like states. Hence, the position of the Fermi level in an undoped, uniform a-Si:H sample in the dark, E_{Fo}, found from the neutrality condition, is shifted closer to the bottom of the conduction band, E_c. For intrinsic a-Si, $E_2 \approx 90$ meV, $E_4 \approx 130$ meV (see Fig. 11), and $E_c - E_{Fo} \approx 620$ meV. A detailed account of material properties of a-Si:H was given in Ref. 1.

The position of the Fermi level with respect to the conduction band edge near the a-Si–insulator interface may be changed by inducing carriers via field effect, similar to the field effect at crystalline silicon–insulator interfaces. This effect is utilized in a-Si TFTs, although the field-effect mobility in a-Si:H TFTs is quite low (typically 0.5–1 cm^2/V-s). A value for the field-effect mobility close to the electron band mobility may be achieved when the electronic charge induced in the channel is sufficiently large to fill the localized states.[33,34] However, this will require large insulator electric-field–dielectric permittivity products, which are very difficult to achieve for the SiN insulator used in current TFT structures.

In the below-threshold regime, nearly all induced charge goes into the deep localized acceptor-like states in

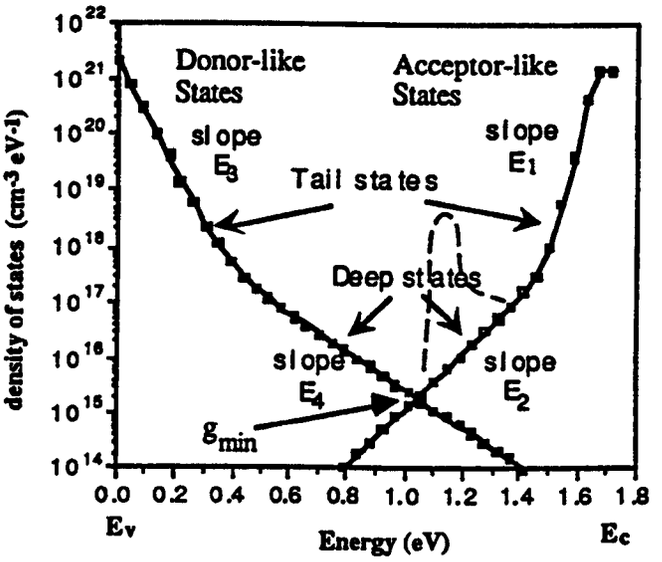

FIGURE 11 — Density of localized states in a-Si:H. E_1, E_2, E_3, and E_4 are characteristic energies for the exponential variation Ref. 15. The dashed line shows a possible peak in the density of states induced by thermal and/or voltage stress.

the energy gap of a-Si:H and into the surface states at the a-Si:H–insulator interface. With an increase in the gate-source voltage, more states are filled, and the Fermi level at the a-Si:H–insulator interface moves closer to the conduction band. This leads to an increase in the concentration of mobile carriers in the conduction band which rises superlinearly with gate bias. There is an important difference between this regime and the subthreshold regime in crystalline MOSFETs. In the subthreshold regime for MOSFETs, there is only a small number of free carriers, but all of these carriers are induced directly into the conduction band. In a-Si:H TFTs, the induced carriers in the subthreshold regime do not go into the conduction band but are instead trapped almost exclusively in the localized states.

With a further increase in the gate-source voltage, the Fermi level enters the tail states (see Fig. 11). The characteristic energy of the exponential variation of the density of tail states, E_1, is smaller or comparable to k_BT at room temperature. As a consequence, once the Fermi level is in the tail states, most of the charge is actually induced into the states above the Fermi level. Hence, the shift of the Fermi level with gate-source voltage is considerably smaller than in the below-threshold regime. This is the "above-threshold regime," where the threshold voltage is defined as the voltage at which the Fermi level reaches the tail states.[33] There is an important difference between this regime in a-Si:H TFTs and the above-threshold regime in crystalline MOSFETs. In a-Si:H TFTs, most of the induced charge still goes into the tail states with only a small fraction (less than 10% percent) going into the conduction band. At the same time, the Fermi level moves closer to the conduction band edge with increasing gate-source voltage, resulting in an increase in the field-effect mobility.

In addition to the familiar below- and above-threshold regimes, there are two new regimes of operation.[15] These occur at high densities of induced charge in the a-Si:H TFT channel: a "crystalline-like" regime when the free-electron concentration exceeds the localized charge concentration at the a-Si:H–insulator interface, and a "transitional" regime (between the crystalline-like and above-threshold regimes) at lower densities of induced charge when almost all localized states in the energy gap of the a-Si:H near the interface are filled.

As the induced charge is increased even further in the above-threshold regime, we may reach a situation when the tail states at the a-Si:H–insulator interface are almost completely filled and the Fermi level touches the bottom of the conduction band. Any additional increase in the induced charge is divided between the charge going into the conduction band and the charge induced into the tail states farther from the a-Si:H–insulator interface. At first, the fraction of the mobile charge is small, but it increases with increasing gate-source voltage. We call this the "transitional regime" because it corresponds to the transition between the above-threshold regime and the crystalline-like regime. In the latter, the Fermi level at the a-Si:H–insulator interface has moved high enough into the conduction band so that, finally, most of the induced charge goes into the conduction band. In this case, the field-effect mobility is close to the band mobility and the operation of the a-Si:H TFT is truly similar to the operation of a crystalline field-effect transistor (FETs). As mentioned above, the gate–source voltage necessary to achieve the crystalline-like regime is too large a voltage for typical devices. However, this regime may be achieved if we use a gate insulator with a higher dielectric constant.

As confirmed by 2-D numerical simulations,[30-32] the most important features of the a-Si:H TFT characteristics can be described by analyzing the device behavior in two regimes: below-threshold, when the electron quasi-Fermi level is in the deep states; and above-threshold, when the Fermi level enters the tail states. Here we briefly outline a universal device model for a-Si:H TFTs which allows us to describe both regimes of operation based on the a-Si:H TFT theory developed in Ref. 33. This model is an improved version of the model developed in Ref. 35, which uses a unified expression for the charge valid in both the above- and below-threshold regimes. However, the previous model did not accurately model the leakage regime and contained a description for the leakage current only to ensure convergence in the circuit simulator. The model outlined in this paper describes the subthreshold current, which is sensitive to the density of localized states. The model can, therefore, account for changes in the distribution of localized states which arise from thermal and/or bias stress and reproduce their effect in the subthreshold regime. In addition, this model accounts for the temperature dependence of currents both above and below threshold.

3.1 Subthreshold regime

In order to model the current–voltage characteristics of the a-Si:H TFTs, we first determine the position of the Fermi level as a function of gate bias and of the density of states in the below-threshold regime. This will allow us to calculate the subthreshold sheet carrier density. Then a modified charge-control model will be used to calculate the above-threshold carrier density. Finally, we will combine the expressions for the carrier densities in both regimes in one unified expression and calculate a temperature-dependent current valid in both the above- and below-threshold regimes, suitable for circuit simulation.

In the below-threshold regime the Fermi level is located in the deep localized states, far from the conduction band. Here, nearly all the sheet electron carriers, n_{sb}, induced by the gate bias are trapped in the deep acceptor-like localized states, as explained earlier. The position of the Fermi level is therefore dependent on the density of the deep states, which we have approximated by the exponential function,

$$g(E) = g_{min} \exp\left(\frac{E - E_{min}}{E_2}\right), \tag{17}$$

where E_{min} is the energy corresponding to the minimum DOS, g_{min}. E_2 is the characteristic energy variation of the density of deep localized states, which will be replaced by qV_2 in the following analysis. This expression can be modified to reflect changes in the density of states from thermal or bias stress.

We relate the position of the Fermi level to the density of states and then express the induced below-threshold electron concentration as a function of the density of states and the difference between the gate voltage and the flat band voltage, $V_{gFB} = V_g - V_{FB}$. (A small leakage current will exist even when V_g is equal to V_{FB} or less. This is modeled by introducing an effective gate voltage swing, V_{gFBe}, which is defined in Appendix A. For $V_g >> V_{FB}$, $V_{gFBe} = V_g - V_{FB}$; for $V_g << V_{FB}$, $V_{gFBe} = V_{min}$.) The induced sheet-electron concentration below threshold is given by

$$n_{sb} = n_{so}\left[\left(\frac{t_m}{d_i}\right)\left(\frac{V_{gFBe}}{V_2}\right)\left(\frac{\varepsilon_i}{\varepsilon_s}\right)\right]^{(2V_2/V_e)} \tag{18}$$

where t_m is the charge channel thickness, d_i is the dielectric thickness, ε_i and ε_s are the insulator and a-Si:H permittivities, respectively, $V_e = 2V_{th}V_2/(2V_2 - V_{th})$, and $V_{th} = k_BT/q$. The characteristic sheet carrier density, n_{so}, is given by

$$n_{so} = N_c t_m \left(\frac{V_e}{V_2}\right) \exp\left(\frac{-dE_{Fo}}{qV_{th}}\right). \tag{19}$$

Here, N_c is the effective density of states in the conduction band, $dE_{Fo} = E_C - E_{Fo}$, where E_{Fo} is the dark Fermi level.

$$t_m = \left(\frac{\varepsilon_s}{2qg_{min}}\right)^{1/2}. \quad (20)$$

The full derivation of these expressions is given in the Appendix A.

3.2 Above-threshold regime

We now consider the above-threshold regime following the approach developed in Refs. 33 and 35. Empirically, this approach shows that the ratio of charge induced into the conduction band to the total induced charge in the semiconductor can be expressed by a power law, so that the sheet carrier concentrations induced into the conduction band, n_{sa}, becomes

$$n_{sa} = C_g\left(\frac{V_g - V_t}{q}\right)\left(\frac{V_g - V_t - \alpha V_{dse}}{V_{AA}}\right)^{\gamma}, \quad (21)$$

where $C_g = \varepsilon_i/d_i$ is the capacitance of the gate insulator per unit area, and V_t is the threshold voltage. The αV_{dse} term reflects the reduced number of electrons in the conduction band due to the channel depletion by the drain potential,[37] and V_{AA} and γ are the characteristic voltage and power-law parameter, respectively, determined by the tail state distribution. The V_{dse} term is the effective drain-source voltage, which allows a smooth transition for V_{ds} from below to above saturation: $V_{dse} = V_{ds}$ for $V_{dse} << V_{sate}$, and $V_{dse} = V_{sate}$ for $V_{ds} >> V_{sate}$. $V_{sate} = \alpha_{sat} V_{gte}$, where α_{sat} is a fitting parameter. However, α_{sat} must be less than $\alpha_{sato} = (2^{1/m})/[\alpha/(1 + \gamma)]$, which is the value of α_{sat} at which $d(n_{sa}V_{ds})/dV_{ds} = 0$. $V_{gte} = V_g - V_t$ for $V_g >> V_t$ and $V_{gte} = V_{min}$ for $V_g << V_t$. (See Appendix B for the full expressions of V_{dse} and V_{gte}.)

In Eq. (21), it should be pointed out that n_{sa}, and therefore the channel conductance, is non-zero for $V_{gs} = V_t$. As defined here, the threshold voltage is the turn-on voltage at which the Fermi level reaches the tail states.

We now combine both regions of operation into one universal model as discussed in Ref. 35 for other types of FETs by interpolating the total carrier sheet depletion as

$$n_s = \frac{n_{sa}n_{sb}}{n_{sa} + n_{sb}}. \quad (22)$$

This expression for the free sheet carrier density, n_s, is valid in both regimes and reduces to the equations for the above- and below-threshold regimes at gate biases above and below the threshold voltage, respectively.

The electron field-effect mobility is defined as the band mobility, μ_n, times the ratio of free charge to the total induced charge in the channel, $Q_{ch} = C_g(V_{gFBe} - V_t)$. This yields $\mu_{fet} = \mu_n(qn_s/Q_{ch})$. The field-effect mobility is weakly temperature activated with activation energy E_μ and

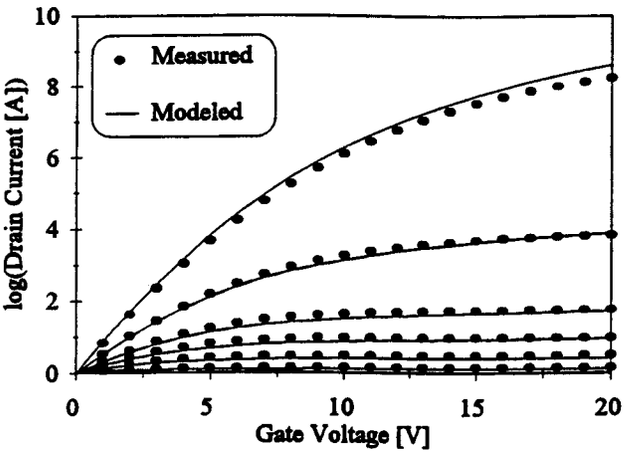

FIGURE 12 — Current–voltage characteristics of an *n*-channel a-Si:H TFT for V_g = 2, 4, 6, 8, 10, 14, and 20 V. (W = 150 μm, L = 60 μm, d_i = 300 nm.) Symbols are experimental data and solid lines are calculated curves. (Above-threshold parameters: V_t = 1.5 V, $V_{AA} = 7 \times 10^4$ V, g = 0.3, a = 0.6, α_{sat} = 0.8, λ = 0, m_{sat} = 1.7, $R_s = R_d$ = 7000 Ω).

$$\mu_{fet} = \mu_{fet,o} \exp\left(\frac{E_\mu}{q}\left[\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right]\right) \quad (23)$$

where $\mu_{fet,o}$ is the room-temperature field-effect mobility, V_{tho} is the thermal voltage at 300K, and E_μ has been shown to be about 60 meV.[37] This expression allows us to model the temperature dependence of the device characteristics. The intrinsic channel conductance is given by

$$g_{chi} = qn_s\mu_n \frac{W}{L_{gate}}, \quad (24)$$

where W is the device width, L_{gate} is the gate length, and n_s is the sheet electron concentration in the conduction band as given in Ref. 22.

Based on the theory considered above, we can now propose a semi-empirical extrinsic circuit model for a-Si:H TFTs similar to the universal MOSFET model developed in Ref. 35. The equations for this model are as follows:

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(R_s + R_d)} \quad (25)$$

$$I_{ds} = g_{ch}V_{dse}(1 + \lambda V_{ds}) \quad (26)$$

$$V_{sate} = \alpha_{sat}V_{gte}, \quad (27)$$

where g_{chi} is defined in Eq. (24), R_s and R_d are the source and drain resistances, and the parameter λ is related to the shortening of the effective channel length that becomes important at large drain voltages. (This effect is similar to gate-length modulation in crystalline FETs[15]). V_{dse} and V_{sate} were defined earlier as the effective drain-source voltage and the effective drain saturation voltage, respectively. The expressions for V_{dse} and V_{sate} are given in Appendix B.

Figure 12 shows typical measured and calculated current–voltage characteristics of an a-Si:H TFT in the above-

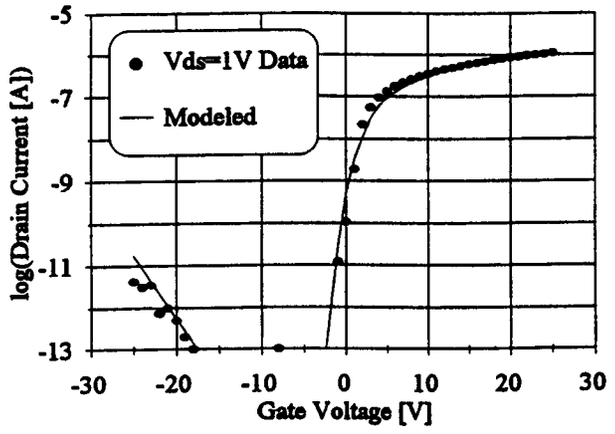

FIGURE 13 — Transfer characteristics of an *n*-channel a-Si:H TFT for V_{ds} = 1 V. (W = 150 μm, L = 60 μm, d_i = 300 nm.) Symbols are experimental data and solid lines are calculated curves. (Below Threshold Parameters: V_{FB} = –3 V, V_2 = 0.13 V, g_{min} = 9 × 10^{22} m^{-3}, I_{min} = 2.7 × 10^{-18} A, E_l = 0.75 eV, V_{dsl} = 5 V, V_{gsl} = 1.5 V.)

threshold regime. The model exhibits good agreement in both the linear and saturation regimes.

The transfer characteristics are shown for both the above- and below-threshold regimes in Fig. 13. The "hole-induced leakage current," I_{hl}, which occurs at large negative gate biases, must be included in order to correctly model the subthreshold current in this region. This is given by

$$I_{hl} = I_{min} \exp\left[E_l\left(\frac{1}{V_{tho}} - \frac{1}{V_{th}}\right)\right]\left[\exp\left(\frac{V_{dse}}{V_{dsl}}\right) - 1\right]\exp\left(\frac{-V_{gs}}{V_{gsl}}\right), \tag{28}$$

where I_{min} is the minimum leakage current, E_l describes the temperature activation, and V_{dsl} and V_{gsl} describe the dependence on V_{ds} and V_{gs}, respectively. Experimental results have shown that the temperature activation energy is between 0.5 and 1 eV.[2]

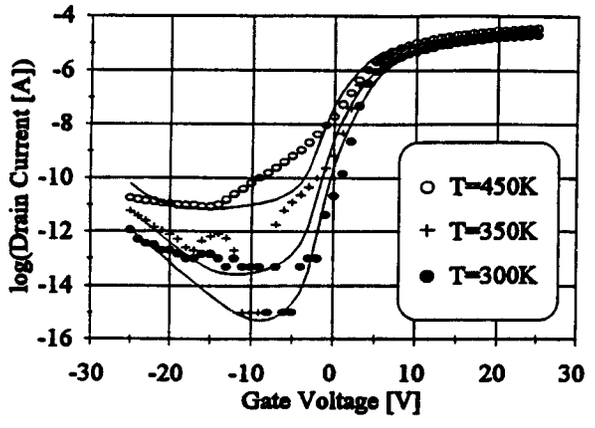

FIGURE 14 — Measured transfer characteristics of an *n*-channel a-Si:H TFT (W = 1 mm, L_{gate} = 15 μm, d_i = 300 nm) measured at 300K, 350K, and 450K (markers) and characteristics generated by the a-Si:H TFT model (lines). (Subthreshold parameters: V_{FB} = 0 V, V_t = 3 V, V_2 = 86 meV, V_{AA} = 3 × 10^3 V, g_{min} = 3 × 10^{22} $m^{-3}eV^{-1}$, I_{min} = 2.7 × 10^{-18} A, E_l = 0.3 eV, V_{dsl} = 3 V, V_{gsl} = 1.8 V.)

TABLE 3 — a-Si:H TFT intrinsic model parameters.

Material parameter	Value used in Figs. 12 and 13	*N*-channel V_{ds} = 1 V, W = 150 μm, L_{gate} = 60 μm, d_i = 300 nm
V_t	1.5 V	Threshold voltage
V_{FB}	–3V	Flat band voltage
V_2	0.13 V	Exponential variation of DOS
g_{min}	9 × 10^{22} m^{-3}	Minimum DOS
I_{min}	2.7 × 10^{-18} A	Minimum leakage current
E_l	0.75 eV	Activation energy of I_{hl}
V_{dsl}	5 V	Exponential variation of I_{hl} on V_{ds}
V_{gsl}	1.5 V	Exponential variation of I_{hl} on V_g
V_{AA}	7 × 10^4 V	Characteristic voltage of tail states
γ	0.3	Tail-states power-law dependence
α	0.6	Channel depletion factor
E_μ	60 meV	Band mobility activation energy
α_{sat}	0.8	Saturation proportionality constant
λ	0	Output conductance parameter
m_{sat}	1.7	I_{ds} saturation parameter (knee)

The effect of the temperature can be clearly seen in the subthreshold regime. Figure 14 shows the TFT characteristics measured at a drain bias of 1 V for T = 300K, 350K, and 450K and the simulated transfer characteristics. The model exhibits fairly good agreement with the actual data over a large temperature range. The effect of the thermal stress on the density of states causes a reduction in the subthreshold slope at higher temperatures. This effect is not yet included in our model.

Table 3 lists the parameters which must be extracted for this model and the values used in Figs. 12 and 13. This model can be further developed by including parameter extraction, short-channel effects, accounting for nonlinear series resistances,[38] and stress effects.

4 Conclusions

Accurate TFT analytic models for circuit simulation must describe the following: (i) I–V characteristics in all regions of operation (to account for the large required on-to-off ratio); (ii) device capacitance; and (iii) the proper scaling of characteristics with length and temperature. The models should also allow for routine automatic parameter extraction and should guarantee convergence when simulating large TFT circuits.

Analytic models for both poly-Si and a-Si TFTs have been presented which satisfy many of the above criteria. The poly-Si TFT model describes the subthreshold and above-threshold currents and subthreshold leakage currents which are then combined into the total drain current. The subthreshold current expression is similar to that used to describe the diffusion currents in c-Si devices. The above-threshold expression accounts for the effect of boundary traps through the field-effect mobility and necessitates the proper extraction of V_t from C_{gc} data. The leakage current model requires only three parameters and is based on the mechanisms of thermionic field emission and drain-induced barrier lowering.

An a-S:H TFT current model for the below-threshold regime is derived by considering the sheet carrier density as a function of Fermi level position. This analysis takes into account the density of localized states, which has been determined by 2-D numerical device simulation and other experimental techniques. The sheet carrier density for the above-threshold regime is given by an empirical expression which relates the ratio of induced charge in the conducton band to the total induced charge. The two carrier densities are then combined to describe the total drain current. The temperature dependence is included for both regimes, but the effect of the thermal stress on the density of states must be taken into account to improve the model.

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Appendix A: Derivation for a-Si:H TFT below-threshold sheet carrier density

The effective gate voltage swing, V_{gFBe}, is given by

$$V_{gFBe} = \frac{V_{min}}{2}\left\{1+\left(\frac{V_{gFB}}{V_{min}}\right)+\left[\delta^2+\left(\left(\frac{V_{gFB}}{V_{min}}\right)-1\right)^2\right]^{1/2}\right\} \quad \text{(A1)}$$

where V_{min} determines the minimum TFT current and δ describes the transition of the gate voltage from below to above the flat-band voltage.[39]

Using the expression for the density of states given in Eq. (17), the solution of Poisson's equation yields the following expression for the interface electric field, $F(V)$:

$$F(V) = \left(\frac{2}{\varepsilon_s}\int_0^{V}\int_0^{V'} g(V'')dV''dV'\right)^{1/2}$$

$$F_s = F(V_s) = \left\{\frac{2qg_{min}V_2^2}{\varepsilon_s}\left[\exp\left(\frac{V_s}{V_2}\right)-\frac{V_s}{V_2}-1\right]\right\}^{1/2} \quad \text{(A2)}$$

$$\approx \left(\frac{2qg_{min}V_2^2}{\varepsilon_s}\right)^{1/2}\exp\left(\frac{V_s}{2V_2}\right)$$

for $V_s > V_2$. This simplified expression is sufficient to describe the TFT characteristics. We can express the gate voltage in terms of the surface potential in the semiconductor ($V_{gFBe} = \varepsilon_s F_s d_i/\varepsilon_i + V_s$), which, assuming $V_s < V_{gFBe}$, yields,

$$V_{gFBe} = \left(2qg_{min}V_2^2\varepsilon_s\right)^{1/2}\left(\frac{d_i}{\varepsilon_i}\right)\exp\left(\frac{V_s}{2V_2}\right). \quad \text{(A3)}$$

Hence, we may assume that

$$V_s \approx V_2 \ln\left(\frac{\varepsilon_i^2 V_{gFBe}^2}{2q\varepsilon_s d_i^2 g_{min} V_2^2}\right). \quad \text{(A4)}$$

Using this expression, we can find the free electron density, N_s, at the interface as

$$N_s = N_c \exp\left(\frac{V_s}{V_{th}}\right)\exp\left(\frac{-dE_{fo}}{qV_{th}}\right). \quad \text{(A5)}$$

Integrating this expression over the thickness of the a-Si:H film and performing a change in variable, we can express the sheet electron charge below threshold as

$$n_{sb} = N_c\int_0^{V_s}\frac{1}{|F(V)|}\exp\left(\frac{V}{V_{th}}\right)\exp\left(\frac{-dE_{Fo}}{qV_{th}}\right)dV \quad \text{(A6)}$$

where F_s, the surface electric field, was given in Eq. (A2). Performing the integration yields Eqs. (18) and (19).

Appendix B: a-Si:H TFT above threshold characteristics

The expression for V_{gte} is given by

$$V_{gte} = \frac{V_{min}}{2}\left\{1+\left(\frac{V_{gt}}{V_{min}}\right)+\left[\delta^2+\left(\left(\frac{V_{gt}}{V_{min}}\right)-1\right)^2\right]^{1/2}\right\} \quad \text{(B1)}$$

where $V_{gt} = V_g - V_t$. V_{gte} reduces to a minimum value, V_{min}, at V_g below V_t, preventing $V_{sate} = \alpha_{sat}V_{gte}$ from becoming a negative value for $V_g < V_t$. As in Eq. (A1), the parameter δ describes the transition of the gate voltage from above threshold to below threshold.

In order that the current [Eq. (26)] be continuous from the linear regime into saturation, we must define an effective drain-source voltage, V_{dse}. V_{dse} is equal to V_{ds} in the linear regime ($V_{ds} < V_{sate}$). In the saturation regime, V_{dse} is equal to V_{sate} ($V_{ds} > V_{sate}$). The parameter m_{sat} provides a smooth transition between the two regions of drain voltage ($V_{ds} < V_{sate}$ and $V_{ds} > V_{sate}$). The expression for V_{dse} is given as

$$V_{dse} = \frac{V_{ds}}{\left[1+\left(\frac{V_{ds}}{V_{sate}}\right)^{m_{sat}}\right]^{1/m_{sat}}}. \qquad \text{(B2)}$$

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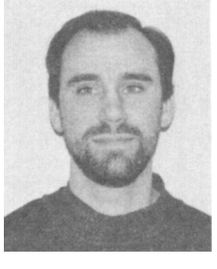

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