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On the Electrical Activity of Misfit and Threading Dislocations in p-n Junctions Fabricated in Thin Strain-Relaxed Buffer Layers

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Abstract. The electrical activity of threading dislocations (TDs), occurring in a thin SiGe Strain Relaxed Buffer (SRB) layer has been investigated by a number of techniques and its impact on the reverse current of p-n junction diodes has been evaluated. It is shown that besides the density of TD, there are at least two other parameters playing an important role. The distance with respect to the metallurgical junction of the 5 nm C-rich layer, used for the strain relaxation and the dopant type in the well region also affect the leakage current. This complex behaviour is further reflected in the Emission Microscopy (EMMI) images, showing different breakdown sites for p+/n or n+/p junctions. Results will be presented whereby one of these parameters is varied, while the others are kept constant, in order to arrive at some idea of the relative importance of the different factors.

Introduction

Traditional dimensional scaling no longer suffices to boost the sub-45 nm transistor performance. An attractive route to achieve higher current drives for next CMOS generations is the use of so-called high-mobility substrates (strained silicon, SiGe or Ge) [1]. In the case of strained silicon (SSi), a strain-relaxed $Si_{1-x}Ge_x$ buffer (SRB) is employed, on top of which a thin (~10 nm), biaxially tensile-strained silicon epitaxial layer is deposited. The tensile strain lifts the degeneracy of the conduction band, thereby enhancing the band gap and the low-field electron mobility. Traditionally, strain relaxation in the buffer layer is achieved by a gradual increase in the Ge percentage between 0 at the silicon substrate and the desired value at the top layer, typically in the range of 20% [1]. This results in a rather thick epitaxial stack (~1 μm), which for several reasons is not optimal. Therefore, alternatives have been sought for, resulting in a thinner buffer layer [2-6]. Here, SSi wafers on thin (250-350 nm) SRBs will be studied whereby strain-relaxation was facilitated by the implementation of a 5 nm carbon-rich layer [7]. The layer structure is schematically represented in Fig. 1.

However, the relaxation in the thin SRB results in the creation of threading (TDs) and misfit dislocations, as represented by the optical micrograph of Fig. 2. An important question is whether devices fabricated in such SSi substrates will not suffer from the electrical activity of these extended defects. A related issue is what the presence of the C-rich layer in the depletion region of a p-n junction does on the leakage current and carrier lifetime [8]. Here, an answer will be looked for by means of p-n junctions fabricated in SSi substrates. Besides the current-voltage (I-V) characteristics, other analytical techniques will be employed that can shine light on this topic.

Experimental

The p+/n and n+/p junctions studied have been processed on what is termed here 'thin' (~250 nm) and 'thick' (~350 nm) $Si_{1-x}Ge_x$ SRBs, as described in more detail elsewhere [8-10]. The Ge percentage in the top layer was 20%. Square diodes with an area of 10^5 µm^2 have been characterized in detail, using different techniques. A TD density of ~10^7 cm^{-2} was derived from counting under a microscope, following defect etching of as-deposited device-quality SSi wafers. Processing was also performed on SSi wafers with TD densities up to ~10^9 cm^{-2} and on commercial graded buffer layers, with a low (~10^5 cm^{-2}) TD density [11]. Reference devices were made in standard CZ silicon wafers.

Current- (I-V) and capacitance-voltage (C-V) measurements were combined to derive a value for the effective generation lifetime (τ_{geff}). Measurements of the leakage current as a function of temperature have also been performed to derive its activation energy. Emission Microscopy (EMMI) analysis was carried out for the detection of the junction breakdown sites, associated with local high electric field regions. Microwave absorption (MWA) measurements have been performed for the extraction of the recombination lifetime (τ_r), as described in detail elsewhere [12,13].

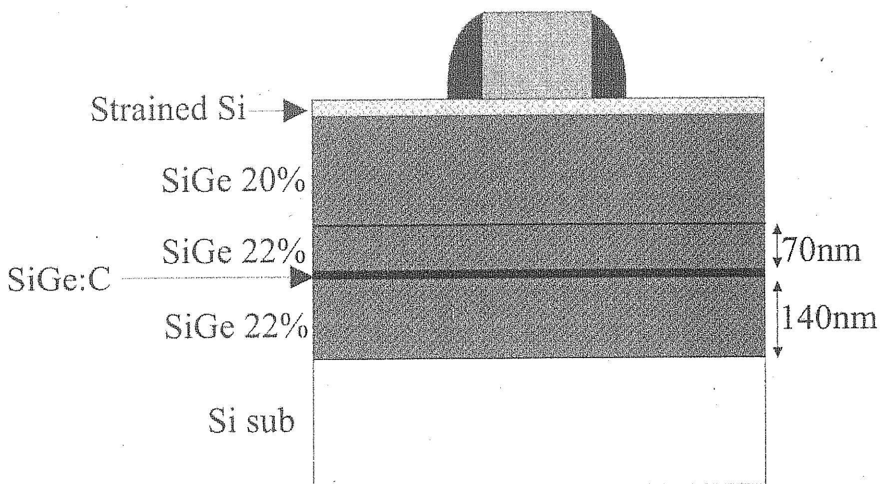


Fig. 1. Schematic view of the strained Si and SiGe virtual substrates.

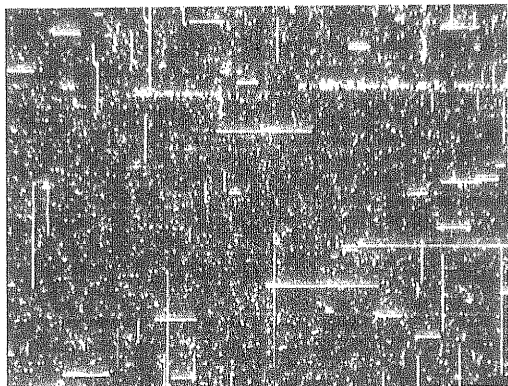


Fig. 2. Optical micrograph of a defect-etched SRB wafer, showing threading -, misfit dislocations and dislocation pile-ups.

Results and Discussion

As shown in Fig. 3, the leakage current density in SSi wafers is 4 to 5 decades higher than in CZ silicon references. This clearly points to the impact of the TDs on the generation lifetime. However, at the same time, the relative position of the C-rich layer with-respect to the metallurgical junction also plays a role, since the leakage current and the corresponding activation energy [9-11] is different for the thin and thick SRBs in Fig. 3. From a comparison of the n+/p and p+/n results in Fig. 3 further follows that the doping type has an impact on the electrical activity of the extended defects in the SRB layers. This is most likely related to the residual ion-implantation damage of the well profiles, after the applied thermal budget (spike anneal).

In order to have a better idea of the different contributions, diodes have been processed on wafers with various TD densities and with a different position of the C-rich layer [11]. As shown in Fig. 4a, the reverse current density (J_R) of the n+/p diodes increases by two decades for the same TD density (~10^7 cm^{-2}) when the C-layer is moved from 270 to 100 nm from the junction. This implies that for the 100 nm layer a high density of electrically active, C-related defects is present in the depletion region, which is responsible for a strong increase of the reverse current. On the other hand, placing the C-rich layer outside the depletion region eliminates this leakage current source and enables the study of the effect of other types of generation centers, like the TDs.

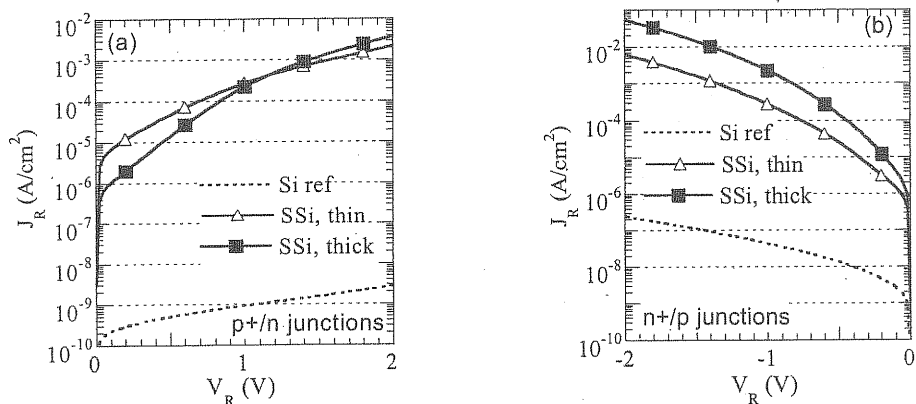


Fig. 3. Current density versus reverse bias for p+/n (a) and n+/p junctions (b), fabricated in different substrates: standard silicon wafers (ref); a thick and thin strained-silicon (SSi) substrate. All diodes received a 1000°C spike anneal.

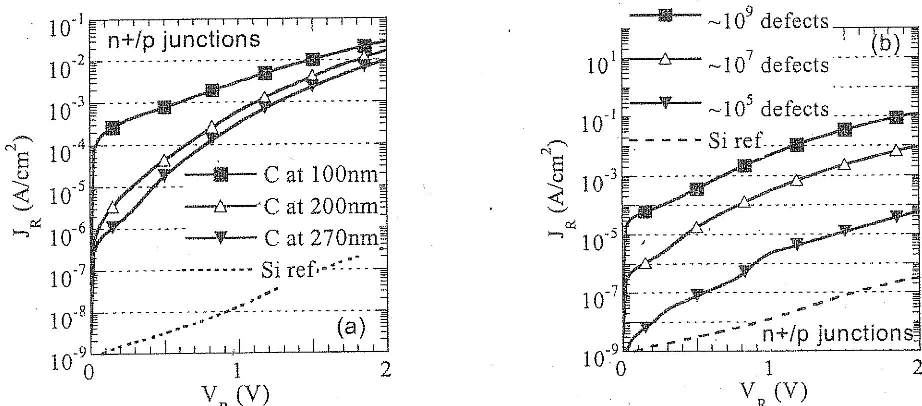


Fig. 4. Current density versus reverse bias for n+/p junctions, corresponding with a different position of the C-rich layer and a fixed TD density of ~10^7 cm^{-2} (a) and for various TD densities, with a C layer at 270 nm (b). A 1000 s spike anneal was employed here.

This is done in Fig. 4b, for a C-layer at 270 nm from the junctions, far enough to have no impact and showing that the reverse current density exhibits a strong correlation with the TD density. It should be remarked that the SSi wafers corresponding to a TD density of ~10^5 cm^{-2} are commercial graded-SRB wafers, without a C-rich layer. In the case of the n+/p junctions, a close to linear increase has been found [11], in agreement with earlier literature data [14]. The dependence for the p+/n junctions is sub-linear [11], again emphasizing the impact of the doping type on the leakage current density.

In order to further study the role of the well doping type on the reverse current in SRB layers, activation anneals have been performed at different spike temperatures [10]. The resulting effective generation lifetimes at 0 V bias are summarized in Fig. 5. Both the Si references and the thick SRB junctions show an increased τ_{geff} (reduced J_R) for increasing spike anneal temperature. This points to a more efficient removal of well implantation damage at higher thermal budgets. The dashed line represents an estimate of the generation lifetime based on the data of Giovane *et al.* [14] and corresponding to a TD density of 10^7 cm^{-2}. This again demonstrates that for the thick SRB wafers, the dominant generation centers are related to the TDs, while for the thin SRB junctions, the presence of the C-layer in the 0 V depletion width yields a reduction of τ_{geff} by one decade.

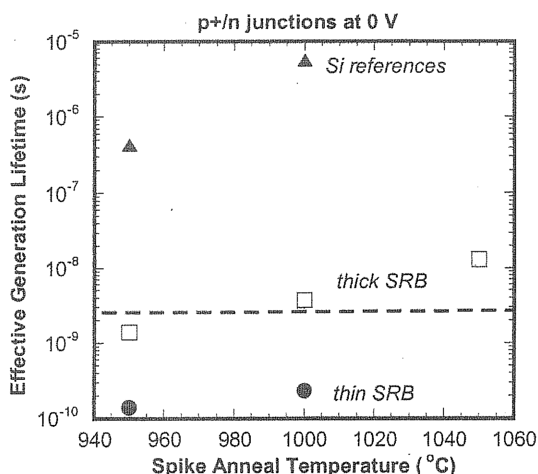
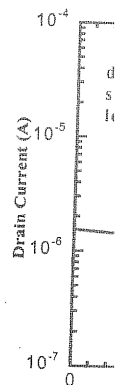
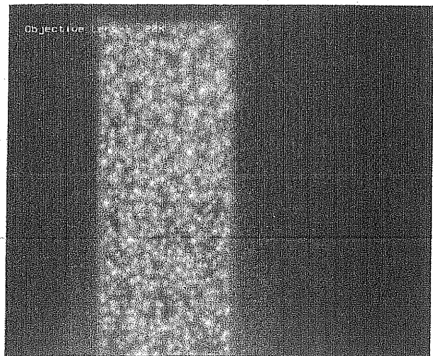


Fig. 5. Effective generation lifetime at 0 V versus spike annealing temperature for p+/n junctions made in different substrates.

The complexity of the leakage current problem is further illustrated in Fig. 6, representing EMMI images of the breakdown sites at high reverse bias in a p+/n and n+/p junction, respectively. In the first case, local breakdown occurs at the TDs in the depletion region, giving rise to light emission in the high electric field surrounding a dislocation line. For the n+/p junction in a thin SRB substrate, micro-plasmas are generated preferably at the misfits residing at the bottom Si-SiGe interface as evidenced by Fig. 6b.

The recombination lifetime measurements show a different picture than the leakage current (generation lifetime), whereby τ_r is generally larger than τ_{geff} [8]. In addition, the experimental dependence of τ_r on the TD density is weaker than expected from a first-order theory. As outlined elsewhere [12,13], this is related to the high injection level used in the MWA measurements. Moreover, recent EBIC measurements of SSi wafers have revealed that the recombination activity of the TDs becomes visible only at lower temperatures (77 K), while it is rather weak at room temperature [15].





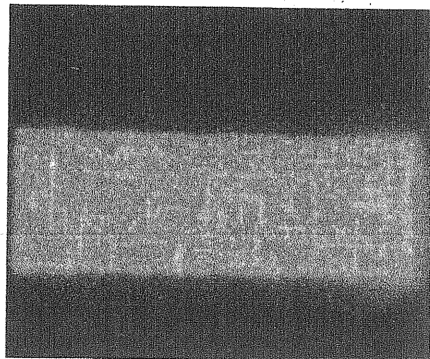


Fig. 6. (a) Emission Micrograph at +15 V of a p+/n junction made in a thick SRB substrate, showing breakdown sites at TDs and pile-ups. (b) Emission Micrograph at –15 V of a n+/p junction made in a thin SRB substrate, showing breakdown sites at misfit dislocations.

Finally, Fig. 7 illustrates the impact of a dislocation on the subthreshold or off-state leakage current of an n-MOSFET, processed in a thin SRB SSi wafer, using a 65 nm CMOS technology. The mechanism proposed for such a leakage is as follows [16,17]: during device processing of a SSi wafer, the buffer layer can further relax, giving rise to the creation of misfit dislocations at the $Si_{1-x}Ge_x$-strained silicon interface [18]. These dislocations, when running from the source to the drain of a transistor can give rise to a locally enhanced dopant or pipe diffusion, creating a leakage path (short). The off-state leakage is thus not a direct consequence of the electrical activity of the dislocation but follows from the interaction with dopant atoms.

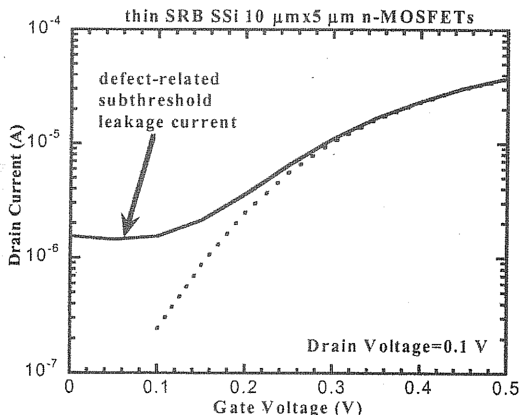


Fig. 7. Input characteristics of two 10 μmx5 μm n-MOSFETs on a SSi substrate, comparing a leaky with a normal device. A drain voltage of 0.1 V was applied. Implantations of the SSi transistor have been adjusted to match the threshold voltage of the Si reference device.

Summary

It has been shown that different leakage current mechanisms are active in SSi wafers. While a high density of TDs certainly enhances J_R, a significant contribution can come from the presence of the C-rich layer, used in this work to relax the thin buffer layers. In addition, it has been shown that the electrical activity of the TDs depends on the doping type of the substrate. The latter effect is most likely due to the interaction between the well implantation damage and the dislocations. Moreover, due to the specific nature of a TD, different recombination and generation behaviour can be expected in n- or p-type silicon.

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