GaAs/Ge/Si SOLAR CELLS

B-Y. Tsaur, John C. C. Fan, G. W. Turner, B. D. King,
R. W. McClelland, and G. M. Metze

Lincoln Laboratory, Massachusetts Institute of Technology
Lexington, Massachusetts 02173-0073

ABSTRACT

Shallow-homojunction GaAs solar cells fabricated on Ge-coated Si substrates have achieved conversion efficiencies of 14 and 11% (AM1, one sun) for areas of ~0.093 and 0.51 cm^2, respectively. The electrical characteristics of the cells have been studied by quantum efficiency, junction diode factor and dark current measurements, and their structural properties by transmission electron microscopy and electron-beam-induced-current imaging. The effects of dislocations, which are the predominant defects in the GaAs layers, on solar cell performance are discussed. Recent advances in monolithic GaAs-Si tandem cells are also reported.

INTRODUCTION

We have previously reported (1) the fabrication of small-area (0.6 mm diameter) shallow-homojunction $n^+/p/p^+$ GaAs solar cells with conversion efficiency of 14% (AM1, one sun) that were prepared on Ge-coated p^+ Si substrates. In this paper we report the successful fabrication of much larger cells of this type, a development made possible by improvements in both material preparation and cell fabrication procedures. The electrical and structural properties of the GaAs/Ge/Si cells have been studied in detail, and the effects of material defects on the solar cell characteristics are discussed. We have also previously reported (1) the fabrication of monolithic tandem cells composed of a shallow-homojunction GaAs top cell and a Si bottom cell that are connected by a thin Ge layer. We have now fabricated such cells in which a substantial increase in photocurrent has been achieved by etching stripe openings in the GaAs cell to expose corresponding regions of the Si cell directly to solar radiation. The results indicate that GaAs/Ge/Si structures could be used for the fabrication of single-junction cells on inexpensive Si sheets and also to provide substrates for the growth of AlGaAs or GaAsP for monolithic AlGaAs/Si or GaAsP/Si tandem cells.

CELL FABRICATION

To form the GaAs/Ge/Si structures, the Si substrate is first coated with a Ge layer deposited by e-beam evaporation (2), and GaAs layers are then grown by chemical vapor deposition (CVD) in an $AsCl_3$-GaAs-H_2 system. The sample preparation and growth procedures are similar to those reported previously (1). Mirror-smooth, crack-free GaAs layers can be produced routinely. However, it is difficult to fabricate large-area GaAs/Ge/Si cells, mainly because cracks tend to develop in the GaAs layer during device processing as a result of the large tensile stress generated by the differential thermal contraction of GaAs and Si. By optimizing processing procedures, we have succeeded in obtaining GaAs/Ge/Si wafers a few square centimeters in area without crack formation.

The techniques used for solar cell fabrication were similar to those described in Ref. 3 for GaAs cells on single-crystal GaAs substrates, which we shall refer to as conventional cells. The back contact and the front contact bar and fingers (defined by photolithography and lift-off) were vacuum-evaporated Au. The n^+ layer was thinned to ~600 Å by anodization and stripping, using Si_3N_4 as a protection mask for the Au metallization. Anodic oxide was used as an AR coating. The cell areas, which were defined by mesa etching, were ~0.093 or 0.51 cm^2.

CELL CHARACTERISTICS

Figure 1 shows typical illuminated I-V curves for 0.093 and 0.51 cm^2 cells under simulated AM1, one-sun conditions. Both cells have an open-circuit voltage V_{oc} of ~0.8 V and short-circuit current density J_{sc} of ~23 mA/cm^2. The smaller cells have a better fill factor ff of ~0.75, giving an efficiency of ~14%. The efficiency of the larger cells is ~11%. Compared to the values for our conventional GaAs cells, J_{sc} of the GaAs/Ge/Si cells is ~10% smaller, and V_{oc} is ~20% smaller.

The external quantum efficiency of the cell of Fig. 1(a) is plotted as a function of wavelength in Fig. 2. In comparison with values for conventional cells, the efficiency values in

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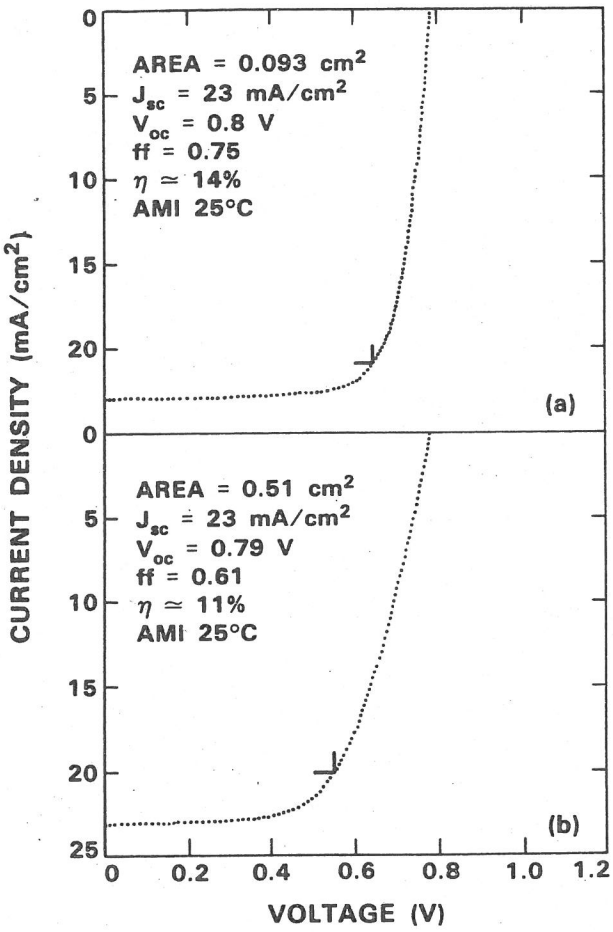

Fig. 1. I-V characteristics (AM1, one sun) of two GaAs cells on Ge-coated Si substrates.

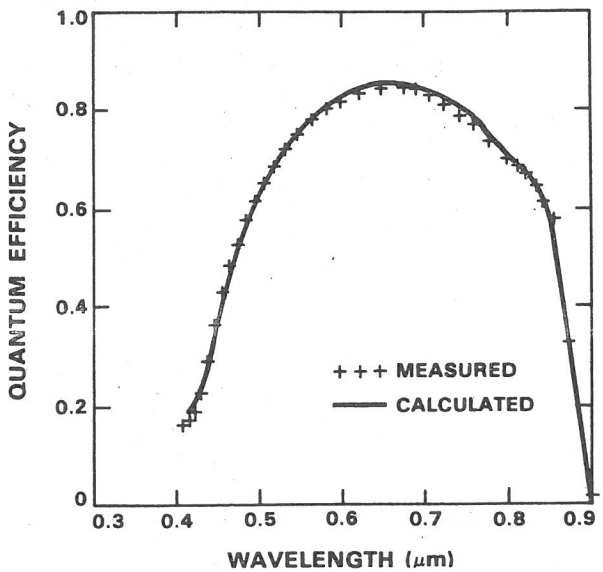

Fig. 2. External quantum efficiency as a function of wavelength for the cell of Fig. 1(a). The solid curve is calculated for a minority carrier diffusion length of 2 μm.

Fig. 2 are nearly the same at wavelengths up to 0.65 μm but 10-20% lower at the longer wavelengths. The relative decrease at the longer wavelengths indicates a lower minority carrier diffusion length in the base (p) region. Computer fitting of the quantum efficiency data (solid curve in Fig. 2) yields a diffusion length of 2 μm, compared with 10-20 μm for conventional cells. Since the GaAs layers on Ge-coated Si contain ~10^7 cm^{-2} dislocations (1), the reduction in the diffusion length is attributed to recombination at dislocations.

To investigate the diode properties of the solar cell n-p junction, the dependence of J_{sc} on V_{oc} was determined by measuring these quantities at illumination levels up to 15 suns. The result for the cell of Fig. 1(a) is shown in Fig. 3. From the relationship $V_{oc} = A(kT/q)\,\ln[(J_{sc}/J_o) + 1]$, the diode factor A is

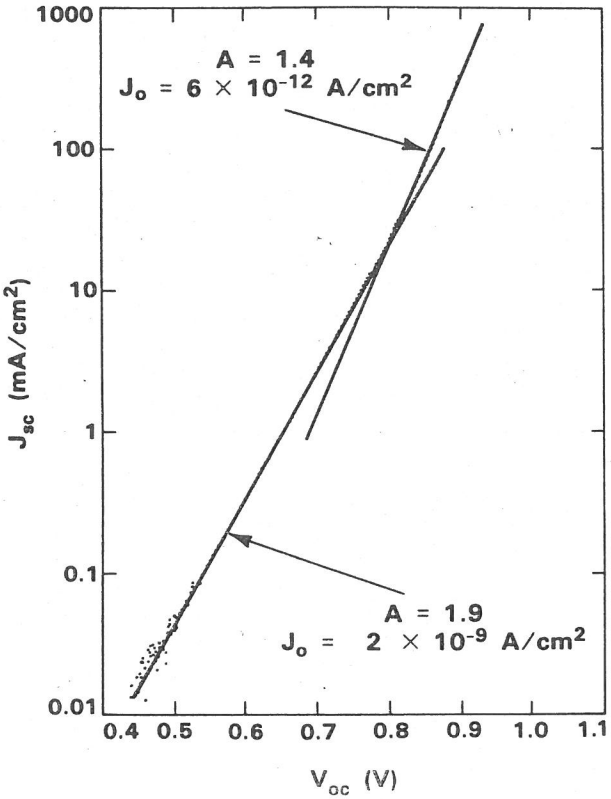

Fig. 3. Short-circuit current density J_{sc} as a function of open-circuit voltage V_{oc} at different illumination levels for the of Fig. 1(a).

1.9 and the saturation (dark) current density J_o is 2 x 10^{-9} A/cm² for V_{oc} less than 0.8 V (illumination level less than one sun). The corresponding values for V_{oc} larger than 0.8 V (multiple-sun illumination) are 1.4 and 6 x 10^{-12} A/cm².

The diode factor of almost 2 for low V_{oc} indicates that the dark current is predominantly space-charge recombination current (4) due to the presence of dislocations near the junction region, rather than injection current, as in an ideal junction. From the relationship $J_o \simeq qn_iW/2\tau$, where n_i is the intrinsic carrier concentration (1.8×10^6 cm^{-3}) and W is the space-charge layer width ($\sim 2.5 \times 10^{-5}$ cm), the minority carrier lifetime τ is estimated to be ~1.8 ns for J_o = 2×10^{-9} A/cm^2. The diffusion length L ($= \sqrt{D\tau}$, where D is the diffusivity) is then ~3 μm, in reasonable agreement with the value obtained from the quantum efficiency data. The large diode factor also results in a degradation of the fill factor. The fill factor calculated (4) for a cell with V_{oc} = 0.8 V and A = 2 is equal to 0.75, in agreement with our measured value for one-sun illumination. For high V_{oc} (multiple-sun illumination), the diode factor and saturation current density improve, indicating that both injection current and recombination current contribute to the diode foward current.

DISLOCATION STUDIES

Although the dislocation density in GaAs layers grown on Ge/Si substrates is ~10^7 cm^{-2}, 3-4 orders of magnitude higher than in layers grown on GaAs substrates, the minority carrier diffusion length is only about 5-10 times smaller for the former layers than for the latter. Because the thickness of the base region in our shallow-homojunction cells (~2.5 μm) is comparable to the minority-carrier diffusion length (~2 μm), most of the photocarriers generated in the base region of the GaAs/Ge/Si cells are still collected by the p-n junction, resulting in only a small reduction of J_{sc}. However, the dislocations significantly degrade the junction quality and reduce V_{oc}.

The dislocation morphology has been studied by transmission electron microscopy (TEM). Figure 4 is a cross-sectional TEM micrograph of a (110) plane of an as-grown GaAs/Ge/Si structure. There is a high density of dislocation located near the GaAs-Ge interface, and they interact and tangle with each other to form a network. Some of the dislocations propagate upwards and these tend to bend over near the surface. As a result, a large number of dislocation segments parallel to the junction plane are formed near the junction, which is only about ~1500 Å below the surface. The dislocations can also be revealed by the electron-beam induced current (EBIC) technique (5). Figure 5 is the EBIC micrograph of a region of a 0.51-cm^2 cell showing short dark lines oriented parallel to the [110] or [$\bar{1}$10] crystallographic directions. These dark lines have the same density (~10^7 cm^2) as the dislocations found by TEM and are believed to correspond to dislocation segments.

The formation of dislocation segments near the n-p junction is shown schematically in Fig. 6. Threading dislocations originating from the Ge layer propagate up during growth of the GaAs layer [Fig. 6(a)]. Near the junction region, the

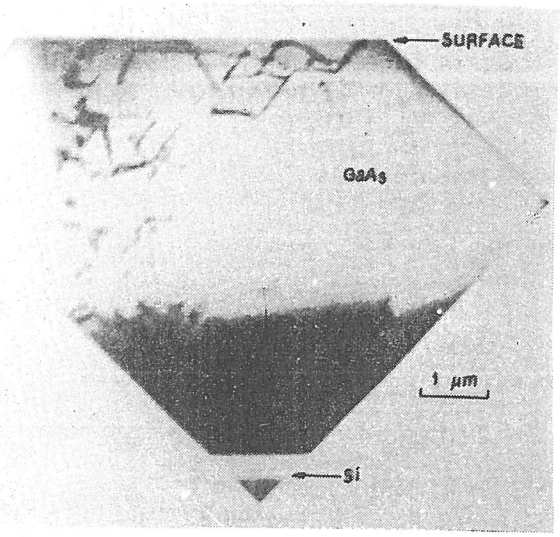

Fig. 4. Cross-sectional TEM micrograph showing propagation and bending over of dislocations in a GaAs layer grown on a Ge/Si substrate.

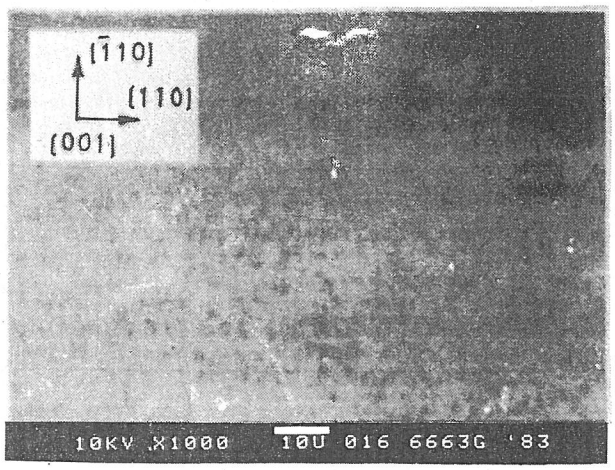

Fig. 5. EBIC micrograph of a region of a 0.51 cm^2 cell showing recombination at dislocations (short dark lines).

dislocations have a tendency to bend over because the heavy n^+ doping produces a local lattice strain that can cause dislocation glide [Fig. 6(b)]. As in layers grown on GaAs substrates (6), glide tends to occur along <110> crystallographic directions. After the growth of GaAs is complete as the sample is cooled down to room temperature further dislocation glide occurs along the <110> directions because the GaAs layer is heavily stressed by differential thermal contraction [Fig. 6(c)]. The poor junction properties observed for the GaAs/Ge/Si cells are believed to be due to those dislocation segments located near the junction that run parallel to the junction. Improvement in junction quality should be achieved by reducing the overall dislocation density in the GaAs and by preventing dislocations from bending parallel to the junction. Possible

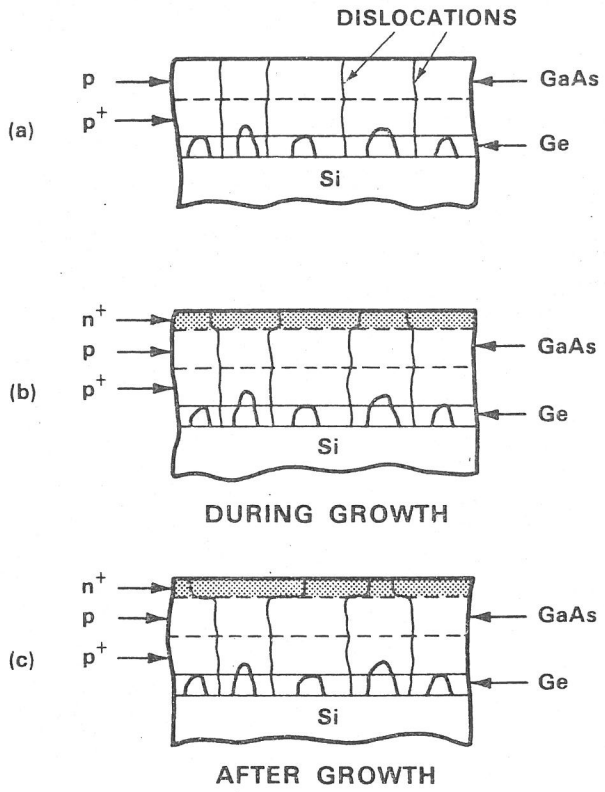

Fig. 6. Schematic diagram showing dislocation bending near the junction.

techniques for accomplishing both of these improvements are currently under investigation.

GaAs-Si MONOLITHIC TANDEM CELLS

We have also fabricated tandem cells composed of a GaAs top cell and a Si bottom cell. These devices use a monolithic structure formed by growing a GaAs shallow homojunction on a Ge layer 0.1 μm thick that is deposited on a lightly doped (0.1-1 Ω cm) p Si substrate. As a result of As diffusion through the Ge layer during GaAs growth, an n-p junction is formed in the Si substrate close to the Ge-Si interface. Several 0.093 cm^2 cells have been fabricated with V_{oc} of 1.1-1.2 V and J_{sc} of ~7 mA/cm^2. Figure 7(a) shows the I-V characteristics of a typical cell. The current density is relatively low because it is limited by the photocurrent generated in the Si cell.

To increase the photocurrent, in some tandem devices stripe openings were etched in the GaAs cell to expose the corresponding regions of the Si cell to direct solar radiation as shown schematically in Fig. 8. When ~25% of the GaAs area was removed, J_{sc} rose to ~12 mA/cm^2 [Fig. 7(b)], an increase of ~70%. The V_{oc} remained nearly the same, but the fill factor decreased somewhat because the sheet resistance of the As-diffused n^+ layer in Si is quite high due to the extremely shallow junction. For this

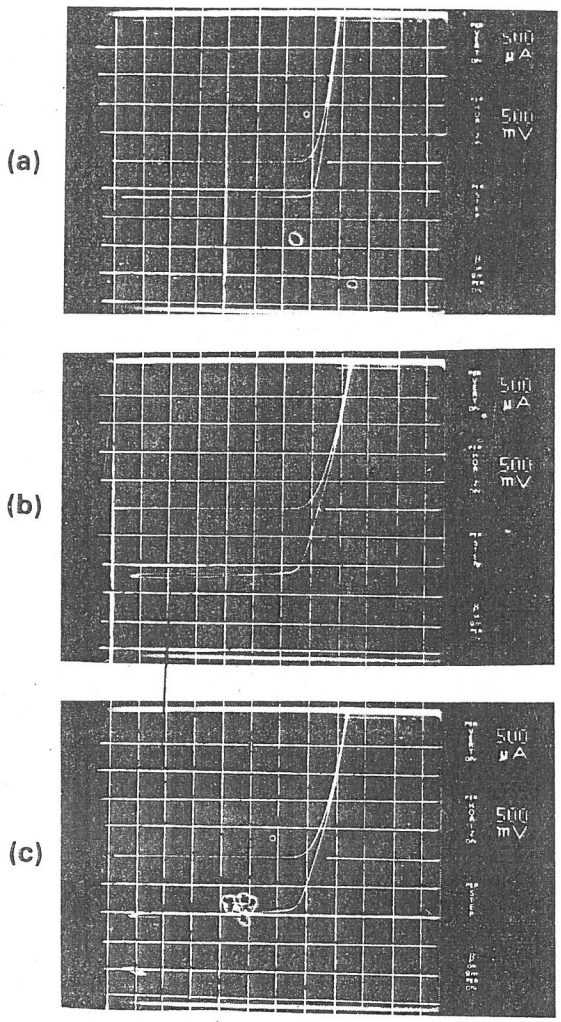

Fig. 7. I-V characteristics of GaAs-Si tandem cells for which (a) none, (b) 25%, and (c) 50% of the GaAs area was removed by etching.

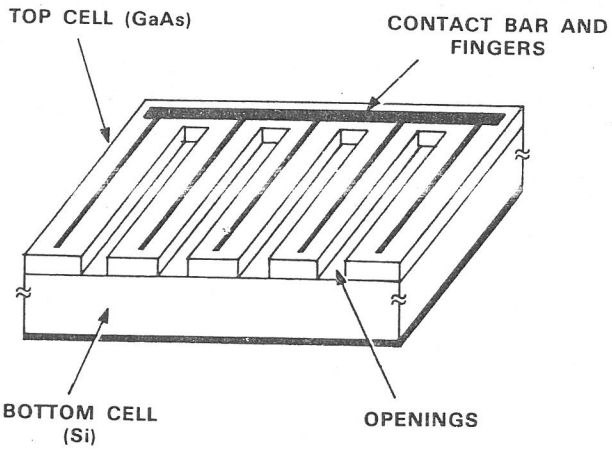

Fig. 8. Schematic diagram showing a GaAs-Si tandem cell with openings etched in the GaAs layers.

device the current density in the GaAs cell is now ~12/0.75 = ~16 mA/cm^2, smaller than the J_{sc} of 23 mA/cm^2 observed for the single-junction GaAs/Ge/Si cells, indicating that the current is still limited by the Si cell. When 50% of the GaAs area was removed, J_{sc} decreased to ~10 mA/cm^2 [Fig. 7(c)]. The current of this device is limited by the GaAs cell. The best result should therefore be obtained when the portion of the GaAs area removed is between 25 and 50%, consistent with the calculated optimum value (7) of ~30%. Use of this unequal-area design, in which the area of the top cell is less than that of the bottom cell, would enhance the potential usefulness of GaAs-Si tandem cells and in general permit a broader choice of materials for the component cells in series-connected tandem structures.

For monolithic GaAs-Si tandem cells it would be desirable to grow the GaAs layers directly on the Si substrate, without an intermediate Ge layer, since absorption in even a thin Ge layer causes some reduction in the solar radiation reaching the Si junction. Although direct growth of GaAs on Si using the $AsCl_3$-GaAs-H_2 CVD technique has not been accomplished because nucleation is impeded by surface contamination, in recent MBE experiments we have succeeded in growing single-crystal layers of both GaAs and $Al_xGa_{1-x}As$ ($0.2 \leq x \leq 0.5$) directly on Si substrates.

CONCLUSION

By improving material and device processing, we have fabricated shallow-homojunction GaAs/Ge/Si cells with conversion efficiencies of 14 and 11% for areas of ~0.093 and 0.51 cm^2, respectively. Improvement in cell performance could be achieved by reducing overall dislocation density and by preventing dislocations from bending over parallel to the junction. We have also fabricated monolithic GaAs-Si tandem cells and demonstrated a novel technique for significantly increasing the photocurrent by removing a portion of the top GaAs cell

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