

OVERVIEW ON SOME RECENT ADVANCES IN WAFER BONDING TECHNOLOGIES

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ABSTRACT

In this overview some recent advances in wafer bonding technologies are illustrated by many examples. Bonding techniques associated to a film transfer process enable to obtain either thick or thin layer bonded structures. Most of the results concern hydrophilic bonding processes. Such processes use either direct bonding or via insulating or conductive layers. In particular hydrophilic bonding onto insulating substrates, specific bonded heterostructure transfers as well as patterned film transfers are illustrated for large size structures. Most of the results are obtained using the Smart-Cut[®] process which appears more and more generic. On another side hydrophobic bonding advances are depicted through Si-Si bonding. Recent results involving ultra thin Si layers (<10nm) bonded onto Si wafers are reported. Buried dislocation networks are obtained enabling a new applications based on self organized growth of nanostructures.

INTRODUCTION

Direct bonding of hydrophilic or hydrophobic surfaces are more and more attractive topics for many laboratories [1-4]. Some of them have already induced industrial applications. Currently, wafer bonding can be achieved in a clean room, at room temperature, between two wafers after preparation of their surfaces. Surface qualities (morphologies, particle contaminations...), physical parameters, and surface chemical bonds, mainly involved in bonding mechanisms, have been investigated both before contacting the two wafers and after bonding. For instance, effects due to surface micro-roughness or additional thermal treatments have been highlighted. Specially quite high bonding energies have been targeted, keeping the objective of a high quality for the bonded structure. Hereafter, we present recent results on various homo-structures (film and substrate of the same material) or hetero-structures (film and substrate of different materials) obtained by wafer bonding.

Recent advances have led, for instance, to the development of silicon on insulator (SOI) structures and emergence of bonded structures suitable for new applications, as microelectronics, sensors, MEMs, optical devices...

Depending on the application, it may be necessary to reduce the thickness of one of the two wafers after bonding. To get bonded structures of a few microns thick layers, a grinding and etching process is well suited. However in microelectronics, active device layers are generally very thin. To achieve bonded structures in which layers are thinner than $\sim 2\mu\text{m}$, processes leading to a good homogeneity of film thicknesses and a high quality of the active device layer can be used as Smart-Cut[®], epitaxial layer transfer (Eltran[®]) or bond and etch back silicon on insulator (BESOI) processes.

BONDING OF HYDROPHILIC SURFACES

In microelectronics, bonding of bare or thermally oxidized silicon surfaces remains one of the most well known examples for bonding of hydrophilic surfaces, as used in achievement of SOI bonded structures. In parallel, deposit processes of oxide layers (e.g. SiO_2) have been extensively developed on any type of materials and surface cleaning procedures have been widely studied to obtain hydrophilic surfaces. Deposit and cleaning of SiO_2 layers as a way to allow wafer bonding between wafers whatever their nature was more and more very attractive.

In this work, wet cleaning processes have been performed by wet chemical etching to obtain hydrophilic surfaces. Modified RCA solutions are commonly used to remove particles as well as metallic contaminants or hydrocarbon contamination. They are based on ammonium peroxide mixture (APM) and hydrochloric acid peroxide mixture (HPM) [5]. It has been previously shown that particles left at the bonding interface could induce unbonded areas leading to macroscopic bonding defects [6].

For the hydrophilic bonding of thermally oxidized Si surfaces, a micro-roughness threshold value of 0.5nm RMS has been previously reported by Abe et al. [7]. More recently Rayssac et al. have shown for SiO_2 surfaces that this micro-roughness threshold value can be increased up to 0.63nm RMS measured by AFM. Above this value macroscopic bonding defects or even no bonding can occur [1]. Moreover in the case of (Si onto SiO_2) structures, they observed that the bonding energy, measured by the crack opening method [8], decreases when the surface roughness increases, whatever the annealing temperature.

Replacing SiO_2 layers by CVD Si_3N_4 layers at the bonding interface, microroughness values of Si_3N_4 surfaces have been highlighted higher than the ones of SiO_2 surfaces. Using the same assumption of a bonding energy depending on surface micro-roughness, we can assume that Si_3N_4 surface micro-roughness induces in either (Si_3N_4 onto SiO_2) or (Si_3N_4 onto Si_3N_4) structures a bonding energy lower than the one corresponding to (Si onto SiO_2) structure. This has been observed as long as annealing treatments are performed at temperature below which surface flowing can occur. Above this temperature, comparable bonding energies can be reach. As shown in figure 1, bonding energies of (Si onto SiO_2), (Si_3N_4 onto Si_3N_4) and (Si_3N_4 onto SiO_2) structures have been investigated after 1h annealing over the [20°C-1200°C] temperature range [9].

Mechanisms leading to strong bonds, such as covalent siloxane bonds in (Si onto SiO_2) structures, seem to occur at lower temperatures for (Si onto SiO_2) than for (Si_3N_4 onto SiO_2) structures.

In order to monitor the chemical bond evolutions at the interface versus the annealing temperature, infrared multiple internal transmission (FTIR-MIT) measurements have been successfully performed using prism coupling as previously described by Maleville et al. [6]. The evolution observed in the bonding mechanism of Si/ SiO_2 structures appears

to be in a good accordance. FTIR-MIT results have shown a strong decrease of the intensity of the peaks in the range [300°C - 900°C] (figure 2b) [12] is due to the decomposition which occurs in this range, $\text{Si-N}_x\text{-O}_y\text{-Si}$ (x bonding energies.

Bonded silicon layers, can be high performance for photonics, sensors and optoelectronics instead of silicon. Advantages for low voltage Smart-Cut[®], Eltran[®] substrates. For instance Insulator (SOI) wafer in large quantities.

Thick SOI structures

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to be in a good accordance to the one described by Weldon et al. [10]. Three temperature ranges have been identified. Below 200°C, bonding is mainly attributed to hydrogen bonds between adsorbed water molecules. For temperature ranging from 200°C to 800°C, water desorption occurs leading to hydrogen bonds between silanol (Si-OH) groups and creation of siloxane (Si-O-Si) groups. Above 800°C complete closure of the bonding interface is achieved by covalent siloxane bonds.

FTIR-MIT results have shown (figure 2) that the (Si₃N₄ onto SiO₂) structures present also a bonding mechanism evolution in three different temperature ranges [9]. Below 300°C, a strong decrease of the Si-OH group density (3400-3600)cm⁻¹ can be observed. In the range [300°C - 900°C] a slight water desorption is still occurring. Above 900°C, a slight increase of the peaks linked to SiH (2075 cm⁻¹, figure 2a) [11] and NH groups (3340cm⁻¹, figure 2b) [12] is also evidenced. These behaviors have been attributed to water decomposition which induces a slight increase of Si-H or N-H bonds. In this temperature range, Si-N_x-O_y-Si (x, y = 0 or 1) covalent groups are mainly involved, leading to strong bonding energies.

SOI BONDED STRUCTURES

Bonded silicon on insulator (BSOI) wafers, with thick top silicon or buried oxide layers, can be high added value substrates for applications such as power devices, photonics, sensors and micromachining purposes. At the opposite, use of SOI wafers instead of silicon wafers to achieve integrated circuits provides very interesting advantages for low voltage or low power applications. For thin layer processes such as Smart-Cut[®], Eltran[®] or BESOI have to be used to transfer thin films onto dedicated substrates. For instance, the Smart-Cut[®] process, developed first to obtain Silicon On Insulator (SOI) wafers, is now an industrial process which provides high quality materials in large quantities.

Thick SOI structures

For power device applications, thicker buried SiO₂ layers (up to ~3µm) and Si layers of few tens microns thick are needed. After cleaning the wafers to obtain hydrophilic surfaces, oxidized silicon wafers are classically bonded onto bare or oxidized wafers. Then, thermal annealing treatments are performed at high temperature typically for 2h. Finally one of the two silicon wafers is reduced in thickness to make the SOI layer, using a classical grinding and etching process, such as in a BSOI technique.

Bonding energies have been investigated in the [200°C-1300°C] temperature range. It has been pointed out that thermal treatments have to be tuned above 1000°C. For instance the temperature is depending on oxide layer thicknesses. If annealing treatments are done at a too low temperature, it is worth noting that a chemical etch such as Wright etch of cross-sections of (Si bonded onto SiO₂) structure reveals the weak bonding interface by a faster Si etch rate. Typical SEM observation of such an "under-strengthened" structure is shown in figure 3a, where the buried oxide and the top Si layer are 3µm and 20µm thick respectively. By using an appropriate thermal treatment to strengthen the bonding, a complete closure can be observed by SEM on SOI cross-sections. Comparison with the

same Si or SiO₂ thicknesses and the same Wright etch revelation is illustrated in figure 3b.

Furthermore, use of such thick buried oxides could induce important curvatures of bonded structures. Curvature characterizations (bows, warps...) have been performed by a capacitive method (Ultrage from ADE Corp.). Possible under certain bonding conditions quite low values have been measured for bonded structures with 3μm thick buried oxide, respectively in the [10μm to 20μm] range for bows and in the [20μm to 40μm] range for warps. But such SOI structures made of thick layers can not be easily obtained with a thickness homogeneity better than ~0.5μm.

Thin SOI wafers made by the Smart-Cut® process

The Smart-Cut® process is well suited for obtaining SOI wafers, especially for very thin top silicon layers (< 1.5μm) [13]. This process has several advantages from both technical and economic points of view [2]. It allows a large flexibility in top Si layer thickness with a very high thickness homogeneity (<10nm for 200mm wafers). Among other advantages, the capability of transferring thin layers with a high crystalline quality onto different materials deserves to be highlighted. From an economic point of view, the possibility of reusing the remainder of the implanted substrate helps in reducing costs.

Moreover this process appears as a good way to evaluate the quality of bonding and the efficiency of bonding strength at low temperature. As a matter of fact, effects of bonding defects are enhanced at a macroscopic scale because of the thin thickness of the bonded layer.

This process is mainly based on ion implantation and wafer bonding (figure 4). During the first step, ion implantation (hydrogen, helium...) induces, in the "donor" wafer, the formation of an in-depth weakened layer, located at the mean ion penetration depth. At the second step, the implanted wafer and a second wafer are bonded together. Then the splitting (third step) is induced in the weakened layer leading to transfer a thin film. The remainder of the donor wafer can be recycled. Using thermal treatments at a low temperature enables a strengthening of the bonding and, consequently, the second wafer to play the role of a stiffener for the splitting mechanism. A final step consists in a soft touch polishing to remove any roughness at the surface of the bonded structure.

Results, obtained on new generation of standard (0.2μm Si, 0.4μm SiO₂) SOI bonded wafers, indicate a density of Secco defects of a few hundred defects/cm² for a silicon thickness, remaining after Secco etching, as thin as 30nm [2]. In parallel, the density of HF defects is in the 1cm⁻² range for SOI made from CZ wafers and less than 0.1cm⁻² when SOI are made from initial low Cop wafers. In CZ wafers HF defects are essentially induced by grown-in defects, present in the initial silicon wafer used to obtain the top silicon layer.

Beyond the crystalline quality, one target for developments of SOI bonded structures is the achievement of bonded structures with thinner films. For microelectronic applications, ultra thin SOI wafers, made of Si and SiO₂ layers a hundred nanometers thick and below, have been successfully transferred by the Smart-Cut® process. For instance, (~0.1μm Si, ~0.1μm SiO₂) SOI structures have been produced. High crystalline qualities and thickness uniformities are achieved, comparable to those of standard (0.2μm Si, 0.4μm SiO₂) SOI structures, over the whole 200mm wafers. Quality of bonding interfaces investigated by SEM observations have shown very sharp interfaces for SOI structures made by Smart-Cut®. Chemical etches, either by buffered-HF or by Wright

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solutions, are used to highlight weak bondings. After high temperature annealing (about 1100°C), bonding interface closure is complete as shown in figure 5, where the oxide and top silicon layers are respectively 50nm and 80nm thick. Further actions to reduce Si and SiO₂ layer thickness in the few ten nanometer range with the same level of quality for SOI structures are underway.

Multiple SOI layers stacked by multiple "Smart-Cut"® transfers

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Beyond these simple SOI wafers, structures made of multi-layers are more and more emergent. Wafer bonding, based on molecular or hydrogen bonds, requires pretty good substrate surface quality, especially in terms of roughness and surface defect density. Roles of both surface micro-roughness and surface cleaning before bonding have been underlined, evidencing that SOI surfaces, as-achieved by the Smart-Cut® process, are suitable to direct bonding. Standard SOI wafer exhibits the same surface roughness than silicon wafers. As a matter of fact, wafer bonding can be applied similarly between two SOI wafers. The flexibility of both the bonding and the Smart-Cut® processes can be used to realize complex structures. So (Si-SiO₂) bilayers have been bonded on a same structure periodically. It can be done by transferring again a single layer transfer several times onto a same wafer, or transferring SOI layer stacks already formed onto either a single substrate or a SOI wafer, etc...

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So, multiple SOI layers stacks can be easily made using SOI wafers as top and base wafers in the Smart-Cut® technology, as shown in figure 6, where [Si/SiO₂] bilayers were stacked up, four times, on 100mm silicon substrates [14]. The SEM view of the final structure reveals sharp interfaces and perfect intra-layer insulation.

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Thanks to the high versatility of such process, thickness of each layer can be easily adapted, depending only on the targeted application. In the same manner, materials of each layer can be chosen. The Smart-Cut® process can then be considered as a basic process step for obtaining multilayer SOI wafers, allowing different crystalline and/or amorphous layers to be stacked. This capability enables to enlarge the field of applications from 3D process integration to optical filters, micro machining, sensors...

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Thanks to improvements in bonding techniques, it is now possible to make single crystalline over-layers, such as silicon, on top of a large variety of insulating layers and large size substrates. Recently, 200nm thick silicon films have been successfully transferred onto insulating multi-layers (SOIM) by the Smart-Cut® process [9]. Such SOIM structures should be used in micro-electronic and micro-technology applications soon, where thermal dissipations are to be taken into account. This is the case of devices submitted to a self heating effect. For instance, SOIM structures have been made by bonding oxidized silicon wafers to Si wafers coated by CVD deposited Si₃N₄ films. The thickness of each insulating film is in the [0µm-0.4µm] thickness range. Such SOIM structures seem to be attractive due to the high thermal dissipation power of Si₃N₄ films, as confirmed by comparing thermal conductivities (30 W m⁻¹K⁻¹ instead of 1.01 W m⁻¹K⁻¹ for SiO₂).

To achieve SOIM bonded structures, made of Si film/Si₃N₄ bonded onto SiO₂/Si bulk, no chemical mechanical polishing of Si₃N₄ surfaces is required for Si₃N₄ surfaces. It has been shown whatever the thickness up to ~0.5µm. In this study, a wet chemical cleaning step has been chosen to obtain hydrophilic surfaces before bonding, whatever the Si₃N₄ film thickness in the [0nm-400nm] range. After cleaning, Si₃N₄ surface microroughnesses were measured at about 0.35nm-RMS, for both 200nm and 400nm thick Si₃N₄ films.

Various structures have been bonded by contacting Si₃N₄ surfaces either to bare Si wafers or to SiO₂ or Si₃N₄ film surfaces. After splitting, SOIM structures were annealed at 1100°C to strengthen the bonding. High quality of bonding is pointed out by TEM observations as in figure 7 for a (Si₃N₄ onto Si₃N₄) structure interface.

Varying the ratio between SiO₂ and Si₃N₄ film thickness induces a wafer curvature modification. Without silicon nitride, the structure is very slightly convex, while with 200nm thick Si₃N₄ layer, the structure becomes slightly concave, keeping the SiO₂ thickness constant (400nm) [9]. Introduction of silicon nitride layer appears therefore as a simple route to control bows of bonded structures.

SPECIFIC HETEROSTRUCTURES

Wafer bonding processes are particularly advantageous to obtain thin single crystalline layers onto supports which basically are not suitable for epitaxy of such layers. Various studies are underway to develop new structures, allowing a large number of material combinations to be achieved [15-19]. Using the Smart-Cut® process to transfer thin films, hetero-structures have been successfully achieved with GaAs, (S-, Sn-, or Zn-) doped InP, insulating InP, (4H, 6H, 3C)-SiC, LiNbO₃...films, enlarging the field of applications in microelectronics, opto-electronics, microwaves, and sensors. Usually, most of the film transfers are first studied by bonding onto substrates of the same nature (homostructures) and are then fitted onto substrates suitable for their applications (fused silica, poly-crystalline SiC, sapphire, Si via metallic films...)

Transfers onto insulating substrates

For some applications, such as displays, micro-wave devices..., it may be required to get thin silicon films onto insulating substrates, such as fused silica, sapphire, high resistivity silicon wafers... Because of different thermal coefficients between films and substrates, specific bonding conditions had to be tuned to succeed. For instance, surface microroughness has to be smoothed enough to enable an efficient bonding at low temperature since thermal treatments have to be limited to avoid too high stresses at the bonding interface. Moreover transfers by the Smart-Cut® process of thin Si films have been demonstrated onto fused silica wafers, as illustrated in figure 8.

In parallel, stacking processes to achieve bonded multi-layer structures have been investigated despite the different thermal expansion coefficients. Here again, specific bonding conditions have been adapted to succeed in, using thin PECVD oxide layer as a bonding layer. Example is given by bonding 525µm thick Si wafers onto silicon-on-sapphire (SOS) substrates, as shown in figure 9. A 0.5µm thick oxide layer has been deposited onto each surface and wet cleaning has been used to achieve hydrophilic

surfaces before bonding, grinding and etching

Transfers via conductive

For some other applications, a bonding layer and substrate are demonstrated [20]. For these bondings, because of the palladium silicide layer, to achieve the bonding, a layer coated by ~0.05µm. After contact, a bond is formed spontaneously at room temperature (onto SiO₂) hydrophilic energy strongly increased by diffraction to be Pd₂Si. Moreover, to evaluate the process, hydrogen-implanted bonded to a 0.1µm layer splitting occurred in the structure made of a substrate in view of the transferred film indicating therefore the

Structures with silicon

Transfer of SiC is attractive for the development of GaN based applications both the bonding layer and bonding SiC wafers. SiC wafers, via oxidation of the Smart-Cut® technique, SiC films [21]. It is recycled several times. For some applications, epitaxial growth, bonding onto polycrystalline SiC of interesting electronic properties. For some other applications, across the bonded structure, polycrystalline SiC is performed via tungsten physical considerations.

into SiO₂/Si bulk, no Si₃N₄ surfaces. It has wet chemical cleaning, whatever the Si₃N₄ microroughnesses, thick Si₃N₄ films, then to bare Si wafers. These were annealed at 1000°C as pointed out by TEM. It is a wafer curvature, convex, while with SiO₂, keeping the SiO₂ appears therefore as a

to obtain thin single epitaxy of such layers. Using a large number of Smart-Cut® process to transfer GaAs, (S-, Sn-, or Zn-) enlarging the field of view of sensors. Usually, Smart-Cut® of the same nature for applications (fused

it may be required to bond silica, sapphire, high strength between films and substrates. For instance, surface energy dependent bonding at low or high stresses at the interface of thin Si films have

structures have been investigated. Here again, specific CVD oxide layer as a bonding layer onto silicon-on-silicon oxide layer has been used to achieve hydrophilic

surfaces before bonding. In that case, silicon thickness has been reduced to 15µm by grinding and etching.

Transfers via conductive layers

For some other applications, a contact with a low electrical resistance between top layer and substrate is required. For that purpose metallic bonding has been recently demonstrated [20]. For instance, thin palladium films have been used to obtain metallic bondings, because it readily reacts with Si, GaAs, InP... at low temperatures (e.g. palladium silicide layer is made at temperature slightly above 200°C).

To achieve the bonding of silicon-metal-silicon structures, two 100mm silicon wafers, coated by ~0.05µm of palladium, were first wet cleaned to obtain hydrophilic surfaces. After contact, a bonding wave was observed by infrared transmission showing that spontaneous bonding occurred between these two metallic surfaces. Bonding energies at room temperature have been measured close to 100 mJ/m² and are comparable to (SiO₂ onto SiO₂) hydrophilic bonding energies. After annealing at 300°C during 30mn, bonding energy strongly increases due to the formation of a silicide layer determined by X-ray diffraction to be Pd₂Si (figure 10).

Moreover, to evaluate the compatibility of such a metallic bonding with the Smart-Cut® process, hydrogen-implanted silicon wafer with 0.1µm of Pd deposited thereon was bonded to a 0.1µm Pd-coated silicon wafer. Using an appropriate thermal treatment, splitting occurred in the weakened hydrogen implanted region, leading to a bonded structure made of a single crystalline Si film onto a silicide Pd₂Si film. The macroscopic view of the transferred structure shows a transfer of a good quality over the whole wafer, indicating therefore that metallic bonding is also compatible with large size wafers.

Structures with silicon carbide films

Transfer of SiC thin films, bonded onto low-cost and large-size substrates, is attractive for the development of high-temperature, high-power, high-frequency SiC or GaN based applications. Different structures can be obtained depending on the nature of both the bonding layers and the substrates. Some studies have been first focused on bonding SiC wafers onto various substrates, mainly such as silicon and polycrystalline SiC wafers, via oxide layers [4]. Wet cleaning is used to get hydrophilic surfaces. Using the Smart-Cut® technology enables the transfers of thin high-quality single crystalline SiC films [21]. It is worth noting that the delaminated single crystalline SiC wafer can be recycled several times which is particularly relevant for expensive material such as SiC.

For some applications, requiring very high temperature treatments such as CVD SiC epitaxial growth, bonded structures have to be adapted. 4H-SiC films have been bonded onto polycrystalline SiC supports via Si₃N₄ layers. Such a structure meets the advantages of interesting electronic characteristics and high thermal dissipation.

For some other applications (e.g. high power electronics), a vertical electrical conduction across the bonded structure is required. In this case, bonding of 4H-SiC wafers onto CVD polycrystalline SiC substrates or low cost single crystalline SiC substrates has been performed via tungsten silicide layers. These bonding layers have been chosen according to physical considerations such as thermodynamical equilibrium with SiC, refractory

behavior and capability to form ohmic contacts with SiC (film and substrate). Furthermore, this has led to the demonstration of SiC thin film transfers using the Smart-Cut® technology [22].

Structures with GaAs or InP films

A structure made of a thin GaAs film bonded onto a silicon substrate is of great interest for the fabrication of opto-electronic and microwave devices since it takes advantage of both materials. Because SiO₂ layers are not chemically stable on GaAs when heated thin GaAs layers have been bonded onto Si wafers via Si₃N₄-SiO₂ bilayers. The feasibility of transferring a 3-inch GaAs film onto a Si substrate using the Smart-Cut® process has been demonstrated [6]. Because of the different thermal coefficients, thermal treatments have to be limited to a low temperature range. So, transfers of thin single crystalline GaAs films onto silicon substrates have been achieved at a splitting temperature of about 250°C.

In the same way, bonding of InP films onto silicon wafers is attractive for applications such as low cost InP pseudo-substrates, integration of optical functions on silicon or high speed optical communication systems. So bonding processes have been investigated taking into account the differences between thermal coefficients. Direct bonding of InP onto silicon has been performed. Moreover, the capability of the Smart-Cut® process to transfer InP films has also been pointed out and splitting mechanisms have been described elsewhere [17]. For instance, splitting occurs when a thermal treatment in the [250°C-400°C] range is used. Semi-insulating InP films and InP with various dopants (S, Sn and Zn) were transferred onto Si substrates successfully (figure 11). Furthermore, it has been also shown that bonding via a metallic layer is also compatible with the transfer of either GaAs films, semi-insulating and (100) oriented, or InP films, Sn-doped (100)-oriented, onto silicon substrates [3,17].

Structures with lithium niobate films

In this study, the possibility of bonding directly thin LiNbO₃ films onto different supports has been demonstrated. Here again, wet cleaning has been used to prepare hydrophilic surfaces. Complete closure of the bonding interface has been achieved as observed by SEM (figure 12).

As a matter of fact and up to now, the Smart-Cut® process had been mainly used to transfer successfully materials with cubic or hexagonal crystalline structures. This process has been shown to be attractively extending to other crystalline structures. For instance, a thin LiNbO₃ film has been successfully transferred onto silicon wafers. Moreover some studies have indicated that bonding and transfer has been achieved with other complex oxide materials, such as SrTiO₃ onto glass substrate... [19].

Structures with partially or fully processed films

The possibility of transferring an integrated circuit as a thin film onto any substrate is very attractive for various applications such as thin film transistors for TFT-LCD's,

sensors, smart-power... wafer onto another wafer... the deposit of an oxide... mechanical polishing... morphology has to be controlled... bonding surface). Surface... high frequency range (surface... lower than ~0.6nm RMS... cleaning to avoid any... surfaces. Using this bonding... layers.

The first transfer to... been proved to be suitable... device layer with AlCu... wafer. The device layer... Smart-Cut® process was... possible provided that... leading to the transfer... section observed by SEM... linked to the device part.

The second transfer... this paper, we are repeating... previous technique, a... required to eliminate bonding... cleaning is again used... When the upper surface... structure, transfer of pre... Planarized patterned wafer... Then, removal of initial... Furthermore, these intermediate... substrates... Electrical characterization... that specifications of the... Provided that transfer... done through the back... that case the last bonding... in figure 15, for a 200nm... fused glass wafer.

Similarly, (Si onto... contacting) has led to... Si bulk wafers were... difficult to obtain. In... carefully surface preparation... the surface micro-roughness... wafers is really lower...

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sensors, smart-power... The main problem encountered for the bonding of a patterned wafer onto another wafer is the planarization of its surface. Planarizing can be done by the deposit of an oxide layer (e.g. TEOS-SiO₂ layer) first followed by a chemical mechanical polishing. Because of the CMP process used to planarize, surface morphology has to be controlled on a long lateral size scale (few hundred microns at the bonding surface). Surface microroughness is of course checked before bonding in the high frequency range (scans of 1μm x 1μm) by atomic force microscopy and has to be kept lower than ~0.6nm RMS. Removal of slurry contamination and particles is done by wet cleaning to avoid any bonding defect and to achieve a convenient hydrophilic state of surfaces. Using this bonding procedure, two possibilities exist for the transfer of device layers.

The first transfer technique is based on the Smart-Cut[®] process which has already been proved to be suitable for transferring patterned layers [23]. As a demonstrator, a device layer with AlCu plots patterned into an oxide layer was achieved onto a 100mm Si wafer. The device layer has been planarized by the deposit of a SiO₂ layer. Then the Smart-Cut[®] process was applied to achieve its transfer. Bonding onto a new substrate was possible provided that surfaces are hydrophilic. Splitting occurred inside the silicon wafer leading to the transfer of both the device layer and a thin Si layer. In figure 13, a cross section observed by SEM is shown. One can observe the thickness change of the Si layer linked to the device patterned underneath.

The second transfer technique is based on bonding, grinding and polishing [24]. In this paper, we are reporting on transfer of 200mm films fully processed. As for the previous technique, a planarization (e.g. using SiO₂ layer) of the device surface is required to eliminate both the device morphology and the surface microroughness. A wet cleaning is again used in order to obtain sufficient hydrophilic surfaces.

When the upper surface of the initial device has to be the top surface of the final bonded structure, transfer of processed films requires the use of intermediate handling substrates. Planarized patterned wafers are first bonded onto intermediate substrates (figure 14 a,b). Then, removal of initial substrates is done by grinding and polishing (figure 14 c). Furthermore, these intermediate structures are bonded onto final substrates and intermediate substrates are removed by a final grinding and chemical etch (figure 14 d,e). Electrical characterizations of such transferred patterned films have been done proving that specifications of the initial devices have been preserved.

Provided that transferred films are thin enough, contact opening can advantageously be done through the back side of the devices (i.e. final top surfaces of bonded structures). In that case the last bonding step onto the final substrate is only required. Example is given, in figure 15, for a 200mm SOI CMOS which has been reversed by bonding onto a silica fused glass wafer.

BONDING OF HYDROPHOBIC SURFACES

Similarly, (Si onto Si) hydrophobic bonding (surfaces are HF last treated before contacting) has led to new emerging technologies. First studies based on bonding of two Si bulk wafers were previously published [25]. The hydrophobic bonding is usually more difficult to obtain. Indeed, the bonding energy at room temperature is very low and more carefully surface preparation has to be used. As a matter of fact, we have pointed out that the surface micro-roughness threshold value (0.18nm RMS) to achieve bonding of two wafers is really lower for hydrophobic surfaces than for hydrophilic surfaces. For

smoother silicon surfaces (0.07nm.RMS) it is worth noting that a very fast bonding wave propagates through the 100mm interface during less than 2 seconds instead of the 15-20 seconds observed for standard ~0.1nm RMS Si surfaces. Concerning the application of the direct hydrophobic bonding, new substrates for self-organized deposit of nanostructures (such as few nanometer wide quantum dots) have been investigated, for a few years [26], by bonding ultra-thin 100mm Si films onto 100mm Si wafers. A film thickness down to 10nm is achieved using a film transfer technique. As explained in figure 16, a SOI wafer is bonded to a bulk silicon wafer. After a thermal stabilization ($T > 1100^{\circ}\text{C}$), the backside of the SOI wafer is removed by grinding and chemical etching using the buried oxide layer as a convenient etch stop layer. Then, using a sacrificial thermal oxidation, the silicon film thickness is tuned down to less than 10nm with a very good thickness homogeneity over the whole wafer, comparable to the thickness homogeneity of the starting silicon SOI film. When two crystalline networks are put into contact, dislocation networks can be generated in order to accommodate the crystalline disorientations. In fact, in-plane rotations of crystalline axes (twist) lead to 2D-networks of periodic screw dislocations and surface inclinations (tilt), mainly due to silicon wafer dicing, induce mixed dislocation networks.

Buried at the crystalline bonding interface, these dislocation networks induce periodic strain fields at the surface of the ultra thin bonded films and could then be used to organize the nanostructure growth. Provided that the twist and tilt angles are controlled during the direct bonding, lattice parameters of self-organized nanostructure networks can be selected. As an example 2.75° twisted and $\sim 0.34^{\circ}$ tilted bonded structure was achieved with a 10nm thick top silicon layer. TEM observations highlighted respectively square networks, linked to the screw dislocations, with a 8nm lattice parameter, and a linear periodic grid, due to mixed ones, with a 46nm period (figure 17).

To manage the organization of the nanostructure growth in two directions, lower and tunable twist angle is required [27]. Moreover, to avoid the mixed dislocation perturbation, no tilt disorientation between the two silicon surfaces is attractive.

Twist bonded interface of $0.44^{\circ} \pm 0.005^{\circ}$ with an interface tilt disorientation below 0.01° has also been obtained as shown in figure 18 (0.44° leads to a distance of 50nm between the dislocations). Such substrates, exhibiting pure square strain field networks produced by the screw dislocations, are presently under evaluation for their capability to organize nanostructure growths.

CONCLUSION

Wafer bonding processes, already in production for SOI structures, appear also as very promising technologies well adapted to many material combinations. Hydrophilic bonding appears well suitable for most of the materials, especially when a wet cleaning can be easily used or when thin layers, as oxide or metallic layers, can be deposited onto wafers to enable the bonding. Comparatively, hydrophobic bonding is used in a less proportion, such as in Si-Si structures, as the bonding process has to be more specific of the material to bond. In that case two oriented single crystalline wafers have to be bonded. It has been demonstrated how powerful and flexible the wafer bonding can be to realize complex structures. The ability to obtain thin films by means of a layer transfer process has been also demonstrated combined either through a direct bonding or via a specific bonding (insulating layers, thermally conductive layers, metallic layers...). Since a transfer by the Smart-Cut[®] process is demonstrated for one material, it can be integrated

in a layer stack structure shown suitable not. Especially based on the generic process too, which opens up new

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in a layer stack structure. Moreover these bonding and transfer processes have been shown suitable not only for homogeneous thin film but also for patterned layers. Especially based on these results, it is worth emphasizing that the Smart-Cut[®] process is a generic process too. It allows a great deal of combinations (material and bonding layer) which opens up new scope for developments.

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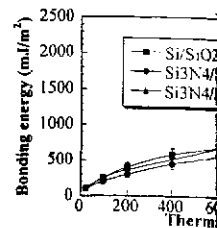
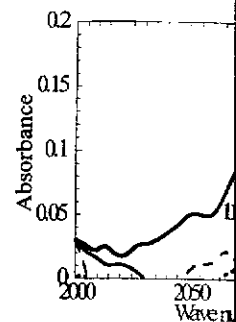
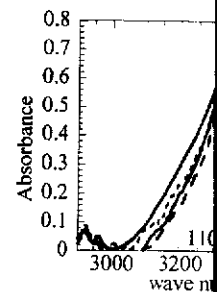


Figure 1: Bonding energy versus annealing temperature of 1h annealing.



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Figure 2: FTIR-MIT Absorbance versus annealing temperature onto Si₃N₄ structure.

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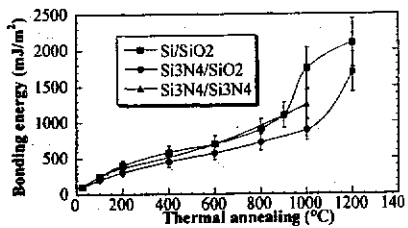
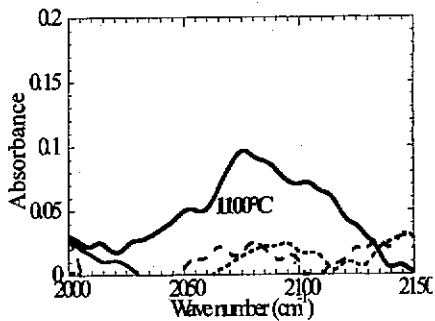
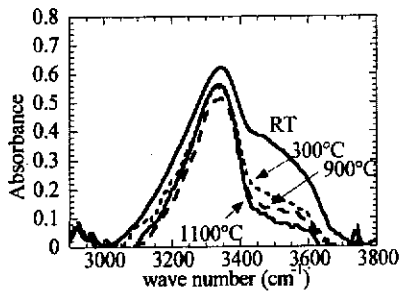


Figure 1: Bonding energy evolution versus temperature of 1h annealing.

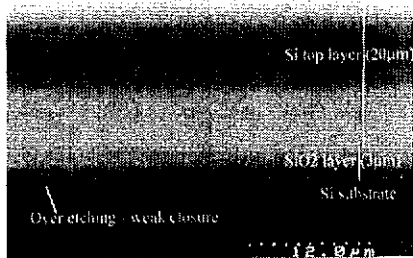


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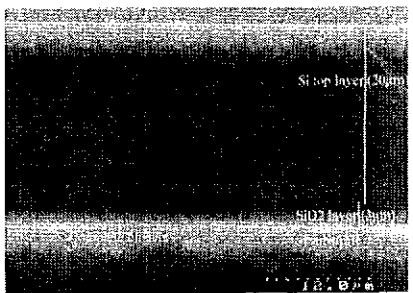


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Figure 2: FTIR-MIT spectra evolution versus annealing temperature of a (SiO₂ onto Si₃N₄) structure.



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Figure 3 : SEM observations of (a) an over-etched interface linked to a typical "under-strengthened" structure and (b) a complete closure interface after an appropriate thermal treatment.

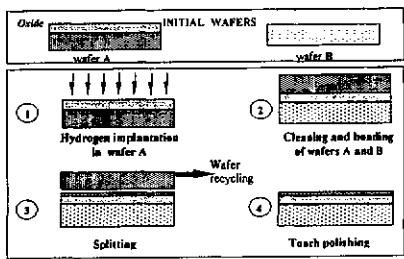


Figure 4 : Four main steps of the Smart-Cut process.

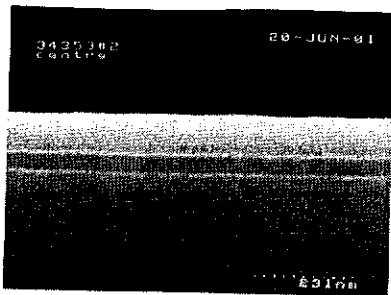


Figure 5: SEM observations of thin layered SOI wafers. The oxide and top silicon wafer (left) and seed wafer remaining after transfer (right) thick.

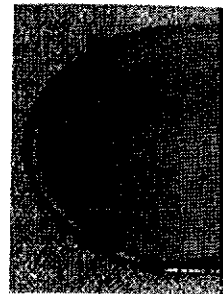
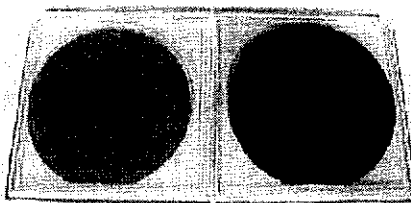


Figure 11: Bonding and InP film onto a Si substrate layer.

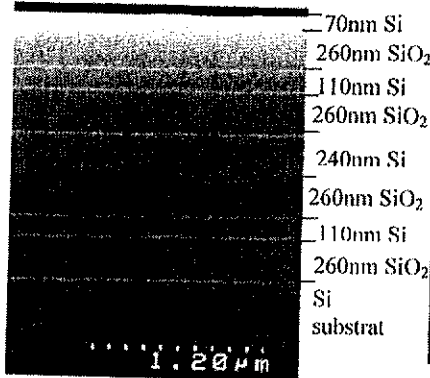


Figure 6: SEM view of stacked SOI layers.

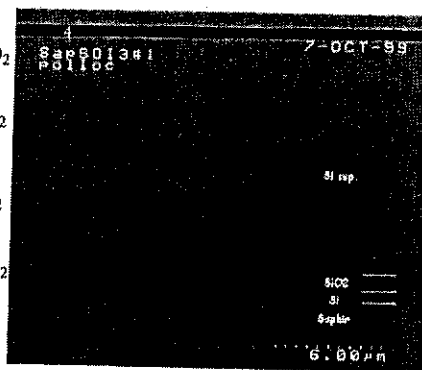


Figure 9: 15 μm thick Si films bonded onto SOS substrates via deposited oxide layers.

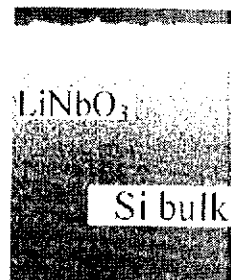


Figure 12: Thin LiNbO₃ onto silicon wafer.

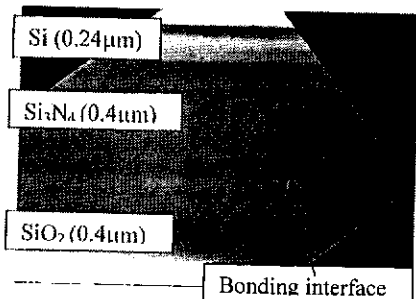


Figure 7: TEM cross-section observation of a Si_{film} / Si₃N₄ / SiO₂ / Si_{bulk} structure.

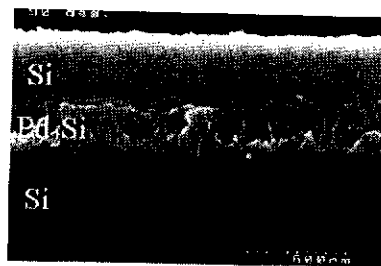


Figure 10: Bonding energy strongly increased by the formation of a silicide layer, determined by X-ray diffraction to be Pd₂Si. Transfer has been done by the Smart-Cut® process.

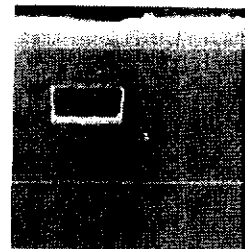
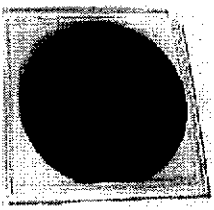


Figure 13: Cross section of AlCu plots have been on oxide layer onto a substrate. Planarization has been done by oxide layer. Transfer has been done by Smart-Cut® process.



onto a fused silica wafer remaining after

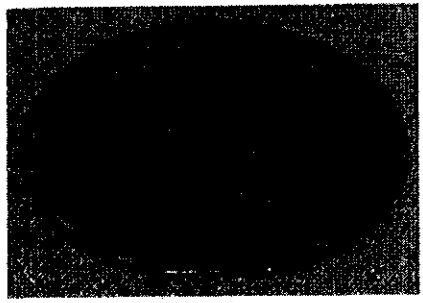


Figure 11 : Bonding and transfer of a 50mm InP film onto a Si substrate via an oxide layer.

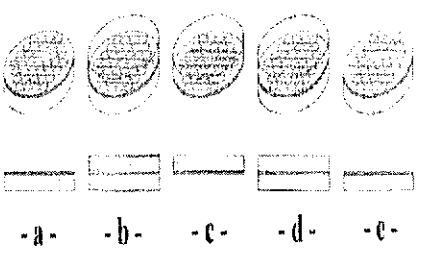
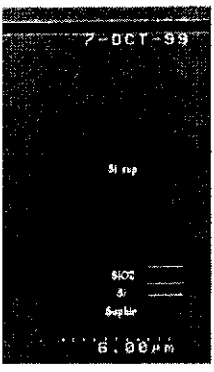


Figure 14 : Transfer technique based on bonding, grinding and polishing.



Si films bonded onto oxidized layers.

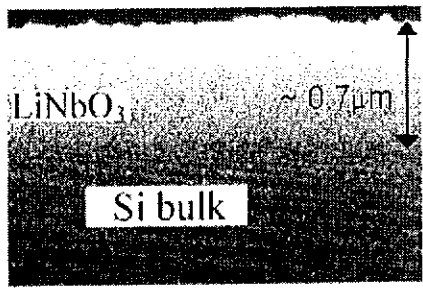


Figure 12 : Thin LiNbO₃ film transferred onto silicon wafer.

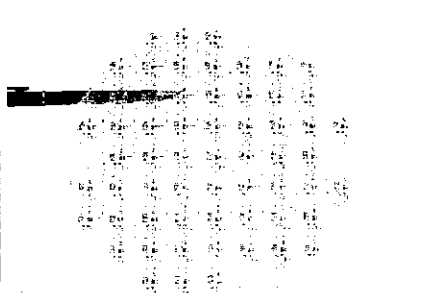
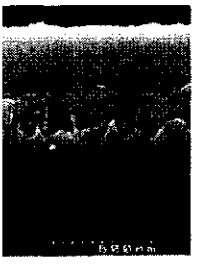


Figure 15 : 200mm SOI CMOS device layer reversed by bonding onto a silica fused glass wafer.



ng energy strongly promotion of a silicide X-ray diffraction to be been done by the

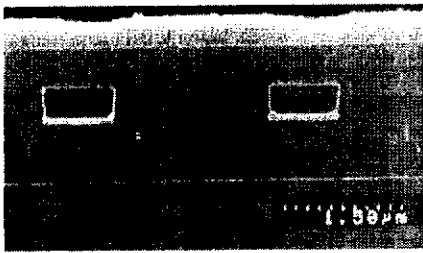


Figure 13 : Cross section observed by SEM. AlCu plots have been patterned into an oxide layer onto a 100mm Si wafer. Planarization has been done thanks to an oxide layer. Transfer has been done by the Smart-Cut® process

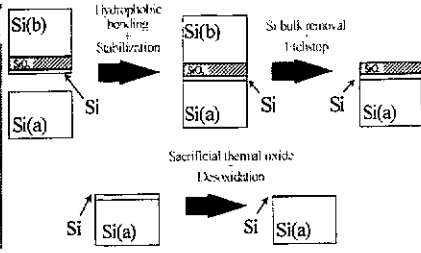


Figure 16 : Process used to make 10nm ultra thin silicon layer, bonded onto silicon wafer, by hydrophobic bonding.

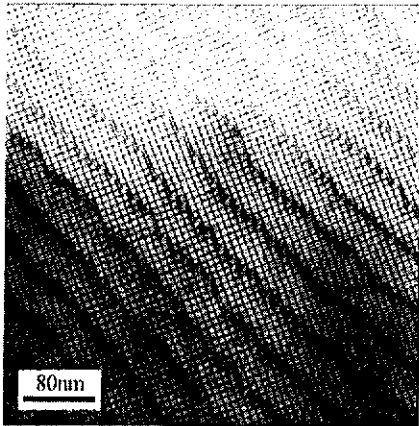


Figure 17 : TEM plane view of a typical silicon/silicon bonded interface. A 2D network of screw dislocations perturbed by a 1D network of mixed dislocations is obtained with an interface with a twist disorientation of $2.75^{\circ} \pm 0.1^{\circ}$ (3° targeted) and tilt disorientation of $0.34^{\circ} \pm 0.05^{\circ}$ respectively.

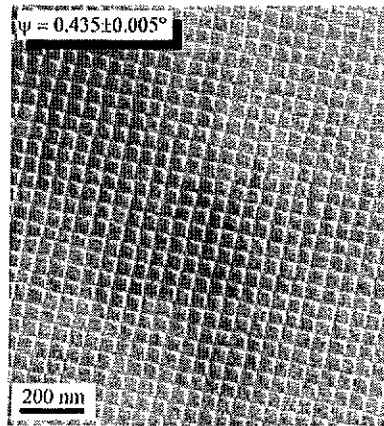


Figure 18 : Large area TEM plane view of a pure twist grain boundary fabricated by wafer bonding. The period of the screw dislocation network ($\sim 50\text{nm}$) gives a twist angle of $0.435^{\circ} \pm 0.005^{\circ}$. The absence of mixed dislocation indicates an interface tilt angle below 0.01° .

Since the realization of wafer bonding and hybrid bonding (Smart Cut[®]) by wafer bonding, succeeded in transferring layers including GaAs, Si, LaAlO₃ and sapphire. Wafer bonding and H 17 co-implantation can realize either reduction of the required for exfoliation of stiffer substrate or transfer of substrate as in, for example, wafer fabrication process. This process must provide the wafer with the internal force to separate the interface allowing the semiconductor film to be transferred at a relatively low, and low energy wafer bonding technique and layer transfer process as low as 300°C in the past. Recently, room temperature mechanical separation processes. These processes are performed at a temperature which is lower than the preparation of the wafer. This paper will report on the transfer using interfacial applications will

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