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High-efficiency hydrogenated amorphous/crystalline Si heterojunction solar cells

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The heterojunction crystalline silicon (c-Si) solar cell is one of the most promising cell structures for high-performance and low-cost solar electricity generation. Efficiencies of more than 22% and the highest open-circuit voltage (0.739 V) for c-Si solar cells have been achieved by the Sanyo group with this structure. A thin intrinsic layer of hydrogenated amorphous silicon combined with doped layers effectively passivates the c-Si surface, reducing surface defects, but also allows carriers to pass through the passivating layer without significant loss. It is this feature that makes a-Si:H uniquely different than other dielectric passivation layers, such as silicon dioxide or silicon nitride. The heterojunction structure uses wider bandgap materials to contact c-Si, preventing carriers from moving onto the wrong side of the junction and then recombining. In this paper, we will review c-Si solar cells with hydrogenated amorphous silicon emitters and back contacts.

Keywords: a-Si:H; crystalline interface; Si; solar cells

1. Introduction

One of the successful applications of hydrogenated amorphous silicon (a-Si:H) is in crystalline silicon heterojunction (SHJ) solar cells. This type of cell combines a crystalline silicon (c-Si) wafer with amorphous Si technology. It uses a hydrogenated amorphous silicon intrinsic (*i*-) layer as a thin (a few nm) and wide bandgap layer that wraps around a high-quality c-Si wafer to passivate the emitter at the front and the contact in the back. The heterojunction is then formed from a-Si:H doped layers. There are many advantages to using an a-Si:H/c-Si heterojunction solar cell. For example, the minority-carrier lifetime in the bulk is preserved because it is a low-temperature process ($<200°C$), in contrast to more than 800°C for the standard diffused c-Si solar cell process. The surface recombination in crystalline silicon can be greatly reduced; in particular, a low surface recombination velocity of 15 cm/s has been achieved. This is as good as other dielectrics, such as thermally deposited silicon dioxide (SiO_2). High efficiencies of more than 22% have been achieved for a large-size (100 cm^2) cell [1]. The highest open-circuit voltage (V_{oc}) reported was 0.739 V for a single-crystal cell at AM 1.5 [2]. High V_{oc} is crucial to obtaining a low-temperature coefficient for power output. This implies that the SHJ solar cell will produce more

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energy over time. The hydrogenated amorphous Si/crystalline Si heterojunction process can be readily adapted to the mass-production of solar cells. The low processing temperature and symmetric process on both sides of the c-Si enables a low thermal budget and minimizes the bowing of thin c-Si wafers. With wafers as thin as 85 μm, solar cells with efficiencies of $>20\%$ have been reported [2]. This is one of the most promising approaches to near-term manufacturing of high-efficiency c-Si wafers <100 μm.

In 1985, Yablonovitch et al. stated [3] that, for maximal performance, solar cells should resemble semiconductor lasers, i.e. they should be constructed in the form of a double heterojunction. Heterojunction solar cells use wider bandgap materials to sandwich a narrow bandgap material, such as c-Si absorbers. Wider bandgap layers create the proper band offset at the conduction and valance bands such that electrons will be reflected back to the absorber at the *p*-type contact and holes will be reflected at the *n*-type contact. The heterojunction acts like a 'carrier mirror'. With these mirrors, the recombination loss at the contacts can be further reduced. The bulk leakage current density can be very low – in the range of 10^{-14} A/cm^2. The paper also emphasized the importance of surface passivation to reduce surface recombination loss. One consequence of using the heterojunction configuration is a higher V_{oc}.

Prior to the a-Si:H heterojunction, Yablonovitch et al. [3] used a mixture of small-grain microcrystalline silicon and silicon dioxide as the wider bandgap layers. The *n*-type microcrystalline silicon was doped with P. Proper annealing of the SiO_2 can passivate the c-Si wafer well. The best V_{oc} in this proof-of-concept device was reported as 720 mV using a *p*-type c-Si wafer with a light intensity of 1.3 suns (roughly the AMO spectrum).

Carrier transport in the amorphous/crystalline Si heterojunction can be unique and different than the simple *p–n* or metal–semiconductor junction because the Fermi level can be varied by doping. The early work of Grigorovici et al. in 1965 and 1968 [4,5] studied the heterojunctions between evaporated amorphous Ge or Si (no hydrogenation) and c-Si. The conclusion was that amorphous Si behaved as a *p*-type semiconductor: it showed poor rectifying properties of the junctions of amorphous Si and *p*-type c-Si compared to good rectifying properties of the junctions of amorphous Si and *n*-type c-Si.

In 1974, Fuhs and his group [6] were the first to study carrier transport using intrinsic a-Si:H on c-Si. They found that there is a heterojunction at the a-Si:H/c-Si interface measured from the spectra photovoltage.

The Sanyo research and development (R&D) group was the first to apply an a-Si:H heterojunction to a c-Si solar cell in 1991 [7]. The Sanyo group also stated that inserting a thin, intrinsic a-Si:H layer between the c-Si and doped a-Si:H layers led to better cell performance. With this *i*-layer, the surface defect states were greatly reduced. It has been clearly shown in the comparisons between structures with and without the *i*-layer that the bulk leakage current is reduced by more than an order of magnitude and V_{oc} is higher with the *i*-layer. Sanyo's trademark 'HIT', which stands for 'heterojunction with intrinsic thin layer', emphasizes the important of the thin intrinsic layer. With nearly 18 years of steady progress, in 2008, the best SHJ solar cells have resulted in a record V_{oc} of 0.739 V and an efficiency of 22.3% in a 100-cm^2 c-Si wafer [2].

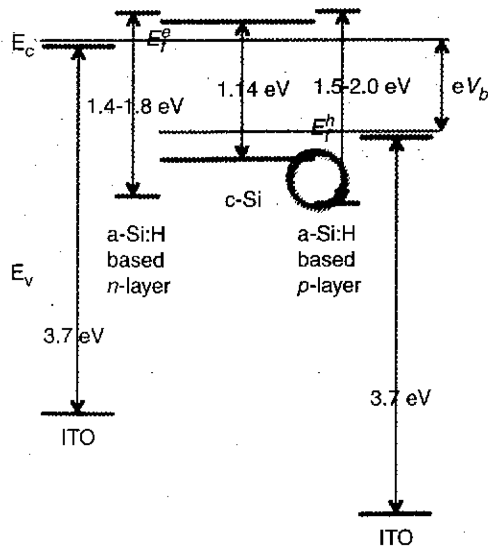

Figure 1. Energy diagram of a double-sided a-Si:H/c-Si heterojunction solar cell biased at forward voltage V_b. Top solid lines are conduction band (E_c); bottom solid lines are valence band (E_v). The dashed lines are Fermi energy for electrons (E_F^e) and holes (E_F^h). The circle indicates a high barrier at a p-type interface.

An energy diagram of a double-sided a-Si:H and c-Si heterojunction biased at a forward voltage V_b is shown in Figure 1. The value of bandgaps for various materials are chosen as follows: from 1.4 to 1.8 eV for a-Si:H-based P-doped layers including a-Si:H and nanocrystalline Si; 1.14 eV for crystalline Si; from 1.4 to 2.0 eV for a-Si:H-based B-doped layers including a-Si:H, nanocrystalline Si, and a-SiC:H alloys; and 3.70 eV for indium tin oxide (ITO). They are all important parts of the SHJ device. The ITO layer plays a significant role in the depletion width of the doped layer. The Fermi level of ITO is slightly above its conduction band (0.1 eV). In general, the contact between ITO and the doped layers is an ohmic contact. For simplicity, a thin intrinsic layer was ignored in our diagram. In principle, a SHJ cell does not need the i-layer. However, the doped a-Si:H contact to c-Si does not passivate the c-Si surface well. The heterojunction has inherited potential barriers or band offsets at the conduction band which are very small at the n-contact and relative high at the p-contact. With this configuration, electrons are only allowed to travel toward the a-Si:H n-layer side. At the valence band, both ends have a higher barrier due to the nature of a-Si:H. It is desirable to have a barrier at the a-Si:H n-layer and c-Si interface to reflect holes, but not at the a-Si:H p-layer and c-Si interface, as indicated by the circle. A high barrier prevents holes from moving freely to the a-Si:H p-layer. Therefore, the a-Si:H heterojunction is a nearly ideal structure for electrons, but not for holes. It is fortunate that holes do pass through the barrier at the a-Si:H p-layer. Under optimized conditions, holes can tunnel through band-tail states and defects near the middle bandgap. An optimized a-Si:H p-layer and c-Si interface will be addressed in a later section.

For c-Si solar cells, surface passivation is crucial in improving cell performance. Defects at the surface (both sides) act as a recombination center for photogenerated carriers. Further reducing these defects will result in an increase in V_{oc}. Many questions surround why heterojunction cells need the *i*-layer. Clearly, the best a-Si:H heterojunction solar cells require both the heterojunction and surface passivation. The passivation layer effectively moves the surface states away from the crystalline silicon. Cells without surface passivation result in a lower V_{oc} than those with proper surface passivation. A doped a-Si:H layer has a high defect density of states (more than $10^{18}/cm^3$). Direct contact of the doped a-Si:H to the c-Si forms a heterojunction to suppress this loss, but carriers can be lost at the interface due to defects at the interface.

The hydrogenated amorphous Si intrinsic layer has shown a superior surface passivation of c-Si. A low recombination surface velocity of 15 cm/s has been demonstrated [8]. This is as good as the best dielectric surface passivation, such as SiO_2 and amorphous silicon nitride (SiN_x) [9]. More importantly, the a-Si:H *i*-layer can be inserted between the c-Si and a doped layer without significant restriction of carrier transport. A thin layer of SiO_2 or SiN_x in place of the a-Si:H *i*-layer will block the carriers and cause an S shape in the current density–voltage (J–V) characteristics.

A thin Si layer deposited directly on c-Si has been studied by many groups [10–16]. From the point of view of growth, deposition conditions affect the structure of the thin Si layer. It has been observed that a-Si:H, microcrystalline Si (μc-Si), epi-Si, or mixed-phase Si of a-Si:H and nano-Si can grow on c-Si at very low substrate temperature. With advances in *in situ* optical monitoring, such as reflectance, ellipsometry, second-harmonic generation, and infrared absorption, one can study the growth of the thin Si layer in real time. This provides rapid feedback for the layer, rather than using tunneling electron microscopy or other post-deposition analytical tools. For solar cell performance, experimental results suggest that only a-Si:H on c-Si gives the highest V_{oc}. Other phases of thin Si layers result in V_{oc} values of ~ 0.6 V. This conclusion is consistent with the passivation of c-Si by measuring the carrier's lifetime: a-Si:H layers give the longest lifetimes. Other forms of Si thin layers will not passivate the surface well and result in a low V_{oc}.

The Helmholtz Zentrum Berlin (former Hahn-Meitner-Institute Berlin) group studied the density distribution of bandgap states in several-nm thick a-Si:H layers on c-Si using X-ray photospectroscopy (XPS), ultra-violet photospectroscopy (UPS) and ultraviolet-excited photoelectron yield spectroscopy (UV-PYS) measurements [17]. It compared the layers of doped and undoped a-Si:H and found that the density of bandgap states in doped a-Si:H is enhanced in comparison to that in intrinsic a-Si:H. The enhanced bandgap states are responsible for recombination at the a-Si:H/c-Si interface.

Phosphorous- and boron-doped layers possess higher defect densities than a-Si:H intrinsic layers [18]. It is believed that the doped layer is the major source of absorption of light, especially in the blue and near-infrared region, due to its higher middle-bandgap defects and greater thickness. Optimizing the doped layer thickness and reducing middle bandgap defects are as important as the doping level in controlling the conductivity.

In the past, many groups following Sanyo's lead have worked on SHJ solar cells. a-Si:H heterojunctions have been fabricated from plasma-enhanced chemical

Table 1. Summary of best V_{oc} and efficiency values of SHJ solar cells on *p*- and *n*-type c-Si (results from 12 groups).

		n-type		*p*-type	
	Area (cm^2)	Best V_{oc} (V)	Best η (%)	Best V_{oc} (V)	Best η (%)
Sanyo [2]	100	0.739*	22.3*		
HZBME (HMI) [32]	1	0.660	19.8**	0.639	17.4
NREL [33]	0.9	0.694	18.2	0.693***	19.2***
IEC [20]	0.56	0.694	18.4***		
Univ. of Neuchatel [12]		0.713	18.4	0.695	
ENEA [30]	2.25			0.601	17
Utrecht Univ. [24]	1			0.595	14.9
AIST [26]	0.21[a]	0.610	15.8		
Univ. of Stuttgart [25]	0.5			0.655	14.1**
CAS [23]	0.5			0.582	14.02
CNR-IMM [11]	1	0.638	14	0.579	13.3
Univ. of Kaiserlautern [27]					10.8

*Independently confirmed by AIST, Japan; **Independently confirmed by CalLab ISE Freiburg, Germany; ***Independently confirmed by NREL PV Performance Characterization Team, USA.
[a]Active area (other areas are total area).

vapor deposition (PECVD), hot-wire CVD (HWCVD) and very-high-frequency PECVD (VHF-PECVD). Table 1 summarizes the best V_{oc} and cell efficiency on *p*-type or *n*-type c-Si wafers from representative research groups around the world [19–33]. This table will serve as an updated version of Jensen's 2002 table [25]. Currently, no groups have repeated what Sanyo has achieved in terms of high V_{oc} and high efficiency. Only two groups have reached beyond 19% efficiency: Helmholtz Zentrum Berlin on *n*-type wafers [32] and the National Renewable Energy Laboratory (NREL) on *p*-type wafers [33]. Over the years, many groups have employed these principles in an attempt to increase the V_{oc}, but progress seemed to have stalled out ~0.65 V. Recently, a few groups have achieved high V_{oc} of more than 0.69 V with the help of understanding surface cleaning and the importance of the a-Si:H interface. The difficulty of repeating Sanyo's high V_{oc} and high-efficiency illustrates that the a-Si:H/c-Si heterojunction is a very challenging structure to fully understand. However, as more groups work on this type of cell using powerful computer simulations [34–36] and adapt more advanced characterization tools for nanoscale interface application, we are in a better position to answer these questions and unravel the mystery of the process.

2. SHJ cell process

This section will describe the typical complete process for a-Si:H and c-Si double-side heterojunction solar cells. This type of solar cell uses c-Si as the bulk absorber to

convert light into electron-hole pairs and the a-Si:H process to make the front emitter and back contact.

For a laboratory-scale SHJ solar cell structure, thin Si layers are symmetrically wrapped around the c-Si. From top to bottom, these include a metal grid, transparent conducting oxide (TCO), a-Si:H (*p* or *n*), c-Si(*n* or *p*), a-Si:H (*n* or *p*), TCO, and the back metal contact. Depending on the type of c-Si wafer, light is incident on the emitter side which is the a-Si:H (*p*)/c-Si(*n*) or a-Si:H(*n*)/c-Si(*p*). The finished cell has an area of 1 cm^2 or larger with a 4% metal grid obscuration on the front surface. For SHJ cells, the larger the area, the smaller the effect of the perimeter leakage. The top metal grids are composed of an evaporated multi-layer stack of Ti/Pd/Ag/Pd or Cr/Ag. This stack uses Ti to enhance the adhesion to the transparent conducting oxide (TCO) layer and Pd to prevent Ag from diffusing in or out. Ag provides most of the thickness and acts as the conduction layer. Photolithographic or patterned physical masks were used to generate the grids. The bottom contact can be Al or Ag or a stack of Ti/Pd/Ag/Pd using e-beam or sputtering deposition. The TCO was deposited from a reactive evaporator or sputtering. The TCO can be indium tin oxide or Al-doped zinc oxide (ZnO). The front TCO acts as an antireflection layer as well as a conducting layer. The thickness of the TCO ranges from 760 to 900 Å.

High quality float-zone (FZ) and Czochralski (CZ) c-Si wafers, both *n*-type and *p*-type crystalline Si, were used for high-efficiency cell development. The Si wafers are (100) or (111) orientation, up to 300 μm in thickness, and 0.5–4 Ω/cm in resistivity. The crystalline Si wafer (100) was chosen for creating a random pyramid texturing. The minority carrier lifetime after surface passivation is in the order of 1 ms measured by a Sinton lifetime tester. Both FZ and CZ c-Si wafers can produce a high efficiency cell as long as its minority carrier lifetime is in the order of 1 ms.

All the c-Si wafers are subject to a thorough wet chemical-cleaning process to remove saw damage and surface impurities [37]. Often, chemical oxides such as H_2O_2 were used intentionally to grow SiO_2 on the c-Si wafer and then removed by a dilute HF solution to get a fresh surface before processing. A final 2–5% HF cleaning was applied to the c-Si wafer before loading it into an a-Si:H deposition chamber.

Most heterojunction solar cells are processed by plasma-enhanced chemical vapor deposition (PECVD) or VHF-PECVD [7,12,14,20,28]: the standard a-Si:H deposition technique using an RF electric field to decompose silane gas. Other groups used hot-wire (HW) CVD for a-Si:H. the HWCVD used hot-filament (2100°C) to decompose silane [8,23].

The first *i*-layer was grown at very low temperature (around 100°C) with an optimized thickness of a few nm of a-Si:H. Low temperature was used to ensure the growth of a-Si:H on c-Si, although high quality a-Si:H is grown at a much higher temperature (200°C). a-Si:H was deposited from pure SiH_4 but some groups add H_2 to the process so that the film still stays in a-Si:H phase. HWCVD has the advantage of little or no ion bombardment of the c-Si surface in comparison to PECVD. After coating both sides with the *i*-layer, both sides of the c-Si wafer are ready for the doped layer of 4–8 nm at ~200°C. For the *n*-layer, SiH_4 is mixed with PH_3 or $PH_3 + H_2$, and the *p*-layer uses SiH_4 mixed with B_2H_6, $B_2H_6 + H_2$ or $B_2H_6 + CH_4$. After the doped layer, the TCO is deposited. The front TCO layer thickness ranges from 760 to 900 Å for a planar or textured surfaces, respectively. At the back of the cell, the TCO can be as thick as 100 nm. After the TCO, the metal grid for the front

and a planar metal contact for the back are deposited. Finally, the front TCO is patterned, defining the cell size into a typical size of $1\,cm^2$.

Texturing of c-Si is used to enhance light trapping. This can be done by applying 3–5% KOH with IPA at 80°C for both *p*-type and *n*-type c-Si wafers. A random pyramid was created in less than 30 min. The characteristic size of the pyramids is $< 10\,\mu m$, measured with scanning electron microscopy. Just textured c-Si wafer needs a further cleaning to remove heavy metal and other impurities. A standard RCA 1 and 2 clean procedure can be used before a-Si:H deposition. This clean procedure was sufficient to remove residual impurities, resulting in a good V_{oc} close to that realized for planar c-Si wafers. A more efficient cleaning method may be developed in the future.

For textured or rough surfaces, the challenge is for conformal layers to cover the peaks and valleys. Fortunately, the a-Si:H process, both from PECVD and HWCVD, can provide conformal coverage.

The J–V characteristics of finished cells were tested under AM1.5 conditions using a solar simulator. One should pay particular attention to the sampling rate between points for high-efficiency and long carriers lifetime solar cells [38, 39]. Global reflectance was used to measure textured or planar cells for internal quantum efficiency (IQE) and external quantum efficiency (EQE). From the IQE or EQE, one can estimate the short circuit current density (J_{sc}) and current loss with respect to the spectra. One can also deduce the diffusion length and surface recombination velocity.

3. SHJ cell performance

This section will address the issues relating to SHJ cell performance. The heterojunction process preserves c-Si wafer quality and prolongs carrier lifetime. A high V_{oc} is the signature of the SHJ, but there are many minor issues that must be understood and resolved to further improve this type of solar cell. These issues are surface passivation, relatively low fill factor (FF), low short-circuit current density (J_{sc}), S-shape J–V in a double-sided cell, light-induced degradation, and *p*-type versus *n*-type c-Si wafers.

The double heterojunction is essential for high performance and high V_{oc}. This is simply because a c-Si wafer has a double side and both surfaces need to be passivated. The lifetime of minority carriers can be over 1 ms, and the back-surface recombination velocity can be reduced to $\sim$15 cm/s when proper surface passivation is applied to both sides. High lifetime and low surface recombination velocity are key factors when improving cell performance. Many other groups have also reported effective surface passivation using other materials such as hydrogenated amorphous Si and O alloy (a-SiO:H) to c-Si [26].

In addition to the prolonged lifetime of minority carriers, contact formation on the thin, doped a-Si:H layer is also critical [40]. NREL reported previously that Ti deposited directly on a thin, doped a-Si:H layer at the back contact caused a decrease in V_{oc}. For example, with an indium tin oxide (ITO) contact on the back doped layer, a high V_{oc} of 0.680 V was routine; when using Ti directly in contact with the same doped layer, the V_{oc} decreases by 56 mV. However, when depositing a much thicker doped a-Si:H layer (a six-fold increase in deposition time) with a Ti contact, V_{oc} is

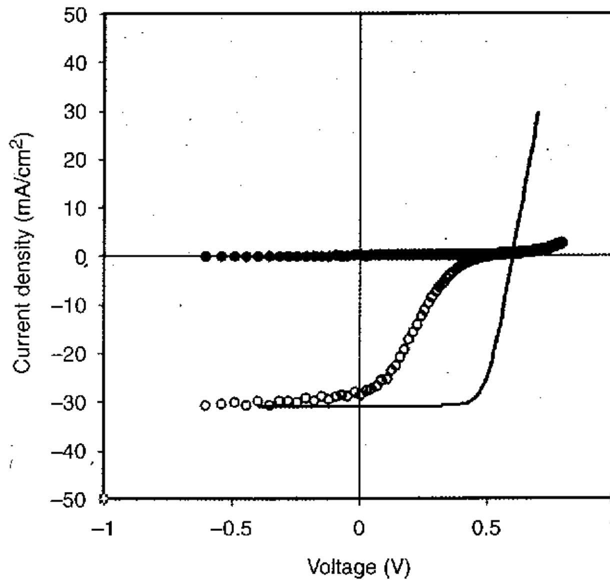

Figure 2. Typical J–V characterization of a SHJ solar cell with an S shape. Figure shows a dark J–V (solid circles), a S-shaped J–V (open circles), and a good SHJ cell J–V (line).

restored to ~0.680 V. This effect is important to avoid possible metal interdiffusion at the back contact and in constructing a cell with high V_{oc}.

The observation of low FF in SHJ cells can be attributed to the c-Si wafer, contact and junction resistances. Most reported FFs are in the range of 0.76–0.79, whereas the FF of a typical diffused cell is greater than 0.80 when using the same c-Si wafer for comparison. The loss in FF is believed to occur at the metal contact to the a-Si:H emitter and the back contact. At NREL, a high FF of greater than 0.80 was achieved when the front and back contacts were optimized. Thus, it is important to consider the conductivity of the doped layers, ITO conductivity and thickness of the layers.

The double-sided structure helps by increasing V_{oc}, but it often leads to a characteristic S-shaped J–V curve [41]. For example, if the thin native oxide is not properly removed, an S shape will appear in the J–V measurement. Figure 2 shows a typical J–V curve for such a cell. The S-shaped J–V feature can be attributed to many factors. Assuming the native oxide was properly removed, as mentioned earlier, it is possible that either the normal a-Si:H p-contact was not optimized for hole transport or an improper i-layer or p-layer caused this feature. The S shape is related to the potential barrier that blocks the carrier from moving into the p-layer. Experimentally, directly depositing the p-layer on the c-Si often avoids the S shape, but with a low V_{oc}. Therefore, optimization of the i- and p-layers is key to preventing the S shape while retaining the passivation layer. In other words, a new p-contact is required to perfect the SHJ solar cell.

Figure 3 shows an internal quantum efficiency (IQE) plot for a SHJ cell and passivated emitter rear locally diffused (PERL) cell to illustrate the possible cause of

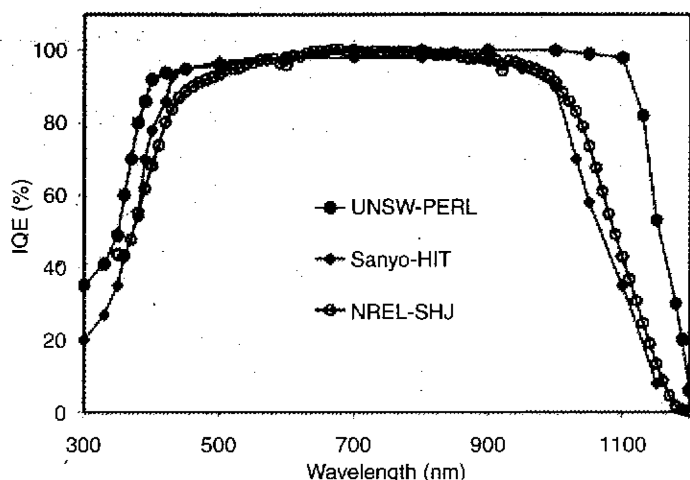

Figure 3. Comparison of internal quantum efficiency between SHJ cells and a high J_{sc} PERL cell.

the SHJ cell's low J_{sc} and a possible pathway to even higher efficiencies. Quantum efficiency data measure the cell's solar spectra response and has been widely used to diagnose problematic response regions. The figure shows IQE data for a PERL cell from the University of New South Wales [42], a HIT cell from Sanyo [19] and a SHJ cell from NREL [33]. Results show that Sanyo's HIT cell and NREL's SHJ cell have a similar IQE. However, both IQEs have a lower response in the infrared region – from 1000 to 1200 nm – compared to the PERL cell. This leads to a J_{sc} deficit of about 4 mA/cm^2. A record PERL cell has a J_{sc} of about 43 mA/cm^2 and the best HIT cell has a J_{sc} of 39 mA/cm^2. There is also some loss in the blue region, attributed to the absorption in the a-Si:H layers, especially the doped layer. A recent publication from Sanyo [1] describes a number of factors, including red response, necessary to increase the J_{sc}. Increased red response in the SHJ cell is another key area for further improving cell efficiency and ultimately reaching a target efficiency of more than 25% in combination with optimal voltage.

Does the SHJ solar cell experience the same rate of light-induced degradation as the a-Si:H solar cell? Many groups have tested the SHJ solar cell under prolonged light exposure [7,20,30], concluding that, unlike the a-Si:H cell, the SHJ cell does not exhibit light-induced degradation. Illumination causes defects to increase in a-Si:H materials. In SHJ cells, the a-Si:H *i*-layer was located inside the depleted junction region and is very thin. Light-induced defects are minimized due to the strong electric field and less absorption. This result is consistent with the present design of a-Si:H solar cells that use thinner *i*-layers to reduce light-induced degradation.

Some consideration is being given to using normal *p*-type c-Si wafers (0.5–2 ohm/cm in resistivity) with high O level in SHJ cells owing to the few percent of light-induced degradation related to the B–O complex. However, this degradation can be eliminated using low-level O c-Si wafers. In current production, only *n*-type c-Si

wafers are used in c-Si SHJ solar cells, as it is easier to obtain a long minority-carrier lifetime with *n*-type c-Si than *p*-type wafers.

4. Summary

The advantages of crystalline silicon heterojunction solar cells are as follows: (1) high V_{oc} and the potential for further improved cell efficiency, (2) a low-temperature power coefficient for more energy output throughout the year, and (3) a symmetrical structure and low-temperature process suitable for next-generation ultra-thin c-Si wafers. SHJ cells are also one of the mass production technologies that can produce more than 20% efficient cells. Ultimately, disordered amorphous silicon can be combined with ordered crystalline silicon to produce a high-efficiency solar cell.

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