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Plasma TEOS as an Intermetal Dielectric in Two Level Metal Technology

ABSTRACT

The use of plasma enhanced TEOS as an intermetal dielectric is discussed. Some of the electrical, mechanical, and structural properties required for its use in a submicron CMOS, two level technology are examined.

A simplified cross section of a two level metal technology is shown in Fig. 1. The quality of the intermetal dielectric film, D2, is a crucial factor in controlling the yield and reliability of such devices. The large development effort required to incorporate the dielectric into the process flow is shown by the many papers on this subject presented over the past six years at the annual Multilevel Interconnect Conferences[1]. If the deposited dielectric simply replicates the underlying topography (e.g., field oxide, gate, Al-1, etc.), then poor metal coverage will result at subsequent metallization steps. Microcracks or thinning in the Al-2 can then lead to long term reliability issues, e.g., decreased electromigration resistance.

Excessive time at high temperature during the dielectric deposition can lead to excessive hillock growth in the underlying Al-1 metallization. Such hillocks could become exposed during dielectric resist etchback planarization or during the via etch (if the oxide to resist selectivity is poor) and thus produce intermetal shorts. Even without exposing the hillocks, the dielectric could be thinned sufficiently to cause leakage or its eventual breakdown. This represents a long term reliability issue for Al-1 to Al-2 isolation. Dielectric films deposited by plasma enhanced chemical vapor deposition (PECVD) are preferred over low pressure CVD (LPCVD) for hillock reduction during deposition.

Voids in the dielectric between closely spaced Al-1 lines can lead to poor Al-2 coverage or to Al-2 to Al-2 stringers if Al-2 is insufficiently etched. The former situation would lower the device reliability while the latter would impact device yield. If the stringers were not continuous, there would be an increased likelihood of Al-2 to Al-2 leakage, again a reliability issue. The stringers in the void can be removed by an additional overetch in the Al-2 RIE step. However, there is generally poor

Al to photoresist selectivity in an aluminum etch. This fact, coupled with the severe topography of multilevel devices at this process step, can lead to exposure of the Al by excessive removal of the (initially) thin photoresist in the higher regions. Device yield or device reliability degradation can occur. [SiO.sub.2] films, derived from PECVD of [SiH.sub.4]/[N.sub.2]O films, are particularly prone to "bread loaf" profiles and thus void formation[2]. A simulation of a deposition process using SAMPLE[3], appropriate for [SiH.sub.4]/[N.sub.2]O, is shown in Fig. 2. Even at a modest aspect ratio of 0.33, e.g., a 0.5 [micro]m Al-1 thickness at a spacing of 1.5 [micro]m, a void can form in the film.

One can thus predict the properties of the dielectric required to avoid the aforementioned problems. The film must deposit void-free and smoothly across the severe underlying topography. The smoothing feature of the deposition modifies the abrupt aspects of the topography. Coupled with all the topographic requirements, the film must satisfy stringent mechanical and electrical quality requirements. It must further exhibit low electrical leakage, low mobile ion and low heavy metal content, and be stable over time with respect to moisture.

The [SiO.sub.2] film generated from an rf plasma in tetraethoxysilane (TEOS) and oxygen can be made to satisfy these film requirements[4]. Although the main application of plasma enhanced TEOS (PETEOS) is as the intermetal dielectric in multilevel metal technologies, the film is also widely used as the oxide for LDD spacers on gate structures. As a doped film, PETEOS can be used as the dielectric, D1, between the gate polysilicon and the first metal interconnect.

PETEOS films show better conformality and less tendency to develop bread loaf profiles and voids than films from [SiH.sub.4]/[N.sub.2]O. The increased tendency towards surface diffusion shown by LPCVD TEOS films[2] seems to also apply to PETEOS films. A SAMPLE[3] simulation appropriate for PETEOS is shown in Fig. 3. The diffusivity factor is increased in Fig. 3 compared to that in Fig. 2 and, as a consequence, fewer reentrant profiles occur and void formation is less apparent. However, as seen in Fig. 3, voids still form at an aspect ratio of about 0.5 (for a 0.5 [micro]m step).

Several approaches have been described for a satisfactory intermetal dielectric process at submicron technology sizes[1]. The ultimate flat surface can be obtained by planarization methods. Widely used today are resist etchback methods[5], but other methods such as sacrificial etchback of [B.sub.2][O.sub.3][6] or mechanical polishing[7] have recently received much attention for advanced applications. The disadvantage of such planarization approaches is the formation of vias with different oxide thicknesses and the consequent difficulties in covering the various aspect ratio contacts with adequately sputtered metal. Full planarization methods will likely be best suited for advanced devices using tungsten plugs.

Spin-on glass has been used in conjunction with silane-based or TEOS-based plasma oxide. [1,8,9]. Much work has been reported on obtaining the correct deposition and curing sequence and developing the appropriate etchback method so as to avoid such phenomena as poisoned vias and interface grooves[9].

Another general approach to a satisfactory intermetal dielectric is to use PETEOS without planarization. Here, however, smoothing methods are required.

PETEOS as an Intermetal Dielectric

PETEOS technology and process characterization have been discussed previously[10-14]. The required properties of PETEOS for use as a dielectric-2 level metallization include:

* Good electrical characteristics * Good mechanical properties * Smooth surface over topography at all spacings including

the zone of concern[15] * Void-free fill at minimum design rule spaces * Elimination of low density regions.

Mechanical and Electrical Properties

Mechanical considerations important for films include minimization of particulate levels, pinhole density, hillock density, and hillock heights. Films must also possess low compressive stress and experience zero water absorption with time. This latter may be monitored by FTIR after the film is boiled in water ([H.sub.2]O or [D.sub.2]O). A good quality PETEOS film does not pick up appreciable quantities of moisture over time[12]. Hillock heights [is less than] 1000 A[Angstron] on 5000 A[Angstron] thick aluminum have been reported after the deposition of a low temperature (330 [degrees] C, low deposition rate (| 500 A[Angstron]/min) PETEOS film[12,13]. Even for a 400 [degrees] C film, the hillock height was less than 2000 A [Angstron][12]. Stress levels, generally compressive, of less than 1 x [10.sup.9] dynes/[cm.sup.2] have been reported[12] for a wide range of thicknesses.

Response surface methodology was used to optimize film properties, with particular focus on deposition rate, uniformity, and density. These factors also represent a good means of measuring the stability of the process. Density is frequently monitored by the wet etch rate of the PETEOS in HF or in buffered HF solutions. A good quality PETEOS film etches at 100 A [Angstron]/min in 100:1 [H.sub.2] 0:HF at 25 [degrees] C. For comparison, a thermally grown oxide, a thermal ozone TEOS film[15], and a poor quality oxide (e.g., a low temperature downstream oxide) etch at 40, 700, and [is greater than] 2000 A [Angstron]/min, respectively.

Electrical properties of the film were monitored by the triangular voltage sweep method (TVS) to detect leakage, [Na.sup.+][16] and [H.sup.+] contamination[17]; CV to determine leakage, dielectric constant, flat band shift, and conductivity[12,16]; and by high temperature dc bias aging, transistor aging, and Al-1 to Al-2 leakage[16].

Sodium levels in the PETEOS film are low and values of [is less than] 2 x [10.sup.9] [cm.sup.-2] have been reported[12]. The films are deposited at low temperature without gettering agents. Carbon levels of about 0.2 atomic percent are typical in plasma deposited TEOS[18]. Film resistivity [is greater than] [10.sup.18] ohm-cm has been measured to 300 [degrees] C[13] and is comparable to that of thermal oxide. A much more important electrical consideration for PETEOS concerns the increased presence of sodium after the etchback step.

Topography and Morphology

As devices shrink in lateral dimensions, increase in interconnect complexity, but maintain vertical thickness, topography issues increasingly dominate process design for an advanced VLSI interconnect technology[14]. Depth of focus limitations for fine line patterning, linewidth control over severe topography, step coverage of sputter deposited films, and etch residues (or stringers) along the edges of steep topography all highlight the need for surface smoothing.

One feature of ASIC and microprocessor designs is that Al-1 to Al-1 spacings occur over a wide range, from a minimum at the design rule limit to very large spacings ([is greater than] 10 [micro] m). It is important, therefore, to obtain suitable oxide coverage for dielectric-2, i.e., void-free at small spaces, elimination of severe cusps at intermediate spaces (| 2.5 [micro] m), and smooth coverage at wider spaces. The next metal layer will then have good step coverage at all spacings. The overall strategy for the fill sequence involves two steps:

1) The formation of a more favorable aspect ratio for the metal-metal fill at the smallest metal-metal spacings. The necessary sequence could involve intermediate spacer formation in the PETEOS via RIE (Reactive Ion

Etching) or MERIE (Magnetically Enhanced RIE), argon faceting of an intermediate oxide, or the sloping of the metal itself prior to PETEOS deposition. 2) The formation of a smooth contour at wider spaces (including the zone of concern[15]) by the use of thick films ([is greater than] 2 [micro] r), anisotropically etched back to suitable thicknesses (| 0.9 [micro] m)[12,13,15,19-21].

The need for improvement in the aspect ratio can be seen in SAMPLE contour plots of Fig. 3, which show the evolution of film contours suitable for a PETEOS film over a 0.5 [micro] m metal at 1 [micro] m spacing. At small spaces, voids will form.

Figure 4 shows the actual coverage of PETEOS over 0.5 [micro] m high Al lines at various spacings representative of an ASIC device. Voids form at a spacing of [is less than] 1.25 [micro] m for a 0.5 [micro] m Al line. Another interesting aspect of PETEOS deposition is shown in Figs. 3 and 4. At wider spacings than the ones where real voids form, i.e., regions with a total absence of material, there exist low density regions in the glass. These low density regions result from the fact that the advancing film fronts from the sides of the two aluminum runners form a worsening aspect ratio[22]. Eventually the two advancing fronts coalesce and the final thicknesses prior to the sealing of the seam are not subjected to the same surface migration and ion bombardment effects[23] experienced by film growth in the other regions. These regions along the seam have lower density than the bulk and etch much faster in dilute HF and in dry etch chemistries.

Figure 4 shows a PETEOS film deposited in a series of 16 x 1250 A [Angstron] steps which have been decorated in HF. Voids and areas of low density are clearly indicated in these figures. To obtain this contoured appearance in the PETEOS, the plasma deposition was merely interrupted after each 1250 A [Angstron] by switching the rf off. There is sufficient difference between the film deposited at the end of the rf sequence and that deposited at the beginning to show the interface when the sample is etched for 3 seconds in BHF (10 [NH.sub.4] F:1HF).

The deleterious impact of the low density region is shown in Fig. 5 where a single 2 [micro] m deposition has been etched back to 0.8 [micro] m. Following the dry etch (and also wet etch) grooves are opened in the low density regions. The metal deposition and patterning over these grooves present reliability and device yield problems. Even though the coverage of D2 at wider spaces is smooth, grooves due to real voids and low density regions form at smaller spaces. Therefore, a single deposition and etchback are not possible for a reliable device[19].

PETEOS Intermetal Oxide Schemes

Three methods were evaluated for the 0.9 [micro] m technology to eliminate voids, to reduce low density region formation, and to achieve smooth coverage at wider spaces: 1) formation of a spacer intermediate within the film by RIE or MERIE, 2) a sputter etchback, and 3) the use of sloped metal[19]. They all improve the aspect ratio of the opening by sloping the intermediate film, thereby reducing void and low density region formation within the space after a subsequent oxide deposition. All three approaches were then followed by a thick deposition of PETEOS ([is greater than] 2.0 [micro] m) and an RIE etchback step.

The effectiveness of a slope change in the 90 [degrees], higher aspect, small space region can be seen by computer simulation. Figure 6 compares a SAMPLE simulation of PETEOS coverage for Al-1 profiles from 105 to 60 [degrees]. Voids form with the more vertical profiles but not when deviation from vertical is greatest. One can picture a spacer formed in the intermediate oxide on a vertical metal as performing the same function as that of the sloped metal.

For the spacer approach[24] the slope of the spacer is important and is controlled by the deposition and etch thickness as well as the etch process. Initial depositions of 6 to 12 kA [Angstron] and etchbacks to 2 kA [Angstron] were studied for a wide range of etch conditions. Subtle changes in profile were seen as the etch conditions were varied. Profiles with some vertical components were formed at high pressure and with oxygenated chemistries. Such profiles still led to void formation when the thick oxide film was deposited as shown in Fig. 7a (10kA [Angstron] (multiple) - 8kA [Angstron] - 14kA [Angstron]). However, the void is now within the final D2 and does not constitute a reliability issue. The vertical slope in the intermediate spacer was removed by increasing the physical sputter component, i.e., by decreasing the pressure and increasing ion flux. The optimized spacer shape and the lack of void formation are shown in Fig. 7b, where a sequence of 10 kA [Angstron] deposition, 8 kA [Angstron] RIE etchback, 25 kA [Angstron] deposition, and 18 kA [Angstron] RIE etchback was used.

The optimum spacer was formed primarily by a reactive ion etch but with a physical sputter contribution[24] so as to achieve a sloped shape without a vertical foot. An alternative approach to sloping the intermediate profile is to facet the initial PETEOS deposition by purely physical sputtering[25]. This sequence consists of a 10 kA [Angstron] deposition, an argon sputter, a thick PETEOS deposition, and an RIE etchback to | 9 kA [Angstron]. The sputter etch time is chosen to eliminate void formation in the second PETEOS deposition. The situation before the

RIE etchback is shown in Fig. 8. The 10 kA [Angstron] deposition in this figure was used to cap the structure so as to identify the void and allow measurement of the profile angle and the vertical and lateral sputter rates.

The final approach investigated for obtaining a void-free fill was to slope the profile of the Al-1 by a sidewall growth mechanism[14,26]. Figures 4, 9, and 10 show PETEOS growth contours for a 2 [micro] m film over Al-1 sloped at 101 [degrees], 82 [degrees], and 64 [degrees], respectively. The lack of voids and smooth contours at all spacings are clearly evident at 64 [degrees]. At 82 [degrees] the coverage is less smooth (more of a chance of cusp formation) and a low density seam is evident. For a 101 [degrees] reentrant profile, voids form and steep profiles are seen at intermediate spacings. The main advantage of the sloped aluminum approach is the necessity of only a single, thick, PETEOS deposition step and only one RIE etchback step. Disadvantages, such as the need for resizing masks, assessing particular behavior, and evaluating electromigration and corrosion resistance of the sloped Al-1 have been considered elsewhere[19]. The approach has been applied to a 1.25 [micro] m technology[14].

One very important aspect of the etchback sequence chosen to achieve a smooth, although not planarized, dielectric is that of film contamination. Heavy metal contamination is best detected with SIMS analysis. In the SIMS method many of the important heavy metal contaminants are masked on an oxide film by the silicon isotopes, [Mathematical Expression Omitted] and [Mathematical Expression Omitted] interference peaks. Thus it is hard to detect [Mathematical Expression Omitted] in the presence of [Mathematical Expression Omitted]. Analysis could, however, be done on alternative substrates, e.g., silicon or aluminum. Heavy metal contamination can be reduced or eliminated by careful selection of the etch chamber components.

Sodium contamination in the etchback film is a much harder problem to eliminate. The level of sodium contamination can be studied by SIMS or the TVS method. Thoma et al.[16] discussed the influence of sodium contamination in the PETEOS of a 1.25 [micro]m two level metal technology. Sodium contamination within the PETEOS moved with time and bias. This charge movement created image charges, in the silicon under the field oxide, which led to [n.sup.+]-to-[n.sup.+] leakage[16].

One of the primary sources of sodium in the PETEOS was found to be from the etchback step. Studies on a variety of batch and single wafer reactors from three vendors showed sodium levels of [10.sup.12] to [10.sup.13] [cm.sup.-2] in the oxide after RIE etchback or physical sputtering[16]. These sodium levels were confirmed by both TVS and SIMS measurements. The reactors had been used routinely with photoresist covered wafers in contact etches and it was reasoned that the sodium came from photoresist and sodium based developers[16]. The contamination derived from dedicated etchback systems is better and sodium levels of [is less than or equal to] 2 x [10.sup.11] [cm.sup.-2] are achievable for RIE etchback and argon sputter. Thoma et al.[16] reported the need to add a brief HF treatment after etchback steps in nondedicated reactors to remove at least the top 100 to 200 A of the surface.

Summary

Plasma enhanced TEOS has been shown to be a suitable intermetal dielectric in a production, 0.9 [micro]m CMOS, two level metal technology. Suitable film and control characteristics required to achieve desired device performance have been described and problems inherent in the technology have been discussed. Troublesome voids and low density regions caused by deposition limitations at smaller spacings have been eliminated by three process sequences. The modification of an intermediate PETEOS contour by spacer formation, sputter etch, or sloped Al-1 combined with a thick deposition and RIE etchback step has been applied to a submicron, two level metal device. The method chosen for dielectric-2 must offer the best combination of cost, yield, and reliability. [Figure 1-10 Omitted]

References

[1]Proc. Intl IEEE VLSI Multilevel Interconn. Conf., (VMIC) 1984-1989. [2]A.C. Adams, "VLSI Technology," S.M. Sze, ed., 2nd edit., chap. 6, p. 233 (1988) [3]SAMPLE, Electronics Research Laboratory, Dept. of Elect. Eng'g. and Comp. Sci., UC Berkeley, 1982. [4]L.J. Olmer et al., Proc. ECS, Philadelphia, PA, May 1987. [5]L.de Bruin, J.M.F.G. van Laarhoven, Proc. 5th VMIC IEEE, p. 404 (1988) and references therein. [6]J. Marks, K. Law, D. Wang, Proc. SPIE Symp., vol. 1188, to be published. [7]For a general discussion see ref. 2, p. 41, and references therein. [8]S.N. Chen, et al., Proc 5th Intl IEEE VMIC, p. 306, and references therein (1988). [9]C. Chiang, et al., Proc. 4th Intl IEEE VMIC, p. 404 (1987); D.L.W. Yen, G.K. Rao, Proc. 5th Intl IEEE VMIC, p. 85, and references therein (1988). [10]M.L. Chen, et al., IEDM Tech. Dig., p. 50 (1986). [11]L.V. Tran, et al., Proc. IEEE Custom Integrated Circuits Conf., Rochester, NY, p. 46 (1986). [12]M.J. Thoma, et al., Proc. 4th IEEE VMIC, p.20 (1987). [13]G.W. Hills, et al., Proc. 5th IEEE VMIC, p.35 (1988). [14]C.A. Fieber, et al., Proc. 6th IEEE VMIC, p. 55 (1989). [15]M. Kawai, et al., Proc. Intl IEEE VMIC, p. 419 (1988). [16]M.J. Thoma, et al., TMS Conf., Las Vegas, Feb. 1989. [17]N. Lifshitz, G. Smolinsky, J. Electro Chem. Soc., vol. 136, p. 2335 and references to TVS therein (1989). [18]S. Ngyuen, et al., Proc. 9th Intl Symp. Plasma Chemistry, IUPAC, Pugnochiuso, Italy, p. 1134 (1989);

A.S. Harrus, G.W. Hills, M.J. Thoma, 9th Intl Symp. Plasma Chemistry, IUPAC, Session XXVIII (1989). [19]G.W. Hills, A.S. Harrus, M.J. Thoma, Proc. SPIE Symp., vol. 1185, to be published. [20]A. Bergendahl, D. Harmon, ibid. [21]J. Perchard, et al., ibid. [22]A.S. Harrus, G.W. Hills, unpublished. [23]P. Hey, et al., Solid State Technology, this issue. [24]D.P. Hambler, A. Cha-Lin, J. Electrochem. Soc., vol. 135, p. 1816 (1988); S.H. Dhong, E.J. Petrillo, ibid., vol. 133, p. 389 (1986). [25]H. Kotani, et al., J. Electrochem. Soc., vol. 130, p. 645 (1983). [26]T. Arikado, et al., IEDM Tech. Dig., p. 54 (1986).

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