2001 International Symposium on Microelectronics

The integration of RF passives using thin-film technology on high-ohmic Si in combination with thick-film interconnect

Joost van Beek, Marc van Delden, Andre Jansman, Arjen Boogaard, Anton Kemmeren
Philips Research, Prof. Holstlaan 4, 5656AA Eindhoven, The Netherlands
Phone: ++31-40-2742141, Fax: ++31-40-2743352, E-mail: j.t.m.van.beek@philips.com

Nick Pulsford, Arnold den Dekker
Philips Semiconductors, Gerstweg 2, 6534AE Nijmegen, The Netherlands
Phone: ++31-24-3522612, E-mail: nick.pulsford@philips.com

Abstract

A technology platform is presented for the integration of passive components in RF circuits. The platform consists of a thin film process on high-ohmic Si combined with thick film technology. The thin film process is used for sections in RF circuit where a relatively high degree of component accuracy is needed, e.g. for impedance matching. The thin film process uses $\rho > 4\ k\Omega.cm$ *Si substrates on which IC compatible layers, such as sputtered Al and CVD silicon nitride and oxide, are deposited and structured. This process is capable of fabricating inductors and capacitors with a performance that does not differ significantly from inductors and capacitors processed on an insulating substrate, such as glass and alumina. Inductors with a Q-factor between 40 to 60 and capacitors with an ESR* $< 200\ m\Omega$ *in the 1-2 GHz frequency range are realized. Using the thin film process in combination with thick film interconnect a* $2\ \Omega$ *to* $50\ \Omega$ *impedance matching circuit is realized with an insertion loss of 0.8 dB at 900 MHz.*

Keywords: RF, passive integration, thick-film, thin-film

I. Introduction

Integration of passive components in RF front-end modules is one of the main enablers for module miniaturization. Integration of RF passives can be realized using several technologies, such as low-loss laminate, thick film on alumina, plated bonded copper, LTCC, and thin film technology. The commercial success of these technologies is mainly determined by three factors:

- Electrical performance
- Cost of manufacturing
- Time-to-market

The electrical performance of an integration technology can be split into its ability to integrate different kinds of passives and the component accuracy by which it can make these passives. For example, plated bonded copper, LTCC, and laminate technology can integrate only inductors and low value capacitors with limited accuracy. Other technologies, such as thick film on alumina and thin film technology, can integrate both inductors, high value capacitors, and resistors.

Often there is a trade-off between cost of manufacturing and electrical performance for a certain technology. For example, thin film technology offers superior layout accuracy over other technologies, but at a high price. Thick film technology on the other hand, is a relatively low cost technology, but with a limited layout accuracy due to the use of screen printing and firing techniques. Therefore, the optimal technical solution for the integration of RF passives should be sought in a combination of different interconnect technologies.

The third aspect determining the success of a new technology is the time-to-market. The market for wire-less devices, such as mobile phones, is a high-volume market with short product cycle times. With the introduction of a new technology attention should therefore be paid to the process compatibility to existing manufacturing infrastructure.

In this work, a technology platform is presented in which the electrical performance, cost of manufacturing, and the process compatibility to existing IC manufacturing infrastructure are considered. A five-mask thin film process on high-ohmic Si is combined with thick film interconnect technology. The thin film process is used for sections in the RF front-end where a high level of component accuracy is needed, e.g. for impedance matching. Less critical parts of the RF front-end are made using the more cost-effective thick film technology. The thin film process uses Si substrates on which IC process compatible layers, such as sputtered Al and CVD silicon nitride and oxide, are deposited and structured. A manufacturing base for this 3 metal layer passive integration process, called PASSI3, is therefore readily available. Together with the available manufacturing base for thick film technology, a short time-to-market for this technology platform is made possible.

In this paper, a description of the PASSI3 process is given. Data are presented showing the RF performance of individual thin film components. The performance of the PASSI3 passives is compared with thin film passives processed on insulating substrates, such as glass and alumina. An impedance matching network in a GSM power amplifier has been built to demonstrate the PASSI3-thick film technology platform.

II. Thin Film Technology Outline

In the PASSI3 process, high-ohmic silicon wafers with a specific resistivity of $\rho > 4$ kΩ.cm are used as a carrier for the fabrication of inductor-capacitor networks. High-ohmic Si is used in order to limit the dissipation of RF power that is coupled into the substrate. The Si substrate is isolated by a layer of thermally grown oxide. Two relatively thin sputtered Al layers separated by a PECVD SiN_x dielectric are used for defining the capacitors. The process continues with the deposition of a PECVD SiO_x decoupling layer. This layer electrically decouples the capacitor from the Al top metallization, which is deposited next. The 5 μm thick Al top metallization is used for defining high-Q inductors. The process ends with the deposition of a PECVD SiN_x scratch protection layer. A technology cross section is shown in Fig.1.

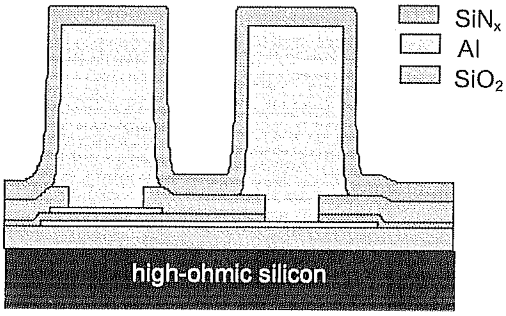

Fig.1 Technology cross-section of the PASSI3 process. The bottom and middle Al layers define the capacitor electrodes using the SiN_x as a capacitor dielectric. The 5 μm thick top Al layer defines low loss, high-Q inductors and interconnect.

III. Performance of Capacitors and Inductors

For individual capacitors and inductors made using the PASSI3 process the RF performance has been measured. In Fig.2 the Q-factor of a 3 nH single-turn inductor processed on different substrates is shown. The outer diameter of the inductor is 1.3 mm and the linewidth of the inductor turn is 100 μm. From Fig.2 it can be seen that the Q-factor for the PASSI3 inductor ranges from 40 to 60 in the GSM-DCS frequency range (1-2 GHz). These values are sufficiently high for RF front-end applications.

For comparison, Q-factors of the same inductor layout but processed on an insulating substrate and a thermally oxidized, low-ohmic Si substrate are shown. The insulating substrate consists of 97% alumina with a dielectric constant of $\varepsilon_r = 9$. It can be seen that the Q-factor of the PASSI3 inductor does not differ significantly from the same inductor processed on alumina. When the same inductor is processed on 9-16 Ω.cm *n*-type Si, which is a substrate resistivity most commonly used in BiCMOS processes, the Q-factor is much lower than the one processed on high-ohmic Si. For low-ohmic silicon it is clear that the substrate induced losses limit the Q-factor.

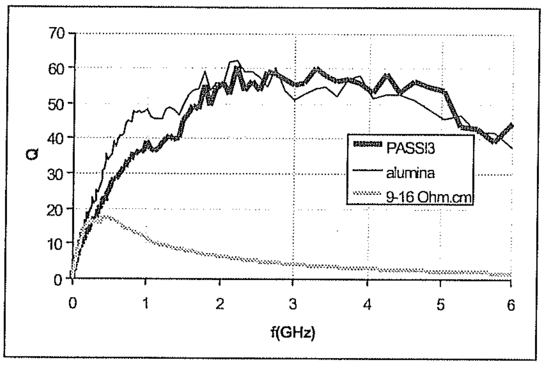

Fig.2 Q-factor as a function of frequency for a single-turn 3 nH inductor processed using the PASSI3 process. For comparison the same inductor is processed on 97 % alumina and 9-16 Ω.cm oxidized *n*-type Si.

Fig.3 shows the equivalent series resistance (ESR) of a 3 pF and a 10 pF capacitor made using the PASSI3 process. It is shown that in the GSM-DCS frequency range the ESR is below 200 mΩ. For comparison, also the ESR is plotted for the same capacitors processed on a glass substrate. It can be seen that at frequencies >1 GHz there is no significant difference in ESR between PASSI3 capacitors and capacitors processed on glass. The ESR of the 10 pF capacitors is slightly larger than that of the 3 pF capacitors. This is attributed to a larger electrode area and therefore a higher electrode resistance for the 10 pF capacitors.

The steep increase of the series resistance of the PASSI3 capacitors at low frequencies is caused by a parasitic parallel resistance through the Si substrate. This substrate resistance is equivalent to a frequency and capacitance dependent series resistance, as is schematically shown in Fig.4. For low capacitor values the increase in ESR shows up at higher frequencies, see Fig.3. It can be seen that the ESR for the 3 pF PASSI3 capacitor starts to increase around 1 GHz. PASSI3 capacitances much smaller than 3 pF will show a significant higher ESR in the GSM-DCS frequency bands compared to the same capacitor processed on glass.

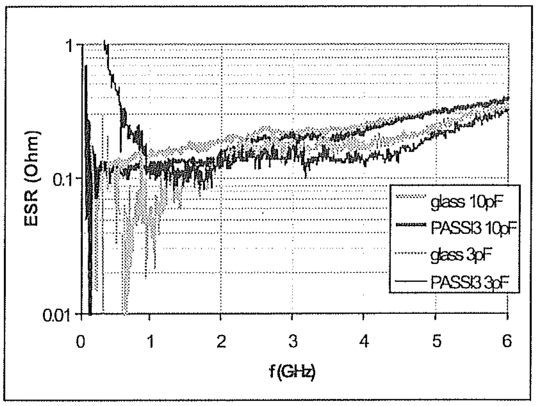

Fig.3 Series resistance of a 3 pF and 10 pF PASSI3 capacitor as a function of frequency compared to the same capacitors processed on glass.

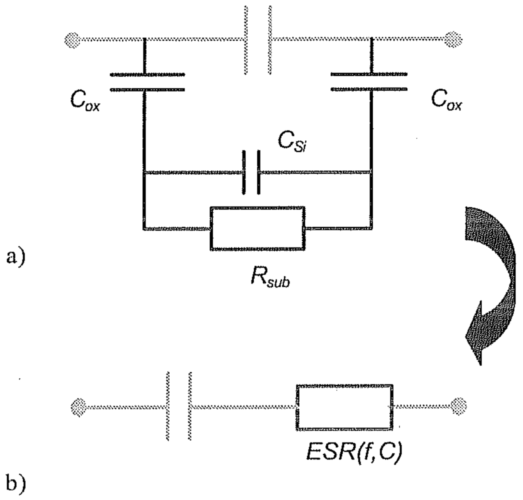

Fig.4 a) Equivalent circuit of a capacitor processed on a semi-conducting substrate. Part of the RF power is coupled into the substrate through the thermal oxide, C_{ox}. Part of this power is subsequently dissipated in the substrate by the substrate resistance, R_{sub}. b) The parasitic substrate resistivity R_{sub} is equivalent to a frequency and capacitance dependent series resistance, *ESR(f,C)*.

IV. Impedance Match Circuit Using a Combination of Thin Film on High-Ohmic Si and Thick Film Technology

A 900 MHz impedance matching network as part of a GSM power amplifier module is made using a PASSI3 die mounted on a thick film ceramic substrate, see Fig.5. The impedance is transformed from to 2 Ω to 50 Ω using a four stage LC ladder network. The four capacitors and small inductances connecting the capacitors are realized on the PASSI3 die. A larger inductor at the output side of the impedance matching network is realized on the thick film ceramic substrate. The distribution of passives between the PASSI3 die and the thick film substrate gives a good illustration of this technology platform.

The impedance transformation network has a measured insertion loss of 0.8 dB. The rejection of 2nd and 3rd harmonics is better than 20 dB.

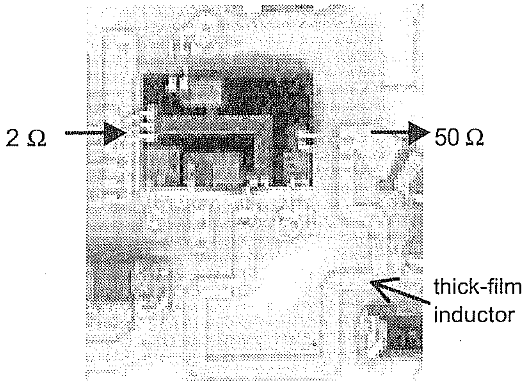

Fig.5 A close-up of a RF front-end power amplifier module showing the 2 Ω to 50 Ω impedance matching network realized using a PASSI3 die mounted on a thick film ceramic substrate.

V. Conclusion

The integration of passive components using a combination of thin film technology on high-ohmic Si and thick film interconnect on ceramic is demonstrated. The thin film PASSI3 process is used for sections in the RF front-end where a high level of component and layout accuracy is required, in this case for impedance matching. Less critical sections are realized using the more cost effective thick film technology.

Using the thin film PASSI3 process, Q-factors between 40 and 60 in the 1-2 GHz frequency range are realized for a single-turn 3 nH inductor. A series resistance below 200 mΩ for frequencies in the 1-2 GHz range is obtained for a 3 pF and a 10 pF capacitor. The performance of these passives processed on high-ohmic silicon does not differ significanlty from the same passives processed on an insulating substrate at operating frequencies above 1 GHz.

A 2 Ω to 50 Ω impedance transformation network is realized demonstrating the thick film-PASSI3 platform. The network has an insertion loss of 0.8 dB at 900 MHz and a higher harmonic rejection better than 20 dB.

Acknowledgement

The authors would like to thank the people of Philips Semiconductors Nijmegen, Business Line RF modules for their valuable contributions. Special thanks to Stephane Bertonnaud, Jeroen van der Bijl, Johan Dijkhuis, Roene de Koning, Jan-Willem Lobeek, Frans Meeuwsen, Kirsten Rodle, Atanas Pentchev, Lenhard van Teeffelen, Arjan Tuinhout, and Paul van der Wel. Also special thanks to Ronald Dekker and Eugene Timmering from Philips Research.