Thermal characterization of vertical silicon nanowires

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Arrays of vertically aligned silicon wires of 250 nm–4 μm in diameter were fabricated in a top–down process using photolithography and deep reactive ion etching at cryogenic temperatures. Using the 3-omega method, thermal conductance of vertical silicon nanowires, i.e., nanopillars, was measured immediately on-chip without the need of breaking off single wires and mounting them into a special testing device. The Seebeck coefficient was measured with 2-mm^2 arrays of pillars of 260 nm in diameter, which were pressure-joined with bulk chips for testing. Testing was performed in the temperature range between 50 and 470 °C at applied temperature gradients of up to 190 °C. We found a reduction of the thermal conductivity to less than 30% of the bulk silicon, confirming that arrayed vertical nanowires fabricated in an economical top–down process can strongly promote silicon as a thermoelectric material.

I. INTRODUCTION

Research on semiconductor nanowires has been dramatically increased over last two decades.[1] Among a variety of fields, nanowire-based thermoelectrics has emerged, which is caused by a significant reduction of thermal conductivity κ in these structures with respect to the bulk. Strong interaction of the phonons with the surface is the origin of this diameter-dependent and surface morphology–related effect, which can amount up to a two-orders-of-magnitude reduction of κ of bulk silicon.[2–4] Silicon offers several advantages over the standard thermoelectric materials, Bi_2Te_3 and PbTe, which can be essential to overcome the present restriction of thermoelectrics to niche applications. For waste heat recovery, e.g., from combustion engines,[5,6] high-temperature stability, environmental compatibility, safe medium- to long-term availability, and ongoing price reduction are mandatory, which is provided by silicon. Basic research on the thermoelectric (TE) properties of silicon nanowires is ongoing, but so far has been limited to single elements. However, nanowire-based thermoelectric generators will require a dense arrangement of nanowires in parallel to provide the necessary output power, e.g., for maintenance-free electronics or sensorics.

With respect to economical fabrication of nanopillar (NP) arrays, top–down fabrication using photolithography and deep reactive ion etching (DRIE) followed by thermal oxidation have been developed, which may be preferable over bottom–up approaches based on self-assembling.[7–9] For packaging into thermocouples, vertically aligned nanowires, i.e., nanopillars (NPs) of both *n*- and *p*-type doping and having uniform diameter and length, are required. Figure 1 shows a schematic of a thermocouple comprising *n*- and *p*-doped NP arrays joined using a high-temperature-stable silver sintering process.[10]

The thermal properties of nanowires are conventionally measured by heating at one end and sensing at the other using thermally isolated microfabricated heating and sensing areas or by heating across suspended wires joined integrally between large thermal contacts.[11,12] For TE devices based on NP arrays, however, these approaches are not applicable. Therefore, in this study, we use a technique based on the 3-omega method as recently reported for vertically aligned carbon nanotubes.[13] For characterizing single pillars, a Wollaston wire probe on a nanopositioning stage in a scanning electron microscope (SEM) was used. Furthermore, we address the thermal characterization of NP arrays via Seebeck voltage measurements in an extended temperature range up to 460 °C.

II. FABRICATION OF NANOPILLARS

Silicon pillar arrays of various diameter and height were fabricated using deep reactive ion etching (DRIE) with SF_6/O_2 at cryogenic temperatures.[9] Standard optical lithography was used for patterning a resistent layer into circular discs, which served immediately as the etch mask, i.e., hard masks were not required. As a result of underetching, the resulting pillar diameters were smaller than the masking disc diameters. Typical SEM photographs of realized silicon pillar arrays of different diameter, height, and shape are shown in Figs. 2(a)–2(c). From the enlarged view of a pillar sidewall edge in Fig. 2(d), a surface roughness of a few nanometers can be estimated.

For basic studies, the NP diameter was further reduced by thermal oxidation and subsequent oxide stripping. For TE devices this procedure may not be efficient since the fraction θ_{NP} of the device cross-sectional area covered by

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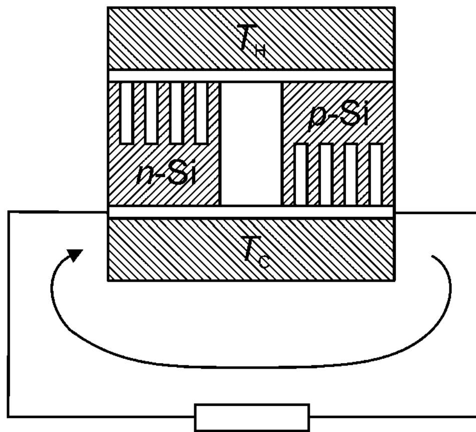


FIG. 1. Schematic configuration of a nanopillar-based thermocouple operated as a thermoelectric generator.

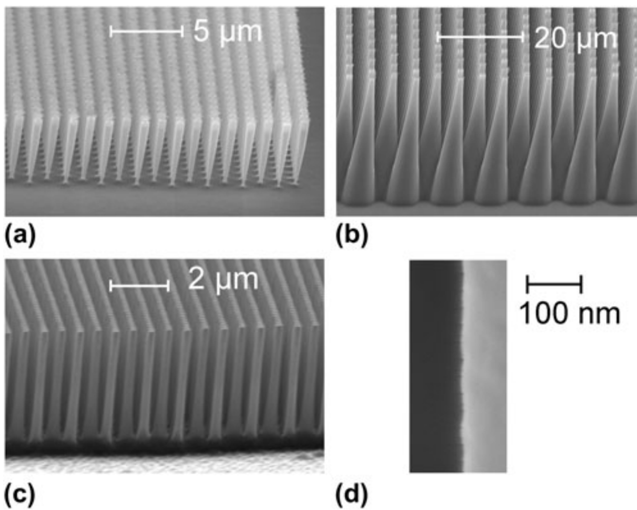


FIG. 2. Scanning electron microscope (SEM) photographs of deep reactive ion etching-fabricated pillar arrays (a) inverted frustum, top diameter = 0.7 µm, l_{NP} = 6 µm; (b) frustum, top diameter = 1 µm, l_{NP} = 30 µm; (c) cylinder, diameter = 0.2 µm, l_{NP} = 6 µm. In (d), the sidewall surface of a typical pillar is displayed at large magnification.

NPs, i.e., the current-carrying area, is reduced. In Table I, the geometrical dimensions of NPs are given, which were realized using the described top–down process.

III. THERMAL CHARACTERIZATION OF SINGLE PILLARS

A Wollaston wire–based 3-omega setup was used to measure the thermal conductance of the realized silicon pillars.[14,15] Figure 3(a) shows a schematic representation a Wollaston-wire probe over a silicon pillar array mounted on a nanopositioning stage (Kleindiek MM3A-EM, Reutlingen, Germany) in an SEM (Leica S360, Oberkochen, Germany). Wollaston-wire probes were fabricated from Pt wires of 5.8 µm in diameter having an Ag cladding. The Ag cladding was removed from Pt core over a length of

TABLE I. Geometrical dimensions of silicon pillars realized using top–down fabrication.

	DRIE	DRIE, oxidation, and stripping
Diameter (nm)	200–4000	174
Density (10_8 cm^{-2})	0.04–6	
Height (µm)	1–30	27
Aspect ratio	2.5–30	>180

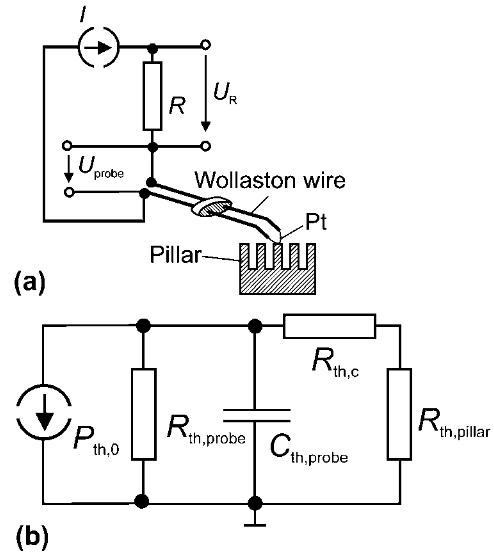


FIG. 3. Wiring of (a) Wollaston-wire-based 3-omega setup for thermal measurements with pillars and (b) simplified equivalent thermal circuit diagram of Wollaston-wire-based 3-omega setup for thermal characterization of pillars.

250 µm using wet etching. This part of the probe served as the heating element and the thermometer for the 3-omega measurements. It had a resistance of $R_{Pt} = 1\ \Omega$, which was much less than the bias resistor $R = 100\ \Omega$ through which the current I of a lock-in amplifier (Perkin-Elmer 7265, Wokingham, UK) was supplied to the probe. The temperature increase of the probe was then related to the in-phase 3-omega component of the amplitude U_{probe} of the voltage drop over the probe according to Refs. 14–16:

$$\Delta T = 2\frac{U_{probe}R}{U_R R_{Pt} \times TCR_{Pt}} \quad , \tag{1}$$

where $U_R = 2.5$ V as defined in Fig. 3(a) and R_{Pt} and $TCR_{Pt} = 3.9 \times 10^{-3}$/K denoting the Wollaston wire resistance and the temperature coefficient of resistivity of platinum, respectively. Typical values of the temperature oscillation amplitude were around $\Delta T = 1$ K, corresponding to a heat flux around 500 W/cm^2 dissipated into a 10-µm long pillar.

Figure 3(b) shows a simplified equivalent thermal circuit diagram of the measuring circuit. $R_{th,probe}$, $R_{th,pillar}$, and $R_{th,c}$ denote the thermal resistances of the probe, the nanopillar, and the contact to the NP, respectively. $P_{th,0}$ is the thermal

input power and $C_{th,probe}$ is the heat capacitance of the probe. Contributions to heat storage by the nanopillar and its contact are neglected in the considered frequency range much below 100 kHz. Considering the probe as a semi-infinite medium, we have $R_{th,probe} \sim C_{th,probe} \sim 1/\omega^{-1/2}$.[13] The temperature oscillation related to the in-phase 3-omega voltage, which was measured using the Wollaston probe, was assumed to be proportional to the real part of the thermal impedance of the equivalent circuit in Fig. 3(b).

The Wollaston wire probe was mounted on a nano-positioning stage on a SEM and arranged over a silicon pillar array as shown in Fig. 4. In repeated measurements, the reproducibility of probing was investigated assuring that the probe is in contact with only one pillar. Owing to the Wollaston-wire-diameter of 5.8 μm, a minimum pitch of the pillar arrays of more than ~2 μm was necessary to avoid unintentional probing of two neighboring pillars. As a result of the vacuum conditions in the SEM, a thermal contact radius of ~20 nm was assumed,[15] which was much less than the diameters of the investigated pillars.

Samples (*n*-type silicon; length = 10 μm) comprising silicon pillars were analyzed having diameters and distances in the range of 250 nm to 4 μm. In Fig. 5(a), typical 3-omega plots are displayed. They show a decrease in the 3-omega voltage with a frequency as expected according to the thermal equivalent circuit. Fitting performed to these curves using the real part of the thermal impedance of the circuit in Fig. 3(b) and the thermal resistance of the pillar as adjustable parameter yielded very good agreement as can be seen exemplarily in Fig. 5(b). Measurements with pillars of diameters from 250 nm to 3.7 μm were analyzed accordingly. Relative thermal conductivities related to the value of bulk silicon, which were calculated from these measurements, were plotted against the pillar diameter as depicted in Fig. 6. As expected, the conductivity shows a decrease toward smaller diameters.

Superimposed to the measurements, a semi-phenomenological dependence of the thermal conductivity normalized to the bulk silicon value was drawn (solid line), which was derived assuming frequency-independent diffuse phonon-boundary scattering as the dominant effect for thermal conductivity in nanostructures[17]:

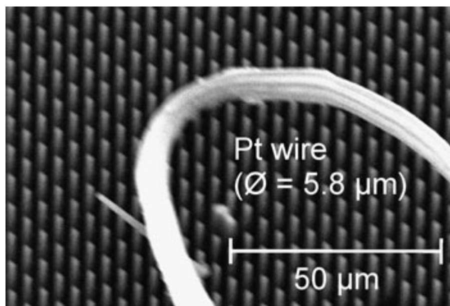


FIG. 4. Wollaston wire in a SEM (Leica S 360, Reutlingen, Germany) positioned over an array of silicon pillars using a Kleindiek probe (MM3A-EM, Oberkochen, Germany).

$$\frac{Cv_g}{3\kappa} = \frac{1}{\Lambda} + \frac{1}{d} \quad , \tag{2}$$

where $\Lambda = 250$ nm and $Cv_g = 1.7 \times 10^9$ W/m^2/K denote the mean free path of phonons of silicon nanolayers and the heat capacity–group velocity product of silicon nanowires, respectively.[17] Fitting of Eq. (2) yielded a better agreement for diameters less than 1,000 nm assuming a phonon mean free path of $\Lambda = 290$ nm (broken line).

The deviation of the measured values from the curve is assigned to the uncertainty of our 3-omega thermal conductivity measurements. As the dominant error source, we consider the small heat impedance of the Wollaston wire, which may have caused virtual thermal shorting of the pillar. Higher thermal impedance can be expected using nanomechanical thin-film probes.[14] A thin-film 3-omega probe of increased thermal impedance is under development, which furthermore, is designed to enable measurements with pillar arrays instead of single pillars to reduce the uncertainty. Thermal measurements with pillar arrays are feasible due to the accurate definition and knowledge of height, diameter, and position of pillar fabricated using the described top–down process.

IV. PILLAR ARRAYS

For thermal characterization of pillar arrays, stacks of *n*-type silicon chips of doping level of 5×10^{18} cm^{-3} were investigated. In Fig. 7(a), bulk-silicon and pillar-array chips are shown in addition to stacks of chips permanently joined using pressure-assisted silver sintering. The schematic in Fig. 7(b) shows a cross-sectional view of a stack composed of Au/Cr-metalized bulk silicon and a pillar-array chip pressed between blocks of brass (CuZn). We measured the Seebeck voltage $U_{Seebeck}$ with these stacks for hot-side temperatures in the range of $50 < T_H < 470$ °C at increasing temperature difference $T_H - T_C$ between the brass blocks. An oscillating signal was observed, which is caused by the thermal impedance of the brass blocks. Therefore, a settling time of 4 s between each temperature increment of 4 K had to be maintained until a nearly constant temperature gradient across the stack was achieved. As a result of the temperature loss across the brass blocks and the contact layers, a decreased residual temperature gradient within the stack and thus a reduced Seebeck voltage was expected according to

$$\frac{U_{Seebeck}}{T_H - T_C} = \frac{\alpha_{Si}}{1 + 2\dfrac{\kappa_{st}}{\kappa_c}\dfrac{l_c}{l_{st}}} \quad , \tag{3}$$

with the Seebeck coefficients α_{Si} and α_{CuZn} of silicon and brass, respectively. Because of the constant area, we consider sheet thermal resistances of the silicon stack and the contact layers that are denoted as l_{st}/κ_{st} and l_c/κ_c, respectively. Neglecting the thermal contact resistances

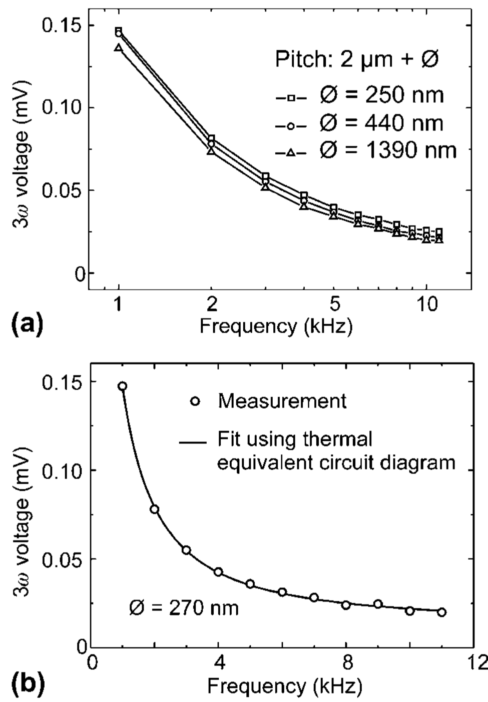


FIG. 5. (a) 3-Omega voltage measured with three single silicon pillars of different diameters and (b) 3-omega voltage measurement with a pillar of 270 nm in diameter superimposed by the curve from a fit using the thermal equivalent circuit in Fig. 3(b).

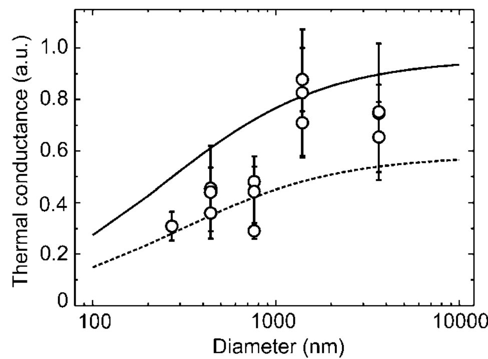
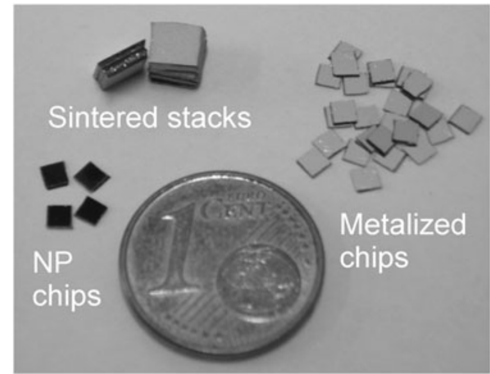


FIG. 6. Normalized thermal conductance measured with silicon pillars of various diameters using the 3-omega method. The solid and broken lines represent normalized thermal conductivities obtained using a semi-phenomenological model.[17]



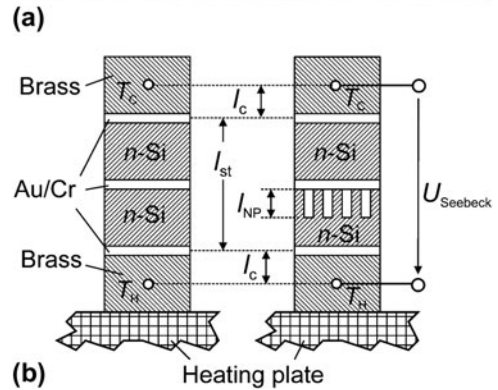


FIG. 7. (a) Pillar/bulk and bulk/bulk silicon chips in a photograph and (b) in a cross-sectional schematical representation.

between the brass blocks and the metalized chips and between the chips, only the thermal path resistances through the silicon and through the brass blocks have to be taken into account.

Regarding the small value of $\alpha_{CuZn} = 0.5$ μV/K for the Seebeck coefficient of brass, its contribution to the measured Seebeck voltages of 40–250 μV/K of $U_{Seebeck}/(T_H - T_C)$ measured with reference bulk/bulk silicon stacks of $l_{st} = 500$–4000 μm is negligible. Using Eq. (3), $\kappa_{st} = \kappa_{Si} =$ 148 W/m/K, $\kappa_c = \kappa_{CuZn} = 113$ W/m/K, and $l_c = 1.5$ mm, we find for the Seebeck coefficient of silicon $\alpha_{Si} = 375 \pm 30$ μV/K, which is a reasonable value for both bulk[18] and nanowire[19] n-type silicon of doping level of 5×10^{18} cm^{-3}. Measurements with a pillar/bulk silicon stack of $l_{st} =$ 500 μm yielded $U_{Seebeck}/(T_H - T_C) \sim 85$ μV/K, which is more than a factor of 2 higher than the bulk/bulk reference. From this value, a sheet thermal resistance of the NP/bulk silicon stack of $l_{st}/\kappa_{st} = 8.5 \times 10^{-6}$ m^{2}K/W can then be calculated using Eq. (3). The pillar/bulk silicon stack comprises an array of NPs of length $l_{NP} = 7$ μm, a diameter of 260 nm, and a pitch of 1.26 μm, i.e., a coverage of the chip area at a fraction of $\theta_{NP} = 3.3\%$. Neglecting the heat conduction through the ambient air, we can model the sheet thermal resistance of the pillar array by $l_{NP}/\theta_{NP}/\kappa_{NP}$. It is connected in series with the sheet resistance of the bulk, resulting in a sheet resistance of the entire pillar/bulk stack of

$$\frac{l_{st}}{\kappa_{st}} = \frac{l_{NP}}{\theta_{NP}\kappa_{NP}} + \frac{l_{st} - l_{NP}}{\kappa_{Si}} \quad . \tag{4}$$

Using Eq. (4) we were able to calculate the thermal conductivity of the NPs as displayed in Fig. 8. We found values of κ_{NP} between ~35 W/m/K and ~50 W/m/K in the considered temperature range. The measured room temperature value of ~40 W/m/K is somewhat lower than the thermal conductivity along silicon films of 250-nm thickness,[17,20] but is consistent to an extrapolation of the findings for nanowires of surface roughness in the nanometer

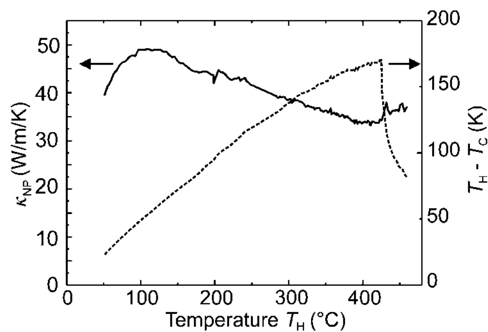


FIG. 8. Thermal conductivity κ_{NP} versus the temperature T_H of the hot side and temperature difference $T_H - T_C$ measured with a pillar/bulk stack of silicon in the temperature range between 50 °C and 470 °C.

range.[3,4] This applies also to the observed decrease of thermal conductivity with increasing temperature of ~0.05 W/m/K^2, which corresponds nearly to the findings for smooth silicon nanowires of 115 nm in diameter above 200 K.[3] As shown in Fig. 2(d), our nano pillars have sidewalls of low surface roughness in the nanometer range as could be expected for silicon-etched NPs using the cryogenic process.[21] The measured low thermal conductivity and the stable operation of arrays of silicon NPs of 260 nm in diameter in a large temperature range from 50 to 470 °C at temperature differences up to 190 °C confirmed that silicon is an attractive material for high-temperature TE applications.

V. CONCLUSIONS

Silicon pillars of 200 nm–4 μm in diameter were fabricated in a top–down process using optical lithography and DRIE at cryogenic temperatures. Thermal characterization was performed with single pillars using the Wollaston wire–based 3-omega method in a SEM. The results were analyzed using a simplified thermal equivalent circuit model. Pillar arrays were characterized in the temperature range between 50 and 470 °C by measuring the Seebeck voltage of pressure-joined chip stacks. In both cases, we found a considerable decrease of thermal conductivity for the pillars with respect to bulk silicon, confirming their potential for thermoelectric devices.

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