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Si/SiC Heterojunctions Fabricated by Direct Wafer Bonding

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The physical and electrical properties of Si/SiC heterojunctions formed by direct wafer bonding are presented. Atomic force microscopy (AFM) and imaging reveal an improved bonding quality when Si wafers are transferred to on-axis substrates as opposed to off-axis epitaxial layers. AFM analysis of the bonded wafer achieves a smoother surface when compared to molecular beam epitaxy–grown Si layers. A reduced roughness of only 5.8 nm was measured for bonded wafers. Current-voltage measurements were used to extract the rectifying characteristics of Si/SiC heterojunctions. These Si layers could lead to improved high quality and reliable SiO_2 gate oxides.

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At present, silicon carbide (SiC) is the best positioned wide bandgap semiconductor for the next generation of power electronic devices due to its material properties and native thermal oxide.[1] However, after two decades of intensive research, SiC Schottky-barrier unipolar devices remain the only commercial product available today.[2] The absence of a commercially available electronic switch, in particular, a successful metal-oxide-semiconductor (MOS) field-effect transistor (MOSFET), is one of the main factors preventing the widespread uptake of SiC technology.[3] The key issue relating to the performance of a MOS device is the quality and reliability of the gate dielectric, especially a low Si/SiO_2 interface state density. Unfortunately, thermally grown gate oxides for SiC MOSFETs exhibit low inversion layer mobilities ($<5\ \text{cm}^2/\text{V s}$), which are attributed to the high SiO_2/SiC interface state densities, that act as scattering or trapping sites.[4] Though SiO_2 is the native oxide of SiC and can be thermally grown on the surface, the presence of carbon and how efficiently it is removed during the consumption of the SiC surface is believed to influence the SiO_2/SiC interface and bulk insulator properties. Since the late 1990s, reported channel mobilities using modified thermal oxidation (nitridation, metallic contamination, and high-*k* stacks) are routinely in the range of $20–50\ \text{cm}^2/\text{V s}$.[3,5,6] Although being an order of magnitude lower than Si-based devices, this mobility value is believed to be high enough for SiC MOSFETs to compete with Si power devices.[1] However, for the time being, the problem for commercial SiC devices lies in the SiO_2 gate oxide reliability.

In this article, we pave the way toward the realization of overcoming the poor reliability (and high interface trap density) of SiC thermal oxidation: the use of Si/SiC heterojunction structures. An alternative approach to direct thermal oxidation of SiC is the thermal oxidation of a silicon layer, deposited on a SiC substrate.[7] This layer would potentially produce SiO_2 with Si complimentary MOS quality, which should be considered as the perfect insulator.[8] Another application of this direct wafer bonding is the monolithic integration of both Si and SiC devices onto the same chip. One can envisage smart power integrated circuits with the control part implemented in Si and power devices based on SiC. The main problem of both of these concepts is how to implement a large, monocrystalline Si layer on top of SiC. In the last two years, we have investigated several techniques to grow Si on SiC: Chemical vapor deposition, molecular beam epitaxy (MBE), and electron beam evaporation (EBE) under ultrahigh vacuum (UHV) conditions (EBE-UHV).[9,10] The large lattice mismatch between Si and SiC has thus far prevented each of the aforementioned techniques from achieving a Si layer with enough quality for a MOS gated device. Here, we report on a successful 3 in. wafer layer transfer (LT) of thin silicon layers via wafer bonding (WB), which is suitable for MOS device fabrication. We present a WB process based on the SmartCut technique to form Si/SiC heterojunctions. The SmartCut process, previously developed for silicon-on-insulator technology, is based on shallow ion implantation of a wafer, subsequent WB, and cleaving of the silicon wafer along the implantation plane, leaving behind a thin silicon layer bonded to a substrate.[10] The bonded wafers have been characterized both physically and electrically in the form of imaging, atomic force microscopy (AFM), and current-voltage (*I-V*) analysis. *I-V* measurements were performed using a mercury probe and by using photolithographic defined mesa structures, with Ti as the gate metal. These results have been compared to those from Si/SiC heterojunction MBE rectifiers. MBE experimental details have been discussed elsewhere.[9]

Wafer bonding has been performed on commercial 3 in. on- and off-axis SiC substrates from Cree Inc., USA. 4H-SiC epitaxial layers grown 4 °-off axis, doped at $1.4 \times 10^{18}\ \text{cm}^3$ and on-axis substrates, highly doped at $1.0 \times 10^{19}\ \text{cm}^3$ have been utilized. The Smartcut process transferred a 300 nm p-type Si wafer doped at $1 \times 10^{17}\ \text{cm}^3$ employing a hydrogen-ion implant, room-temperature wafer bonding, and subsequent heat-treatment for wafer splitting. Before wafer bonding was performed, the Si wafer was implanted with H_2^+ ions with an energy of ~ 200 keV and dosage in the range of $1 \times 10^{16}–1 \times 10^{17}\ \text{cm}^{-2}$. Both wafers were then cleaned using an oxygen (O_2) plasma treatment and a modified SC1 (NH_4OH: H_2O_2: DI water), SC2 (HCl: H_2O_2: DI water), and piranha ($H_2O_2 + H_2SO_4$) cleaning procedure for 20 min. Rinsing and drying of the wafers was performed before bonding. The wafers were then bonded in a vacuum at room temperature followed by a 150°C anneal in order to achieve a sufficient bond strength for cleaving. Next, the wafers were cleaved at a temperature of 300°C with further annealing performed at 1100°C for 2 h for further strengthening the chemical bonds. A summary of the wafer-bonding process can be seen in Fig. 1. A comparison of the wafer bonding on on-axis and off-axis wafers is presented in Fig. 2. From Fig. 2, it can be inferred that there is a higher degree of bonded wafer coverage (Si/SiC) achieved for on-axis SiC when compared to the off-axis material. This can be observed visually from the dark regions, which have a much higher prevalence with respect to the on-axis SiC substrate. Prior to the wafer-bonding process, AFM measurements were conducted on both on and off-axis SiC wafers. AFM analysis showed a root mean square (rms) roughness of 1.5 nm for the off-axis epitaxial 4H-SiC material, due to the 4 °-off step bunch. AFM measurements performed on the on-axis 4H-SiC material yield a low rms value of 0.6 nm, which approaches the limit for SiC wafer bonding.

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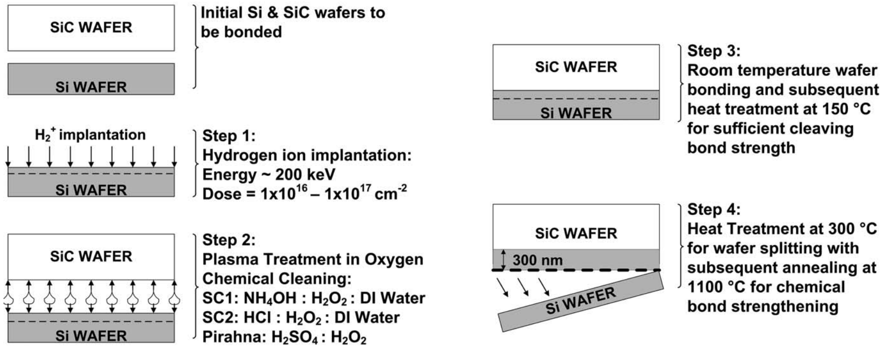

Figure 1. Summary of the layer transfer process utilized in this work for the formation of Si/SiC heterojunctions.

It is assumed that SiC requires a rms roughness of ~0.5 nm or less for successful room-temperature bonding.[11] The Si/SiC bonding coverage is much better on on-axis material because of its inherent lower surface roughness value, and in the case of an off-axis wafer, only few atoms (on the peaks) are actually contacting the Si layer. We expect to improve the off-axis bonding coverage by using polishing techniques along with predeposition cleaning procedure optimization.

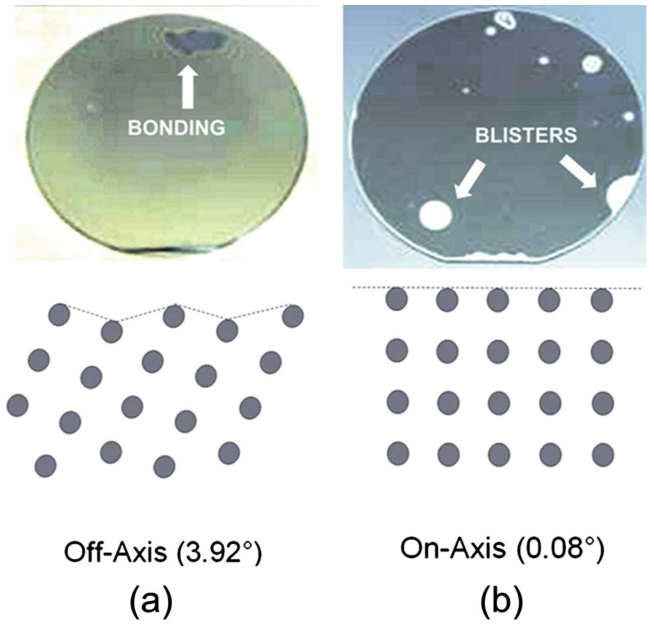

Figure 2. (Color online) (a) Si/SiC off-axis wafer bonding and (b) Si/SiC on-axis wafer bonding. Dark regions indicate area on the wafer at which bonding occurred.

We have previously reported on achieving Si/SiC heterojunction diodes, depositing Si layers by MBE.[8,9] MBE deposited Si layers were 0.1–1 μm thick having been deposited at 500 (low *T*) and 900°C (high *T*). Figure 3 shows AFM images of Si/SiC heterojunctions formed by the wafer-bonding technique alongside MBE Si deposited at 500 and 900°C. The advantage of heterojunction formation by direct wafer bonding is clear from Fig. 3 when considering the surface topology obtained. It can be seen that the wafer-bonding technique displays the lowest rms roughness of only 5.8 nm with respect to 210 and 12 nm for MBE Si deposited at 900 and 500°C, respectively. It is well known that the roughness associated with MBE-grown Si layers is due to the high isostructural lattice mismatch between Si and 4H-SiC.[12] Growth of silicon on SiC by both MBE and EBE-UHV results in an initial layer by layer growth. However, as the thickness of the layer increases, a Stranski–Krastanov growth mode or islanding becomes apparent. Temperature has a strong influence on the MBE silicon growth characteristics, with lower temperature growth producing a more even but low-crystallinity film and higher temperature growth (900°C) producing a much higher degree of crystallinity, but increased silicon island or grain formation. The wafer-bonding technique avoids the need for such growth mechanisms and consequential island formation by deploying a room-temperature plasma activation process. This process is sometimes referred to as hydrophilic direct wafer bonding,[11] with the most common plasma gases being argon, nitrogen, and oxygen. Nitrogen and oxygen gases were utilized for the plasma activation performed in this work. The strong bonding associated with the Si/SiC interface has survived a high-temperature anneal of up to 1000°C.

Typical *I-V* curves for the Si/SiC heterojunctions formed by WB are shown in Fig. 4. *I-V* curves are compared to MBE Si/SiC heterojunctions. It can be seen that the *I-V* curves for both MBE Si growth and wafer-bonding regimes are similar. Both present a Schottky-barrier like conduction mechanism. The barrier is formed due to the conduction Si–SiC band offsets. From capacitance-voltage (*C-V*) measurements, we have demonstrated that the Si/SiC

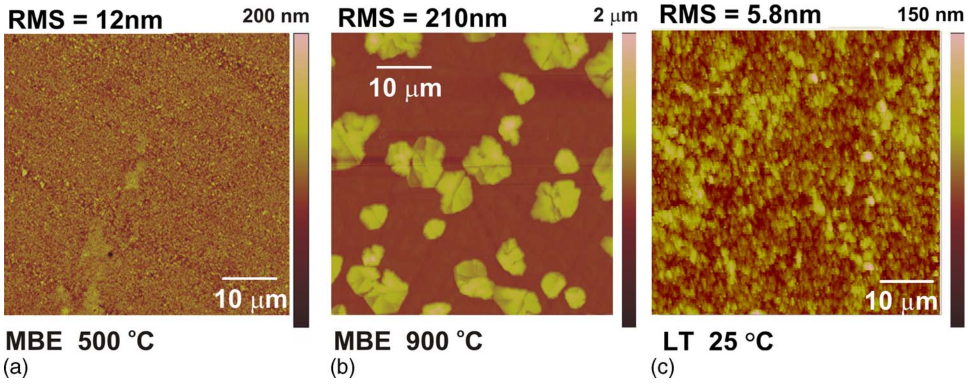

Figure 3. (Color online) AFM image and corresponding rms roughness measurement of the MBE Si layers grown on 4H–SiC at (a) 500°C, (b) 900°C, and (c) wafer bonding performed at room temperature.

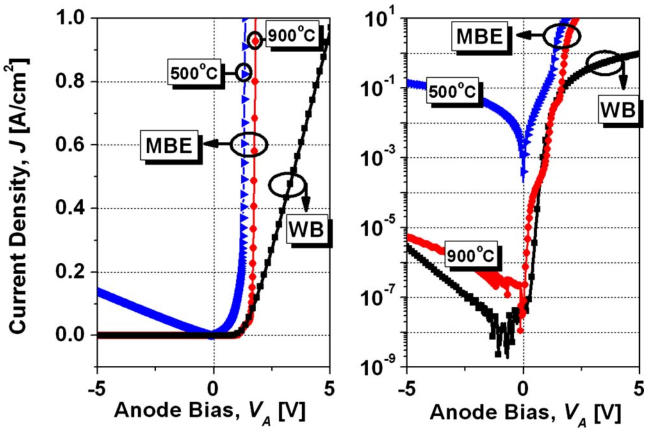

Figure 4. (Color online) Typical *I-V* curves comparing MBE Si layers grown (500 and 900°C) on 4H–SiC with Si/SiC p-n heterojunction bonded wafer.

heterojunction has a built-in potential (1.9–2.2 eV) substantially larger than the thermal voltage, justifying the full depletion approximation for the depleted region of SiC.[8] Hence, we suggest a situation analogous to that of a metal-semiconductor junction, where the SiC region is depleted but has a small voltage across the semiconductor as in a Schottky barrier with small applied voltages. The Si region is accumulated as in an ohmic contact. Therefore, transport across a Si/SiC heterojunction is similar to that of a metal-semiconductor junction. Diffusion, thermionic emission, and tunneling of carriers across the barrier can occur.[13] The experimental extracted conduction band offsets[8] are ~1.4 to 1.6 and ~2.0 to 2.2 eV for p-n and n-n Si/SiC, respectively. WB and MBE rectifiers both present reduced turn-on voltages when compared to SiC metal-semiconductor and p-n junctions, which bode positively with respect to reduced semiconductor device conduction losses. The *I-V* plot of the Si/SiC bonded wafer presents a higher resistance compared to MBE-grown Si layers. However, this can be explained by the low doping concentration within the p-type Si wafer used for the wafer-bonding process. The ideality factors extracted from the slope of the semilog *I-V* plot for Si/SiC p-n heterojunction diodes are in the range of 1.9–2.0. Similar values have been observed for MBE-grown Si layers with 1.6–1.7 and 2.0 for growth temperatures of 500 and 900°C, respectively. An interfacial suboxide (SiO_2) is inevitable at the Si/SiC interface due to the nature of the LT method utilized in this work. Therefore, it can be inferred that this thin SiO_2 layer will increase the resistance of the interface. This higher interface resistance suggests that, even if the samples have been subjected to sufficient thermal annealing, the transport of majority carriers at the interface boundary is still heavily influenced by scattering and trapping processes from the interface imperfections.[14] The interfaces created after the LT are usually associated with interface traps and interface energy states, which result in the accumulation of a considerable amount of electric charge across the heterojunction. This in turn affects the electrical properties of such fabricated devices. With respect to the Si/SiC interface characterized in this work, a reduced turn-on voltage after the hydrophilic bonding suggests that the thin SiO_2 barrier layer at the Si/SiC interface promotes tunneling processes through this barrier. However, the ideality factor value (~2) indicates the presence of recombination centers in the active region. If one assumes that electrons are able to tunnel through the hydrophilic bonding interface oxide, the interface charge trapping can cause the junction resistance to increase further. Hence, the interface charge trapping could increase with applied bias, which counteracts the lowering of the potential barrier and hence accounts for the additional source of a more gradual current increase with applied bias. The leakage current and the saturation level on the WB heterojunction diodes remains low even with a simple mercury probe measurement. This implies that the interface between Si and SiC defined by direct bonding wafer is basically abrupt, in accordance with Ref. 15. It can be inferred from Fig. 4 that low-temperature MBE samples, which exhibit a reduced islanding effect, displayed much higher leakage currents. The successful Si/SiC conduction across the WB heterojunction paves the way for innovative power rectifier fabrication with a reduced anode contact resistance. The formation of low-resistance contacts to Si is much easier to achieve with respect to SiC, especially p-type SiC.[16] Layer transfer on on-axis SiC substrates is also highly desirable because these are free from stacking fault generation from basal plane dislocations, with respect to minority carrier injection.[3] Current investigations are aimed at the study of the rectifying properties of Si/SiC diodes after annealing at different temperatures, the oxidation of Si/SiC structures, and a heterojunction MOSFET fabrication on the WB Si/SiC layers.

In conclusion, we have demonstrated that Si/SiC direct wafer bonding is a simple route for achieving a smooth, crystalline, high-quality electrical interface, suitable for innovative heterojunction device fabrication. Further work is aimed at examining the wafer-bonding technique for the fabrication of reliable, stoichometric, and completely carbon-free SiO_2 on SiC.

Acknowledgments

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