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Chemical Composition and Characterization of the Si/C Interface in Poly-Si Thin Films on Graphite Substrates

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Abstract. Polycrystalline silicon thin films on graphite substrates have been prepared by a two step process. On isostatically pressed, high purity graphite a 3-5 μm thick amorphous silicon layer is deposited by sputtering or plasma enhanced chemical vapour deposition. This seed layer is then recrystallized in a zone melting process by means of a line electron beam. High temperature gradients cause a dendritic crystal growth leading to large grains (in the order of cm in length) and a preferential (110)-orientation. Transmission electron microscope pictures and electron diffraction investigations show that during the recrystallization the molten silicon reacts with the carbon on the graphite surface forming β-silicon carbide particles as well as a "reaction zone" with Si, SiC and C. Dark current-voltage-characteristics of heavily boron doped seed layers show an ohmic contact, while lightly phosphorous doped, epitaxially thickened layers have blocking diode properties. Both kinds of layers have low resistivity and are therefore suitable for the application in thin film silicon solar cells on foreign substrates.

Introduction

There is now a large effort in photovoltaics to reduce the cost of solar cells in order to make them more competitive with conventionally generated electric power. One possibility is the more economic use of semiconductor materials. Single crystalline silicon solar cells have a thickness of 200 μm or more. But for the absorbtion of 85% of the sunlight already 30-50 μm are sufficient. If the thickness is reduced to less than 50 μm, the silicon, however, is not self-supporting anymore. Therefore a substrate is required. As a substrate material it is in principle possible to use glass, ceramics, steel, metallurgical grade silicon or graphite. In order to keep the cost for the solar cell low enough, the price for the substrate has to be smaller than \$ 0.5 for 1 dm^2. In addition the basic material should have a sufficient electrical conductivity for use as a backcontact and high temperature stability to get a good crystal quality.

Cheap *glass* is not stable in the temperature range above 600°C. Nevertheless the first successful depositions are already achieved by liquid phase epitaxy (LPE) on a special type of glass, which is thermally stable up to 850°C [1]. *Ceramics* are already used as a substrate for thin film silicon layers grown by a LPE process with solar cell efficiencies of more than 10% on 10*10 cm^2 [2] or even 15.7% on 1 cm^2 [3]. In order to detain the impurities from diffusing out of the substrate, a "diffusion barrier" [3] is necessary. An additional process, however, causes a further increase in production cost of the solar cell. This is also the reason, why *steel* (prevention of iron diffusion by a diffusion barrier) and *metallurgical grade silicon* (long time purification process) are, up to now, not suitable for thin film solar cells. *Graphite* is a good conductor, thermally and chemically stable and is available in high purity and with the same thermal expansion coefficient as silicon (suitable for high temperature gradients and therefore for fast annealing processes). Although graphite is the most expensive of the compared substrates, its advantages and the direct usability without any further treatment make it, at the same time, the most promising starting material.

For the deposition it is possible to use cheap thin film methods like PVD (physical vapour deposition, e. g. sputtering or evaporation) and CVD (chemical vapour deposition, e. g. plasma enhanced, PECVD, or using high temperatures, HTCVD). With PVD methods and the PECVD only amorphous or nanocrystalline layers with slow deposition rates (range of nm/min) are achievable. Their direct use for solar cells is not efficient enough, because the polycrystalline layer should have a grain size of at least twice the layer thickness (i.e. larger than 100 μm) to provide a sufficient carrier lifetime. Since the direct deposition of polycrystalline layers by a HTCVD process on graphite was not successful (only 1.5% efficiency of a 50 μm thick layer with grains of 1-30 μm size [4]), the most promising way is to recrystallize an amorphous layer to achieve a seed layer with large grains, which is then enlarged in thickness (up to 30-50 μm) by epitaxial methods, such as LPE or HTCVD, to form a coarse-grained layer thick enough for the absorption of the sunlight. This three step process is supposed to be the best way for the application of thin films in photovoltaics [5, 6, 7].

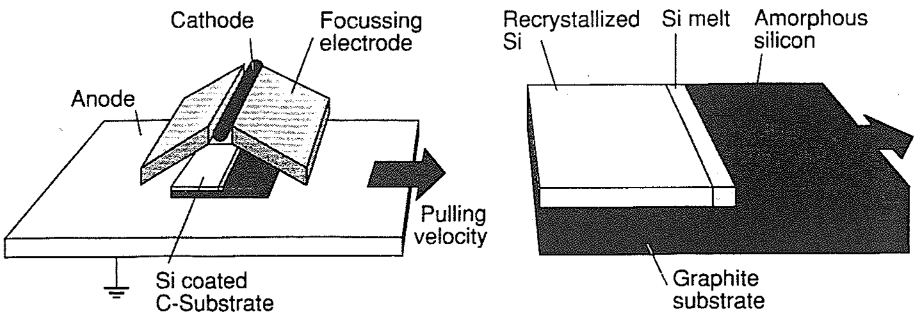
In our research group we use isostatically pressed, high purity graphite, which is covered with 3-5 μm amorphous silicon by sputtering or PECVD. This layer is recrystallized by means of a line electron beam at high pulling velocities. In this work we are investigating the basic properties of our system, i. e. the crystallographic and electric behaviour of the graphite, the silicon and the interface at the contact surface. Therefore we examined so far only a "two step process" (deposition and recrystallization) without epitaxy (except for a few electrical measurements).

Sample Preparation

We investigated the graphites of two different suppliers "A" and "B". Both materials have a low open porosity (less than 10%) and a surface roughness in the range of 1-3 μm. The substrates are used either directly or after a short wet chemical treatment. The graphite samples ($70*70*1$ mm^3) are covered with 3-5 μm amorphous silicon deposited by sputtering or conventional PECVD. Afterwards the samples are recrystallized by means of a line electron beam. The electron beam is generated between a heated tungsten rod (cathode), which emits electrons, and the graphite anode carrying the samples. The electrons are focussed by a Pierce optic and accelerated by a high voltage between the rod and the anode. Fig. 1 shows the scheme of the system, which is located in a high vacuum chamber. The most important process parameters are also given in Fig. 1. For recrystallization the samples are preheated up to 850°C from the rear using halogen lamps. By applying the electron beam the silicon seed layer is molten up in the focussed area, which is usually less than 1mm wide. The electron beam is absorbed directly by the amorphous silicon, in contrast to strip heater methods, where the infrared irradiation penetrates the amorphous layer heating up the substrate. The silicon is then molten indirectly by heat conduction of the substrate. Therefore our recrystallization occurs faster by one order of magnitude (cm/s compared to mm/s with strip heaters). In addition the high pulling velocity causes that the period of time the silicon is in the molten state is short enough that the silicon does not coagulate. Thus no capping layer is required.

Most of the investigated silicon seed layers have been heavily boron doped ($B>10^{20}$cm^{-3}) in order to generate a doping source for successive intrinsic epitaxial enlarging of the thickness by high temperature CVD (decomposition of $SiHCl_3$ at 1180°C) and to form in-situ a highly p-doped area at the rear contact, which acts as a "back surface field" (BSF). A few samples were also prepared with a light phosphorous doping level ($P<2*10^{15}$cm^{-3}) in the seed layer. After HTCVD epitaxy the doping level decreased to less than 10^{15}cm^{-3}.

For dark I(V)-characteristics Ti/Pd/Ag-contacts at the front have been evaporated onto the samples, while the back contact on the graphite was achieved with a gold contact spring exactly positioned underneath the front contact dot.



Process parameter

- ☐ Pulling velocity: v = 5...45 mm/s
- ☐ Power/Length: p = 80...320 W/cm
- ☐ Halfwidth: FWHM = 0.8...1.5 mm
- ☐ Acceleration voltage: U_H = 12...16 kV
- ☐ Substrate temperature: T_{sub} = 650...850 °C
- ☐ Si layer thickness: d = 3...10 μm

Figure 1: Scheme of the line electron beam system

Experimental Results

Recrystallization and formation of β-SiC. During the recrystallization the molten silicon is filling up the pores of the graphite forming a large contact surface to the substrate (see Fig. 2).

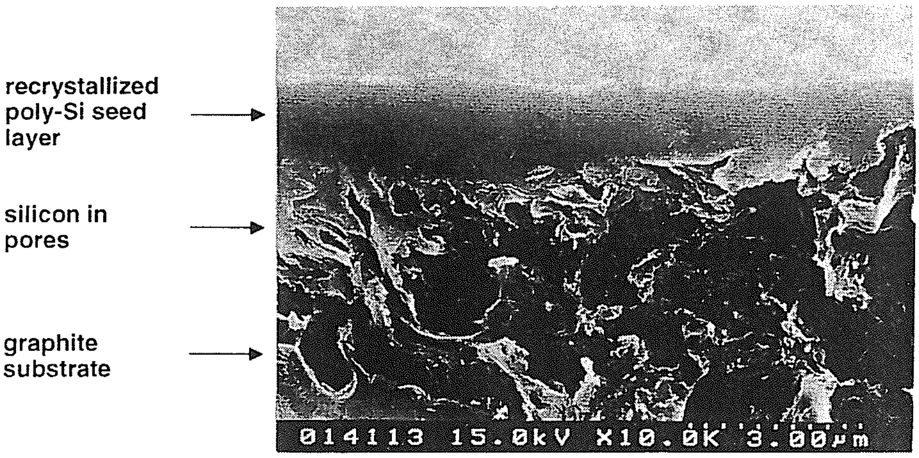


Figure 2: Cross-sectional view of the recrystallized silicon seed layer on graphite (SEM)

The silicon melt is saturated with carbon, since the carbon concentration in both investigated types of graphites (see Fig. 3) exceeds the solid ($3.5*10^{17}$cm^{-3}) and the liquid solubility ($4*10^{18}$cm^{-3}) of carbon atoms in silicon [8]. At sites with an energetic minimum heterogeneous nucleation occurs. This was earlier already observed on bubbles within the silicon layer originating from Ar built-in during sputtering [9]. The main part of the SiC formation, however, starts nucleation at the interface between silicon and graphite (see "TEM analysis" below). The silicon carbide provides a better wetting of the graphite with the melt and is therefore another reason for the low tendency of the silicon to coagulate. The large temperature gradients lead to dendritic crystallization with a preferential (110)-orientation. The silicon surface is mirror-like and the grain size is 50-100 μm in width and up to centimeters in pulling direction.

TEM analysis. Fig. 4 shows a TEM picture of the Si/C interface. It reveals that there is no continuous SiC layer formed, but single β-SiC particles (see Fig. 5) with a light preferential orientation of (111) normal to the substrate (average over numerous samples) as well as a "reaction zone", where

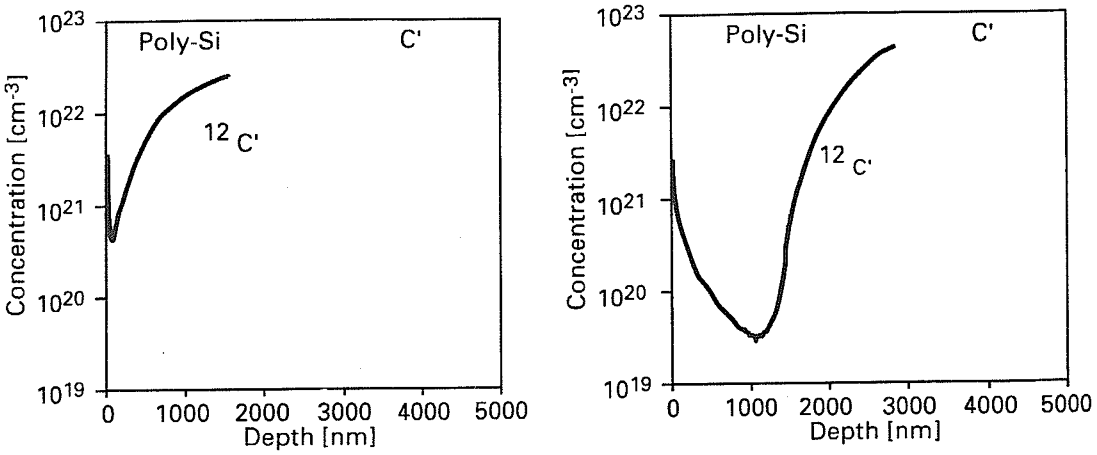


Figure 3: SIMS analysis of the carbon concentration in silicon seed layers grown on graphite "A" (left) and "B" (right)

Si, C and β-SiC are found (see Fig. 6). A continuous SiC layer would act as an insulator between the silicon and the graphite. As a consequence we would get a high series resistance between the silicon thin film and the conductive substrate, which is intended to be the back contact of the solar cell.

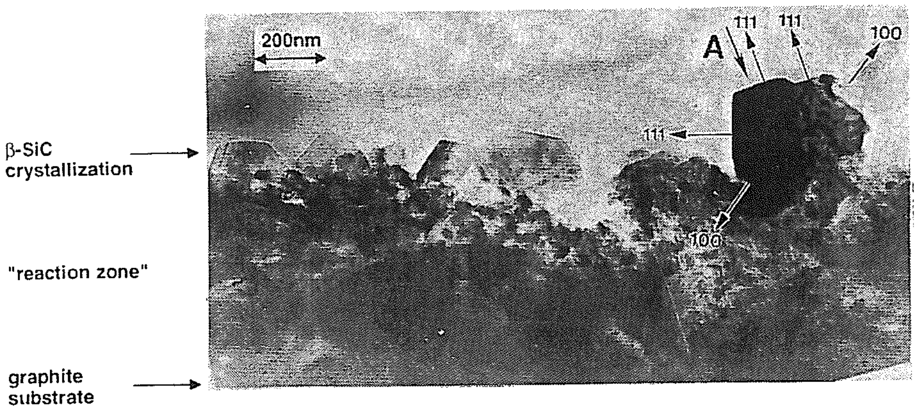
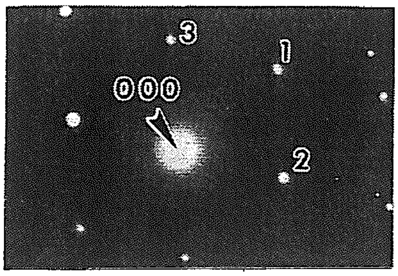


Figure 4: TEM picture of the Si/C interface

Electrical behaviour. Heavily boron doped (B>10^{20}cm^{-3}) seed and epitaxially thickened layers show an Ohmic contact in the system Ti/Pd/Ag–silicon–interface–graphite–gold (see Fig. 7). After removing of the silicon by plasma etching (layer sequence: Ti/Pd/Ag–interface–graphite–gold) the straight I(V)-curve and the low resistivity are retained. The experimental values for the resistivity are in the range of 5-9$*10^{-2}\Omega$cm with and 2-5$*10^{-2}\Omega$cm without the silicon layer. Unfortunately there is no quantitative analysis possible, because the single contact resistances are not known.

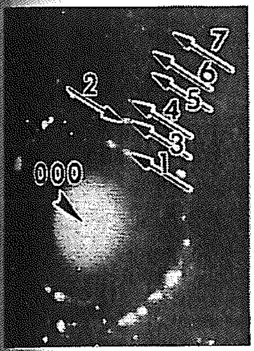
Lightly phosphorous doped (P<2$*10^{-2}$cm^{-3}) epitaxially thickened layers show a blocking diode characteristic (see Fig. 7). The resistance for small voltages in forward direction (less than 600 mV), however, are small enough for the application in solar cells.

Correlation between β-SiC particles and electrical behaviour. The dependence of the electrical properties from the nature of the SiC was derived from the comparison of the measured resistivities and the properties of SiC particles formed on graphite "A" and "B". The carbon concentration in the silicon layer on graphite "A" is larger by one order of magnitude compared to "B" (see Fig. 3 and 4). Concerning the size of the SiC particles the crystallites on graphite "A" are, as a consequence of the higher level of carbon within the melt, 2-5 times larger. Finally an increase of the



Number	d[Å] measured	Silicon carbide d[Å] JCPDS (no. 29-1129)	hkl
1	2.18	2.18	200
2	2.499	2.52	111
3	2.49	2.52	111

Figure 5: Electron diffraction pattern of crystallite A and comparison of lattice parameters with the data of the Joint Committee on Powder Diffraction Standards (JCPDS)



Number	d[Å] measured	Silicon d[Å] JCPDS (no. 27-1402)	hkl	Silicon carbide d[Å] JCPDS (no. 29-1129)	hkl	Graphite d[Å] JCPDS (no. 41-1487)	hkl
1	3.31	–	–	–	–	3.38	002
2	2.67	–	–	2.54	111	–	–
3	2.53	–	–	2.54	111	–	–
4	2.19	–	–	2.19	200	–	–
5	1.68	1.637	113	–	–	1.68	004
6	1.52	–	–	1.54	220	1.548	103
7	1.32	1.358	004	1.314	311	–	–

Figure 6: Electron diffraction pattern of the "reaction zone" and comparison of lattice parameters with the data of the Joint Committee on Powder Diffraction Standards (JCPDS)

resistivity in the range of 20% was observed comparing the average resistivities (with and without the silicon layer) of thin films on graphite "A" and "B". Consequently a higher carbon concentration in the silicon layer leads to larger β-SiC particles. With the increase of the particle size the conductivity decreases.

Discussion and Conclusions

The filling up of the pores and formation of the β-SiC crystallites, which are able to form chemical bonds to the silicon as well as to the graphite, are responsible for the excellent adhesion of the silicon thin films prepared by the electron beam recrystallization. The silicon carbide, however, does not build a continuous insulating layer between the silicon and the substrate. The resistivities, which are correlated to the particle size of the SiC (larger particles lead to a decrease in the resistance) of the silicon/interface/graphite system are small enough for the application in solar cells. Especially highly boron doped layers show Ohmic behaviour of the Si/C interface, which can probably be attributed to an in-situ doping of the SiC by excess boron. In the same way the blocking diode properties of lightly phosphorous doped epitaxially thickened layers are due to a negligible autodoping effect or due to a high barrier to the substrate. To evaluate the exact reasons for the low resitivity and to determine the defect density at the interface further investigations are necessary. Nevertheless the large grained polycrystalline silicon layers on graphite substrate offer a great potential for the application in thin film solar cells.

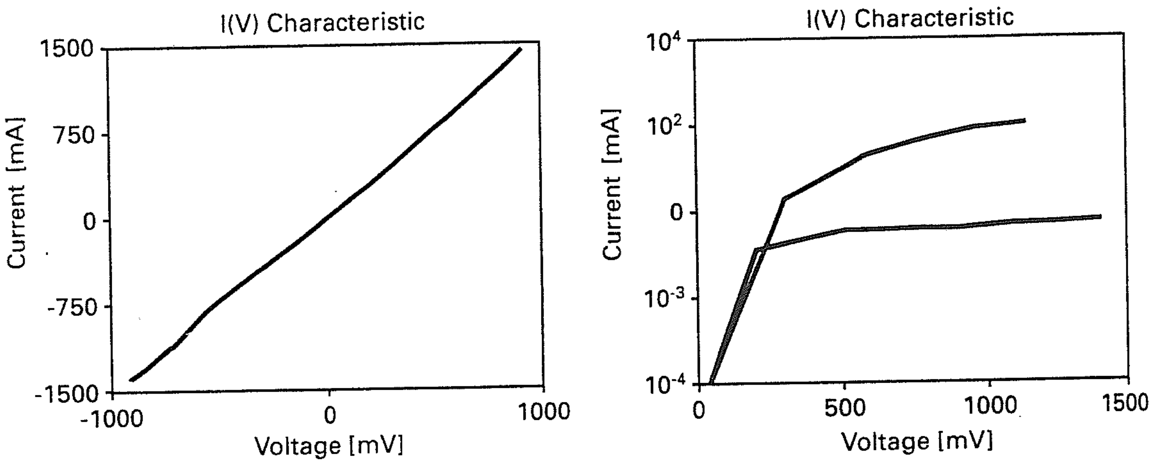


Figure 7: Dark I(V)-curve of heavily boron doped seed layer (left) and lightly phosphorous doped epitaxially thickened layer (right)

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