Stress Compensation Techniques in Thin Layers Applied to Silicon Micromachining

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Abstract

Stress in thin films is one of the mayor technological problems of silicon micromachining. Therefore stress reduction by a compensation method increases the technological use of a material. Three methods to obtain stress free films are investigated:

1. Stress in SiO_2 and Si_3N_4 can be compensated by ion implantation.
2. Sandwich layers of SiO_2 and Si_3N_4 can be made internally stress compensated by variation of the thickness ratio.
3. Polysilicon is stress reduced by appropriate doping and annealing.

The film stress is evaluated by the measurement of the bending of the substrate. Examples of processed membranes, bridges and cantilevers made of stress compensated films are given.

Introduction

The deposition of thin films is an important field of technology. Most thin films exhibit stress after deposition. This stress has many different causes. Most films are deposited at elevated temperatures. If the thermal expansion of the film and the substrate are not identical, there will be stress between them after cooling. Other sources for film stress are lattice mismatch, crystallisation and texture effects in the films. Stress may cause problems for thin film technology: It changes the behaviour of the films often in an uncontrolled way, reducing the yield and the long term stability and causing fracture. In the recently developed technology of microsystems more and more free standing thin film structures are used, e.g. resonators and moveable parts in surface micromachining, thin film membranes in transducers. For those applications the thin films used must be stress–free or stress compensated. In this paper, a number of the most important films for microsystem technologies are investigated and stress compensation methods are tested experimentally. For the measurement of film stress, the substrate bending method is used[1]. When a stressed film is deposited, the substrate, in our case a silicon wafer, is going to bend. This deformation is measured by the deflection of a laser beam. From the deformation and the known elastic data of the substrate the stress in the film is calculated.

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1. Stress compensation by ion implantation

Silicon nitride deposited by the LPCVD process is a very important dielectric layer in semiconductor technology and in micromechanics. Among other applications it is used for electrical insulation, as a masking layer for etching and to fabricate free standing membranes for transducers. After deposition silicon nitride shows a high tensile stress. This stress can be compensated by ion implantation[2]. For our experiments we used a layer of 300 nm on a 4 inch silicon wafer. The stress in the film after deposition was 1.9 GPa tensile stress. The layers are implanted with boron ions, the energy is 100 keV. The compensation occurs at a dose of $3 * 10^{15}$ atoms/cm^2. At higher doses the implantation induced stress saturates at a value of 2.1 GPa, corresponding to an actual compressive stress of 200 MPa in the nitride layer. A subsequent annealing for 1 hour at 500^0 C reduces this saturation value to a correct compensation.

The method has been applied in membrane technology. Membranes of silicon nitride are realized using anisotropic etching of silicon in KOH. The size of the membranes is from some mm to some cm sidelength. Due to the high tensile stress, membranes of as deposited nitride mostly break during etching. An implantation dose of $5 * 10^{14}$ adds sufficient compressive stress. Slightly tensioned (about 600 MPa) flat membranes can be obtained with a high yield.

Thermally grown 500 nm thick silicon dioxide shows a compressive stress of 470 MPa. When implanting with 160 KeV carbon ions, this stress can be changed into tensile and into compressive again as shown in Fig. 1. Stress compensation occurs at $5 * 10^{13}$ atoms/cm^2 and $6 * 10^{14}$ atoms/cm^2. Further investigations concerning this unexpected behaviour show that it is not dependent of the type of the implanted ions, nor an effect of in situ annealing during the implantation process or caused by ions penetrating into the substrate, but is an effect of the implantation damage and reorganisation process in the silicon dioxide. In a technological process often the stress compensation will be followed by further high temperature steps. Fig. 2 shows the effect of annealing on the stress compensation. The curves show a gradual reduction of the implantation effect, which disappears completely between 900^{0}C and 1000^{0}C, where the oxide shows a viscous transformation.

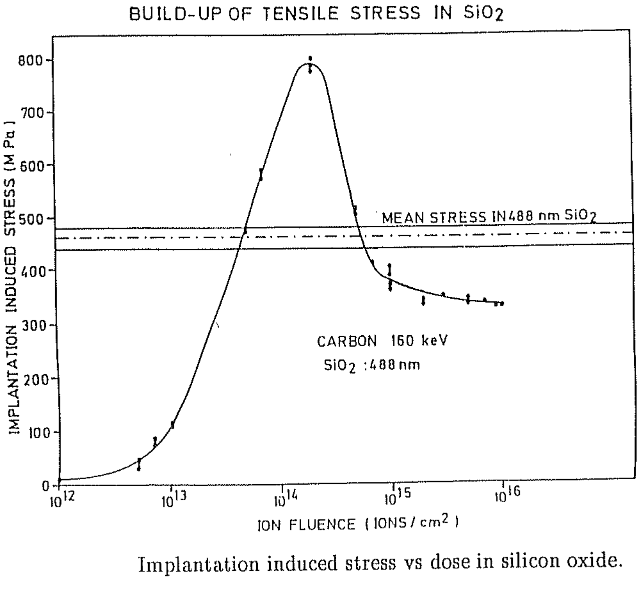

Figure 1: Implantation induced stress vs dose in silicon oxide.

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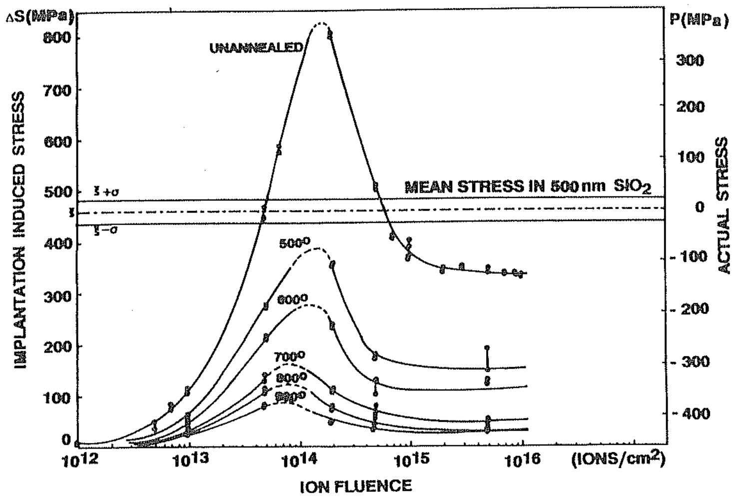

Figure 2: Effect of annealing on the implantation effect.

2. Silicon oxide / nitride sandwich layers

The stress conditions in silicon dioxide (SiO_2), LPCVD silicon nitride (Si_3N_4) and sandwich layers thereof on double side polished 4 inch <100> silicon wafers with a thickness of 300 μm were determined in an extensive programme of experiments. The curvature of the wafers is measured after double–side deposition, then one side is etched and the curvature is measured again.

As expected, the LPCVD nitride films show a tensile stress while the silicon dioxide films are compressive. The experimental results for the film stress of the SiO_2–layers processed by dry (x) and wet (o) thermal oxidation at 950° C and 1050° C are shown in Fig. 3. The film stress decreases with increasing process temperature. This is also reported in literature[1]. This is due to the fact that the intrinsic part of the stress decreases faster than the thermal stress increases. The experimental results for single layers are summarized in Table 1. The film stress for silicon nitride is tensile and was found to be about 1.3 GPa. Silicon dioxide films exhibit a compressive stress. The value depends on the oxidation parameters and ranges from –0.27 GPa to –0.38 GPa.

Si_3N_4	LPCVD	760° C	1.33	+/– 0.1	GPa
SiO_2	dry	950° C	–0.38	+/– 0.04	GPa
SiO_2	dry	1050° C	–0.33	+/– 0.04	GPa
SiO_2	wet	950° C	–0.28	+/– 0.01	GPa
SiO_2	wet	1050° C	–0.27	+/– 0.01	GPa

Table 1: Film stress for single layers of LPCVD Nitride, dry and wet thermal oxide.

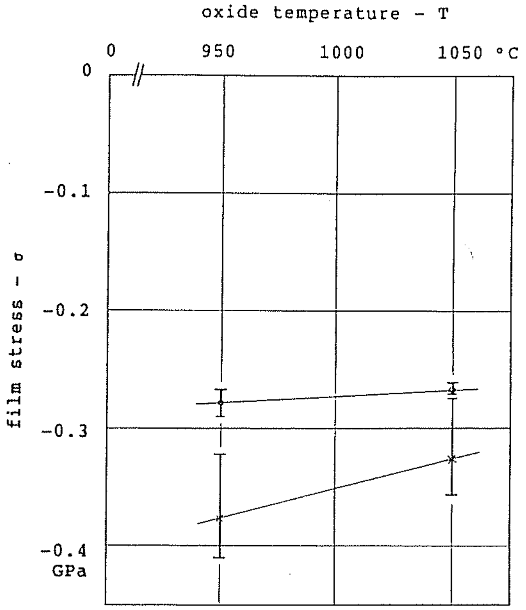

Figure 3: The films stress of dry (x) and wet (°) thermally grown silicon oxide vs the deposition temperature T.

If films with tensile and compressive stress are combined in a sandwich layer, a film with a resulting stress of zero should be possible. The aim of this investigation is to develop SiO_2/Si_3N_4 sandwich combinations with optimized stress compensation. As an example, Fig. 4 shows the resulting wafer bow d as a function of the film thickness ratio t_f(oxide) / t_f(nitride). The thickness of the nitride is 50 nm for all samples. The compensation occurs at a ratio of 4:1. Table 2 gives the experimentally determined values depending on the process parameters:

Nitride	Oxide	$t_f(O)/t_f(N)$	
LPCVD, 760°	dry 950°C	3.6	+/–0.4
LPCVD, 760°	dry 1050°C	4.0	+/–0.2
LPCVD, 760°	wet 950°C	4.1	+/–0.1
LPCVD, 760°	wet 1050°C	4.5	+/–0.2

Table 2: Stress compensation ratio for different sandwich combinations

Figure 4:

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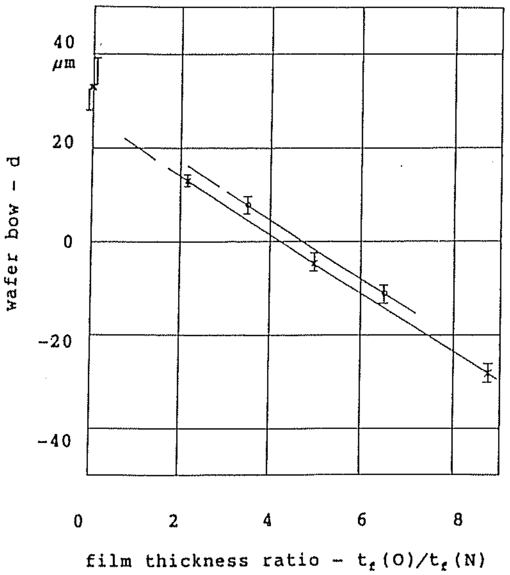

Figure 4: Resulting wafer bow d as a function of the film thickness ratio t_f(oxide) / t_f(nitride) for a sandwich layer.

3. Polysilicon

Stress control in polycrystalline silicon deposited by the LPCVD technique is important for micromechanical processes involving surface micromachining. The stress in polysilicon thin films is greatly influenced by the film structure, and this depends on the deposition and processing conditions. It has been reported that n–doping and/or annealing the polysilicon films can lead to low stress values[3 4]. In this work polysilicon thin films are deposited from pure silane by LPCVD, with deposition temperatures between 580° and 630° C and a deposition pressure of 80 mTorr. Some samples are doped by ion implantation with boron or phosphorus, and some samples are annealed in N_2 between 850 anf 1150° C.

Stress values have been obtained from measurements of the bending of the substrate and by using micromechanical structures. Mechanical strain of thin films can be determined by means of micromechanical structures obtained with the surface micromachining technique[5]. As an example, a bridge buckles under an axial compressive stress more than a critical value, and conversely, for a given stress value, all bridges longer than a critical length will buckle. Therefore, free–standing polysilicon bridges and cantilevers of several length are fabricated. Then the strain of the film can be obtained from the dimensions of the smaller structures that show permanent buckling. Fig. 5 shows a SEM micrograph of the bridges used as test structures. The largest bridge is 250 µm long. Straight free–standing bridges and cantilevers made of stress–compensated polysilicon are shown. Stress measurements have also been performed by FTIR spectroscopy on polysilicon – silicon dioxide structures and by Raman spectroscopy, and the results agree qualitatively with the mechanical measurements.

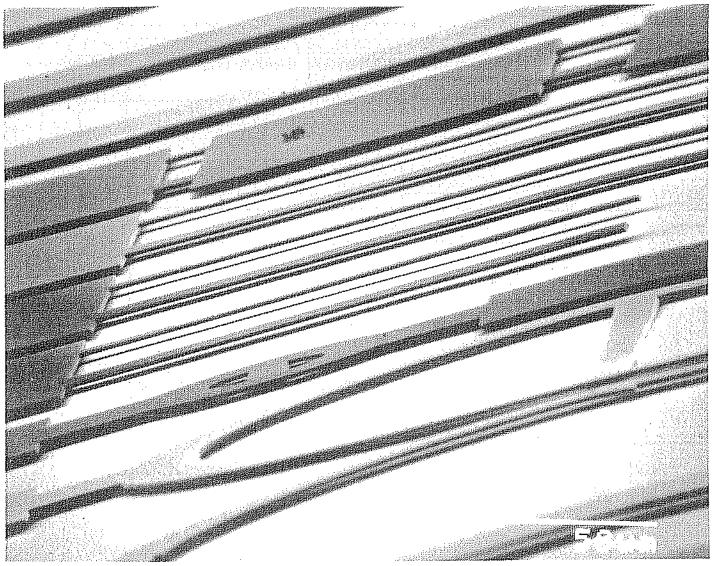

Figure 5: Bridges of stress–free polysilicon.

Fig. 6 shows the measured strain values versus the annealing temperature. A part of the samples is doped by ion implantation with a dose of 10^{15} at/cm^2. The results from these experiments can be summarized as follows: Unannealed polysilicon films show high compressive strain values. Annealing reduced the polysilicon strain, and the reduction is higher at higher annealing temperatures. Very low strain ($<7 * 10^{-5}$) is obtained for polysilicon deposited at 580^0 C, implanted with phosphorus and annealed in nitrogen at 1150^0 C for 30 min. This strain value is the low resolution limit of the measurement methods.

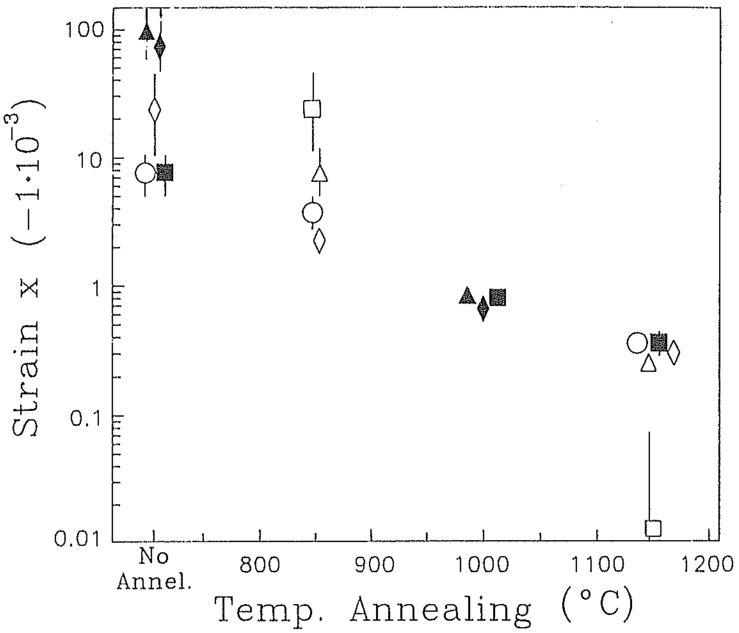

Figure 6: Polysilicon strain vs annealing temperature for different deposition temperature T and different doping.

▲ T = 580°C, undoped
◆ T = 605°C, undoped
■ T = 630°C, undoped
△ T = 580°C, B–doped
◊ T = 630°C, B–doped
□ T = 580°C, P–doped
○ T = 630°C, P–doped

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