The silicon nanowire Accumulation-mode MOSFET (AMOSFET)

Pranav Garg†, Jian Wu†, Yi Hong†, Md Mash-Hud Iqbal‡,
Piero Migliorato‡, Stephen J. Fonash†

†Center for Nanotechnology Education and Utilization,
The Pennsylvania State University, University Park, PA
16802, USA

‡Centre for Advanced Photonics and Electronics (CAPE),
University of Cambridge, 9 J. J. Thomson Avenue,
Cambridge CB3 0FA, U.K

There are many groups around the world who are fabricating FETs on silicon nanowires (SiNW) grown using the vapor-liquid-solid (VLS) method. The silicon nanowire material is often referred to as being intrinsic but, in fact, at least when Au is used as the VLS catalyst, the SiNWs are unintentionally doped p-type [1 - 3]. We have shown the Au-related site responsible for the unintentional p-type doping is 0.42 eV above the valence band edge for VLS growth catalyzed by Au [2]. The transistor devices that are being made using SiNWs can be N+ source and drain doped n-channel MOSFET devices but more commonly they are not inversion layer MOSFETs but are AMOSFETS. These are FETs using ohmic contacts and the single (unintentional) p-type doping which function as accumulation devices [1-4]. They can be fabricated to be enhancement or depletion transistors. The AMOSFET device, since it only utilizes one doping type and ohmic contacts, is extremely easy to fabricate. Most importantly, we have demonstrated SiNW AMOSFETs are capable of attaining on-off ratios of six to seven orders of magnitude and subthreshold swing values as low as 70mV/decade [3].

Most of the groups fabricating AMOSFETS analyze these devices using standard MOSFET equations, although this picture is not valid for these AMOSFET accumulation devices. In fact, we have shown the invalidity of a standard MOSFET analysis and further have shown that these AMOSFET accumulation devices have a novel weak linear and saturation region dependence on gate capacitance [4]. Using the standard MOSFET equations, many of these groups have deduce hole mobilities of dubious validity.

We further discuss here our development of the AMOSFET device and continue our use of the grow-in-place approach to fabricating our AMOSFETs [1-3]. We report on a comparison of non-confined and confined AMOSFET structures using unintentional and intentional doping. We also report on the new AMISFET structures which utilize an ALD deposited hafnium oxide as the gate dielectric. A comparison with our previous modeling work is also presented. In addition, we discuss the applicability of our AMOSFET devices for nonvolatile memory applications.

References:

1) Y. Shan and S. J. Fonash, *ACS Nano* **2**, 429 (2008)
2) Y. Hong, P. Garg, and S. J. Fonash, *Appl. Phys. Lett.* (in review)
3) P. Garg, Y. Hong, M. M. Iqbal, P. Migliorato, and S. J. Fonash, *ECS Trans.* **16,** 159 (2008)
4) M. M. Iqbal, Y. Hong, P. Garg, F. Udrea, P. Migliorato, And S. J. Fonash, *IEEE Trans. Electron Device* **55**, 2946 (2008)

Figures and captions:

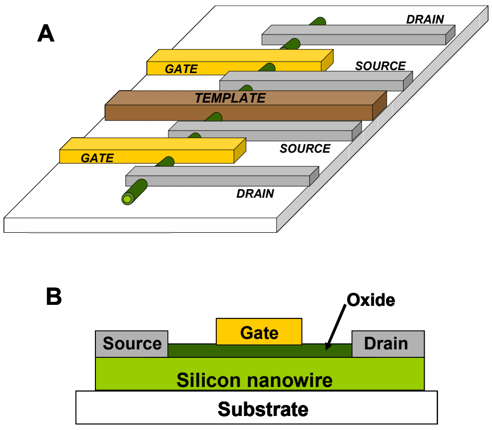

Figure 1: A) Schematic view of two AMOSFETs fabricated on SiNW grown using our ‘grow-in-place’ template. B) Schematic cross-section of AMOSFET.

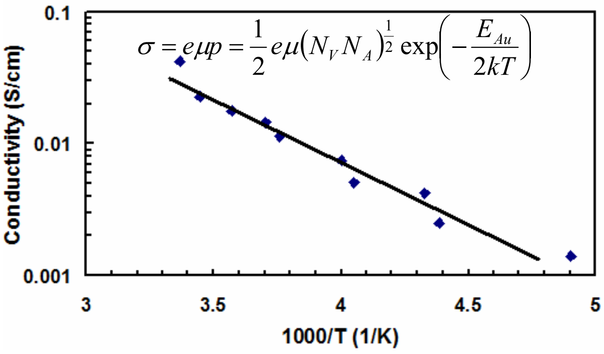

Figure 2: Temperature vs. conductivity behavior of a ~100 nm grown-in-place SiNW, indicating a gold acceptor level of 0.42 eV above valence band edge. Also shown is the relationship between conductivity and doping concentration for partially ionized acceptors.

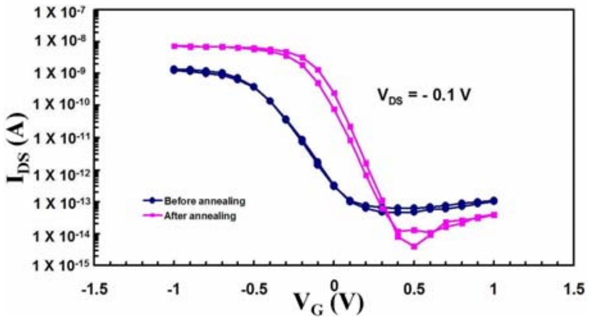

Figure 3: Transfer characteristics of AMOFET on ‘grow-in-place’ SiNW, before and after annealing. Post annealing, AMOSFET show I_{ON}/I_{OFF} ratios of 10^6, and subthreshold slope of 70 mV/dec.