Enclosed pillar arrays integrated on a fluidic platform for on-chip separations and analysis†

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Due to the difficulty of reliably producing sealed 3-D structures, few researchers have tackled the challenges of creating pillar beds suitable for miniaturized liquid phase separation systems. Herein, we describe an original processing sequence for the fabrication of enclosed pillar arrays integrated on a fluidic chip which, we believe, will further stimulate interest in this field. Our approach yields a mechanically robust enclosed pillar system that withstands mechanical impacts commonly incurred during processing, sealing and operation, resulting in a design particularly suitable for the research environment. A combination of a wafer-level fabrication sequence with chip-level elastomer bonding allows for chip reusability, an attractive and cost efficient advancement for research applications. The characteristic features in the implemented highly ordered pillar arrays are scalable to submicron dimensions. The proposed fluidic structures are suitable for handling picolitre sample volumes and offer prospects for substantial improvements in separation efficiency and permeability over traditional packed and monolithic columns. Our experimental observations indicate plate heights as low as 0.76 μm for a 10 mm long pillar bed. Theoretical calculations confirm that ordered pillar arrays with submicron pore sizes combine superior analysis speed, picolitre sample volumes, high permeability and reasonably large plate numbers on a small footprint. In addition, we describe a fluidic interface that provides streamlined coupling of the fabricated structures with off-chip fluidic components.

Introduction

Highly ordered arrays of high aspect ratio pillars created on a chip using lithographic techniques offer substantial fundamental advantages[1–4] over more traditional separation phases, such as packed and monolithic columns. As the sizes of the separation media shrink, the random nature and polydispersity of porosity in the latter two systems becomes a significant factor that limits the separation efficiency.[1,2,5,6] Surmounting this limitation is particularly crucial for designing on-chip separation systems with lengths 1–2 orders of magnitude shorter than conventional macroscopic separation columns. Indeed, decreasing characteristic pore sizes in a separation bed allows one to proportionally decrease the column length thus making it more compatible with an on-chip format. Recent studies by Desmet and coworkers[5] provide convincing evidence that breakthrough advances in on-chip separation technology can be gained by adapting lithographic patterning and wafer-level processing techniques similar to those developed for the semiconductor industry and capable of delivering fabrication accuracy of tens of nanometres. However, identifying specific technological approaches that can lead to successful implementations of efficient on-chip separation beds is far from being trivial. This can largely explain the fact that, despite the fundamental advantages of lithographically patterned ordered separation beds first proposed and implemented by Regnier *et al.*[3,7] more than a decade ago, few researchers have chosen to further explore this idea.

The first applications of ordered pillar arrays as related to pressure driven separations have been reported only recently.[1,5,8,9] Notably, some of the previous studies explored pillar arrays as a platform for a newly emerging particle separation technique based on deterministic lateral displacement[8,9] rather than conventional liquid chromatography. While groundbreaking studies by Desmet and coworkers have convincingly demonstrated the potential of on-chip separation columns based on ordered pillar arrays, they also identified important experimental, technological and methodological challenges of such systems. One clear indication of the difficulty of these challenges is that only a few researchers have tackled them successfully. To our best knowledge, no successful implementation of lithographically patterned pillar arrays for pressure driven liquid phase separations analogous to those conducted using conventional packed or monolithic columns have been reported by researchers outside Desmet's team and their collaborators.

The key challenges involved in fabrication and operation of lithographically patterned separation columns can be broadly divided into the four categories: (i) decreasing the pillar sizes while increasing their aspect ratios without compromising mechanical robustness of the system, (ii) sealing of the pillar bed and coupling of the on-chip separation bed with macroscopic off-chip fluidic components, (iii) creating retentive properties of the arrays, and (iv) sample injection and detection compatible with very small plate heights. The main goal of our present work is to

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address the first two challenges. By combining and refining technological approaches similar to those described previously in several independent studies,[2,7,10–13] we established an innovative fabrication sequence that yields high-aspect-ratio pillar arrays embedded into channels on a re-sealable fluidic chip that facilitates experiments and further optimization. Our fabrication sequence relies on standard cleanroom processing techniques, in particular, photolithographic patterning, anisotropic reactive ion etching (RIE) of silicon and plasma enhanced chemical vapor deposition (PECVD) of silicon oxides. As compared to pillar arrays for on-chip separations implemented by De Malsche *et al.*,[5] He & Regnier,[7] and Kaji *et al.*,[13] the key advantage of the technological strategy presented here is the formation of a robust network of pores scalable down to submicron characteristic sizes and enclosed into a silicon oxide scaffold. Moreover, the enclosed array of pores is seamlessly integrated into a system of fluidic channels that can be sealed using either soft (elastomer based) or hard (such as frit) bonding techniques. At this stage, we focus on a chip level sealing technique using elastomer bonding since this approach streamlines chip assembly and is compatible with various surface modification techniques that can be applied prior to the final chip assembly. The proposed approaches yield re-sealable fluidic chips that are especially suitable for extensive studies of separation and transport phenomena in a laboratory setting. While being beyond the scope of the present study, the scaled up fabrication of analytical separation systems based on the proposed strategy may ultimately benefit from wafer-level anodic or frit bonding. At the same time, it is the absence of complicated and irreversible anodic bonding in our processing sequence that, we believe, will stimulate more extensive exploration of the ordered pillar arrays in conjunction with various liquid phase separation techniques.

Experimental

Chip design and fabrication of enclosed pillar arrays

As a starting material, we used p-type Czochralski grown 100 mm, (100) orientation single side polished silicon wafers with nominal thickness in the range of 300 to 500 μm and resistivity in the range 0.01 to 20 Ω cm. Our designs accommodated 9 chips on a 100 mm wafer. Each chip in our design was 22 mm × 22 mm and contained one main straight channel with approximately 10 mm of its length populated with a pillar array. Using the CAD software, pillars in the arrays were defined as hexagons placed in the corners of equilateral triangles by analogy with ordered pillar arrays first proposed and evaluated by Gzil *et al.*[2] Among several possible ways to terminate a pillar array at a channel side wall, we choose the "embedded pillar" design[14] with 50% of the pillar embedded into the side boundary of the array. In addition to several pillar array parameters (Table 1) varied to elucidate a technologically viable design space, we explored alternative channel geometries that provided sample injection upstream from the pillar array as well as the addition of a detection reagent downstream from the pillar array.

Our fabrication sequence involved two photolithographic patterning steps applied to, respectively, the front and back side of the wafer. Photolithography was performed using a contact aligner (Quintel, Inc). The front side pattern included an array of hexagons placed on the equilateral grid and boundaries of fluidic channels and reservoirs. The back side pattern for each chip consisted of 10 through-wafer access ports arranged in an equally spaced pattern centered on an 18 mm diameter circle matching our fluidic interface. In the first step, wafers were spin-coated with a double-layer resist system (lift-off resist LOR-3A overcoated by positive tone photoresist 955CM-2.1, MicroChem Corp) capable of submicron resolution and optimized for the subsequent lift-off patterning of a 15 nm thick Cr masking layer. Physical vapor deposition of the 15 nm thick Cr layer was performed using an e-gun evaporator. Once a patterned Cr layer was formed on the front side, anisotropic deep reactive ion etching (DRIE) of silicon was performed using a Bosch process (System 100 Plasma etcher, Oxford Instruments, detailed etch parameters are included in the ESI†) until targeted channel depths and pillar heights were achieved. The etched profiles and patterns were inspected using a contact profilometer (Dektak, Veeco Inc.) and scanning electron microscopy (JSM-7400F SEM, Jeol, Inc.). The front side processing was concluded by deposition of a non-conformal capping layer of silicon oxide with a nominal thickness in the range of 2.5 to 6 μm using PECVD (System 100 plasma deposition tool, Oxford Instruments). This step was followed by deposition of a 2 to 2.5 μm thick masking PECVD silicon oxide layer on the back side. Spin-coating and photolithographic patterning of a positive tone photoresist (SPR 220-4.5, MicroChem Corp) on the back side created a mask for RIE to etch through the masking silicon oxide layer and to expose the Si substrate in the areas corresponding to the through-wafer ports. In the final processing step, Si in the exposed areas was etched entirely through the wafer using the DRIE Bosch process. The processed wafers were scribed and cleaved and silicon oxide membranes remaining on the front side of the through wafer ports were removed manually using sharp pointed tweezers.

Table 1 Geometrical design parameters of fabricated pillar arrays

Design iteration	Channel width/μm	Pillar diameter/μm	Pillar pitch/μm	Etch depth/μm
A1	1800	0.8	1.8	10–12
A2	2100	0.8	1.8	12–15
B1	250	1.4–1.6	2.4	18–25
C1	100	1.4–1.6	2.4	18–22

Sealing procedure

Adhesive cover windows were prepared by spin-coating a photopatternable silicone compound (Dow Corning WL5150) to a film thickness of approximately 10 μm onto 2 mm thick glass slides. The silicone coated glass slides were then cured using a modification of the procedures described previously.[15] More specifically, the coated slides were placed onto hotplates using the following sequence: 2.5 min at 90 °C, 2.5 min at 115 °C, and 5 min at 130 °C. Further curing of the silicone compound was initiated by a flood exposure on a contact aligner for 55 s followed by heating on a hotplate for 15 min at 115 °C. Finally, the prepared glass cover window and the processed silicon

microfluidic chip were placed into contact, creating a sealed device, which was further cured for an additional 20 min at 90 °C under a pressure of approximately 20 psi.

Fluidic interface

Our experimental setup included a fluidic interface designed to facilitate coupling of the fabricated chips and an external fluidic system that provided controlled eluent flow and sample injection. Fig. 1 depicts the main components of our experimental setup. The overall design of this system is analogous to those previously used in conjunction with medium pressure separation chips.[5,16] A pressure regulator on the nitrogen tank provided nitrogen flow at pressures of up to 120 psi that was split into three channels. Each of the channels contained a precision regulator (Airtrol Components Inc.) that enabled further attenuation of pressure in the range of 0–120 psi with an accuracy of ±0.1 psi. A 10-port valve (Valco Instruments Co. Inc.) provided switching between the two regimes: (i) injection of the sample plug into the main channel and (ii) sweeping the plug with the eluent. Fluorescein sodium salt (Sigma Aldrich) and Rhodamin B (Lambda Physik) in a form of methanol (Sigma Aldrich) or methanol–water solutions were used as model analytes in our sample injection experiments.

Table 2 shows the valve connections which provided the functionality required for sample plug injection and separation experiments. In addition to the sample and eluent channels, a third channel was included in our setup in order to explore prospective new modes of post-column detection, for instance, based on generation of fluorescence or Raman scattering signals[17,18] upon addition of an appropriate reagent. This channel was controlled with a separate in-line shut-off valve (Idex Health and Science) inserted between the chip and a pressurized vessel.

In order to provide a quick, reliable and reversible connection of the chip to several fluidic inlets, we have designed and implemented a chip holder that also serves as a chemically inert fluidic manifold. The overall idea of this interface is analogous to that recently described by Burg *et al.*,[19] except that no electrical connections are needed for our experiments. The chip holder is comprised of a delrin disc with 10–32 threaded ports that can be readily attached to 1/16″ OD tubing *via* standard HPLC type

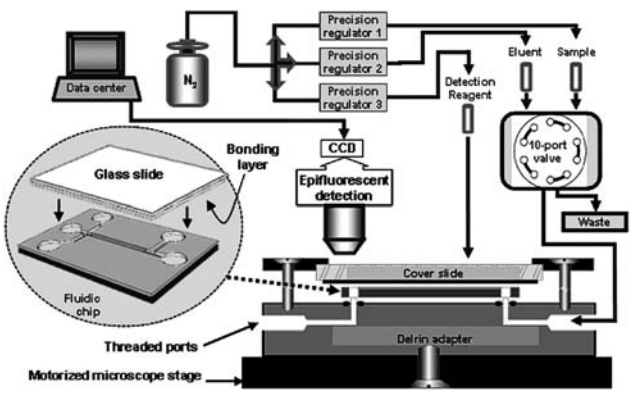

Fig. 1 Schematic illustration of the experimental system with a fluidic interface for fluorescence imaging and functional characterization of the chips with pillar arrays.

Table 2 10-port valve for injecting sample plugs into the column: port connections in the system shown in Fig. 1

Eluent flow		Sample Injection	
(1) Eluent	(2) Column inlet	(1) Eluent	(10) Blocked
(3) Blocked	(4) Sample injection	(2) Column inlet	(3) Blocked
(5) Sample	(6) Blocked	(4) Sample injection	(5) Blocked
(7) Column outlet	(8) Waste	(6) Blocked	(7) Column outlet
(9) Sample Waste	(10) Blocked	(8) Waste	(9) Sample waste

fittings (Upchurch Scientific Inc.). A series of 1/16″ diameter holes drilled in the delrin disc form a fluidic manifold; top portions of the holes are machined to accommodate standard size O-rings (size 0, SIMRIZ perfluoroelastomer, Small Parts Inc.). An aluminium ring placed on top of the chip and secured by six screws provided the pressure necessary to hold the chip and seal it against the top surface of the manifold while allowing for microscope objective access, *i.e.* a clear view of 75% of the area of the chip. The dimensions of the components in this assembly mounted onto a motorized microscope stage of a Nikon Eclipse 100 microscope were chosen to accommodate 5× to 20× microscope objectives with working distances as small as 3 mm. The microscope was equipped with a high pressure Hg light source, a multicolor filter cube, and a Digital sight CCD camera (DS-2M, Nikon, Inc) controlled by NIS-Elements software. The joystick controlled motorized stage was used to match the field of view to the part of the channel with a sample plug. In particular, the motorized stage enabled convenient tracking of sample plugs along the fluidic channel during time series image acquisition at rates of up to 12 frames per second. The CCD camera acquisition times were in the range 80 to 120 ms.

Results and discussion

Optimization of pillar shapes and the capping layer

Fabrication of enclosed pillar arrays with high aspect ratios and approaching perfectly cylindrical shapes required several iterations of fabrication sequence and down selection among alternative processes. This primarily involved optimization of the Bosch etch of silicon and non-conformal PECVD of silicon oxides. It is worthy to note that non-conformal deposition of PECVD layers is frequently used as a technological strategy for sealing or capping high aspect ratio structures for on-chip fluidic applications. Examples include a method for sealing high aspect ratio channels[10] and producing porous SiO_2 microfluidic channels for electrokinetic separations.[20] In the majority of such studies evolution of pore shapes as a result of PECVD capping was not critical and, therefore, no particular attention was paid to maximizing non-conformality. By contrast, the predicted performance of highly ordered pillar arrays for pressure driven separation depends critically on the constant pore size along the

channel depth.[21] Hence, our key task was to optimize a sequence of the Bosch etch and the PECVD process so that near perfect vertical sidewalls could be formed in the resulting structures.

Fine tuning of the Bosch process involved varying the duration of the etch and deposition steps. As a result, pillar arrays with nominal diameters of 0.8 to 1.6 μm, aspect ratios (height-to-diameter) as high as 25 : 1 and sidewall angles with deviations of less than one degree from vertical were obtained. Reliance on a Cr film as a hard masking layer for Bosch etch rather than on a silicon oxide or photoresist appeared to be quite critical to reliably achieve high aspect ratio pillar shapes and to eliminate possible photolithographic artifacts. In addition to the excellent masking capacity of 15 nm thick Cr layers for the Bosch silicon etch, we also found that a slight overhang of a Cr mask formed on the top of each pillar was favorable for subsequent sealing with PECVD silicon oxide. In order to identify parameters of the Bosch etch that corresponded to optimal pillar geometries, SEM images of the pillar arrays were taken and analyzed at different stages during the non-conformal PECVD deposition of silicon oxide. As can be seen in Fig. 2(a–c), in addition to capping pillar arrays with PECVD silicon oxide, this step tends to widen the pillars slightly, preferentially in their top portion. Therefore, pillars with slightly negatively slopped sidewalls (*i.e* with base narrower than top) resulted in almost perfectly cylindrical pillars after PECVD sealing was completed. In order to achieve the maximum degree of non-conformality and minimize "keyholing" effects, several parameters of the PECVD process were adjusted. In particular, relatively high pressures in the range of 1.4 to 1.8 Torr were used. Other parameters of the optimized PECVD process included RF power of 60 W and flow rates of silane (5% SiH_4 in Ar) and nitrous oxide of, respectively, 170 sccm and 710 sccm. The silane to nitrous oxide ratio was selected to obtain nearly stoichiometric silicon dioxide verified by a refractive index of 1.46 to 1.47 at 633 nm. We found that deposition of silicon oxide on the sidewalls in the upper part of the pillars became much more pronounced at pressures below 1.4 Torr while pressures above 1.8 Torr did not cause further improvement in the capping layer. The PECVD parameter space used in this work is included in the ESI.†

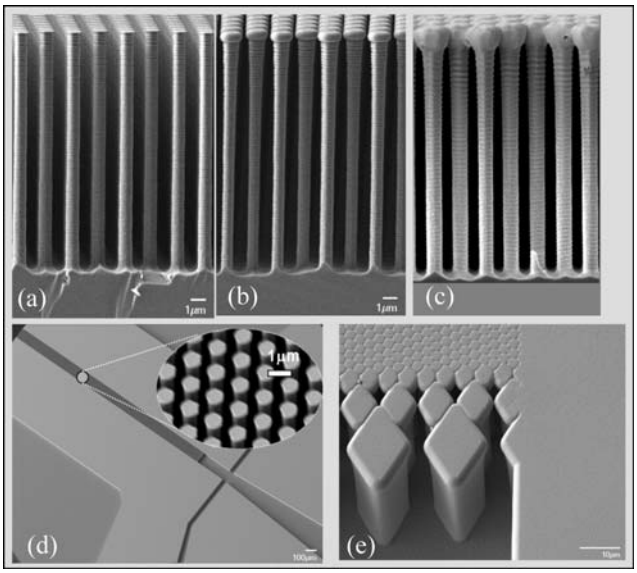

Fig. 2 Top: cross-sectional SEM images illustrating different stages of capping of high aspect ratio silicon pillars with PECVD silicon oxide layer: (a) before capping, (b) partially capped pillars and (c) completely sealed pillar array. Bottom: fragments of the chip viewed in the SEM at a 30 degrees tilt: (d) before and (e) after capping with PECVD silicon oxide.

Fig. 2(d–e) show bird's eye views of the array before and after silicon oxide deposition. Based on the obtained SEM images, it was evident that a PECVD silicon oxide layer of varying thickness covers the whole surface of the pillars. This observation justified a streamlined fabrication sequence without any cleaning of the residual fluoropolymer inevitably formed on the pillar sidewalls as a result of the Bosch etch. The surface of the pillars was thus coated with a non-porous, rather hydrophilic PECVD silicon oxide layer. Although no retentive coating was created on the pillar surface for the purpose of the present study, surface silanol groups of the PECVD silicon oxide provide a straightforward pathway for functionalizing the pillars with a reverse phase coating *via* silane chemistry. Our preliminary experiments confirmed that a silane based surface modification[1] applied to the pillar arrays prior to the chip assembly resulted in retentive pillar arrays suitable for chromatographic separation. Characterization of their loading capacity and retentive properties is a subject of our ongoing work.

In the case of pillars with a nominal diameter of 1.4 μm centered on a hexagonal grid with a 2.4 μm spacing, PECVD of a film with effective thickness (*i.e.* thickness on a planar part of the structure) of approximately 4 μm resulted in a pillar array completely sealed under the silicon oxide capping layer. It appeared, however, that the capping layer also tends to seal the pillar array at its boundaries with an open channel, *i.e.* at the pillar array entrance and exit. This challenge was successfully addressed by introducing additional rows of larger, diamond-shaped features at the entrance and exit of the pillar array shown in Fig. 2(e). We found that pillar arrays with two to three rows of such features always retained their permeability after PECVD sealing was completed.

Chip assembly

We explored a soft bonding approach based on a photopatternable silicone compound and established a procedure that provided a good yield and eliminated the need for the more technologically involved anodic bonding used previously in fabricating analogous structures. It is generally accepted that, compared to anodic bonding, soft bonding is more forgiving with respect to minor defects and imperfections on the surfaces to be bonded. Among many candidates, we identified WL5150 silicone as a compound well suited to form a 10 to 20 μm thick film by spin-coating. Although we did not take advantage of the photopatterning capability of this compound, a combination of UV exposure and thermal baking provided gradual and well controllable curing. We identified the curing conditions, which yielded films with significant tackiness, in turn creating a reliable and reproducible seal upon contact with applied pressure without clogging channels. Our tests showed that the seal withstands pressures of up to 100 psi, but tends to fail above this threshold. As will be justified in a later discussion, these pressures are adequate for many separation applications.

Since WL5150 silicone forms a bonding film similar to other crosslinked silicones, its solvent compatibility was expected to be similar to that of the Sylgard PDMS extensively used in microfluidic devices and examined by the Whitesides group.[22] Silicone-solvent compatibility must be considered not only when performing separations, but also when functionalizing the pillars as solvents are commonly used when creating stationary phases for reverse phase chromatography. We examined the solvent effects of several organic solvents typically used as mobile phase components for chemical separations. Of those investigated, methanol was the most compatible solvent. Toluene, acetonitrile, ethanol, and isopropyl alcohol attacked the bonding film, ultimately causing leakage. During the constant flow of pure methanol through the device at 30 psi a slight leakage was sometimes observed after 12 h. However, when decreasing the mobile phase concentration to 70% methanol and 30% water, the structures showed no leakage during several weeks of continuous experiments. Pure water and aqueous solutions are also compatible with the bonding film. Although the question of solvent compatibility is of high importance to chemical analysis, it should also be recognized that methanol–water solutions are routinely used solvents for many chromatographic applications. Another important similarity of this silicon elastomer and PDMS is the adsorption of small hydrophobic molecules on its surface. In analogy to other microfluidic structures with exposed PDMS surface, certain surface treatments may be used to eliminate or minimize these effects.[23]

Due to the swelling of the bonding silicone film in certain solvents, the cover windows can be removed from the assembled chips. This allowed us to reuse them after cleaning. We found that cover windows could be removed by soaking them in isopropyl alcohol or toluene. The residual bonding material could be removed from the chip and cover slide with common oxidizers, for instance, concentrated sulfuric acid.

Theoretical implications

A series of recent studies by Desmet's group provided extensive theoretical and computational analysis of various aspects of chromatographic beds based on ordered pillar arrays.[2,24,25] They provide convincing evidence that the potential of such perfectly ordered chromatographic beds is high. Consistent with the goals of our present work, we would like to reiterate and highlight specific implications of the pillar arrays with higher densities and characteristic sizes on the lower end of the previously explored range. Generally, the performance measure of a chromatographic separation system is given by:

$$H_T = H_c + H_{ec} \quad (1)$$

That is, total plate height, H_T, is a sum of the column, H_c, and the extra-column, H_{ec}, contributions given that band variances, σ^2, are additive. Extra-column variances are attributed to band dispersion due to injectors, connectors, and spatial and temporal contributions from detection. These are factors dependent on system design; they can be improved upon but seldom altogether eliminated. As can be seen from the relationship $H = \sigma^2/L$, the task of minimizing extra-column variances becomes progressively more critical and challenging as the length of the column, L, decreases, as extra-column variances inevitably become a larger contributing factor to the overall plate height for on-chip applications.

According to recent fluid dynamics studies[2,24,25] plate heights smaller than a particle (or pillar) diameter are possible in uniformly packed systems. A simplified semi-quantitative approach to evaluating the separation performance of ordered pillar arrays and predicting important scaling trends can be based on the well established empirical relationship described by van Deemter:

$$H_C = A + \frac{B}{u} + (C_s + C_m)u \quad (2)$$

wherein plate height, H_C, is dependent on eddy diffusion, A, longitudinal diffusion, B, resistance to mass transfer in both the stationary and mobile phases, C_s and C_m, respectively, and linear velocity, u. The A, B, and C terms in eqn (2) further expand to describe kinetics in a packed column as:[26]

$$H_C = 2\lambda d_p + \frac{2\gamma D_M}{u} + \frac{qk' d_f^2 u}{(1+k')^2 D_S} + \frac{\omega {d_p}^2 u}{D_M} \quad (3)$$

where d_p is particle diameter, k' is the partition coefficient, d_f is the average film thickness of the stationary phase, D_S and D_M are the diffusion coefficients in the stationary and mobile phase, and q, λ, γ, and ω are independent factors conditional on the packing or ordering of the column.

As can be seen from eqn (2) and (3), dominating contributions from different terms may lead to plate heights that are either directly or inversely proportional to linear velocity, u. As a result of this relationship, there is an optimum velocity at which the terms combine to yield a minimum plate height. Differentiation of eqn (1) and (2), *i.e.* $\delta H/\delta u = 0$, yields the equations for optimum mobile phase velocity, u_{opt}, and minimum plate height, H_{min}:

$$u_{opt} = \sqrt{\frac{B}{C}} \quad (4)$$

$$H_{min} = 2\sqrt{BC} + A \quad (5)$$

For the purpose of our analysis, we will consider our ordered arrays of high aspect ratio pillars as performing similarly to a conventional packed column under close to ideal conditions. Although there is a strong dependence of plate height on packing factors (λ, γ, and ω), previously reached conclusions about advantages of perfectly ordered packed beds justify this approach to make conservative estimates. Ideally, all paths in the pillar bed are equivalent and there are no stagnant pools of mobile phase, Therefore, it is reasonable to assume that the packing factor λ approaches zero, and thus the A-term contribution to plate height was not considered here.[4] Experimentally, the factor γ has yielded a value as low as 0.5 for the B-term,[27] which results in $B = D_M$. All solutes are assumed to be unretained, *i.e.* having a capacity factor of $k' = 0$, making $C_s = 0$. Finally, for homogeneous packing, the best case packing factor found in literature is $\omega = 0.02$,[28] so that $C_m = 0.02{d_p}^2/D_M$. Central to our analysis is the strong dependence upon d_p, which is typically referred to as equivalent of the particle diameter. It is worthy to note, however, that there is contention concerning this

parameter. Alternatively to d_p, researchers use the term "domain size", d_{dom}, that combines the packing particle diameter and pore size,[6,25,29,30] others describe d_p as dependent upon external porosity and pillar diameter.[31] While delineating the differences that stem from these alternative treatments is beyond the scope of our current study, we focus on the overall scaling trends, in particular, when characteristic sizes (whether it is d_p or d_{dom}) approach and extend into a submicron range.

By taking into account the assumptions above, we calculated H_{min} and u_{opt} for an unretained species and plotted results of these calculations as function of d_p (Fig. 3). As expected, the values of H_{min} decrease linearly with d_p. This relationship shown in Fig. 3 is consistent with more rigorous theoretical studies by Gzil *et al.*[2] that predict plate heights of 0.3 to 2 μm for uniform 2-D pillar arrays with sizes of 1–3 μm (depending upon k' values), and also with experimental plate height values of $H = 0.9$ μm which were obtained for a uniform pillar array column with a pillar diameter of 4.45 μm.[1] As previously discussed, this is a significant improvement compared with both traditional packed and monolithic silica columns.[32]

While decreasing d_p increases the separation efficiency, it is important to ensure that reduced pore sizes do not translate into pressure requirements beyond what would be practically feasible. Thus, along with estimated plate heights, Fig. 3 shows optimum velocities calculated as a function of d_p for analytes with various diffusion coefficients, D_M. We used two values of D_M that are representative for typical analyte samples with molecular masses of roughly 100 and 100 000 amu.[33]

Considering that $N = L/H$, where N is plate number, well ordered on-chip arrays with submicron d_p have the potential to achieve column performances similar to monolithic and packed columns of conventional lengths. A standard 6″ or 8″ wafer can accommodate designs with straight channels up to approximately 10 cm long. For a pillar diameter of 1.9 μm, a 10 cm long array was calculated to yield $N = 130\,000$.[6] It is, however, difficult to fit more than one chip with 10 cm long columns on a single wafer. Although serpentine channels can be designed to decrease the chip size, column curvature is known to have an adverse effect on band dispersion and, as a rule, should be avoided. Therefore, pillar arrays scaled down to submicron characteristic sizes is a prerequisite of high performance separation beds with a footprint comparable to that of integrated circuits.

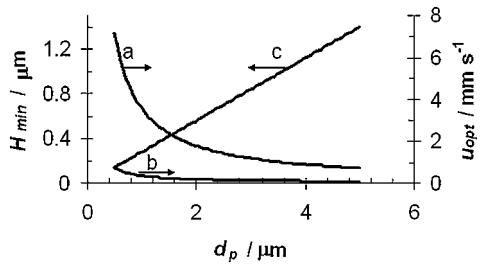

Fig. 3 Theoretically predicted dependencies of u_{opt} (a and b) and H_{min} (c) on pillar size, d_p. Dependencies of u_{opt} are calculated for $D_M = 5 \times 10^{-6}$ cm^2 s^{-1} (curve a) and $D_M = 5 \times 10^{-7}$ cm^2 s^{-1} (curve b), diffusivities representative of typical samples with molecular masses of 100 and 100 000 amu, respectively.

Our implemented design accommodates 9 chips per 100 mm wafer, each with a 10 mm long pillar array integrated into a system of fluidic channels. If theoretically estimated H_{min} is achieved, this design would yield $N = 25\,000$, a sufficient plate number for many applications. Importantly, such a short column length should also translate into decreased analysis times.

Apart from technologically non-trivial aspects of dense pillar arrays with submicron effective pore sizes, their operation may involve challenges of a more fundamental nature, in particular due to the squared dependence of pressure on d_p. Described by Darcy's law and modified for microscopic flow through a packed bed this dependency can be written as:[34]

$$\Delta P = \frac{u_o \eta L \phi}{{d_p}^2} \quad (7)$$

where η is viscosity and $\phi = d_p^2/K_v$ the flow resistance parameter calculated as a function of column permeability, K_v, a term that expresses the resistance of the flow of mobile phase though a packed bed. Of importance to chip applications is the relationship of column length to pressure. Since pressure is directly related to column length it is easy to surmise that decreasing the length of the column may help to alleviate the possible pressure issues that could arise from decreasing pillar/gap dimensions.

To assess permeability of the implemented pillar arrays, flow rate data were collected under varying input pressures. We found that the pressures required to meet the u_{opt} plotted in Fig. 3 are readily accessible for our pillar arrays, even with the employed soft bonding technique. For our C1 design (see Table 1), the pressures in the range of 5–25 psi were sufficient to achieve mobile phase velocities in the range of 0.1 to 0.5 mm s^{-1}. The experimentally measured pressure-flow rate dependency for the C1 design showed an excellent correlation ($R^2 = 0.989$) with a linear function $u_o = 0.026\ \Delta P$, where units of velocity and pressure are mm s^{-1} and psi, respectively.

A notable trend in the plot shown in Fig. 3 is that u_{opt} increases as d_p decreases. This trend means that, as the pillars are scaled down, it may become more challenging to achieve optimal velocities unless the chip retains its functionality under progressively higher pressures. However, as already mentioned above, shorter columns are proportionally more permeable. To make additional quantitative comparisons of the implemented pillar array system to conventional packed beds and monolithic columns, we used our design parameters $L = 10$ mm, $\eta = 5.4$ (*i.e* viscosity of methanol at 20 °C), and $u_o/\Delta P$ and found that the K_v for this system is 2.1×10^{-14} m^2. Using this value of permeability, the flow resistance, ϕ, was found to be 48. This value is in reasonable agreement with a recent study of pillar arrays which predicts ϕ values in the range of 56 to 274, depending upon porosity.[25]

Functional tests

In order to evaluate the overall performance of the designed system and identify areas most critical for its further improvement, we conducted a series of basic functionality tests that included: (i) pressurizing the channels and checking for leaks; (ii) injecting a model fluorescent analyte and analyzing the analyte bands using fluorescence microscopy; and (iii) characterizing permeability (separation impedance) of the pillar array by

measuring fluid velocity as a function of pressure. The protocols for these tests were selected to be analogous to those utilized previously[1] in characterizing similar pillar arrays with larger pillar diameters so that the results of our tests could be analyzed comparatively.

The obtained analyte plug and flow images are shown in Fig. 4. In order to create discrete sample plugs for injection into the pillar bed, our design incorporated a crossed-channel geometry upstream from the array as shown in Fig. 4(a). Using the manual 10-port valve described in the previous section, we performed a two-step injection procedure. In the first step, the sample channel crossing the main channel was loaded by flowing the sample from the sample inlet to the sample waste while the column inlet and outlet were closed. In the second step, the sample plug seen in Fig. 4(a) was swept into the column by closing the sample inlet and waste ports, and opening the column inlet and outlet. Despite timing uncertainties of manual valve switching, this injection procedure could produce sample plugs with a volume below 30 pL. This corresponded to $\sigma \approx 150 \pm 30$ μm, *i.e.* comparable to sample plugs obtained using a computer controlled system of valves and a vertical injection channel design.[5]

Fig. 4(b) and Fig. 4(c) show the sample plug behavior as it enters the pillar bed and 6 mm down the pillar array, respectively. The artifacts seen in the images of the pillar beds in the assembled chips resulted from the air cavities formed frequently upon bonding of the chip and the cover. We found that, upon curing, the silicone elastomer tends to produce a film with slightly undulated (wrinkled) surface, which, in turn, makes it difficult to form a defect free bond. Remarkably, such sealing defects had no adverse effect on the flow behavior and column functionality since the array area of the channel was additionally sealed by the capping silicon oxide layer. This highlights an important advantage of our technological approach that relies on soft bonding combined with pillar capping with a PECVD silicon oxide layer: the silicon oxide layer forms a robust scaffold, protects the pillars from damage and simultaneously seals the pillar bed. On the other hand, in our preliminary fabrication runs there were instances when the silicon oxide capping layer did not seal the pillar array completely. In these cases, permeation of fluorescent sample through the capping layer and its adsorption on the silicone layer could be visualized; nonetheless, the chips maintained its functionality.

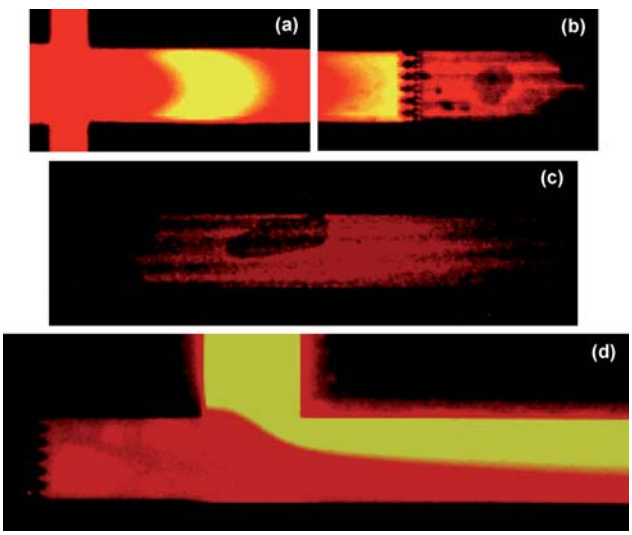

Fig. 4 Fluorescence micrographs of sample plugs injected into the 100 μm wide fluidic channel with an enclosed pillar array: (a) prior to entering the pillar bed, (b) entering the pillar bed and (c) 6 mm downstream inside the pillar bed. The broadening interdiffusion zone at the interface of laminar flows exiting the pillar array and the reagent channel is also shown (panel d). Fluid flow is from left to right. Images obtained using 1×10^{-4} M fluorescein sodium salt in MeOH. Contrast and brightness of the images were adjusted to improve their visual clarity.

Fig. 4(d) shows the flow of a fluorescein solution injected through the auxiliary reagent port into a channel merging with the post-column flow. As expected, the exact flow patterns in this area were found to depend strongly on the pressure difference between the column inlet and the reagent ports. The observed fluorescence images of the sample/reagent interdiffusion zone provide encouraging evidence that, although the flow remains laminar, noticeable flow mixing occurs within 5 mm from the column exit. Therefore, the additional post-column reagent port can be used as a viable means for on-chip modification of the sample exiting the column without any significant band disturbance. We believe this indicates a promising direction in addressing the need to derivatize samples so that they are detectable with a wider range of detection schemes, for instance, based on fluorescent tagging or mixing of a silver colloid to induce surface enhanced Raman signals.[17,18,35] Implementation and evaluation of these approaches is a subject of our future work.

When both the column outlet and the auxiliary reagent port were closed during the sample injection phase, sample plug shapes indicative of a parabolic flow profile were observed (Fig. 4). In the subsequent experiments, we achieved substantial improvement of the plug shapes by leaving the auxiliary reagent port open during the loading phase. Although we could not establish the exact reason for such an improvement, we believe it was related to more abrupt changes in pressure and flow velocity in the system with the column outlet completely blocked during sample injection. Previous studies indicate that profiles of the pressure driven flow in beds of ordered pillar arrays are not always parabolic and, more importantly, negligible local disturbances of the flow at the side walls are possible.[14] In particular, the flat side wall design was shown to create the side wall effect opposite to a commonly observed parabolic flow profile while side walls with 66% of the pillar diameter protruding from the wall caused negligible disturbances of the flow in the wall vicinity.[14]

Using the C1 design (see Table 1 for details), analysis of band dispersion inside the pillar array was performed by collecting time series images as the sample band migrated along the pillar bed and plotting the intensity profiles, as depicted in Fig. 5. As stated in previous sections, no additional stationary phase coating was employed. As can be concluded from our fabrication sequence and SEM images of the pillars arrays (see for instance Fig. 2(a–c)) the pillar surface is presented by PECVD silicon oxide, and therefore, the resulting pillar arrays have little to no retentive properties. In particular, the single component sample of 1×10^{-4} M Rhodamine B in pure methanol was expected to exhibit no retention.

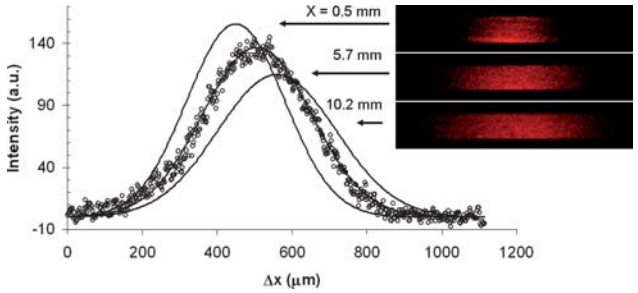

Fig. 5 Intensity profiles and corresponding fluorescence images of a dye plug (injected as 10^{-4} M Rhodamine B solution in MeOH) migrating down the pillar bed of design C1 (see Table 1) at a velocity of 1.7 mm s^{-1}. The experimental intensity profile (open circles in the plot) extracted from the image of the plug centered at $x = 5.7$ mm is shown together with the Gaussian fit (solid lines) of intensity profiles for each image (see details of the fitting procedure in the text). Intensity profiles were measured using unprocessed images prior to any adjustments in brightness and contrast. Contrast and brightness were subsequently adjusted to improve visual clarity of the images shown on the right.

It should be noted that the presence of densely spaced high aspect ratio pillars significantly decreases the efficiency of the optical excitation of the dye and collection of the light emitted within the pillared area. This optical effect is common for high aspect ratio silicon structures, in which light (either incident or generated within) undergoes numerous partial reflections so that very small fraction of the light escapes the structure. In other words, gaps between the pillars act analogously to blackbody cavities. We found that, in the case of submicron inter-pillar gaps with height-to-width ratios in excess of 20 : 1, this effect becomes strong enough to attenuate the measured fluorescence intensity by approximately an order of magnitude in comparison with channel areas without pillars. Due to this factor, the acquired fluorescence images of the sample within pillared areas are characterized by rather low signal-to-noise ratios (see Fig. 5), which, in turn, make analysis of the band dispersion inside the pillar array more challenging. On the other hand, the efficiency of post-column fluorescence band detection is not affected by the blackbody cavity effect of the pillar array.

Since acquisition times of up to 120 ms were used in our experiments, it is reasonable to assume that imaging of fluorescence sample bands moving at a linear velocities of approximately 1.7 mm s^{-1} involved a significant degree of "motion blur". We found, however, that a contribution of the motion blur effect to apparent widening of sample band dispersion, σ, is much less than a product of exposure time, Δt, and linear flow velocity, u. The exposure time effect is particularly small in the case of imaging sample bands with a wide Gaussian profile. We quantified apparent band widening due to a non-zero exposure time by analyzing computer generated Gaussian profiles (see ESI†) and found that for a linear flow velocity of 1.7 mm s^{-1} and band dispersions, σ, in the range of 50 to 200 μm, 90 ms exposure time corresponds to, respectively, a 24 to 6 μm increase in apparent dispersion. Hence, the exposure time effect is stronger for shorter sample bands, and, therefore, it tends to decrease apparent band dispersion. We found that for a sample plug with $\sigma > 120$ μm, the camera blur effect adds less than 10% error when deducing the on-column plate height $H = \Delta\sigma_x^2/\Delta x$ from our experimental data. Therefore, sample plugs with $\sigma > 120$ μm were selected and used in our plate height analysis.

Recognizing the somewhat limited sensitivity of our fluorescent measurements, we assumed that a part of the sample band far from its center corresponded to the fluorescence intensity level below the noise floor. We further assumed that there is no change in the optical response factor or loss of sample material within the column, and, therefore, the area under intensity profiles can be expected to remain constant. Next, the peak height and the dispersion, σ^2, were determined by fitting the experimental data (symbols in Fig. 5) to a Gaussian distribution (solid lines in Fig. 5) using the non-linear fit function in Origin 8. As can be seen in Fig. 5, the experimental data fit reasonably well to the Gaussian distribution when the noise floor is taken into account.

The on-column plate height $H = \Delta\sigma_x^2/\Delta x$ experimentally determined by analyzing intensity profiles centered at $x = 0.5$ mm, $x = 5.7$ mm and $x = 10.2$ mm (Fig. 5) was found to be $H = 0.76$ μm. This indicates that experimentally observed band dispersion is noticeably higher than the theoretically predicted value of $H_{min} = 0.28$ μm. Taking into account previously reported data on the band dispersion in ordered pillar arrays with larger domain sizes,[14] a conclusion can be made that disturbances near the channel side walls as well as bottom and top walls are largely responsible for the difference between the theoretically predicted and experimental values. Indeed, side wall effects are always present and inevitably contribute to on-column band dispersion. As the pillar diameter and channel width decrease, the local flow at the side walls becomes more sensitive to the imperfections and inaccuracies in the pillar array design. In addition to the channel side wall effects, the following factors could contribute to the deviations of the experimentally determined plate heights from the theoretical predictions: (i) the system was operated at flow velocities $u = 1.7$ mm s^{-1}, substantially below the theoretically predicted optimal $u_{opt} = 3.2$ mm s^{-1}, (ii) as discussed previously, a finite A-term in the van Deemter equation may exist even in a perfect pillar array,[36] and (iii) the B and C terms of the van Deemter equation were treated under the assumption of an ideal pillar array with perfectly uniform sizes. Nonetheless, the value of $H = 0.76$ μm, corresponding to remarkably low on-column dispersion, shows improvement upon previous reports and validates the motivation for additional studies of submicron pillar arrays with applications in on-chip analysis and separation.

It is important to emphasize that the theoretically evaluated plate height, H_C, is entirely a result of variances (*i.e.* band dispersion) intrinsic to the column, as described by eqn (1). The total plate height of the system incorporates additional contributions determined by other factors, in particular, the finite length of the injected sample plug. While our current chip designs meet the goal of a streamlined fabrication sequence and characterization of on-column band dispersion, we recognize that improvements in the sample injection will involve significantly more complex chip designs. The task of precise high-pressure injection of sample plugs substantially shorter than 100 μm with volumes below 10 pL is not trivial. Analysis of the literature data as well as our own observations indicate that controllable injection of such sample plugs will require on-chip sample manipulation, for instance by using on-chip valves. Several types

of previously developed on-chip microfluidic valves can be integrated with ordered separation pillar arrays described in the present study. Identifying and implementing the best strategy for injection of very short sample plugs is a subject of our ongoing effort. Our preliminary analysis of several different approaches, in particular bottom slit injection,[5] virtual valve approach,[37] on-chip mobile monolith,[38] and elastomer membrane valves,[39] indicate that the latter is most promising and compatible with the enclosed pillar arrays described herein.

Conclusions

Compared to traditional separation columns, the fundamental advantages of ordered pillar arrays were unambiguously demonstrated in recent theoretical and experimental studies. Technological and experimental challenges of such systems, however, have been an impeding factor for the wide spread adaptation of this novel concept. Theoretical estimates indicate that very dense pillar arrays scaled down to submicron characteristic sizes are a prerequisite of separation beds suitable for high performance separation with a footprint comparable to that of integrated circuits. Therefore, a viable technological path toward submicron pillar arrays with submicron theoretical plate heights is a critically significant milestone in this area. By refining well established fabrication processes and implementing novel technological sequences, we demonstrated ordered uniform beds of pillar arrays that are integrated into a system of on-chip fluidic channels and are scalable well into the submicron range. The implemented structures satisfy the fundamental criteria of high performance separation in the on-chip format while also providing reasonably high fabrication throughput. We anticipate that the demonstrated system will facilitate further experimental studies of ordered pillar arrays with applications in pressure driven liquid chromatography as well as newly emerging separation techniques.[8,16,40]

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