Solid State Lighting Technology and Application Series

Jinmin Li
G. Q. Zhang *Editors*

Light-Emitting Diodes

Materials, Processes, Devices and Applications

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Solid State Lighting Technology and Application Series

Volume 4

Driven by societal needs and challenges, fast development of LED and semiconductors technologies, lighting is going through a radical transformation. This transformation is characterized by continuous and aggressive efficacy increase and cost reduction to replace traditional light sources by LED; revolution of forms and fixtures; seamless integration of LED light sources with semiconductors to create digitalized and smart lighting systems and solutions; emerging of "more than Illumination" functions and applications by using LED for healthcare and wellbeing, horticulture and food, communication, safety and security, etc. The success of this lighting transformation depends on not only the industry and market development, but also the creation and exploitation of new fundamental knowledge and talent development. This book series is the concerted action of global experts from industry and academia. It aims to provide the state-of-the-art fundamental theory and knowledge, the latest technology development, best industrial practices and guidance for academic research, technology and industrial development. It will cover all aspects of development of SSL, such as materials, device technologies, packaging and modules, luminaries & systems, thermal management, testing, reliability, total life time management, equipment, power management, sensors, communication and control, design and architecture, and other newly emerged scientific domains.

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Foreword

From the report of red light-emitting diodes (LEDs) by Nick Holonyak in the 1960s to the Nobel Prize in Physics awarded for the invention of blue LEDs in 2014, we have witnessed many historical milestones of LED research, development, and industrialization. It is no exaggeration to say that solid-state lighting (SSL) based on compound semiconductor materials has revolutionized artificial lighting. Benefits of the progress in lighting technology on civilization have led to a greatly improved standard of living for all of mankind. For instance, SSL has enabled the realization of bright and energy-saving white light sources, full-color display, and projection. Besides, many novel and emerging applications have been possible thanks to the SSL technology, such as visible light communications, LED-enabled medical treatment, and lighting for semiconductor manufacturing, agriculture, fish industry, horticulture, and animal breeding. These achievements have dramatically expanded the application boundary of lighting, marking a brand new horizon of illumination. At the same time, they have also triggered new challenges for future research and technology development.

Contributors to this book are global leading SSL engineers and scientists. They provide an overview of the latest developments in the relevant areas, as well as their personal views about future development directions. It covers wide aspects of the device from deep ultraviolet to the visible spectrum made from compound semiconductor materials. This book is divided into four parts, and the concept covers all key processes of the research, from epitaxial growth of the materials on different substrates, structure design and optimization, packaging, and reliability to the emerging applications. This book will be of interest to scientists and engineers working on LED technology and applications, as well as graduate students in material science, optical engineering, applied physics, and electrical engineering.

Nagoya University, Nagoya, Japan Hiroshi Amano

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Chapter 1
GaN Substrate Material for III–V Semiconductor Epitaxy Growth

Rong Zhang and Xiangqian Xiu

1.1 Introduction

Wide bandgap semiconductor is known as the third-generation semiconductor material, as the engine and key technology of high-temperature, high-frequency, high-power semiconductor devices and IT industry. Wide bandgap semiconductor refers to the wide bandgap in 2.0–6.0 eV semiconductor materials, including SiC, GaN, ZnO, AlGaN, etc. The excellent properties, such as big bandgap, high breakdown electric field intensity, high saturated electron drift speed, big thermal conductivity, small dielectric constant, strong radiation resistance, and good chemical stability, make them well suitable for the radiation-resistant, high-frequency, high-power, and high-density integration of semiconductor devices. Based on the wide bandgap, the blue, green, and ultraviolet light-emitting devices (LEDs) and light detector have been developed and commercialized.

The III-N materials enable new semiconductor devices with previously unobtainable performance capabilities in terms of light output, power handling, and efficiency, and these attributes will make possible the reinvention of existing technologies in ways that benefit many facets of our lives. More application fields accelerate the marketization. While there are many potential applications for these materials, the biggest applications appear to be light generation and the control of electrical power. Driven by optoelectronics, particularly GaN-based laser diodes (LDs) and high-brightness GaN-on-GaN LEDs, the market for bulk GaN substrates is expected to grow at a CAGR (compound annual growth rate) of 10% from 2017 to 2022 and could reach more than 100 M$ in 2022, according to a recent market survey from Yole Développement.

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In this paper, we summarize the major efforts in GaN substrate development and present the current progress in producing large-scale high-quality GaN substrate materials. We discuss the advantages of using the native GaN substrates with respect to the current heteroepitaxial nitride-based devices.

1.1.1 Importance of GaN Substrates

Bulk crystals of nitrides cannot be obtained by well-known direct synthesis methods such as Czochralski or Bridgman growth from stoichiometric melts, because of the extreme physical conditions, such as high melting temperature and very high decomposition pressure at the melting point (molten gallium nitride under 2225 °C and the pressure of 6 GPa). Growth of semiconductor-quality crystals at these conditions would be practically impossible. Therefore the crystals have to be grown by the methods requiring lower temperatures. In the past, large-scale high-quality GaN films are mostly grown on the heterogeneous substrate for a long time.

Sapphire is the most commonly used substrate for the hetero-epitaxy of GaN but is far as a kind of ideal substrate for GaN-based LEDs except the low cost. Its two biggest disadvantages are that the obvious difference of the lattice constant and the thermal expansion coefficient compared with GaN. This will cause the strain in the GaN epitaxial layer, and strain can produce point defects and dislocations, which reduces the quality of GaN epitaxial layers and InGaN quantum wells. The defects and dislocations can limit the light-output efficiency of LED devices.

As a substrate for sapphire, there are two very important obstacles in the manufacturing of high-performance LED. One is the electrical insulating properties of sapphire. Sapphire substrate with the high resistivity is not ideal for the LED devices, because the top contact electrode restrained its transverse current density for the inversion structure of LED devices. This will lead to the current crowding effect and local hotspots, which will be unfavorable factors for the LED luminous efficiency and the maximum brightness of the device. The second, sapphire, has the characteristics of big thermal resistance and also can seriously hinder the ability of heat dissipation, which in turn will further restrict the luminous efficiency and the life and brightness of the devices.

In order to solve these problems, people invented all kinds of technology to improve the luminous efficiency, life, and power. According to the above two obstacles, high-end technology used by LED chip maker is GaN epitaxial layer transferred to the substrates of good electrical and thermal conductivity properties. Usually by laser stripping and wafer bonding process, the LED chip structure will be laser stripping down from sapphire substrate and then transferring to bond with another kind of thermally conductive substrate. The laser stripping process involves usage of pulsed 248 nm KrF excimer laser. The laser is strongly adsorbed at the the sapphire/GaN interface and results in decomposition of the 100 nm thick GaN thin layer, which lead to the separation of sapphire and GaN. The technology is widely applied in the high-power LED device.

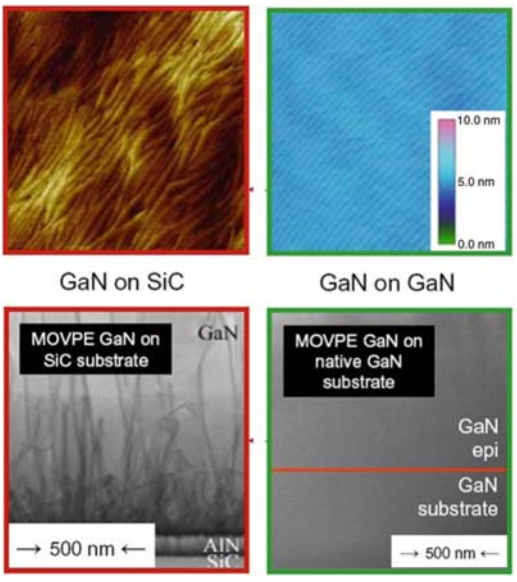

Fig. 1.1 Homogeneous epitaxial GaN films have higher quality and lower dislocation density, even compared with the best foreign substrate SiC

In fact, the most suitable substrate materials for the fabrication of LED should be native GaN substrate. Availability of lattice-matched GaN substrates can bring not only a high quality in GaN-based devices to improving device performance through eliminating the structural defects and providing better vertical electrical and thermal conductivity; moreover, it will lead to cost-efficient device processing through simplification of the epitaxial growth process by eliminating the need for low-temperature buffer layers.

As shown in Fig. 1.1, even if compared with the best foreign substrate, homogeneous epitaxial GaN has a higher quality and lower dislocation density [1]. It can improve the quality of the epitaxial layer and quantum well because of the proper lattice and thermodynamics match. It also has almost all of other advantages as follows. Although GaN substrate is more expensive, the area of one single chip on GaN substrate wafer is greatly reduced, which means that a single chip can use as three traditional chips. LEDs based on the GaN substrate have greater drive current, higher luminous efficiency, and simple process to the very good application prospect. Usually, GaN substrate is n-type conductive, which is beneficial to make vertical structured LED. Compared with traditional vertical structure in production of sapphire substrate to use laser liftoff process, it can bring the simplified processes and can reduce costs, raising the yield to achieve the higher cost performance.

In recent 10 years, researchers around the world have made an important progress in the study of the freestanding GaN substrate. And in the next few years, GaN substrates suitable for the devices with a diameter from 3 in. to 6 in. will be mass production.

1.1.2 *Key Drivers for GaN Substrate Commercialization Success*

One of the areas for the application of GaN substrates is in GaN laser diodes (LDs), where GaN substrates provide a clear and immediate benefit in the earlier days. The new applications for GaN-based LDs are primarily for next-generation, high-definition DVD players and recorders, although other applications include high-definition video projectors and displays, commercial printing, and testing and measurement applications, such as spectroscopy and bio-sensing.

There is no doubt that LED technology will take market share over the traditional lamp and tube business. In either a cautious or a more aggressive scenario, LED applications will certainly be the key drivers for the bulk GaN market, according to Yole Développement.

The report "Bulk GaN substrate market 2017" from Yole notes that while the Blu-ray segment which in the past was the GaN-based laser industry's main driver continues to decline, it is expected to be offset by nascent, growing segments like projectors (office projector, mobile pico projector, head-up display, etc.) and automotive lighting, leading to new growth opportunities for bulk GaN substrates. When new devices are developed and demonstrated and new areas of commercial demand are generated, this can provide further motivation for substrate manufacturers to increase manufacturing capacities. For example, Fig. 1.2 shows the forecast for TIE (2 in. equivalent) GaN wafer volume for device applications, with unit volumes at nearly 350,000 in 2022. This volume forecast represents a tremendous opportunity for GaN substrates but will require significant cost reduction in order to meet expected cost requirements.

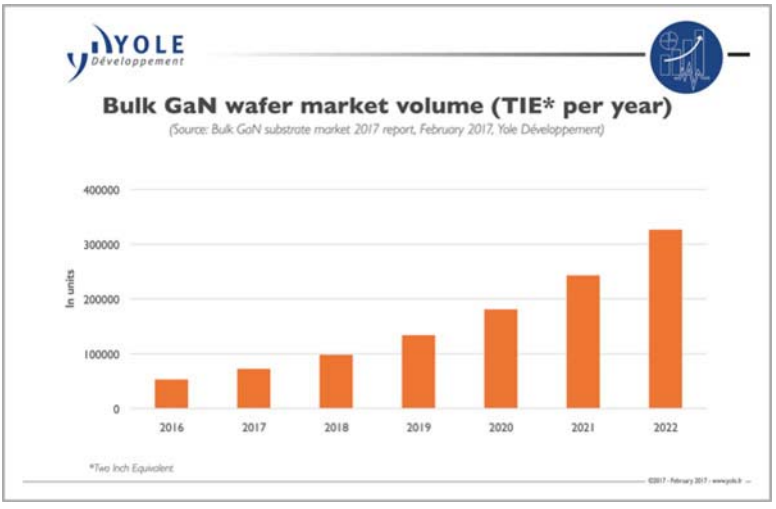

Fig. 1.2 TIE GaN wafer forecast for device applications. Source: Yole Développement

Considerable technology development is needed to enable penetration of GaN devices into the solid-state lighting (SSL) and power electronics markets. The performance of the GaN devices must be improved in many areas: LED luminous efficacy at high lumen output, FET and diode breakdown voltage and on-resistance, and power switching reliability, among others. The latest report reveals more and more GaN-based devices fabricated on advanced GaN substrate. At the same time, with the increase of demand of blue laser diode, UV LED, and high-power, high-frequency devices, the amount of GaN or AlN substrates is increasing. Only the high quality of substrate can provide high-performance device because of lattice matching and excellent thermal management features. Bulk GaN substrates are expected to be used for many devices addressing these market opportunities, but there are numerous challenges facing the adoption of bulk GaN substrate technology.

Above all, substrate cost must also be significantly reduced in order to become economically practical in the device applications, which is particularly challenging due to incumbent GaN device technology based on foreign substrates. GaN substrate materials provide clear and immediate benefits for GaN-based LD applications over sapphire-based approaches, particularly at higher operating current density, and GaN substrate manufacturers are currently focused on addressing this market. Other benefits for LEDs, RF FETs, power devices, and photodetectors have been shown, but commercialization of these devices requires high volumes of low-cost substrates. These improvements will occur through the continued development of bulk growth techniques, such as HVPE, ammonothermal growth, solution growth, and combinations thereof.

As these improvements are made, the potential for III-N devices to do more (more light, more power) with less (higher energy efficiency, less electricity, less waste heat) will be enabled.

1.2 The Technical Routes for GaN Substrate Materials

Because the homo-epitaxy on GaN substrates has better advantages compared with the hetero-epitaxy, then research about GaN substrate is of great practical value. Now the basic ways for GaN substrate materials have generally the following three technical routes (as shown in Fig. 1.3) (Substrates for Nitride Epitaxy, IWN2008, Switzerland, 2008).

1.2.1 Native GaN Substrates

One of the most important approaches to obtain GaN substrate wafers is to obtain a larger dimension of columnar bulk crystals or boule. A lot of experimental studies have shown that GaN at the top of the columnar crystal has very high quality. Bulk GaN crystals can be obtained by high-temperature and high-pressure solution method, ammonothermal growth, Na-flux growth, or the combination of a variety

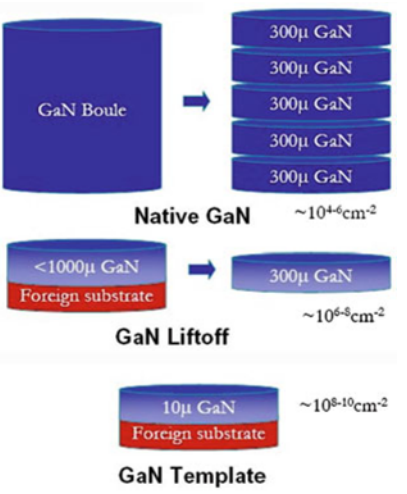

Fig. 1.3 Three technical routes for GaN substrate materials (IWN2008, Switzerland, 2008)

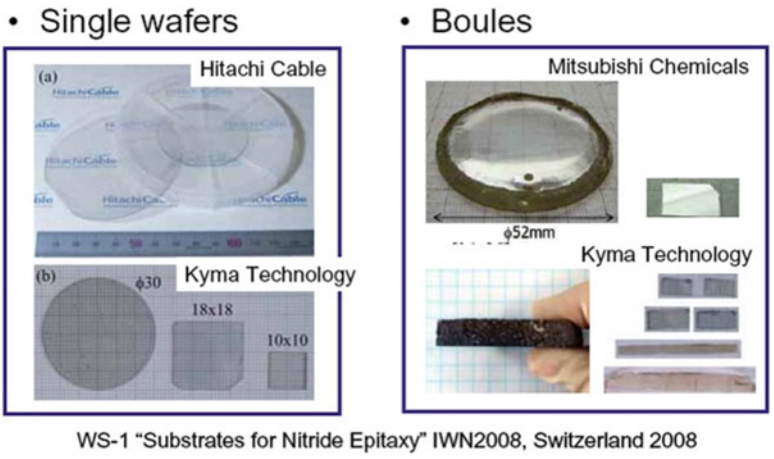

Fig. 1.4 Native GaN substrates reported by some companies (IWN2008, Switzerland, 2008)

of ways. High-quality GaN chips can be got by cutting GaN crystal into flakes and polishing, and the dislocation density for GaN crystal in different ways is usually between 10^4 and 10^6 cm^{-2}. Thicker pear-shaped or columnar crystals can not only produce more chips, but also can further reduce the defect density. So the most ideal solution to solve the problems of GaN substrate is to obtain single crystal GaN substrate chips by the abovementioned methods. But although GaN substrates have been reported (as shown in Fig. 1.4), GaN native substrates with a large size of more than 2 in. have not been commercialized. As shown in Fig. 1.4, the large size of columnar crystal is still mainly grown for a relatively long time by the method of hydride vapor-phase epitaxy (HVPE) or the combination of HVPE and other technologies.

Among all the bulk growth techniques under investigation today for nitrides, HVPE is the most promising technique since it utilizes a process with more favorable conditions, such as the low pressure and relatively low growth temperature. Because of the high growth rate, its growth process is also cost-effective. Other techniques, such as Na-flux or ammonothermal growth, are still under development.

1.2.2 GaN Liftoff Substrate Wafers

Until now, hydride vapor-phase epitaxy is considered as a highly practical method by growing the GaN thick films for quasi-bulk substrates after the separation from the foreign substrates or obtaining GaN boules with a thickness of more than centimeter grades to be sliced to fabricate native bulk substrates.

The biggest advantage of the technique is its ability to produce high-quality material at high growth rates due to a high surface migration of the halide species. The versatility of HVPE as a growth method is motivated for both device applications and substrate application.

HVPE-GaN thick film is usually grown on foreign substrate with the thickness of more than 500 μm and less than 1000 μm at a growth rate of between several microns and 1000 μm. And then the foreign substrate is peeled by laser liftoff (such as sapphire substrate), chemical corrosion (such as Si and GaAs substrate), or mechanical thinning or self-separation by utilizing the change of stress. After the thinning or polishing of self-standing GaN thick film, GaN substrate wafers would be obtained. Due to the lattice mismatch from the heterogeneous substrate, the lattice distortion introduced by the atom cannot completely eliminate the stress, so the dislocation density is roughly between 10^6 and 10^8 cm^{-2}. Now, 2 in. GaN wafers by HVPE method have been commercialized, but the price is quite higher. Due to the technical reasons, the yield is low. The HVPE-GaN wafers are mainly used in industry of GaN LDs; the mass application in the field of LEDs is not yet mature.

1.2.3 GaN Templates

GaN template refers to the compound substrate grown on heterogeneous substrate, which the thickness is more than 10 μm (Fig. 1.5). And compared with MOCVD GaN of the thickness of a few microns, the dislocation density is slightly lower and generally 10^8 cm^{-2}. The increase of the thickness will further reduce the dislocation density, and the dislocation density of free standing GaN substrate can reduce about two orders of magnitude (Fig. 1.6). The results show that with the increase of the thickness of GaN template from 5 to 50 to 150 μm, the dislocation density is reduced from 10^9 cm^{-2} to 5×10^8 cm^{-2} to 1×10^8 cm^{-2}. The thickness of GaN templates is generally less than 50 μm, and GaN template with the thickness of more than 50 μm will be easily cracked due to large lattice and thermal mismatch between

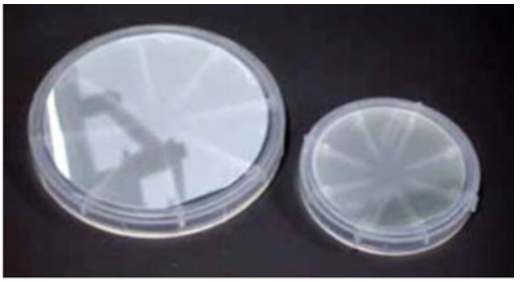

Fig. 1.5 GaN templates on sapphire substrate

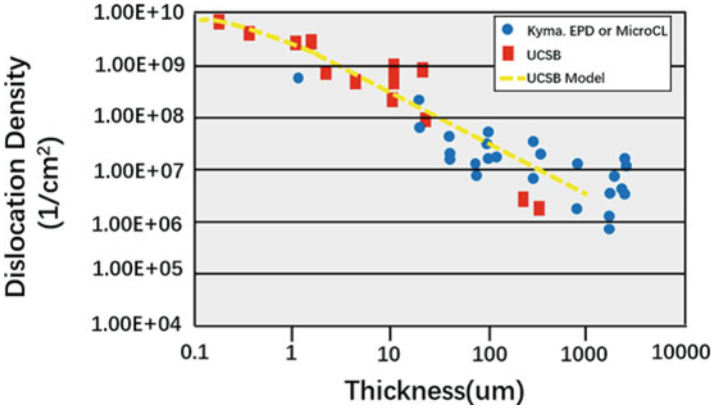

Fig. 1.6 Comparison of the dislocation density of different GaN films (source: Cree, Inc.)

GaN and sapphire. Due to the low cost and high quality, GaN templates by HVPE have the very big potential applications.

1.3 Major Methods for the Growth of GaN Substrate

GaN at high temperatures is decomposed into Ga and N_2, only melting in the physical conditions of more than 2200 °C and 6 GPa above nitrogen pressure. So the traditional Czochralski or Bridgman method cannot be used for the growth of GaN single crystal. At present, GaN is generally grown by hetero-epitaxy of MOCVD and MBE. In order to get high-quality GaN film, almost all the growth of technology and the substrates have been tried. But the high defects in the hetero-epitaxy GaN can limit the improvement of the GaN-based device performance. At the same time, research on the growth technologies for bulk GaN crystals has never stop, and a lot of trial and effort has been carried out, including the liquid-phase and gas-phase growth.

1.3.1 The Liquid-Phase Growth

The common liquid-phase growth methods are mainly high-pressure nitrogen solution growth (HPNSG), Na-flux dissolved agent method, and ammonothermal method, which all these three methods can prepare high-quality bulk GaN crystal.

As the homo-epitaxy substrate, GaN obtained by the liquid-phase growth will overcome the deficiency of the hetero-epitaxy. In addition, the photoelectric properties of GaN crystal by the liquid-phase growth are excellent, which is suitable for the high-performance devices. So the liquid-phase methods have also attracted more attention for the preparation of high-quality GaN crystal.

1.3.1.1 High-Pressure Nitrogen Solution Growth (HPNSG)

In the liquid phase growth technology of gallium nitride, high-pressure nitrogen solution growth is the most commonly used method for single crystal growth. Early in the mid-1970s, GaN single crystal with a diameter of about 1 mm was obtained by this technology. Its growth principle is shown in Fig. 1.7 (left); to put the high-pressure nitrogen gas into the molten state of Ga in the high temperature of crucible, enough N can be dissolved into the high-temperature molten metal Ga; nitrogen molecules on the surface of the molten Ga would be decomposed into N atoms and react with Ga to form GaN. GaN single crystal would be prepared at a certain temperature gradient for the local supersaturation of N atom. At that time, the temperature and pressure were only 1200 °C and 10.8 GPa. Because GaN is very stable at high temperature and high pressure, the dissolvability of N atoms is very

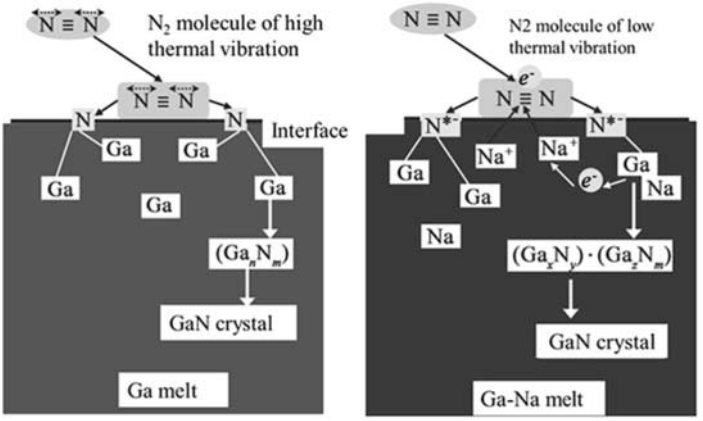

Fig. 1.7 Growth mechanism of GaN by HPNSG (T = 1300–1600 °C, PN_2 > 1 GPa) (left) and Na-flux method (T = 600–850 °C,PN_2 > 0.1 GPa) (right)

low in the molten metal Ga (atomic number scores less than 1%) [2], which leads to a decline of GaN crystal growth rate (about 1 mm/24 h) [3]. So it must be long enough to grow the large-size and high-quality GaN single crystal. Of course, due to the growth conditions of the high pressure, the crystal defect is extremely low and suitable for the preparation of high-quality crystal [4].

After more than 10 years of development, as the experimental conditions change, the temperature and pressure have been effectively improved to 2300 °C and 4 GPa. GaN single crystal by HPNSG method is generally a hexagonal flake structure, along with the [0001] direction of wurtzite structure. A suitable temperature gradient can improve the growth rate of [0001] direction at a certain extent. But too large temperature gradient will affect the stability of the growth, which will lead to the honeycomb structure in the GaN surface [2]. HPNSG GaN single crystal has good crystallization quality commonly by XRD rocking curve test; the full width at half maximum along the major axis and the vertical straight in the axis direction is only, respectively, 0. 028° and 0.017°, which is similar to the quality of the crystal.

High-pressure nitrogen solution method can be used for the preparation of high-quality GaN crystals, but this growth of GaN requires very high pressure in the range of GPa which sets rigorous standards for the growth facilities, the high production costs is not conducive to large-scale industrial production.

1.3.1.2 Ammonothermal Growth

From the angle of the crystal growth, the basic principle of ammonothermal crystal growth is similar with that of hydrothermal method. The ammonothermal process is a solvothermal process that allows the solubilization of polycrystalline III-nitride nutrient or feedstock in supercritical ammonia under high pressure by utilizing a solubilizing agent or mineralizer. The dissolved nutrient is then transported to the region of crystallization, where it recrystallizes on seed crystals or through self-seeding. A schematic of the internally heated growth system and a photo of a 2 in. diameter crack-free, as-grown bulk crystal are shown in Fig. 1.8, respectively [5, 6].

The growth process of GaN single crystal by ammonothermal method can be summarized as follows: dissolve the needed III-nitride nutrient or feedstock in supercritical ammonia fluid (such as KNH_2) containing mineralizer to form a saturated solution under high pressure, and then take appropriate technical measurements to make the saturated solution into metastable supersaturated solution, and begin to grow GaN single crystal on the seed crystal. Here, the choice of mineralizer agent, reaction source distribution, and transport of dissolved material are the key factors in the process of ammonothermal GaN crystal growth.

The specific process is to seal the nutrient, seed the crystal and mineralizer solution in the autoclave, and control the temperature difference of nutrient area and seed crystal area, respectively, so as to accelerate the convection of the solute and seed for the crystal growth. For various kinds of growth process, the largest difference is caused by the different mineralizer, because the solubility of crystal is different from temperature dependence in different mineralization agent solution.

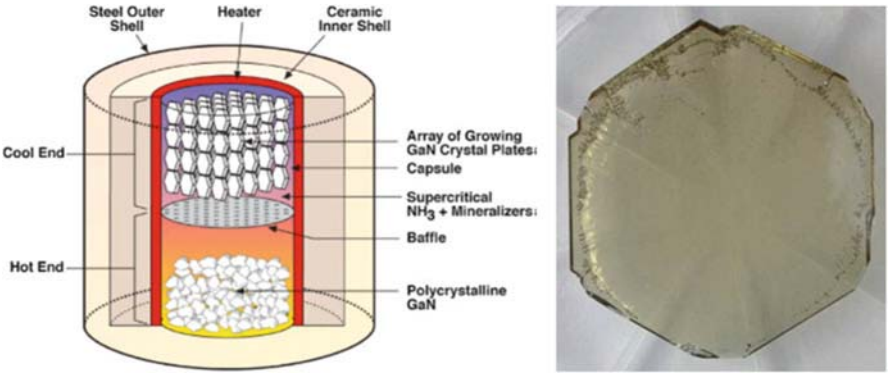

Fig. 1.8 (**a**) Schematic of high-pressure ammonothermal GaN growth apparatus employed at Soraa; (**b**) As-grown nominal 2 in. diameter GaN(0001) crystal produced using the ammonothermal method

The ammonothermal growth is conducted by transporting the mass from high- to low-temperature zones, and this method has been reported to possess several advantages, including lower dissolution density due to solubilizing in the higher-temperature zone, lower contamination probability due to recrystallization in the lower-temperature zone, lower probability for cubic formation, and absence of disastrous effect of the basic solution on the autoclave materials, which results in the improvements of safety and cost-effectiveness. In contrast, the acidic approach requires special, usually costly, Au or Pt liners, and the safety operation still remains problematic.

When the crystal in mineralizer solution has the solubility of positive temperature coefficient (higher solubility while varying with temperature), the bottom of the autoclave used for nutrient is generally designed as the high-temperature zone, and the top of the autoclave as low-temperature area is used to hang the seed crystal. Usually the crystal nucleation can be easily controlled for the growth of the solubility of positive temperature coefficient. When the crystal in mineralizer solution has a negative solubility coefficient (the solubility of crystal drops while varying with temperature), it should be seed crystal hanging in the high-temperature area and put nutrient at low-temperature area.

GaN solubility in pure ammonia is small because of ammonia with weak polarity; thus in the ammonothermal method, pure ammonia solution is not suitable for GaN crystal growth. To refer the hydrothermal method for the selection principle of mineralizer, ammonothermal GaN crystal growth also needs to choose a suitable mineralizer. The type of the mineralizer used determines the main type of the ammonothermal approach, with respective advantages and disadvantages. Selection of mineralizer is conformed to the following two points: (1) the solubility and solubility temperature coefficient of the basic crystal material in the ammonia solution is enough to achieve an effective growth rate; (2) in the ammonothermal system, crystalline materials are the only stable solid phase; thus it will not affect

the system's phase relationship. At present in ammonothermal GaN crystal growth, two kinds of mineralizer are mainly adopted, a kind of alkali XNH (X = Li, Na, K) and another for acidic NHX (X = C1, Br, I). The neutral mineralizer was not suitable for GaN crystal growth. GaN crystal is generally not grown by neutral mineralizer, such as KX (X = C1, Br) and NaX (X = C1, Br). Only when the mineralizer is KI, a small amount of wurtzite GaN is generated, but it is mixed with zinc blende GaN.

Of course, there are many factors, such as temperature and concentration of mineralizer, impurity, growth, and so on, to influence the growth of GaN crystal.

In general, the ammonothermal technique is characterized with relatively low growth rate capacity; but in this technique, the relatively low temperature and reasonable pressure allow controllable recrystallization at close to equilibrium conditions for the production of high-quality material. And the technique also allows large-scale wafer growth and the multiple-seeded growth in a single run. Up to now, Poland Ammono Inc. has been able to achieve the commercial mass production of 2 inch GaN wafer with m- and c- direction. But as a result, the ammonothermal growth needs GaN seed crystal, and it is affected by seed crystal size. GaN single crystal with more than 2 in. in diameter is still in the development stage. Nevertheless, the approach is expected to be capable of handling higher growth rates at higher pressures.

The quality of this type of material is still in the beginning of detailed evaluation. Given the fact that a reasonable large crystal is a result of a very long process, optimization of the growth conditions and a systematic series for thorough analysis will take more time.

1.3.1.3 Na-Flux Method

An alternative solution growth approach by using Na flux instead of nitrogen solution was proposed by Yamane et al. [7] several years ago. So far, as a self-nucleation growth, it is quite similar to that of high-pressure solution growth approach.

On the basis of high-pressure nitrogen solution method, the researchers developed a Na-flux method, and the growth mechanism is shown in Fig. 1.7 (right). Na is added in the molten Ga solution. Because of the very high reducibility of Na, N_2 molecules can be ionized and easily dissolved into molten Ga-Na solution under low temperature and low pressure, which thus greatly increase the N solubility in the solution. So GaN crystal will be synthetized at relatively low pressure. The results of GaN crystal by this self-nucleation growth are quite similar to that obtained by high-pressure solution growth approach. But the advantages of Na-flux method are mostly related to the more favorable growth conditions of typically 800 °C and 5 MPa. In the 1990s, Yamane et al. [7] got the GaN crystal by solvent method using Na as cosolvent for the first time.

In the early stages of Na-flux research period, the crystal nucleation position is uncertain; the crystal has often been found in the crucible wall. So the liquid-phase epitaxy (LPE) has been developed in order to limit the nucleation on the seeds.

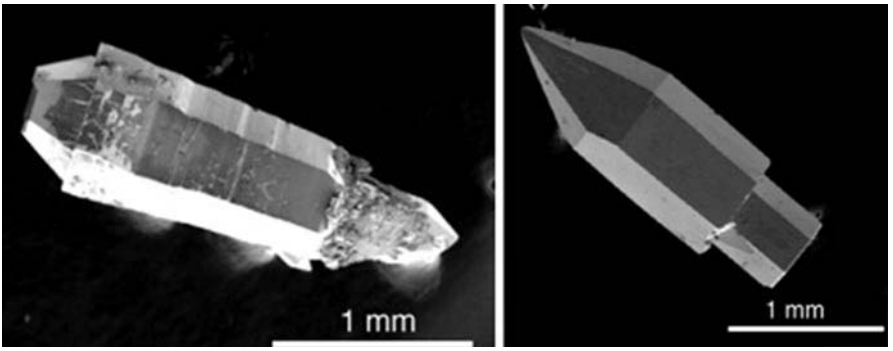

Fig. 1.9 GaN seeded growth with a (left) Na-Ga premixed melt and (right) with the Ga melt and Na vapor

Aoki et al. studied the influence of the growth temperature and N_2 pressure on the crystal morphology and growth rate during the epitaxial growth of seed crystal. However, increasing the solubility of the nitrogen in the molten Ga-Na solution, at the same time, the initial GaN seed and GaN epi-crystal also become much easier to decompose, which make the crystal surface rough before and after the crystal growth. In order to overcome the shortcomings, Yamada et al. [8, 9] proposed the Na-vapor assisted GaN growth to obtain the high-quality surface of GaN crystal, and the obvious difference can be seen from Fig. 1.9.

In the early study, GaN grown by Na-flux method is the colored crystal due to the lack of N in the process of crystal growth, because N solubility is not high in the solutions. In order to improve the N solubility in the Ga-Na melt, joining the alkali metal element such as Li and Ca into the Ga-Na melt in the hybrid cosolvent significantly increased the N solubility in the melt and improved the permeability of GaN crystals [10].

In the absence of the GaN seed, two growth habits were demonstrated—prisms or platelets—with length and lateral sizes of a few millimeters. In order to increase the size of GaN crystal, F. Kawamura and Y. Mori et al. used HVPE-GaN substrate as a seed crystal for the epitaxial growth of 2–4 in. GaN film. Kawamun et al. [11, 12] developed a set of equipment for large-size GaN single crystal substrate. The schematic diagram of the equipment is shown in Fig. 1.10, and one of the most critical improvements is to put the heating system (crucible and electric furnace) in the stainless steel compression cavity with a water cooling system, by shaking the cavity to stir the melt at the same time. After this modification, the growth system can be used to grow large-size GaN chip. In the case of using GaN film grown by MOCVD, growth rates up to 20 μm/h were obtained, and a boule with a thickness of 3 mm was shown.

In order to improve the crystal quality, Kawamura et al. [14] join carbon (C) to inhibit the polycrystalline growth. By optimizing the growth conditions, Mori et al. [13, 15] have successfully carried out the epitaxial growth of 2–4 in. GaN on the large size of seed crystal, GaN crystals are highly uniform and free of cracks, and

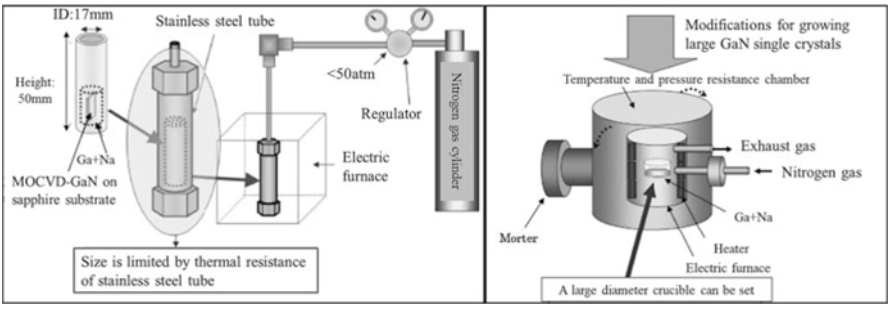

Fig. 1.10 Schematic of the modified Na-flux method for GaN growth on 2 in. templates

the thickness can be up to more than 750 μm, as shown in Fig. 1.29. GaN crystal has a good permeability and lower impurities, although the dislocation density of the initial seed crystal HVPE-GaN is up to 10^8 cm^{-2} orders of magnitude, but the chip dislocation density decreased to 2.3×10^5 cm^{-2} after growth by the liquid-phase epitaxy (LPE). A decrease of dislocation density from 10^8 cm^{-2} in the seeds to 10^4 cm^{-2} in the regrown crystal was reported and explained in terms of a change in the dominating growth mode from vertical in the seed to lateral in the Na-flux solution growth [14]. It is also found that Na and C additives are not doped into the GaN crystals by the test of the secondary ion mass spectrometry.

Although its dislocation density of GaN crystal by Na-flux method has been greatly reduced, but with the demand for higher crystal quality of GaN-based photoelectric device, lower dislocation density or even no dislocation GaN crystal is needed. Similar to the Czochralski method for the growth of Si ingot, a necking technique was adopted to realize the growth of large-size GaN crystal without dislocations [16], as shown in Fig. 1.11. A dislocation generally propagates perpendicularly to the growing surface. Therefore, in the initial growth layer that consists of numerous (10–11) facets, the dislocations propagate perpendicularly to the (10–11) facets, and they are bent. Usually in the necking technique, the dislocation begins to extend like a bent neck from the growth surface and end in the sapphire wall, so that further propagation does not occur. The growth of (10–11) facets in this initial growth layer and the dislocation behavior are unique phenomena of the Na-flux method. Because the area of crystallography is without continuity, and the bent dislocation will end at the interface between the initial growth layer and single crystal, almost all of the dislocations from GaN seed crystal will eliminate inside the hole, and the final GaN crystals show no dislocation. In addition, the dislocations that propagate in the (0001) direction also terminate at the boundary between the initial growth layer and the preferentially grown single grain so that propagation of dislocations to a single grain cannot occur. Almost all dislocations which originated from the GaN seed layer are eliminated in the holes (i.e., the necking region), resulting in a GaN crystal free of threading dislocations. Imanishi et al. [17] have already succeeded in growing dislocation-free bulk GaN crystals with a diameter of more than 2 cm and a height of about 1.2 cm by the GaN small

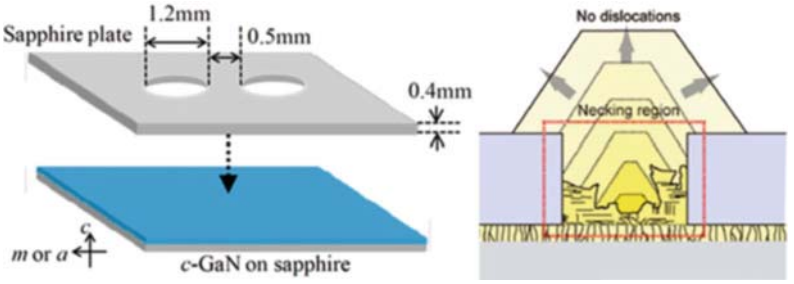

Fig. 1.11 Schematic drawings of the configuration of two GaN point seeds and that of the growth model with a necking technique

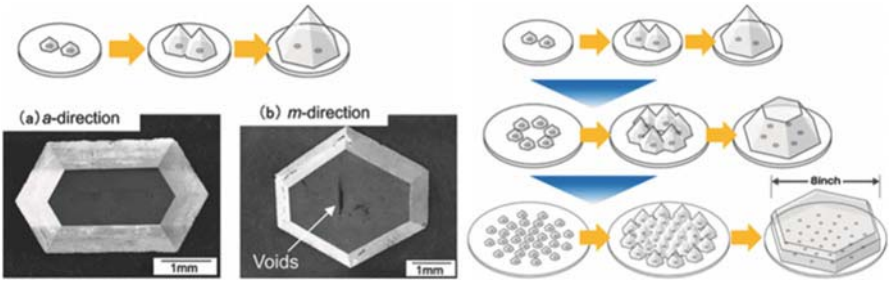

Fig. 1.12 Schematic of coalescence growth from two isolated small seed crystals and SEM images of the sliced crystals (left), and schematic of coalescence growth from many periodically arranged small GaN seed crystals (right) [15]

seed crystal growth. The necking technique in the Na-flux GaN growth may be a major breakthrough for fabricating dislocation-free GaN ingots.

In order to grow large-scale GaN crystal without dislocations, they put forward the joint growth of multiple isolated small seed crystals for the large-scale GaN crystals. Figure 1.12 (left) is the experiment schematic of two seed crystals' joint growth; it can be found that GaN crystal quality is very high along one orientation and poor along the orientation of m-direction with a lot of defects [15]. Recently, they got high-quality GaN crystals from three isolated small seed crystals along a joint growth orientation, as shown for SEM images of GaN crystals in Imanishi et al. [17]. Obviously the joint growth is possible for manufacturing large diameter GaN crystals without dislocations. As shown in Fig. 1.12 (right), it is the schematic for GaN crystal by a periodic array of small seed crystals' growth [15].

One advantage of Na-flux method is simple for the growth equipment and low pressure for crystal growth, which can grow a large-scale, high-quality GaN crystal and even GaN crystals without dislocations using small seed crystal growth. So this method is gradually becoming the key technology of high-quality GaN crystals.

Another advantage of Na-flux method is its ability to reduce some structural defect density, consistent with reports for other material systems such as SiC. The dislocation density of GaN grown by high-pressure nitrogen solution method is lower than 10^2 cm^{-2}, and no dislocation GaN crystal can even be prepared by the union of HPNSG method and Na-flux small seed crystals. Similar results of reducing the dislocation density have been reported for alternative low-pressure solution growth (LPSG) at growth temperature in the range of 900–1020 °C [18] by employing a different chemical solution. A growth rate of 1 μm/h was reported for growth on metalorganic vapor-phase epitaxy (MOVPE) GaN template on sapphire up to 3 in. in diameter. Also, at nearly atmospheric pressure and temperature of about 800 °C, employing another chemical solvent, seeded growth on HVPE-GaN seeds was demonstrated [19].

Up to now, the reported growth rates of a few micrometers per hour are not suited for bulk crystal growth. In addition, in these approaches, since nitrogen has to be dissolved and then diffused through the Ga melt to the growth front, maintaining homogeneous growth over large areas remains a challenge.

1.3.2 Gas-Phase Growth for GaN Substrates

1.3.2.1 Gas-Phase Transport Method

Since Johnson and others synthesized polycrystalline GaN with NH_3 and molten Ga, many people began to study the gas-phase transport method for GaN single crystal growth, which is to transmit the Ga vapor at high temperature to react with NH_3 for GaN single crystal. If the molten Ga metal is replaced with GaN powder as Ga resource, it is known as "sublimation method." The growth rate by the sublimation method is relatively slow but steady. But the sublimation method itself has a technical problem, which must keep a continuous supply of GaN powder during the growth. While molten Ga metal is used as Ga source, it can get the maximum growth rate, but not very much stable. Here, the high growth rate is thought to form the Ga droplets, and the instability of the growth rate is attributed to the formation of GaN shell in the surface of molten Ga metal, causing the growth stopping. Besides, the reaction of Ga and NH_3 at the surface of Ga metal will cause the splash of Ga droplets on the surface of GaN crystal, which will change the growth mechanism.

Now the improved gas-phase transport process is mostly studied, called the sublimation sandwich transport method (SST) [20], as shown in Fig. 1.13. In SST, a powder or polycrystalline material (Ga, GaN, or their mixture) is evaporated, transported across a small gap by a thermal gradient, and recrystallized on a substrate. The evaporation of metallic Ga in the ammonia ambient is a very convenient alternative to grow the thick, high-quality GaN films. This technique has all the characteristics of a vapor-phase epitaxy performed at an unusual high temperature.

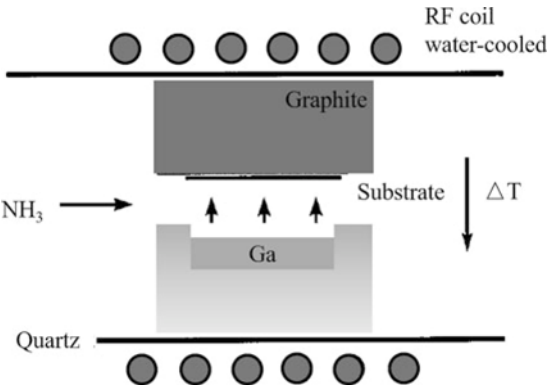

Fig. 1.13 Schematic of the high-temperature vapor-phase epitaxy reactor. The graphite crucible containing the metallic Ga and the substrate is heated inductively via a water-cooled coil. Ga vapor is transported over a short gap of a few millimeters

The distance between the Ga source and the substrate is only several millimeters, the pressure of reaction tube is an atmospheric pressure, and the growth temperature is 1170–1270 °C. The SST growth rate is more than 100 μm/h, and the fastest rate is up to about 1100 μm/h. The SST method is simple, low cost, and faster, but the SST GaN crystal quality is also very poor. There are still some technical problems to solve, not up to the practical level.

1.3.2.2 Hydride Vapor-Phase Epitaxy (HVPE)

Although ammonothermal growth and Na-flux method seem to have more developing potential for the preparation of single crystal GaN substrate, it is not suitable for commercial application because of the small size (≤2 in.) and low growth rate (50 μm per day). Therefore, atmospheric hydride vapor-phase epitaxy is still the main method to obtain large-scale, high-quality self-standing GaN substrate. As a chemical vapor-phase transport, HVPE method has not only high growth rate, compared with other methods of substrate preparation, but also versatility as a method for the fabrication of both substrates and devices, with a larger application direction and development prospects.

In history, HVPE methods have played an important role in the research and development of arsenic and phosphide semiconductor materials. Although the extensive research and full development have been done for HVPE growth for arsenide and phosphide, little is known in terms of nitride growth. The reason is that there is no suitable substrate and the chemical growth is different, leading to HVPE growth of the nitride more complex. In spite of this, HVPE is still the first and the most common method of GaN epitaxial growth until the early 1980s.

The first growth of GaN by HVPE was reported by Maruska et al. in 1969, using a sapphire substrate by modified hydride equipment for gallium arsenide (GaAs) and indium phosphide (InP) [21]. In the 1970s to the early 1980s, the researchers attempted to grow GaN thick film on sapphire and then made the self-supported GaN substrate [22]. However, the HVPE-GaN film has a large number of crystal defects,

high background carrier concentration, and poor crystal quality. At the same time, it is difficult to realize p-type doping and effective doping control, which hinders the production and research of GaN-related devices.

Due to the serious difficulties in reducing the intrinsic carrier concentration and realizing the p-type doping, HVPE technology was almost entirely abandoned after the 1980s. However, there are still some reports about HVPE growth of GaN film, and its optical and electrical properties reported can still be the best results compared with that of GaN grown by metal organic vapor-phase epitaxy (MOVPE) or molecular beam epitaxy (MBE). In fact, even by the standards of the 1970s, the quality of GaN film grown by HVPE is still remarkable [23, 24]. From the late 1990s, most of the attention has been focused on the hetero-epitaxy of GaN on foreign substrates such as sapphire, Si, $NdGaO_3$, and GaAs to realize freestanding GaN wafers. The first thick GaN (approximately 400 μm) with a smooth surface was reported by Detchprohm et al. in 1992, using a ZnO buffer layer on sapphire [25]. Usui et al. [26] achieved a freestanding GaN wafer of 2 in. diameter size by the use of a new technique, epitaxial lateral overgrowth (ELO), to reduce the density of dislocations significantly, and by a laser irradiation from behind to remove GaN thick layer from the sapphire substrate.

HVPE system equipment is relatively simple and convenient to maintain, and with the improvement of growth technology, the crystal quality of HVPE-GaN has been improved unceasingly. Its growth rate is high and it is easy to obtain homogeneous and large-scale GaN thick film, which make it very hopeful to solve the problem of self-standing GaN substrate. Meanwhile, the existence of halide in the growth environment of HVPE can significantly affect the equilibrium of GaN reaction and improve the ELO growth rate. Using the HVPE-ELO technology, GaN thick film can also be grown at high growth rate in situ growth, and then low-density GaN substrates can be obtained by a variety of substrate separation technologies (such as corrosion, laser liftoff technology or mechanical polishing technology, etc.). HVPE, therefore, becomes the important method to prepare freestanding GaN substrates for the large-scale application of GaN-based optoelectronic devices.

1.4 HVPE for GaN Substrate Materials

1.4.1 Chemical Reaction in the Growth of GaN by Hydride Vapor-Phase Epitaxy

HVPE for the growth of nitrides is a chemical vapor deposition method, and the reaction is usually carried out within the atmospheric quartz reactor. The reaction process is to introduce the hydrogen chloride under carrier gas into the reactor, reacting with metal gallium in the low-temperature zone, to flow the generated gallium chloride to the high-temperature zone and being mixed with ammonia to grow GaN. Unreacted gas is absorbed by the tail gas treatment system.

Nitride growth is actually using metal chloride disproportionation reaction, by raising the temperature to improve the stability of low compounds. Ga chloride has a variety of valence states (such as GaCl, $GaCl_3$, etc.), and GaCl is stable at high temperatures in HVPE system, decomposing into $GaCl_3$ below a certain temperature. The above features make us adjust the temperature of the reaction chamber, realize the GaCl generation, and transfer and deposit GaN. So, in usual nitride HVPE growth system, they are divided into a high and low temperature reaction chamber area.

Therefore, the novel of HVPE method is the primary reactant (GaCl) generated in the reactor, where the liquid metal Ga react with HCl gas in the range of 800–900 °C. Then GaCl with the carrier gas are carried into the substrate and mixed with NH_3, depositing GaN on the substrate. Substrate temperature is kept at 900–1100 °C, and N2 or H2 is the carrier gas. The chemical reaction is as follows:

$$\underset{\text{(low-temperature zone)}}{\mathrm{Ga\,(s) + HCl\,(g) = GaCl\,(g) + \tfrac{1}{2}H_2}}$$

$$\underset{\text{(high-temperature zone)}}{\mathrm{GaCl\,(g) + NH_3\,(g) = GaN\,(s) + HCl\,(g) + H_2\,(g)}}$$

The following six species were chosen as the necessary vapor species in analyzing the HVPE growth of GaN: GaCl, $GaCl_3$, NH_3, HCl, H_2, and inert gas (IG) such as nitrogen or helium. Here, group III elements such as chloride (usually a single chloride) were transported to the substrate, so hydride vapor-phase epitaxy is usually known as chlorine gas-phase epitaxy. Due to relatively low saturated vapor pressure of metal chloride at room temperature, chloride molecules can easily condensed on the substrate at room temperature, and HVPE growth usually adopts a hot wall reaction chamber for in situ synthesis of chloride.

Using in situ synthesis chloride and hot wall reaction chamber, the complex gas transportation system and assistant heating systems can be avoided. In addition, if the metal chloride was pre-synthesized out the reactor, the strong absorbent and corrosive metal chloride will make their preservation and transportation very difficult. However, high corrosive HCl gas can also cause some difficulties. For example, if there is air leakage into the gas path or reactor, HCl will soon destroy the reactor. Based on this, some of the research team reported synthetic $GaCl_3$ instead of in situ synthesis of HCl to GaCl [27–29]. Using these precursors, researchers grow single crystal GaN and improve the purity of metal chloride source.

Based on the purity and operability, HCl is usually more common than chlorine. Because the Chloride has higher saturation vapor pressure than bromide and iodide, the chloride is the most commonly used halogen for transportation. Bromide and iodide have a lower decomposition temperature, and it is reported that they are often used in the growth at low temperature [30, 31].

In hydride vapor-phase epitaxy system, the chemical reaction will produce large amounts of NH_4Cl, $GaCl_3$,$GaCl_3$, and NH_3, which will be condensed and even

block the exhaust system, unless they are heated to a high enough temperature (>340 °C) or the reaction is under low-pressure conditions.

Although there are a lot of difficulties in the design of HVPE system due to the chemical reaction, it also provides a unique advantage. For example, unlike MOVPE, HVPE growth process is no carbon in nature, which is easier to grow high-purity GaN film. In addition, strong corrosive chlorine and hydrogen chloride can help to remove the excess growth of metal components on the substrates, so as to suppress the formation of rich gallium materials or separated Ga droplet. The self-stabilization effect and high mobility of adsorbed GaCl can be used to explain that HVPE is much higher in the growth rate than other epitaxial methods. Because of the self-stabilization effect in rich gallium conditions, GaN film by HVPE has a higher quality than that of other epitaxial methods (such as MBE or MOVPE). Although HVPE growth rate is at least one order of magnitude higher than other methods, the dosage of NH_3 is far lower. The impurities from NH3 and the cost are both significantly reduced in the growth of the VPE nitrides.

The consciously introduction of additional HCl to the growth zone at high temperature can effectively improve the Cl/Ga ratio, which plays a very important role in the growth of high-quality GaN film. The introduction of HCl may enhance the GaCl local saturation and improve the lateral growth, leading to a larger grain size. The early experiment research from Nanjing University showed that the introduction of additional HCl can improve the surface morphology and the crystal quality. Some patents point out that additional HCl can also reduce the pre-reacted GaN particles in space before depositing on the substrate. In addition, the presence of HCl can also enhance the decomposition of other impurities.

1.4.2 Hydride Gas-Phase Epitaxial Growth System

It should be pointed out that HVPE-GaN growth with groups' III–V semiconductor materials is completely different in nature. For example, the HVPE synthesis of GaAs, As_4, and As_2 molecules with volatile and chemical activity formed by thermal decomposition of arsenic compounds can continue to participate in the growth of thin films. But in the process of HVPE-GaN growth, the N_2 molecules formed by NH_3 decomposition are very stable in the temperature range which we are interested in. In fact, HVPE-GaN growth is based on the feasibility of the NH_3 relatively low decomposition, which may be helpful for transporting the reactive nitrogen effectively to the growth surface of substrate [32], to prevent the generation of black-rich Ga GaN film [33]. Another difficulty of HVPE-GaN growth is that there are unforeseen gas-phase reaction, space particles, and wall deposition problems except the formation of GaN.

HVPE growth system generally consists of four parts: the furnace, reactor, gas configuration system, and exhaust gas system. There are two types of design including the horizontal and vertical HVPE system. As shown in the abovementioned disproportionation reaction, HVPE growth system is designed into a dual

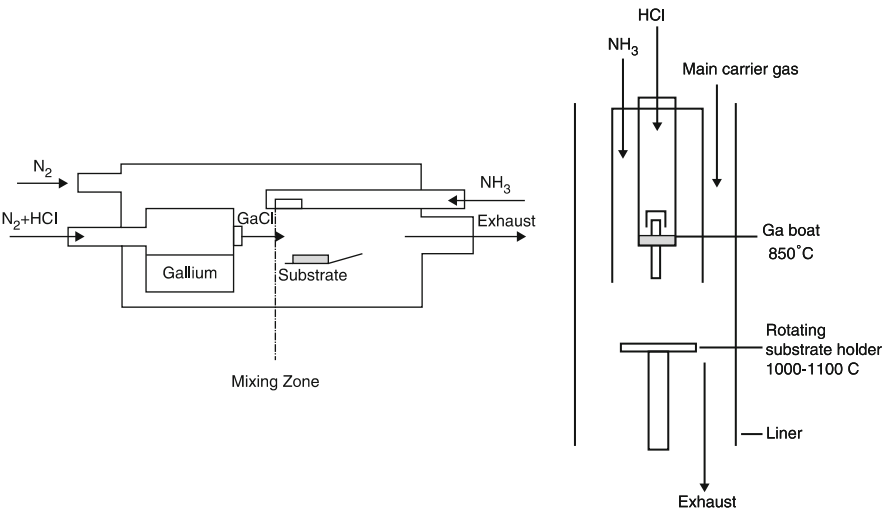

Fig. 1.14 Schematic diagram of (left) horizontal HVPE and (right) vertical HVPE

temperature zone: high- and low-temperature area. Low-temperature zone is used for generating GaCl and high-temperature zone for the deposition for GaN. The growth mechanism in different HVPE system is the same in nature. Figure 1.14 (left) shows the schematic diagram of the horizontal growth system (named as horizontal HVPE) [34], which is widely used in the growth of groups' III–V and II–VI material. At present, most of the reported HVPE for the growth of GaN is based on the horizontal HVPE growth system from RCA laboratory. Figure 1.14 (right) is the schematic diagram of vertical HVPE growth system (named as vertical HVPE) [35], which can improve the uniformity of GaN film by more easily introducing the rotation of the substrate. Substrate can also be dropped down and cooled slowly in ammonia atmosphere, to reduce the decomposition of GaN film.

1.4.3 The Growth and Doping of HVPE Nitrides

One of the difficulties for the growth of high-quality GaN by HVPE is the nucleation on the substrate. A lot of experiments show that the heterogeneous nucleation is very critical for the growth of high-quality GaN. If without any pretreatment, GaN directly on the sapphire is from highly transparent to brown. And the high-temperature growth after depositing the low-temperature buffer layer can often form polycrystalline GaN. Several kinds of different pretreatment, such as GaCl pretreatment of substrate surface and ZnO buffer layer technology [25, 36–38], are used to improve the heterogeneous nucleation density and quality of GaN on sapphire (0001).

In general, HVPE-GaN has the very high intrinsic shallow donor levels, usually in the level of 10^{18}–10^{20} cm^{-3}. Therefore, a great deal of doping research has been done for a suitable acceptor dopant to compensate for the donor and for p-type doping to realize the p-n junction. However, as a hot wall epitaxy, HVPE growth is vulnerable to the quartz reactor and gas-phase dopant in the chemical reaction. Some oxide doping agent might be more stable than SiO_2 in thermodynamics. Possible interactions will occur, such as the reduction of quartz reactor components, deposition of oxidized dopant on the pipe wall, and the corrosion of the quartz tube, leading to n-type Si impurities into the epitaxial layer, etc.

Although p-type conductivity has not been obtained, Mg doping in HVPE-GaN has been reported recently [39, 40]. Some studies by ion implantation in GaN show that zinc may be the third choice of shallow acceptor dopant. As a result, most acceptor doping research is focused on the introduction of Zn acceptor [41]. But the large ionization energy zinc acceptor and typically high intrinsic donor level in GaN made Zn doping for GaN p-type conductivity very difficult.

The HVPE technique was proven to be capable to produce n-type, p-type, and semi-insulating material. Hydride vapor-phase epitaxy is not only used to grow GaN but also to grow other nitride compounds (such as InN and InGaN, AlN and AlGaN, etc.) and the doping growth of nitrides.

Cubic GaN Cubic GaN has a unique advantage in the cleavage and doping. But compared with wurtzite GaN, cubic GaN in thermodynamics is metastable and only observed in the film. Several preparation techniques available have been adopted for the growth of cubic GaN, but the quality is very poor, because there is no lattice match suitable substrate. So far, there have been several research reports, using hydride vapor-phase epitaxy technology to grow high-quality cubic GaN thick film [42, 43]. And the most commonly used substrate is GaAs (100), because it can deposit a homogeneous epitaxial layer first on GaAs to modify the surface polishing damage, forming a nitride buffer layer to prevent further intrusion of ammonia gas. At that time, it was generally supposed that a low-temperature buffer layer of GaN could not be grown on a foreign substrate using HVPE system since only non-equilibrium growth system realized a GaN buffer layer. Here, the researchers think that it is necessary to control the lower growth rate (<4 μm/h) to prevent the formation of wurtzite GaN [44]. Further work is to obtain a device quality GaN material.

AlN-AlGaN Studies show that the growth of AlN-based nitrides is more complex by hydride vapor-phase epitaxy. The schematic diagram of horizontal HVPE for the growth of AlN substrate is shown in Fig. 1.15. And there are very strong interactions between AlCl and hot quartz reactor, which can lead to the excessive impurities introduced into the film and may decrease the quality of quartz reactor. Only a small amount of research has been done about the growth of AlN [45] and AlGaN [46, 47] by hydride vapor-phase epitaxy. Some companies, such as TDI, Crystal IS, The Fox Group, etc., have made progress in the growth of AlN template or AlN substrates by HVPE. Due to patent restrictions of AlN single crystal, TDI turned to the growth of AlN template rather than freestanding AlN substrate, as shown in Fig. 1.16. AlN

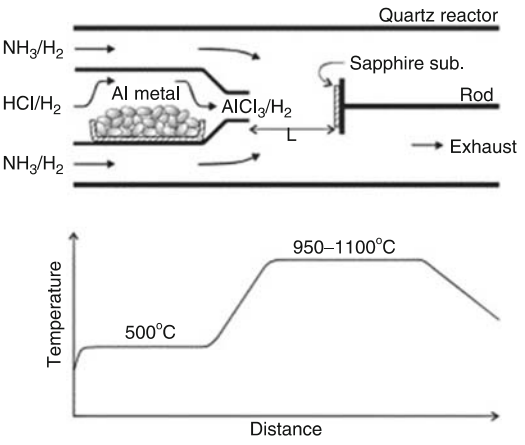

Fig. 1.15 Schematic diagram of horizontal HVPE for the growth of AlN substrate

Fig. 1.16 HVPE-AlN templates by TDI Inc. (2 in. AlN-on-sapphire, 3 in. AlN-on-sapphire, 4 in. GaN-on-sapphire, and 6 in. AlN-on-Si from left to right)

template refers to the deposited AlN layer on the heterogeneous substrates, such as Si or sapphire or SiC, for the further epitaxy of AlGaN devices.

The advantage is that the wafer size depends on that of the original substrate. But for the HVPE growth of AlN template compared with the growth by MOCVD and MBE, there is a same problem that serious cracks would be found while the thickness of AlN layer is up to several micrometers. So TDI developed a new stress control technology for the epitaxy of HVPE AlN template. By their self-owned multi-wafer HVPE growth system, they have achieved AlN templates of the thickness of 75 μm without cracks. The thickness of 2 in. AlN/SiC template without cracks is up to 10–30 μm, and the dislocation density is about 1×10^7 cm^{-2}, which is lower one order of magnitude than that of previous AlN/SiC template.

Research on the growth of AlN single crystals has been conducted for decades. Freestanding AlN substrates have been fabricated by sublimation, physical vapor transport (PVT), or sublimation-recombination technique, flux methods, and solution growth. The two most promising techniques are PVT and solution growth.

At present, freestanding AlN substrate with the diameter of more than 1 in. was prepared by HVPE.

InN-InGaN InN and InGaN compounds can extend the bandgap to the visible region of the spectrum. Thermodynamic instability of InN brings serious limitations to the growth of InN-based film. For example, the growth temperature of InGaN is below 800 °C, and the growth of InN is only at temperatures below 650 °C. The growth of stoichiometric InN is very difficult, because the ammonia at that temperature has very low cracking efficiency. Another important problem is that it is obviously impossible to use InCl to grow In-based compounds. Like the HVPE growth of GaN, $InCl_3$ is stable at low temperature. Presumably, at lower temperatures, an additional product of gas-phase $InCl_3 \cdot NH_3$ plays a very key role for subsequent InN deposition. Even so, the thermodynamic instability of InN and poor efficiency of ammonia cracking make the growth of InN become very difficult.

1.4.4 The Main Difficulties of HVPE

As is known to all, HVPE-GaN growth has the very high growth rate, for the growth of almost of any GaN orientation can reach 100 μm/h in the order of magnitude, which means that HVPE is possible for the preparation of GaN substrates. But up to now, there are only a few research reports that the HVPE growth of large-scale GaN can be sustained for more than 10 h, and the thickness is rarely more than 10 mm, which is mainly caused by the technical characteristics of HVPE method. The main difficulties of HVPE are as follows:

- *Space parasitic reaction.* The parasitic reaction outside the substrate in HVPE system under atmospheric pressure is more outstanding than other growth method. A large number of parasitic GaN particles will be deposited on the exit of GaCl tube, the inner wall of quartz glass tube, and the substrate surface. GaN deposited on the exit of GaCl tube will consume GaCl so as to reduce the growth rate and cause the damage of the GaCl tube; GaN particles deposited on the growth surface forming defects will reduce the quality of the material, while GaN deposited on the wall of quartz reactor can cause the breakage of quartz reactor.
- *Consumption of liquid gallium source.* With the consumption of metal Ga source, the growth rate of GaN will be affected. In the growth process for a long time, the consumption of the gallium source cannot accurately be known, and it is also difficult to add during the growth process. Although we can increase the capacity of Ga container, the weight of Ga is limited at high temperature in quartz glass container. And while the temperature changes between high- and low-temperature changes, the stress from the liquid-solid gallium metal and quartz increases the chances of the breakdown of quartz reactor.
- *Ammonium chloride powder.* Another technical problem in HVPE method is that the growth reaction under atmospheric pressure will produce large amounts

of ammonium chloride powder, aggregating in the downstream blocking the exit of quartz reactor even to explode, which may affect the growth. The long continuous growth is needed for the growth of GaN boule. Although most of HVPE equipment claims to solve the problem, so far, the continuous growth of HVPE system still is little more than 10 h.

- *Brittle quartz reactor*. The HVPE reactor is usually made of quartz because of the strong corrosive gases. The high price of high-quality quartz material, the precision processing, and the difficulties in installation and maintenance greatly increase the cost, which affects the mass preparation of GaN material.

In spite of the disadvantages, with the deepening of the research, most of the problems can be solved with in-depth research.

1.4.5 Epitaxial Lateral Overgrowth by HVPE

The heterogeneous epitaxial growth of GaN will certainly cause high dislocation density in the epitaxial layer, typically up to 10^{10} cm^{-2}. A variety of methods have been used to reduce the dislocation density, achieving preliminary results. Compared with other growth technologies such as MOCVD and MBE, HVPE has the potential advantage in preparing large-scale GaN film with low dislocation density. In HVPE-GaN film, several microns of terrace structure and hundreds microns of honeycomb cell structure can often be observed, which all shows that HVPE-GaN growth has the very high ratio of horizontal/vertical growth rate, more suitable to the ELO technology. Using the ELO technology, Japan Nichia greatly improved the life of blue LDs, more than 10,000 h of continuous running.

The ELO process is to prepare the patterned masks on HVPE- or MOCVD- GaN layer by applying conventional photolithographic processing or wet etching to 130-nm-thick SiO_2 layers deposited by plasma-enhanced chemical vapor deposition. As a result of surface energy choice, GaN is only grown in the window part, and the nucleation on the covered SiO_2 parts is difficult [48, 49]. A variety of mask designs were investigated, including nonparallel stripes arranged in a "wagon-wheel" pattern, arrays of circular apertures, parallel stripes oriented along the <0001> direction, parallel stripes oriented along the <1–100> direction, and parallel stripes oriented along higher index directions. When the thickness of epitaxial GaN in the window is more than that of masked SiO_2 layer, the vertical and lateral growth of GaN will happen at the same time. When the lateral growth reaches a certain degree, full cover GaN epitaxial layers can be obtained. Because the growth is quasi-free and perpendicular to the direction of the climbing dislocation from original GaN layer, GaN in the overgrowth regions ("wings") has a high quality. ELO regrowth was carried out under similar growth conditions to those used for the GaN films by HVPE. It was found that masks consisting of parallel stripes oriented along the <1–100> direction exhibited reproducibly vertical stripe sidewalls and

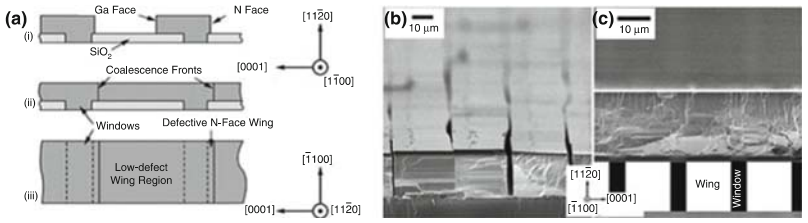

Fig. 1.17 (**a**) Schematics of HVPE LEO a-plane growth using mask stripes/openings oriented along the GaN <1–100> direction, (**b**) inclined cross-sectional SEM images of uncoalesced LEO stripes, (**c**) SEM cross-sectional image of coalesced a-plane LEO GaN film

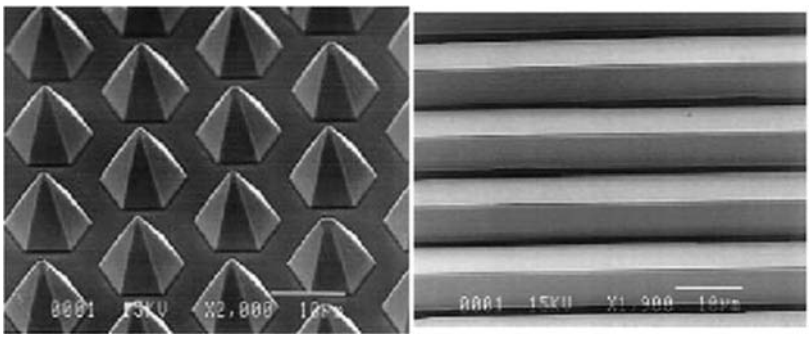

Fig. 1.18 SEM images of GaN ELO growth in the hexagonal window and parallel window along the <11–20> direction

thus were most effective to lower the dislocations and stacking-fault densities in the overgrown regions ("wings"), as shown in Fig. 1.17 [50].

ELO is an effective, direct means of significantly reducing the propagation of such defects via blocking and redirection. In a manner analogous to c-plane ELO, the stripe direction, width, and period all play an important role in the morphology and defect reduction during overgrowth. Figure 1.18 is the morphology of ELOG GaN [51]. The experimental results show that the dislocation density of GaN on the SiO_2 mask is several orders of magnitude smaller than that of GaN on window part.

As above mentioned, the biggest characteristic of HVPE system is high growth rate, which is suitable for the growth of GaN thick film. But when the thickness of GaN on sapphire is more than 20 μm, the cracks will appear in GaN epitaxial layer. ELO technology can effectively alleviate the phenomenon, thus obtaining low-density, large-scale high-quality GaN thick film. In order to further improve the quality of ELO epitaxial layer, new methods have been tried. For example, two-step ELO growth of GaN is one of them, mainly considering that the lateral growth depends on the conditions, such as temperature, carrier gas flow rate, and V/III ratio. The ELO growth is first carried out at a relatively low V/III ratio in order to produce smooth vertical {11–20} interface and then at a higher V/III ratio to promote the lateral growth [52]. Another double-layer ELO technology is used to reduce the

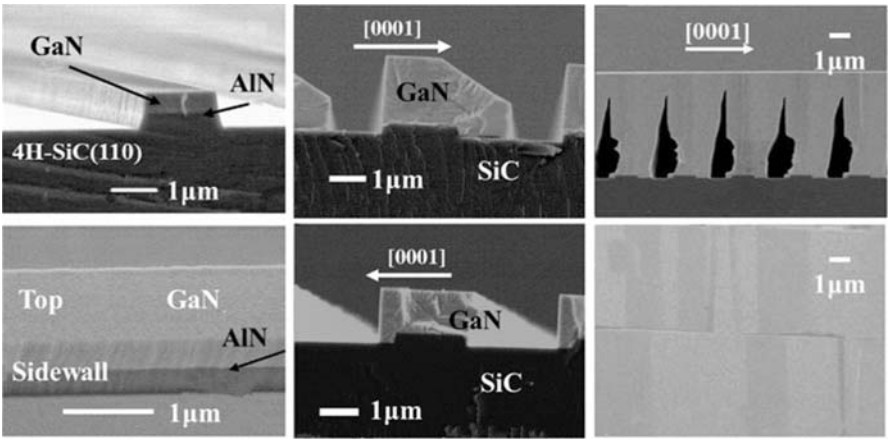

Fig. 1.19 SEM micrographs of GaN by pendeo-epitaxial regrowth

dislocations in the interface of lateral GaN on SiO_2 mask, by changing the direction of second ELO GaN after the first ELO.

In addition, the pendeo-epitaxy growth technology is also very attractive. It is a technique of lateral epitaxy without mask, which is usually on SiC or SiC/Si heterogeneous substrate, using AlN buffer layer as the mask [53]. After etching out part of AlN layer, GaN is not directly grown on SiC substrate but only selective epitaxial growth on the AlN layer. GaN grow up along the longitudinal and lateral directions at the same time, and with the increase of the thickness, the front of lateral epitaxial growth also laterally extends. Because GaN cannot be grown on SiC substrate between adjacent AlN films, it seems that the lateral spreading of GaN on AlN layer is impending, like GaN crystals hanging on both sides of AlN, so-called pendeo-epitaxy. Figure 1.19 shows SEM images of GaN by pendeo-epitaxy process. The characteristic of the pendeo-epitaxy technology avoids the effect of the mask on ELO GaN, especially the impurity and the interface stress, leading to a higher quality of GaN.

1.4.6 Freestanding HVPE-GaN Substrate

An alternative approach for GaN homo-substrates for a long time is the use of thick GaN layers grown by hydride vapor-phase epitaxy on sapphire. These thick layers are subsequently removed from the sapphire substrate by a suitable process and then can serve as quasi homo-substrates for device fabrication. Currently, hydride vapor-phase epitaxy (HVPE) provides the highest growth rate of GaN single crystals, reaching 1 mm/h or more. In addition, because the growth is usually performed at atmospheric pressure, large-scale HVPE reactors are available. For these reasons,

HVPE has considerable advantages for the mass production of large-area GaN crystals for freestanding wafers.

However, the process can suffer from serious problems of cracking of the thick GaN layer due to the large mismatch in the thermal expansion coefficients between GaN layer and the base substrate. Despite strenuous attempts to overcome this problem, difficulties still exist in reproducibly manufacturing GaN crystals that have a sufficiently large area for practical use. Reducing the density of dislocations is another important issue, because the HVPE method still involves hetero-epitaxial growth on a foreign substrate with a large lattice mismatch.

Here is to summarize the present state of research concerning such freestanding GaN homo-substrates, with special emphasis on laser-induced liftoff process and self-separation methods for the separation of the thick GaN layers from their sapphire substrates.

Because thick HVPE-GaN layers are generally hetero-grown on sapphire, a highly desirable process is required to enable a fast, reliable, and high-yield detachment. In practice, such a process will involve a sacrificial layer somewhere between the substrate and GaN layer, which is removed by a specific chemical or thermal treatment. One possibility would be to deposit a sacrificial layer which makes use of selective chemical etching, e.g., of AlN versus GaN in KOH. Another method is developed to cause GaN films to self-detach from its sapphire substrate during cooldown from growth temperature due to the accumulation of thermal stress and the lattice mismatch between GaN and sapphire. A third approach is the complete removal of the substrate by etching or polishing, which is quite time-consuming, especially in the case of sapphire or SiC substrates.

1.4.6.1 Laser Liftoff Process

Another useful process, much more flexible and significantly faster than the abovementioned methods, is the laser-induced delamination from a transparent substrate such as sapphire, or laser liftoff (LLO). In this process, the separation of a GaN layer from the substrate is achieved by irradiation of the substrate-film interface through the substrate with high-power excimer laser pulses at a wavelength which is transmitted by the substrate but is strongly absorbed in the GaN layer [54]. The absorption of such high-intensity laser pulses causes a rapid thermal decomposition of the irradiated GaN interfacial layer into metallic Ga and gaseous N_2 (Fig. 1.20) [55]. High-intensity laser pulses enter the sample via the sapphire substrate and thermally decompose a thin GaN layer at the substrate interface. The energy density of laser pulses is often in the range between 400 and 900 mJ/cm^2, and the threshold is approximately 250 mJ/cm^2. Below this critical absorbed pulse intensity threshold, no visible alteration of GaN layer can be seen. A hot plate can be used to raise the substrate temperature during the process, in order to relieve some of the accumulated thermal strain. The temperature of hot plate is usually above 730 °C but below 830 °C (decomposition temperature of GaN). At this temperature range, the strain and the bowing were visibly reduced and hardly noticeable. Ideally,

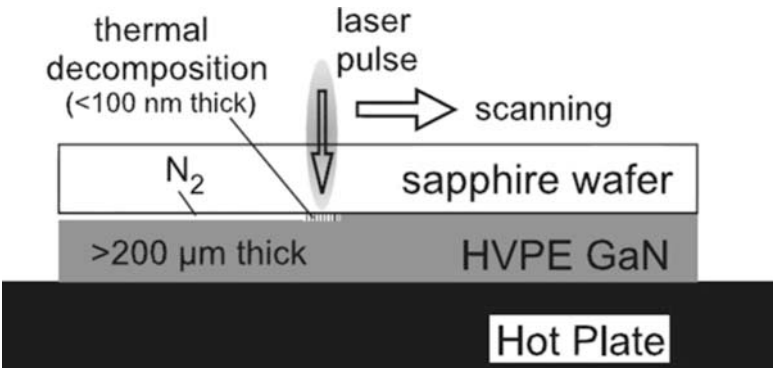

Fig. 1.20 Schematic view of the laser liftoff (LLO) process

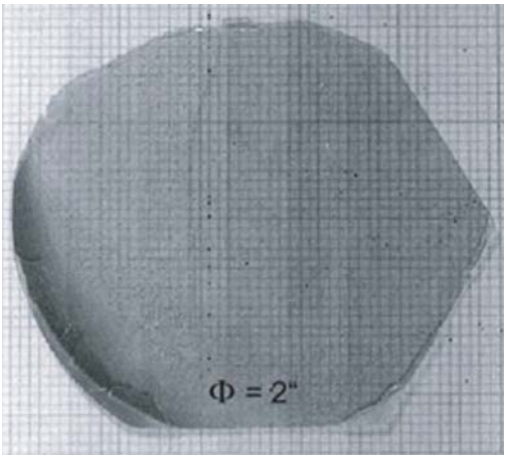

Fig. 1.21 Photograph of a 275-μm-thick freestanding GaN film, after removal from 2 in. sapphire

in situ laser liftoff in the deposition reactor close to growth temperature would be the best solution to avoid all bowing or cracking problems caused by the thermal expansion mismatch between GaN and the sapphire substrate.

A successful separation of thick HVPE-GaN layers from sapphire depends on several factors, including film thickness and thickness homogeneity across the wafer, the stresses, and stress gradients caused by the large thermal expansion coefficient mismatch. The differences of the thermal expansion coefficients result in substantial macroscopic wafer bowing, although most of the wafers exhibited very little or even no near-surface cracking across the whole wafer. But for the laser liftoff procedure, the bowing of thicker GaN films (>100 μm) often gave rise to extensive fracturing because of the strain inhomogeneity at the boundary of already released and thus relaxed areas and still attached portions of the wafer, as shown in Fig. 1.21 [55].

Such a LLO process has some intrinsic advantages compared with other possibilities abovementioned. First, sapphire as the commonly used substrates would

be even possible to recycle the separated sapphire after LLO for further deposition runs. Second, the LLO process does not require any specific sacrificial layers in the growth sequence. Third, the LLO method is quite fast and can be scaled up easily. A 2 in. wafer in principle could be lifted off in a few seconds. Finally, the liftoff process could also in situ occur directly after deposition of the III-nitride film in the deposition reactor before cooldown to room temperature, which would avoid the build-up of critical thermal strain.

The laser liftoff process is not only for the production of freestanding GaN pseudo-substrates starting from thick HVPE-GaN epilayers but also the delamination of thin GaN device heterostructures for the purpose of wafer bonding onto foreign substrates or for flip-chip bonding in device technology. Using optimized processes, the defect-free liftoff of the entire 2 in. wafers can be achieved for GaN film thicknesses ranging from 3 to 300 μm. Separation of thin GaN layer from sapphire substrates opens up new possibilities for the formation of electrical contacts, for the extraction of photons, and for thermal management. The laser liftoff method has already become a major technique in III-nitride devices. Up to now, LLO separation process of thin GaN device heterostructures is widely applied for the vertical-structured GaN-based LED chip.

1.4.6.2 Self-Separation Methods

In addition to the LLO technology, some methods have been developed to realize the separation of GaN layer from sapphire substrate. The self-separation of all these methods is mostly based on the drastic change of thermal stress and the lattice mismatch between GaN layer and sapphire substrate.

In the early twenty-first century, an epitaxial procedure was developed to obtain self-separated GaN films from sapphire substrate during the cooling down to room temperature from the growth temperature [56]. In this example, thick GaN layers have been grown on particular sapphire substrates by hydride vapor-phase epitaxy (HVPE). Sapphire substrates have stripe-shaped GaN seeds (Fig. 1.22), which is formed by a rather complex pretreatment of the wafer including lithography. The separation of thick GaN layer took place during the growth process at the interface of GaN/sapphire, because of the lattice mismatch and the thermal stress between GaN and sapphire. The narrow stripe-shaped structure of the seeds makes the self-separation easy.

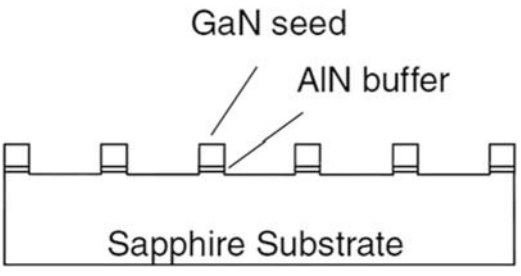

Fig. 1.22 Schematic diagram of substrate structure with GaN seeds

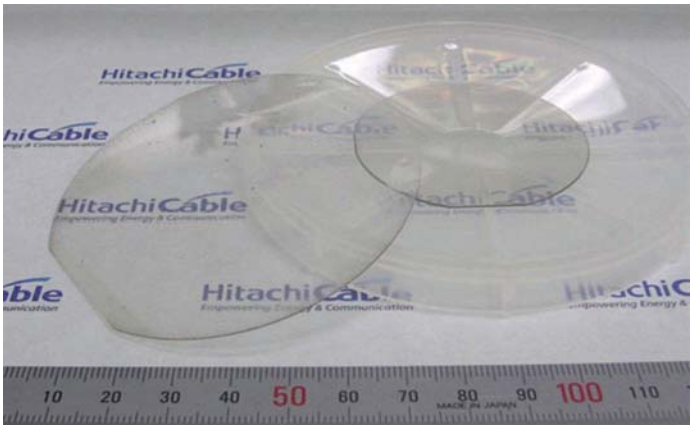

Fig. 1.23 Photograph of a 2 in. and a 3 in. VAS-GaN wafer

An original void-assisted separation (VAS) technology has been successfully established for the fabrication of large-area, high-quality GaN wafers with excellent reproducibility [57–59]. In this case, a fragile TiN layer that contains numerous small voids is formed at the interface between thick GaN layer and substrate. The thick GaN layer can be separated from the substrate by breakage of the fragile layer due to the thermal stress generated during the cooling process after the HVPE growth. The mechanical strength of the fragile layer can be controlled by changing the density of TiN voids. It is therefore possible to cause the separation by the application of a very small thermal stress. By using the HVPE-VAS method, high-quality GaN wafers with the diameter of over 3 in. have been prepared (Fig. 1.23).

Different from the abovementioned methods using a complex pretreatment including lithography, void-assisted separation technology enables highly reproducible large-area separation without producing any cracks. After that, a series of self-separation methods have been developed, by using a sacrificial layer (such as graphene, BN, nitride nanostructured interlayer, etc.) to form a weak interface layer close to substrate like the TiN voids.

All these self-separation approaches are not only to obtain freestanding GaN layer but also to reduce the threading dislocation density of GaN wafer to the order of 10^6 cm^{-2} due to the approximate ELO process.

1.4.7 Current Development Trend in HVPE-GaN Substrate Materials

Hydride vapor-phase epitaxy for the GaN growth is the most important purpose for preparing high-quality GaN substrates, because the high growth rate of HVPE provides the key technology of GaN quasi-substrate. By adopting the method of

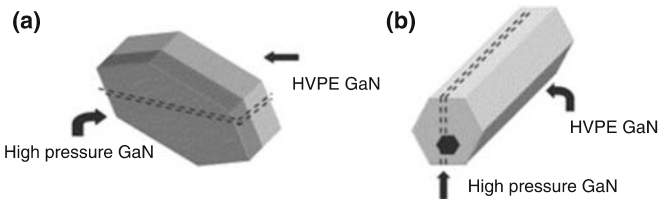

Fig. 1.24 The schematic diagram of the HVPE post-processing technology on the high-pressure platelet (**a**) and needle (**b**) GaN seeds

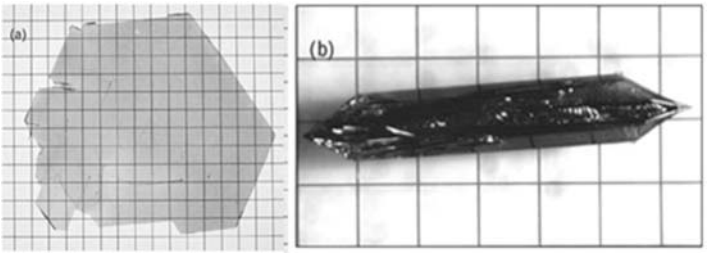

Fig. 1.25 The platelet (**a**) and needle (**b**) GaN single crystal by high-pressure solution method

atmospheric HVPE, a few companies and research institutes have prepared 2–6 in. GaN substrate materials (including GaN substrates and templates), but the price of freestanding GaN substrate is expensive, from $1000 to $5000 per piece of 2 in., which is mainly due to the technology of not fully mature and high cost, in the urgent need of improvement. In recent years, based on the combination of various substrate growth technologies, a variety of new composite technology for the growth of GaN substrates has been developed.

1.4.7.1 Combined GaN Crystal Growth

The combined GaN crystal growth refers to prepare a large-scale high-quality GaN crystal by the combination of different technologies, such as HVPE, HPNSG, ammonothermal growth, Na-flux method, etc.

The TopGaN Inc. claimed that they would expand the size of GaN regrown by HVPE on the platelet and needle GaN single crystal by high-pressure solution method, as shown in the schematic diagram in Fig. 1.24 [2], even though the dislocation density of GaN increased from almost zero to around 1×10^6 cm^{-2}. Two morphological GaN crystals grown under high N_2 pressure, hexagonal platelets and hexagonal needles are shown in Fig. 1.25.

The size of GaN crystal expanded by HVPE process is typically up to 100 mm, after getting rid of the original GaN seed crystal, as shown in Fig. 1.26. If the HVPE growth rate is lowered to 20 μm/h, 100 mm GaN single crystal almost without dislocations on n-type high-pressure GaN seed can be obtained.

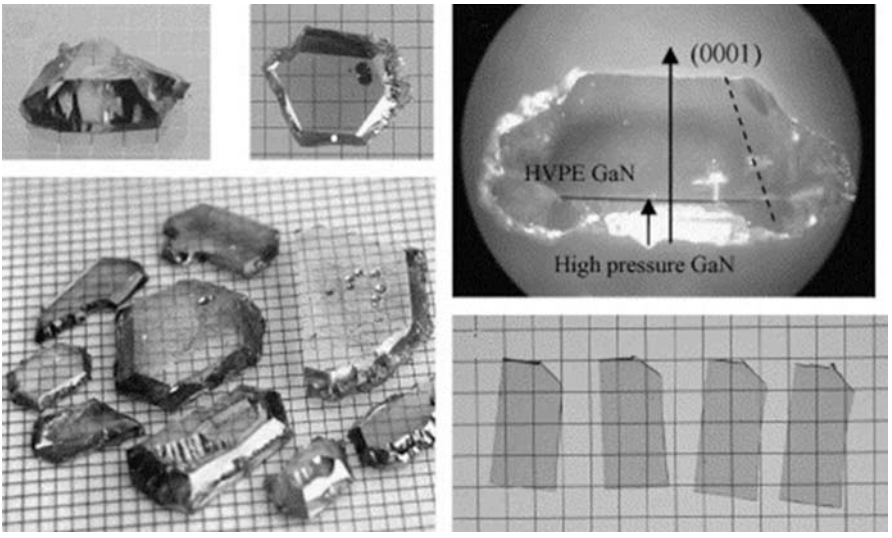

Fig. 1.26 The large-scale GaN crystal by the HVPE post-processing technology on the high-pressure platelet GaN seeds

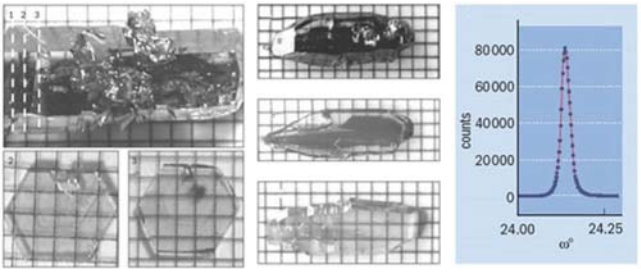

Fig. 1.27 The large-scale GaN crystal by the HVPE post-processing technology on the high-pressure needle GaN seeds

Although the crystallographic plane of GaN needle seed by HPNSG is uncertain, transparent, or pale yellow, GaN crystal with stable crystal shape will be obtained by a series of the same process of HVPE, as shown in Fig. 1.27. Structure analysis showed that crystal quality of epitaxial GaN is very high. After the optimization growth by HVPE on almost dislocation-free high-pressure GaN seed, GaN crystal quality is not much degradation, even lower than 1×10^4 cm^{-2}. Of course, single HVPE process is preferable to expand the size of GaN, but that requires a new HVPE system to grow more than 100 h. This is the only obstacle for the HVPE post-process technology on the high-pressure GaN seeds. But now, only a few of HVPE equipment can continue to grow more than 10 h, which is caused by the characteristics of HVPE growth.

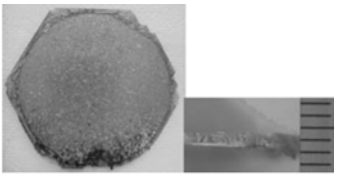

Fig. 1.28 2 in. bulk GaN crystal by Na-flux method on HVPE-GaN seeds

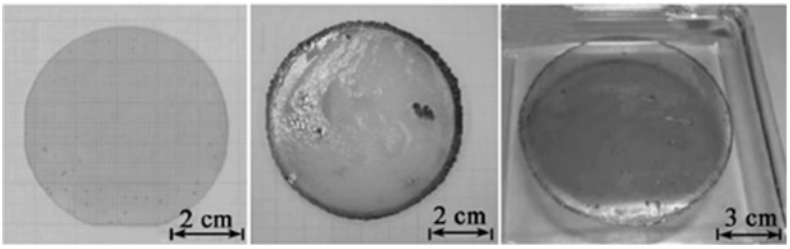

Fig. 1.29 Bulk GaN wafers of different scale by Na-flux method

By the HVPE post-processing technology on the high-pressure needle GaN seeds, a nonpolar GaN substrate can even be got. Nonpolar GaN substrate with high electrical conductivity has a special attraction in preparation of laser diode.

Different from the abovementioned growth technology of HVPE post-process on HPNSG GaN, some researchers studied the reverse growth of homogeneous GaN by high-pressure liquid-phase epitaxy technology on HVPE-GaN crystal. Osaka University finally got the GaN crystal with the thickness of 1.1 mm and diameter of 50 mm by molten Na-flux growth (atmospheric pressure, growth temperature from 40 to 860 °C), using HVPE-GaN chip with diameter of 45 mm as the seed crystal [13, 15], as shown in Fig. 1.28. Dislocation density is reduced from 1×10^8 cm^2 of seed crystal to 2.3×10^5 cm^2. Uniform GaN crystal of more than 2 in. with free of cracks has been already successful grown on the seed crystal, and the thickness is up to more than 750 μm, as shown in Fig. 1.29.

HVPE-GaN wafers can also be used as the seeds for ammonothermal growth of GaN. Poland Ammono Inc. [60, 61] has at present already succeeded in commercial mass production of polar, nonpolar, and semipolar GaN wafers with diameters of 1–2 in. and dislocation densities as low as 5×10^3 cm^{-2} (Fig. 1.30). But GaN single crystal of more than 2 in. in diameter is still in the development stage because of the lack of large-scale GaN seed. A large number of seeds can be placed in the ammonothermal reaction cavity at the same time, which is suitable for low-cost mass production of high-quality GaN.

1.4.7.2 GaN Boule by HVPE Technology

As described earlier, although ammonothermal growth and Na-flux growth for GaN single crystal seem to be a more productive potential, the small size by these

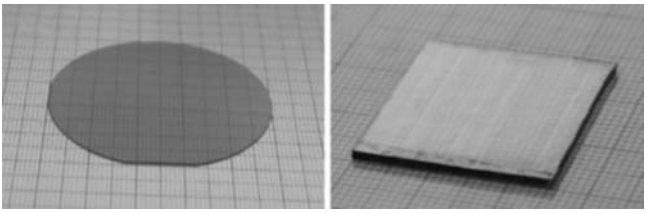

Fig. 1.30 A large dimension GaN single crystal by ammonothermal growth on HVPE-GaN seeds

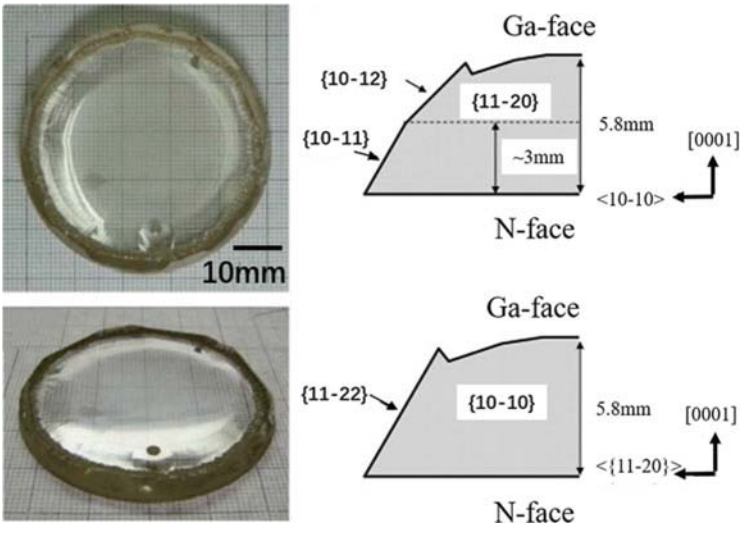

Fig. 1.31 Photograph of GaN boules with thickness of 5.8 mm by HVPE

two methods is still not competitive to the large-scale commercial production. Therefore, atmospheric hydride vapor-phase epitaxy is still a major means to obtain high-quality GaN with a large size. Wafers derived from boules produced by HVPE method will become the choice of substrates for GaN-based lasers and high-performance GaN-on-GaN light-emitting diodes.

Over the past few years, some companies, such as Sumitomo, TDI, Lumilog and Kyma Technologies, have increased the investment in this aspect and have been able to provide 2 in. GaN substrates of the dislocation density around 1×10^6 cm^2. The thickness of 2 in. GaN substrate is up to several millimeters, and a GaN boule grown via HVPE which is essentially the state of the art is shown in Fig. 1.31 [62]. It is said that the latest vertical HVPE system designed by AXITRON can be used for the growth of GaN boule with a length of 7 cm, and they also develop the planetary vertical HVPE system for the growth of multi-wafer GaN substrates at the same time.

If the size of the boules and wafers derived from this technique can be substantially increased in the manner of the evolution of the growth of ever-larger quartz crystals, sufficient cost reduction may be realized to meet the increasing need for chemically similar substrates that contain a very low density of dislocations. At present, the number of useful wafers that can be commonly gleaned from a single boule is in the range of 2–6, as there are multiple challenges in the growth of boules thicker than 10 mm.

1.4.7.3 Nonpolar GaN Substrate

Nakamura, the winner of Nobel physics prize, thinks that there are two ways to improve the quality of nitride material, a larger boule and nonpolar GaN. Nonpolar GaN will bring a new revolution of nitride materials. GaN-based devices are generally grown on the polar GaN, which leads to the strong built-in electric field in the active layer, the tilt of band gap, electron and lower luminous efficiency, etc. The power, efficiency, and life of the devices on the nonpolar substrate will significantly be improved, due to the reducing of the polarization effect and stress.

Nonpolar and semi polar substrates have attracted significant attention, but now the performance is restricted because of the high defect density. However, the substrate size is still very small and unsuitable for mass production. In China, Nanjing University first began to grow nonpolar GaN thick film on lithium meta-aluminate substrate by HVPE technology. In 2007, they obtained the freestanding nonpolar GaN substrate with a size of almost 2 in. by the self-separation due to thermal mismatch between nonpolar GaN and $LiAlO_2$ (Fig. 1.32). The sample, named as m-GaN, has a good (10–10) orientation and good quality. The stacking-fault density is about 10^4 cm^{-1}, while the thickness is only 90 μm. The full width at half maximum of m-GaN (110) by XRD analysis is about 773 arcs.

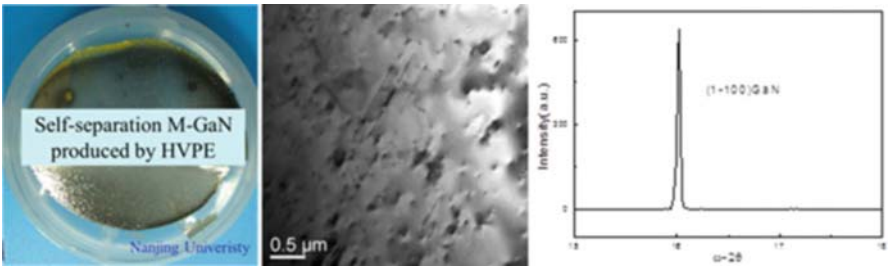

Fig. 1.32 Freestanding m-GaN substrate by HVPE growth (source: Nanjing University in 2007)

1.4.7.4 Low-Cost HVPE-GaN Templates on Sapphire

D. Martin et al. developed a low-cost process for the growth of GaN template directly only grown on sapphire substrate by HVPE method [63]. By this method, the thickness of high-quality GaN template is only 8 μm, far less than that of other high-quality GaN/sapphire template, 20–300 μm. Due to reducing the use of raw materials and simplified growth steps, this new process will greatly cut down the cost of the laser diodes and the transistor on GaN template.

Here, a two-step process similar to that of metal organic vapor-phase epitaxy was used to grow GaN template by Aixtron HVPE equipment. Some research shows that the quality and polarity of GaN are highly affected by the surface treatment of sapphire. First, after the cleaning in H_2 gas, sapphire substrate is exposed to 1050 °C of ammonia for the nitriding process about 4 min. Then the temperature is dropped to 600 °C to grow AlN layer on the substrate, and the temperature is increased to 1045 °C to continue the GaN growth. If the substrate is cooled to room temperature after the nitriding and exposed to the air, GaN layer is Ga-polar, and after the process again from cleaning to high-temperature growth, it will produce mixed-polar or N-polar GaN film. N-polar GaN film has more surface quality problems, and the doping is more difficult to control due to its higher impurity. Instead, Ga-polar GaN has a smooth surface, directly used for the subsequent growth without surface treatment. The surface roughness of GaN grown by this new process is 0.54 nm in the range of 5 × 5 μm by atomic force microscopy (AFM), and there is no crack in GaN template. The dislocation density after the acid etching process is only 1×10^8 cm^{-2}.

And the LED structure has also been grown on 8 μm HVPE-GaN template by MOCVD, whose properties are almost equal to that of the LED structure on MOCVD-GaN template. Some manufacturers of GaN template have interest in this growth technology.

1.5 Summary

The development of freestanding GaN substrate for homogeneous epitaxy is very important to high-power and high brightness LED, LDs and high-power microwave devices, etc. High-quality substrate materials provide excellent lattice-match and thermal-transportation characteristic for high-performance devices of high mass production. Through the use of the native substrate, nitride developers and device manufacturers will benefit its profit from epitaxial growth for the device. In this paper, we review the several methods and the latest progress in the area of the III-nitride substrates. Three main techniques (HVPE, ammonothermal, and Na-flux growth) are currently employed for the development and manufacturing of bulk GaN crystals for substrates. We have a special discussion on the technological aspects of HVPE for the production of GaN substrate materials, because HVPE is mostly suitable for obtaining the large-scale and low-cost GaN substrates at present.

In the near future, while exploring new methods for creating larger, high-quality crystals with the desired structural, optical, and electrical properties at an even lower cost, the size of nitride substrate materials will be continuously increased, and the defect density will reduce, reaching a level of device applications.

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Chapter 2
SiC Single Crystal Growth and Substrate Processing

Xiangang Xu, Xiaobo Hu, and Xiufang Chen

2.1 Introduction for SiC Single Crystal Materials

Silicon carbide (SiC) is a IV-IV compound material. In the basic structure unit of SiC, the silicon atoms and carbon atoms are combined together by sp3 covalent bonding, where each carbon atom is surrounded by four silicon atoms and vice versa. The extremely strong Si-C bonds give it unique physical, chemical, and mechanical properties [1], such as high electric breakdown field, high thermal conductivity, and so on. In addition, SiC is well known for its polytypism. The polytypic nature of SiC is that the crystal structure of SiC owns different ordering sequences in one dimensional with the same stoichiometry. And up to now, more than 250 SiC polytypes have been identified [2]. Meanwhile, different SiC polytypes exhibit distinct properties. Currently, the main polytypes of SiC used for device fabrication are 4H-SiC and 6H-SiC. 4H-SiC is an ideal material for power electronic and high-frequency devices, while 6H-SiC is usually employed for optoelectronic device fabrication.

The study about SiC has a quite long history. SiC was first discovered in the process of synthesizing diamond by Berzelius in 1824 [3]. Later, in 1885, Acheson invented a method for SiC preparation in melting furnace. The synthesis process was named as "Acheson process" afterward [4]. In this process, silica and coke are used as the source materials, while salt is employed as additive. The main product of Acheson process is SiC powder, which is mainly used as an abrasive in the processing technologies such as cutting, grinding, and polishing. The by-products in this process are mainly small 6H-SiC plates. In 1905, French scientist Moissan discovered the natural SiC in meteorites, which inspired the intensive interests in

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the potential application of SiC [5]. After that, a series of simple SiC-based devices were fabricated. In 1907, the first SiC light-emitting diode (LED) was made by an engineer named Round [6]. In 1920, SiC-based sensor was applied in the radio receivers. However, at that time, there was no efficient method to synthesize SiC single crystals with high quality. As a result, the development of SiC growth once got stranded. Up to now, many methods have been invented for SiC single crystal growth, including vapor growth and solution growth.

2.1.1 Vapor Growth Method

In 1955, Jan Antony Lely proposed a sublimation technique to prepare SiC single crystals, which opened up a new era of SiC material and devices [7]. This method was name as Lely method later. The schematic diagram of Lely method is shown in Fig. 2.1. The industrial-grade SiC powder was used as source material and placed around the dense graphite crucible wall. The porous graphite was employed to separate the source material and the growth cavity. In the crucible, the temperature around the crucible wall was higher than in the center of the crucible. As a result, the growth was driven by the temperature gradient in the crucible. At first, the source material sublimated at high temperature (about 2500 °C); thus gas species was produced. After that, the vapors penetrated into the porous graphite to grow lamellar crystals on the inner surface. During the growth, argon was used as inert gas, and the pressure in the growth chamber was kept around 1 atm. The gas species randomly nucleated at the inner cavity wall. The defects and micropipe density in

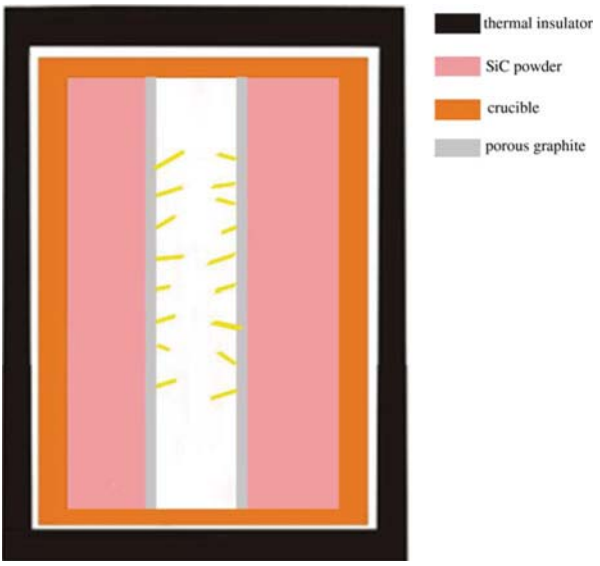

Fig. 2.1 Schematic diagram of Lely method for SiC crystal growth (Provided by Dr. Yan Peng at Shandong University)

the grown crystal are pretty low, which means this method can prepare 6H-SiC single crystals with high quality. However, crystals obtained by this method are in small size and irregular shape. Therefore, the crystals cannot be used for device fabrication. At the same time, due to the random nucleation at the inner cavity wall, 4H and 15R-SiC polytype inclusions often appeared in the grown crystals.

In order to solve the problem of polycrystalline nucleation, Tairov and Tsvetkov modified Lely method by an innovative use of SiC seed in 1978 [8]. The modified Lely method (also called "seed sublimation method" or "physical vapor transport method") was constituted of three steps: (1) sublimation of SiC source material, (2) mass transport of sublimed gas species, and (3) surface reaction and crystallization. The schematic diagram of growth furnace is shown in Fig. 2.2. In this method, SiC powder is put at the bottom of the crucible, and the seed is kept on the lid of the crucible. The distance of source-to-seed is in the range of 30–50 mm. Electromagnetic induction is employed to heat up the crucible in the temperature range of 2100–2400 °C. The graphite felt or porous graphite is used as thermal insulation. During the growth process, high purity argon is flowed as carrier gas, and the pressure in the growth chamber is kept at 20–60 mbar. The SiC powder was decomposed at high temperature, generating Si, Si2C, and SiC2 gas species. The gas species driven by the temperature gradient are transported to the seedand then

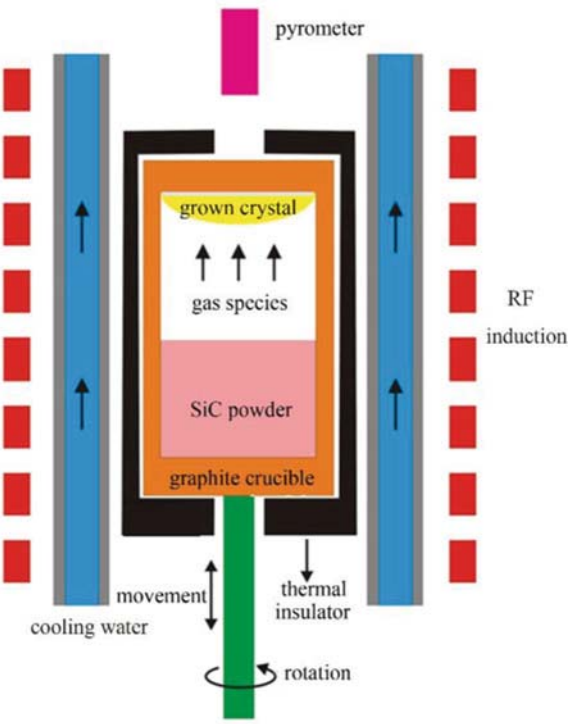

Fig. 2.2 Schematic diagram of a modified Lely method for SiC crystal growth (Provided by Dr. Xianglong Yang at Shandong University)

crystallize on the seed. During the growth, the main reactions were summarized as follows:

$$\begin{aligned} &Si_2C\,(g) + SiC_2\,(g) \leftrightarrow 3SiC\,(s) \\ &SiC_2\,(g) + 3Si\,(g) \leftrightarrow 2Si_2C\,(g) \\ &Si_2C\,(g) \leftrightarrow 2Si\,(g) + C\,(s) \end{aligned} \tag{2.1}$$

In this method, the crystal was grown approximately along isotherm lines. As a result, it is crucial to design the thermal field. Though micropipes and dislocations are commonly observed in the crystals grown by this method, the modified Lely method is currently the most mature method for growing bulk SiC single crystals. Using this method, 6H-SiC and 4H-SiC have been commercialized since 1991 and 1994, respectively. Recently, in Cree Research Inc., 4H-SiC single crystals with a diameter of 200 mm were successfully grown [9].

2.1.2 Solution Growth Method

Besides vapor growth, solution is another SiC single crystal growth method. Different from other semiconductor materials (such as Si and GaAs), SiC does not have any liquid phase in normal engineering conditions. According to theoretical analysis, the liquid phase of SiC appears only under high-pressure (>105 bar) and high-temperature (>3200 °C) conditions [10]. The solubility of carbon atoms in melting silicon varies from 0.01 to 19% in the temperature range of 1412–2830 °C. Recent study revealed that the solubility of carbon atoms in melting silicon can be increased by adding transition metal or rare earth metals to silicon solvent [11]. Consequently, it is possible to grow SiC single crystals by solution technique. As shown in Fig. 2.3, high purity graphite crucible is used as both container and

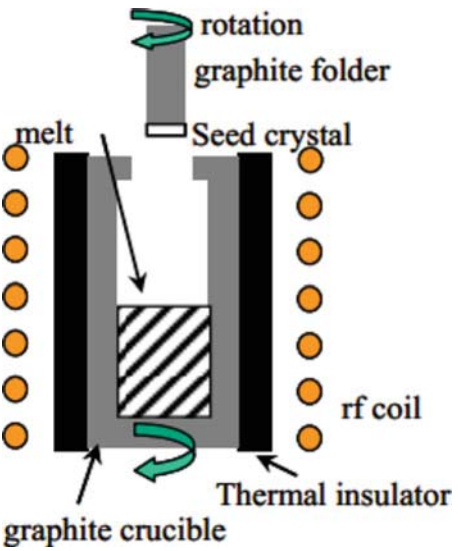

Fig. 2.3 Schematic diagram of a SiC solution growth heated by RF induction

carbon source. High purity Si and metals (such as Ti, Cr) are mixed and put in the crucible at argon atmosphere. SiC seed is mounted on a graphite folder. The typical growth temperature is in the range of 1600–1750 °C. During the growth, the seed is dipped into the ternary solution gradually, while the seed and crucible are rotated in opposite direction. Given that the crystals are grown under near thermal equilibrium condition, there are little micropipes and dislocations in SiC crystals grown by solution method. Therefore, high-quality SiC crystals can be grown by solution method.

2.1.3 *High-Temperature Chemical Vapor Deposition (HTCVD) Method*

HTCVD is the third method for bulk SiC single crystal growth. High growth rates and long SiC single crystals are expected by this method in comparison with PVT and solution methods. Figure 2.4 is a schematic illustration of a HTCVD SiC growth method [12]. A graphite heater is heated by induction coils and a cylindrical insulator is on the outside of the heater. A seed crystal was fixed on the seed holder. The Si and carbon sources are SiH4 and C3H8, respectively. H2 is used as carrier gas. At high temperature, the source gases were cracked and transformed into the reaction species such as Si, SiC2, Si2C, and C2H2. Then the species were deposited on the seed crystal. HTCVD method has the following advantages: one is the continuous gas source supply. This enables long-term growth which contributes to a long SiC crystal ingot; the other is the accurately controllability of the partial

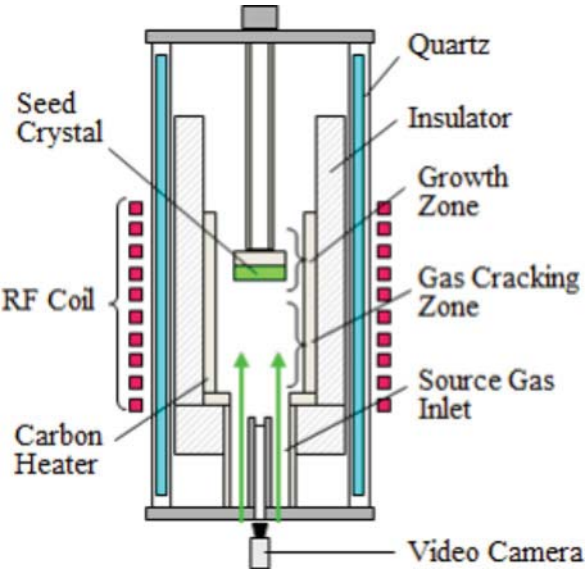

Fig. 2.4 Schematic illustration of the structure of a HTCVD SiC growth method

pressure, the gas flow, and the species ratio of the source gases which make the possibility to grow SiC crystal with Si/C stoichiometry; in addition, high purity semi-insulating SiC crystal can be grown by using high purity gas source.

In summary, SiC bulk single crystals can be grown by PVT, solution, and HTCVD. PVT is a conventional SiC crystal growth method and suitable for mass production. In comparison, the solution and HTCVD are suitable for the high structural quality SiC and the high purity semi-insulating SiC crystal growth, respectively.

2.2 Structure and Physical Properties of SiC

SiC possesses excellent mechanical, thermal, electrical, physical, and chemical properties which make it an ideal semiconductor material for the fabrication of the novel electronic and optoelectronic devices. From a viewpoint of crystallography, SiC is the best known example of polytypism. The variation in occupied sites along the c-axis in a hexagonal close-packed system brings about different crystal structures which were termed as polytypes. Figure 2.5 shows schematically the structures of typical SiC polytypes [13]. There are three possible sites, denoted by A, B, and C. Two layers cannot successively occupy the same site. For example, the next layer on the top of an "A" layer must occupy either "B" or "C" sites. In principle, there are infinite possibilities for the stacking sequence. However, for most materials, only some stacking structures are stable such as the zinc blende or wurtzite structure. For SiC, there are more than 200 polytypes. Polytypes are represented by the number of Si-C bilayers in the unit cell and the crystal system (C for cubic, H for hexagonal, and R for rhombohedral). 3C-SiC is often called β-SiC and other polytypes are termed as α-SiC. The structures of popular SiC polytypes

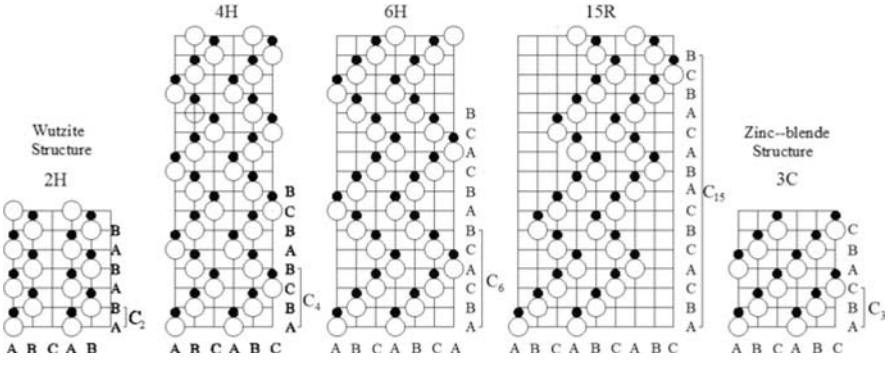

Fig. 2.5 Schematic diagram of SiC structure with different polytypes viewed along [11–20] direction in hexagonal system

Table 2.1 Comparison of basic properties of several semiconductor materials

Property/material	4H-SiC	6H-SiC	Si	GaAs
Thermal conductivity (W/cm K)	4.9	4.9	1.3	0.5
Bandgap (eV)	3.2	3.0	1.12	1.42
Intrinsic material transparent	Yes	Yes	No	No
Available doping	n, p	n, p	n, p	n, p
Saturated electron drift velocity (10^7 m/s)	2.0	2.0	1.0	2.0
Electron mobility (cm^2/Vs)	1000	600	1450	8500
Critical breakdown electrical field (MV/cm)	3	3.2	0.3	0.6
Lattice constant (*a*)	3.073	3.081	3.84	4.00
Lattice mismatch with GaN (%)	3.8	3.5	−17	−22
Thermal expansion mismatch with GaN (%)	−0.11	−0.12	−0.17	0.11

are 4H, 15R, 6H, and 3C as shown in Fig. 2.5 where open and closed circles donate Si and C atoms, respectively.

Considering the immediate neighbor site of Si-C bilayer stacking, the lattice sites with hexagonal-structured surroundings are termed as "hexagonal sites," and those with cubic-structured surroundings are called as "cubic sites." 4H has one hexagonal and one cubic site and 6H-SiC one hexagonal and two inequivalent cubic sites, while 3C-SiC contains only cubic sites. Hexagonal and cubic sites differ in the location of the second-nearest neighbor leading to different crystal fields. As a consequence, the energy levels of dopants, impurities, and point defects are affected by the lattice site or the hexagonal/cubic ratio. It has been found that the bandgap of SiC polytype increases monotonically with the increase of its hexagonality. The bandgap at room temperature is 2.36 eV for 3C-SiC, 3.26 eV for 4H-SiC, and 3.02 eV for 6H-SiC, respectively.

Compared with the first-generation semiconductor Si and the second-generation semiconductor GaAs, the third-generation semiconductor SiC possesses better physical and chemical properties. Table 2.1 lists the basic properties of several semiconductor materials [14]. From this table, we can see that SiC has higher thermal conductivity, wider bandgap, higher hardness, and higher chemical stability.

The basic properties of SiC material make the electronic devices the follow advantages:

1. The bandgap of SiC is nearly three times as that of Si. Wide bandgap can assure the long-term reliability of device which runs at high temperature. At high temperature, intrinsic carrier excitation will occur, which further causes the device failure. The wider the bandgap, the higher the device limit operating temperature. The limit operating temperature for Si device is lower than 200 °C. In contrast, the limit operation temperature for SiC device exceeds 400 °C.
2. The critical breakdown electrical field of SiC is ten times as that of Si. Thus, SiC can sustain much higher voltages than Si. Devices can be shrunk in size reducing the resistive losses. It reduces system complexity and cost while improving reliability.

3. SiC has a much higher thermal conductivity roughly three times as that of silicon. For SiC device, heat is conducted away much more effectively. It greatly reduces complexity of cooling systems.
4. SiC can carry much higher currents almost five times as that of silicon. It can reduce the area of devices and further reduce the parasitic capacitance.
5. Power devices made from SiC can switch roughly ten times faster than those made from silicon. Therefore, the power conversion circuits operate faster for SiC devices. It means much smaller energy storage capacitors and inductors can be made from SiC.

In addition to the above advantages, SiC is also an ideal substrate for the fabrication of GaN-based optoelectronics and radio frequency devices due to small lattice mismatch with GaN.

Therefore, SiC as the representative of third-generation semiconductor materials has extensive application prospects.

2.3 SiC Single Crystal Growth by PVT Method

From the phase diagram of the Si-C binary system, we know that it is very difficult to obtain stoichiometric SiC liquid phase. It is impossible to employ congruent melt method for SiC single crystal growth. Up to now, the most successful growth method for bulk SiC single crystal is PVT method which consists of the following procedures: (1) sublimation of SiC source, (2) mass transport of sublimed species, and (3) surface reaction and crystallization. Therefore, PVT method was also called as sublimation method.

The principle and growth furnace for the PVT method has been introduced. In order to grow high-quality SiC single crystal, both thermodynamic and kinetic factors must be considered. The process control to maintain optimal thermal and chemical conditions is very important so that an ideal growth interface can be obtained.

Figure 2.6 shows the partial pressures of SiC sublimed species from SiC-C(s) and SiC-Si(l) systems at high temperature [15]. In the gas phase, the dominant species are Si2C, SiC2, and Si which are not stoichiometric SiC.

In the procedure of SiC growing, SiC powder was decomposed at the temperature higher than 2300 °C; the gas phase in sublimation growth is usually Si-rich. This causes the source more and more rich in carbon, i.e., the graphitization of source. In order to avoid the formation of carbon inclusion in SiC single crystal, Si-rich SiC source is often used.

For the PVT growth of SiC, the growth occurred in a nearly closed graphite crucible. We can only measure the temperature at the upper surface of crucible lid or bottom of crucible by using a pyrometer. It is impossible to know the thermal field inside the crucible. Because growth experiment alone is not sufficient to develop a well-controlled PVT growth procedure, modeling and simulation of SiC PVT

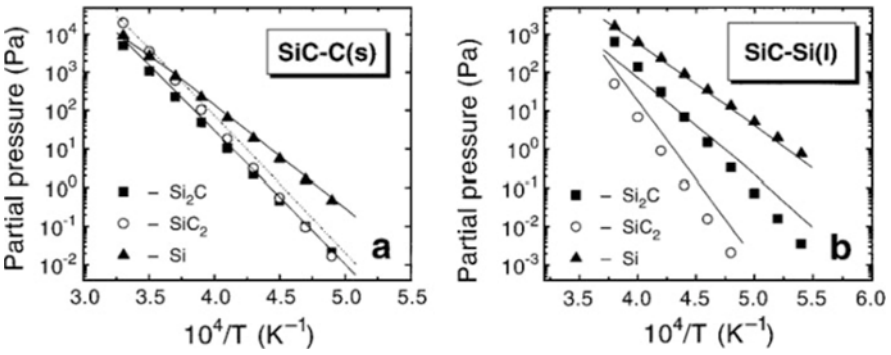

Fig. 2.6 Partial pressures of Si, Si_2C, and SiC_2 vs. temperature calculated for three-phase equilibria: (**a**) SiC-C(s) and (**b**) SiC-Si(l)

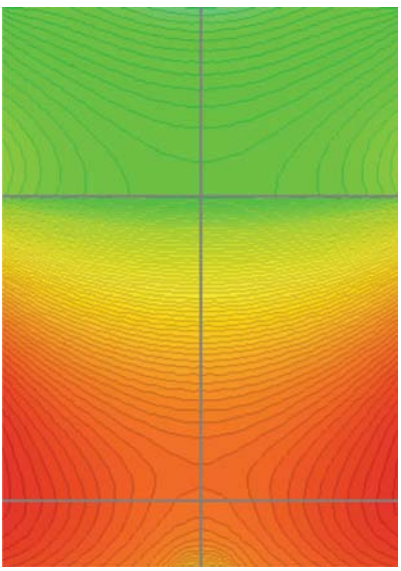

Fig. 2.7 Typical thermal field of SiC PVT growth (Provided by Dr. Yan Peng at Shandong University)

growth are necessary. In the simulation of thermal field, heat transfer by thermal conduction, gas-phase convection, and radiation should be considered. In the heat transfer calculation, the large crystallization energy of SiC must be considered. Heat transfer by radiation is a dominant process at very high temperature in the PVT growth.

Figure 2.7 shows a typical thermal field of SiC PVT growth which was simulated by using a virtual reactor (SiC) software exploited by the semiconductor technology research company. From this figure, the thermal field is described by multiple temperature contour lines. The SiC powder is located in the high-temperature zone of the lower part of the crucible, whereas SiC seed is placed in the low-temperature zone of the crucible lid. At the driving force of temperature gradient, gas species

were transported from the source into the seed, and crystal growth occurred. It has been found that the thermal field was affected by the following parameters such as thickness of insulation shield, shape of crucible, diameter of temperature measurement hole, heating frequency and power, the relative position between crucible and induction coil, etc.

If the influence of mass transport on growth rate is neglected, the shape of SiC growth interface is approximately as same as that of temperature contour lines. For actual crystal growth, a slight convex thermal field is favorable for the thermal stress control and diameter enlargement. Sometimes, to obtain an ideal thermal field, the relative position between crucible and induction coil should be adjusted. Figure 2.8 shows the influence of the relative position between crucible and induction coil on thermal field in which crucible position percent denotes the deviation degree of real crucible position away from standard position.

From Fig. 2.8, we can see that as the crucible move upward corresponding to the increase of crucible position percent, the highest temperature zone shifts toward the crucible bottom. Simultaneously, in the growth cavity, the axial temperature gradient increases, and the radial temperature gradient decreases. Therefore, following the movement of crucible upward, the shape of growth interface will become gradually from convex to plan and vice versa. Figure 2.9 shows a typical as-grown 4H-SiC crystal which has an ideal shape with a slight convex interface.

To predict the growth rate and interface shape, a mass transfer model must be coupled with the heat transfer calculation and the thermodynamic database. In the gas phase, fluid transport is based on the low-pressure kinetic theory of gases. Diffusion coefficients, viscosity, conductivity, and specific heat of species are calculated as a local function of temperature, pressure, and composition. The Stefan flow caused by the phase change of SiC has to be considered. The thermodynamic calculation is performed by minimization of the total free energy of the Si-C-Ar system at high temperature. Calculations indicate that three particular species, Si, Si_2C, and SiC_2, are indeed important to describe sublimation growth [16]. Selder et al. [17] performed the global numerical simulation of heat and mass transfer for SiC bulk crystal growth by PVT. The physical model is based on the two-dimensional solution of the coupled differential equations describing mass conservation, momentum conservation, conjugate heat transfer including surface to surface radiation, multicomponent chemical species mass transfer, and advective flow. The model also includes the Joule volume heat sources induced by the electromagnetic field. Figure 2.10 shows the calculated temperature distribution inside the growth cell and the growing crystal for three different points in time. Due to the existence of radial temperature gradient, the growth front is getting convex. However, the shape of growth front is not only depending on the thermal field at the crystal/gas interface but also influenced by gas species mass transfer especially at the periphery of the growing crystal. As a consequence of two effects, the radial growth rate distribution is smoothed out as the crystal length increases.

Figure 2.11 shows the calculated radial growth rate distributions for the three growth stages. We can see that the growth rate at the crystal center is decreasing with the increase of crystal length, and the radial growth rate distribution is smoothed out

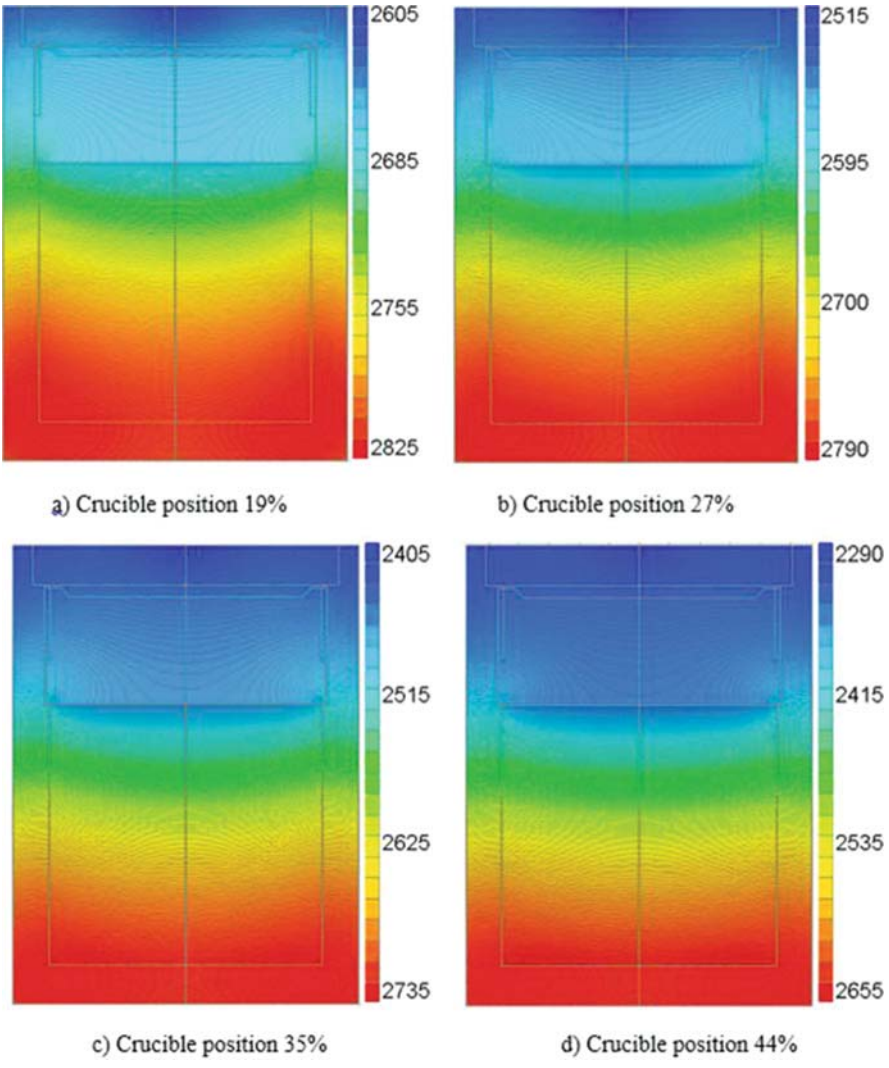

Fig. 2.8 Influence of relative position between crucible and induction coil on the thermal field (Provided by Dr. Peng Y at Shandong University). (**a–d**) Correspond to 19% 27%, 35% and 44% crucible position, respectively

with increasing growth time. The above simulation was confirmed by actual SiC single crystal growth experiment.

Figure 2.12 demonstrates a longitudinal cut slice of a SiC crystal. In this figure, dark regions are nitrogen doped, and bright regions correspond to nominally undoped SiC. The positions of the marked and unmarked regions provide the detailed information about the growth front evolution. The crystal growth process is

Fig. 2.9 Photograph of 4 in. 4H-SiC single crystal (Provided by Dr. Peng Y at Shandong University)

in agreement well with the simulations. Especially, the shape of the growth front is similar to the simulation. For both experiment and simulation, the radial growth rate variation is decreasing with the increase of crystal length. By comparing experiment to simulation, it implies that the modeling is successful.

The actual SiC bulk crystal growth via PVT is a complex process in which a number of parameter have to be controlled. The growth rate is a strong function of temperature gradient, source to seed distance, and chamber pressure. The crystal growth procedure includes the following six stages:

1. Low-temperature and high-vacuum stage: At the initial stage, the water and oxygen gas absorbed by graphite parts in growth chamber have to be exhausted, and the chamber pressure is lower than 100 nbar. In the meantime, the crucible was slowly heated to a temperature lower than 1400 °C so that the nitrogen absorbed by graphite material was released and evacuated. If residual oxygen or water exists in the chamber after high vacuum, the crucible and thermal shield materials will be oxidized and damaged.
2. High-temperature and high-pressure stage: In order to control the growth rate so that the nucleation proceeded steadily, the carrier gas Ar was flushed into the chamber, and the pressure in the chamber reached 800 mbar. Because the SiC powder was decomposed into Si, Si_2C, and Si_2C gas species at high temperature, the partial pressures of SiC gas species will be lowered at high background pressure. In this case, the growth rate was controlled at a very low level. It is favorable for SiC nucleation on seed.
3. SiC nucleation stage: At this stage, temperature and pressure were kept stably. SiC was nucleated on seed at a low growth rate. An ideal status is that a large area facet was formed without any structural defects.
4. Pressure decreasing and crystal growth stage: After SiC nucleation was completed, crystal growth rate was fastened by decreasing growth pressure. The growth pressure was decreased from present into a target pressure. Pressure decreasing rate can be expressed as follows:

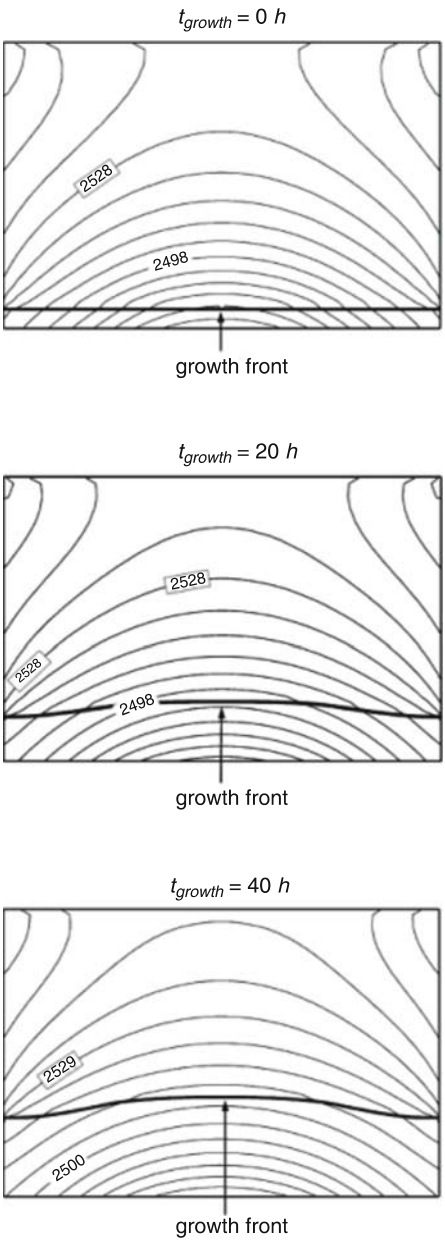

Fig. 2.10 Temperature distribution and growth front for three different points in time during SiC PVT growth. The seed is positioned at the bottom of the individual images. The SiC source is on the top

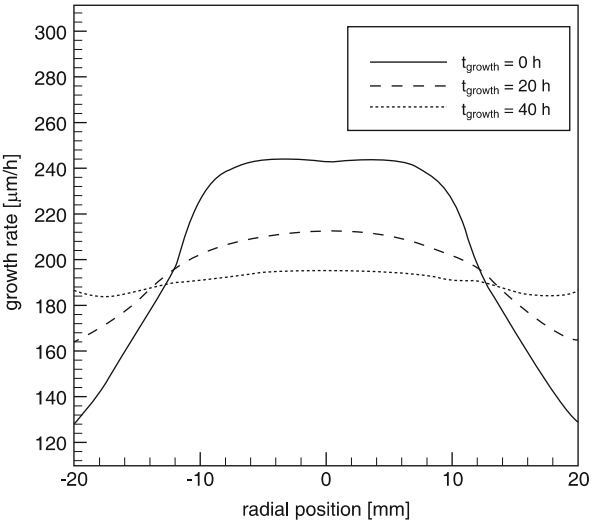

Fig. 2.11 Radial distribution of the calculated growth rate for three different points in time

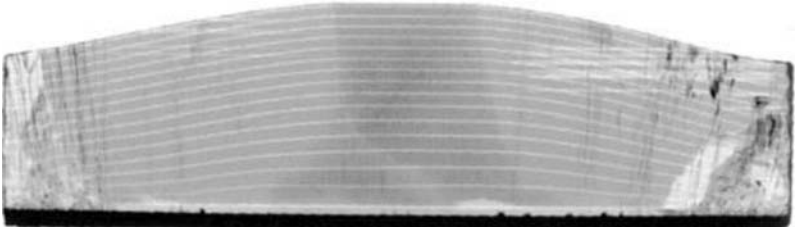

Fig. 2.12 Longitudinal cut slice of a SiC crystal in which the shape of growth front was marked by an interface demarcation technique. Undoped regions exhibit a bright contrast

$$p = p_0 \mathrm{e}^{-t/\tau} \tag{2.2}$$

where p_0 and p donate the present and target pressure, respectively, and τ is constant.

5. Stable crystal growth stage: When the growth pressure reached the target value, the crystal growth proceeded stably at a certain temperature and pressure. The optimal growth rate was proximately 200–300 μm/h.
6. Pressure increasing and cooling stage: When the crystal ingot length was estimated to be 20–30 mm, crystal growth should be terminated by increasing pressure. Then the temperature was lowered slowly into room temperature. The whole growth procedure was ended.

2.4 The Formation and Control of Structural Defects in SiC Single Crystals

SiC single crystals contain various structural defects such as foreign polytypes, micropipes, dislocations, inclusions, point defects, etc. Defects in SiC wafers will deteriorate the device performance and shorten the device lifetime. So defects should be reduced or eliminated.

2.4.1 Micropipe Defects

A micropipe is actually a hollow core associated with a super-screw dislocation. It penetrates through the entire crystal along the c-axis with diameter from tens of nanometers to several micrometers. A SiC device with a micropipe in its active area cannot support significantly high electrical field. Therefore, micropipe is known as a "killer defect" [18]. According to the Frank theory [19], a dislocation whose Burgers vector exceeds a critical value, of the order of magnitude 10 Å, is only in equilibrium with an empty tube at its core. When a micropipe was formed, the elastic strain energy released by the formation of hollow core and surface free energy created by the interior cylindrical surface of hollow core reached a balance. The radius of a hollow core is given by

$$r = \mu b^2 / 8\pi^2 \gamma \tag{2.3}$$

Here γ is the specific surface free energy of the material, and μ the rigidity modulus. The equation has been confirmed by different experiments for micropipes in SiC [20–22].

Figure 2.13 shows an atomic force microscopic (AFM) image of a micropipe in 6H-SiC. At the central region, a circular empty tube can be identified.

Huang et al. [23, 24] have taken the direct image of the super-screw in SiC by back-reflection white-beam synchrotron topography and simulated it by tracing ray method. Based on the dislocation theory, it was considered that the distorted region around a super-screw dislocation core consists of a large number of small crystallites which are orientated by the strain field and diffract X-rays independently according to their local lattice orientations. Under these conditions, calculating the traces of the diffracted X-rays enables one to map the spots where these rays intersect the recording plate, and the contrast intensity of the direct image is then determined by the density distribution of the intersection spots. Figure 2.14 shows the back-reflection synchrotron topograph of a 6c super-screw dislocation in 6H-SiC wafer. Comparison of synchrotron topograph of Fig. 2.6a to the kinematic contrast of Fig. 2.6b for a 6c super-screw dislocation in 6H-SiC wafer indicated that hollow-core micropipes in 6H-SiC the c-axis with Burgers vectors being multiples of the lattice constant c.

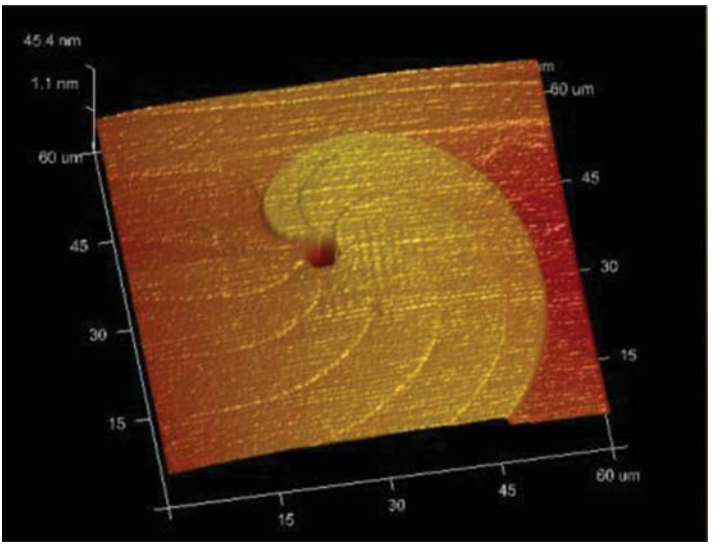

Fig. 2.13 An AFM image of a micropipe in 6H-SiC single crystal (Provided by Dr. Peng Y at Shandong University)

However, it is should be noted that Fig. 2.14a is actually the magnified image of the super-screw dislocation, and the diameter of the circular spot is the function of sample-recording film distance and Burgers vector. Figure 2.15 shows the principle for the contrast formation of a super-screw dislocation. From this figure the formation of the circular contrast feature on the film can be easily understood. From an overall viewpoint, only the different semi-apex angles of the twisted cones determine diffracted X-rays overlap in space and further determine the overall image features of the dislocation on topograph. Obviously, both the magnitude of the Burgers vector and the sample-film distance influence the topographic contrast, especially the diameter of the white-contrast region.

It was found that most of micropipes have the characteristic of mixed dislocations, i.e., their Burgers vectors have both edge and screw contents [23]. Heindl et al. investigated the structures of micropipes in SiC by using AFM and found that micropipes were hollow-core dislocations according to Frank's model but contain dislocations of mixed type [25].

The causes of micropipe generation during PVT growth of SiC include back-side bubble in seed, foreign polytype, inclusion, etc.

Kuhr et al. have observed the formation of micropipes caused by hexagonal void [26]. Figure 2.16a shows a back-reflection topograph of the area above a void, and Fig. 2.16b shows the same area below the void [26]. The area the void will pass through is outlined in white in Fig. 2.16a, and the hexagon of light and dark orientation contrast that occupies the center of Fig. 2.6b represents the trace of the

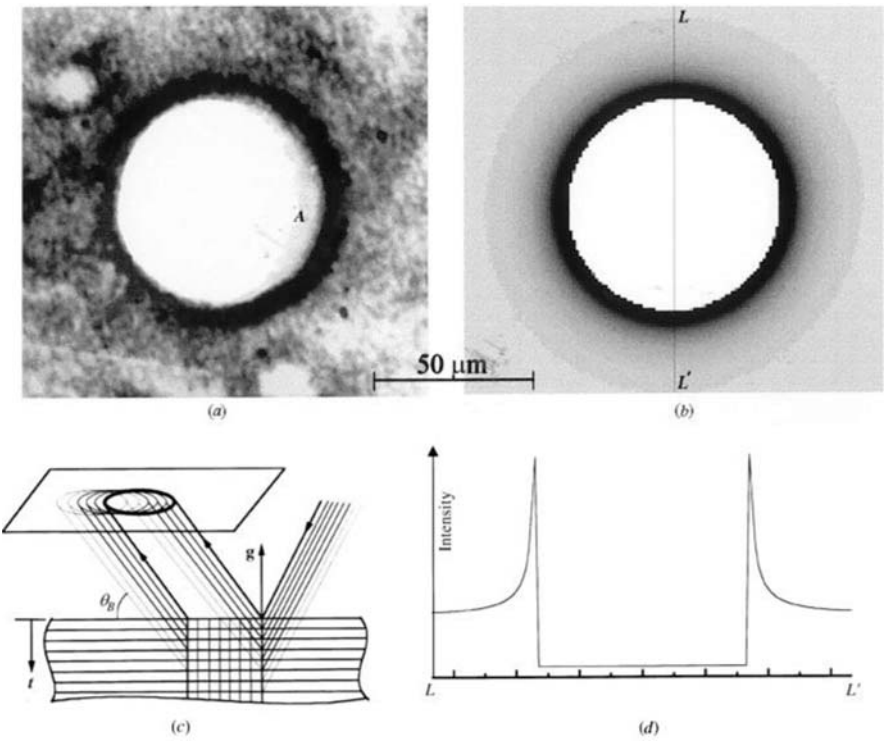

Fig. 2.14 Back-reflection synchrotron topograph of a 6c super-screw dislocation. (**a**) Synchrotron topograph of super-screw dislocation. (**b**) Kinematic contrast of a screw dislocation (Burgers vector magnitude b = 6c = 91.02 Å), simulated by tracing ray method. (**c**) Schematic representation of the displaced diffraction images associated with the deeper layers. (**d**) Radial intensity profile of the simulated image in (**c**)

void's path through the crystal during crystal growth. Large white spots on the left and lower right of the hexagon in both images are micropipes present in both wafers.

Figure 2.17 is a schematic illustration of the void and micropipe formation process. Voids are often formed at the interface between the seed crystal and crucible cap. Evaporation steps at the top of the void and growth steps on the bottom of the void provide strong evidence that SiC transport occurs within the void and that the void moves along the temperature gradient within the growing boule. Dislocations line up along the trace of the void path, and screw dislocations combine to form micropipes at the corners of the void, leaving an area directly beneath the void that is free of screw dislocations. This mechanism for micropipe formation is likely to be dominant in any crystal that contains hexagonal voids. Elimination of hexagonal voids by the use of a back-side evaporation barrier and proper seed mounting techniques was effective to reduce micropipe densities in PVT-grown SiC.

Figure 2.18 is a scanning image of a longitudinal cut 4H-SiC crystal. From this image, we can see that some foreign polytypes including 15R with yellow color and

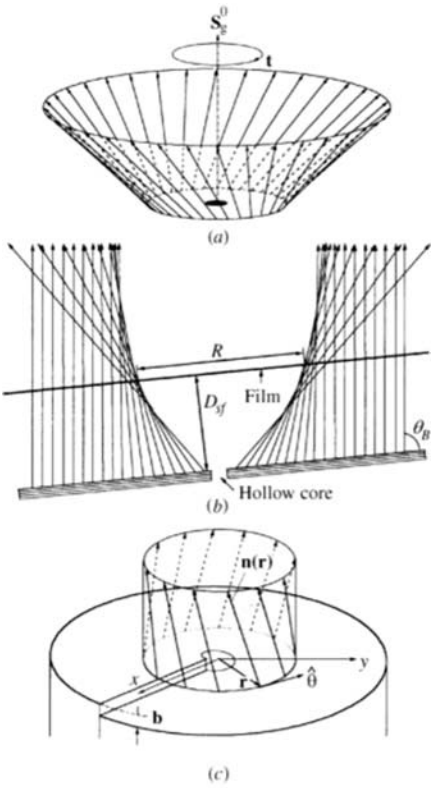

Fig. 2.15 Principle for the contrast formation of a super-screw dislocation in back-reflection synchrotron topograph. (**a**) Schematic drawing of one of the twisted cones. *t* twisting direction. (**b**) Overlap of the twisted cones in space. (**c**) Inclination of coordinate-dependent normal *n* causing the twist of diffracted X-ray

6H with green color appear in 4H-SiC crystal. As soon as the polytype phase transition occurred, a large number of micropipes were formed on the interface between the host polytype and other foreign polytype. Since the foreign polytype causes the serious mismatch in the stacking sequence as the foreign polytype nucleus meets the host polytype, the stacking mismatch and the associated large strains trigger micropipe formation. For 4H-SiC crystal growth, the temperature window for keeping polytype stability is very narrow. Any fluctuation in the temperature profile or pressure in growth cavity may cause unintentional supercooling and deviation of the C/Si ratio at growth front which further lead to the formation of foreign polytypes.

In addition, Si droplets and carbon inclusions in SiC crystals also cause the formation of micropipes.

Glass et al. [27] believed that the excess Si on the growth surface at the initial stage and the accumulation of free C after the source graphitization are the main causes for the formation of micropipes. Figure 2.19 shows an example of (a) a technological issue where a graphite particle has caused a micropipe and (b) a process instability issue where constitutional supercooling has produced Si droplets on the growth surface which have led to micropipe streaming.

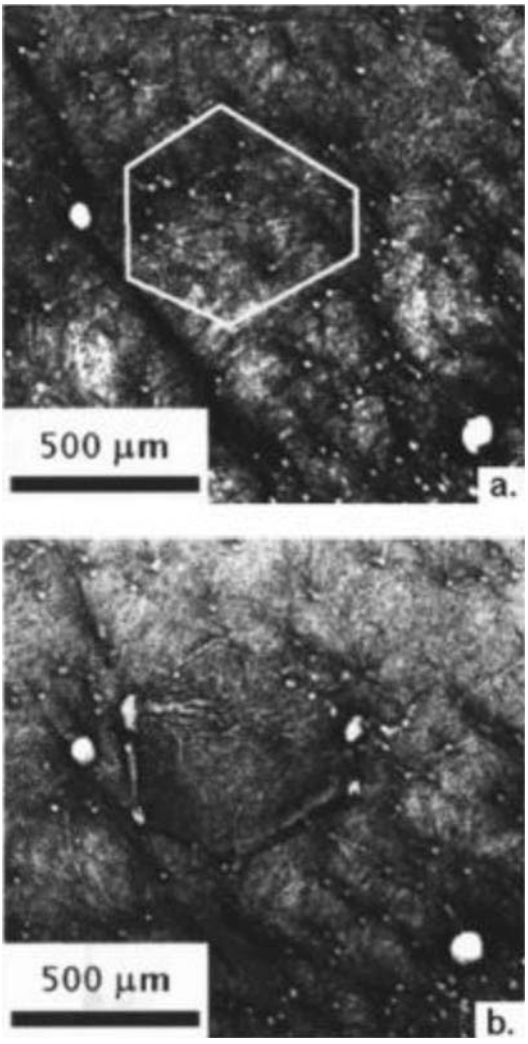

Fig. 2.16 Back-reflection X-ray topographs of the area above a void (**a**) and below a void (**b**) in 6H-SiC. The projected passage of the void has been traced in white. The screw dislocations are visible above the void in (**a**) and are not visible beneath the void in (**b**)

Origins of micropipes in SiC come from two sources. One kind of micropipes was generated from the instability growth conditions or other defects such as seed back-side void, foreign polytype, C or Si inclusion, etc. The others originated from the extension of micropipe in seed, i.e., micropipes have the heredity. For the former case, micropipes were controlled by optimization of the growth conditions such as the seed and the source temperature, the pressure of ambient gas, etc. For the latter case, many efforts have been made in the past decade to reduce or eliminate micropipes in SiC crystals.

To eliminate micropipes in SiC crystals, rhombohedral plane seeds were used to grow SiC crystals [28, 29]. Because the 4H-SiC {0 3−3 8} plane is inclined to the

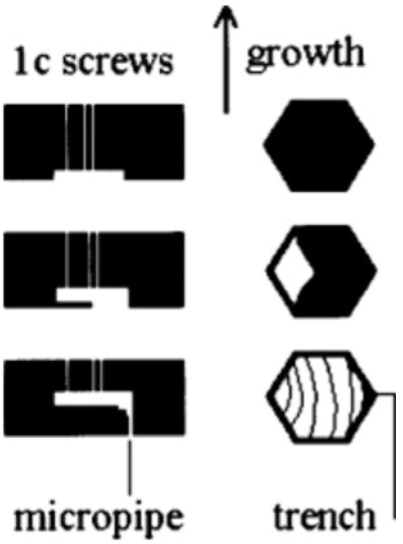

Fig. 2.17 Schematic diagram showing void formation and movement. The void begins as a cavity in the seed attachment layer, growth within the void occurs by lateral attachment and step flow, and the trench closes at the corners of the void, forming micropipes that extend beneath the void

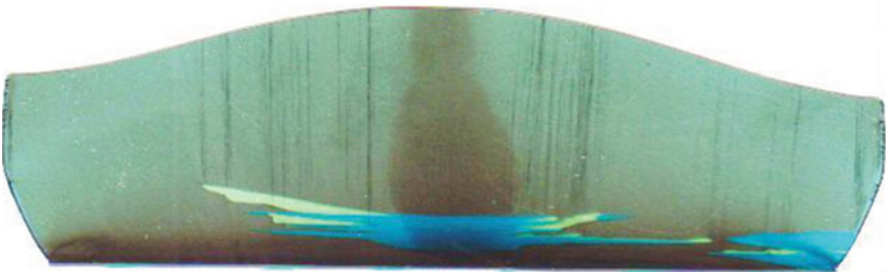

Fig. 2.18 Scanning image of a longitudinal cut 4 in. 4H-SiC crystal (Provided by Dr. Yang X L at Shandong University)

c-plane at 54.7° as shown in Fig. 2.20a and the 4H-SiC {0 3−3 8} plane is semi-equivalent to 3C-SiC {100} as shown in Fig. 2.20b, the 4H-SiC{0 3−3 8} plane has a low surface free energy and can be used as seed plane.

Shiomi et al. [28] found that a micropipe and stacking fault-free region was generated in crystals grown on the 4H-SiC {0 3−3 8} seed, as shown in Fig. 2.21. At the height of H′, there were two regions in the ingot, one was a perfect region without any micropipe and stacking fault (region A) and the other was a stacking fault region (region B). In other words, micropipe and stacking fault-free seed can be obtained by several repeating 4H-SiC crystal growth runs on {0 3−3 8} seed.

Figure 2.22a, b shows the surface morphology of the 4H-SiC {0 3−3 8} wafers after molten KOH etching. Many stripes due to the stacking faults are observed in the wafer from region B. In contrast, region A has high perfection without deep etch pits due to micropipes. It was obvious that the growth on the 4H-SiC {0 3−3 8} seed was suitable to achieve a SiC wafer without micropipes or stacking fault.

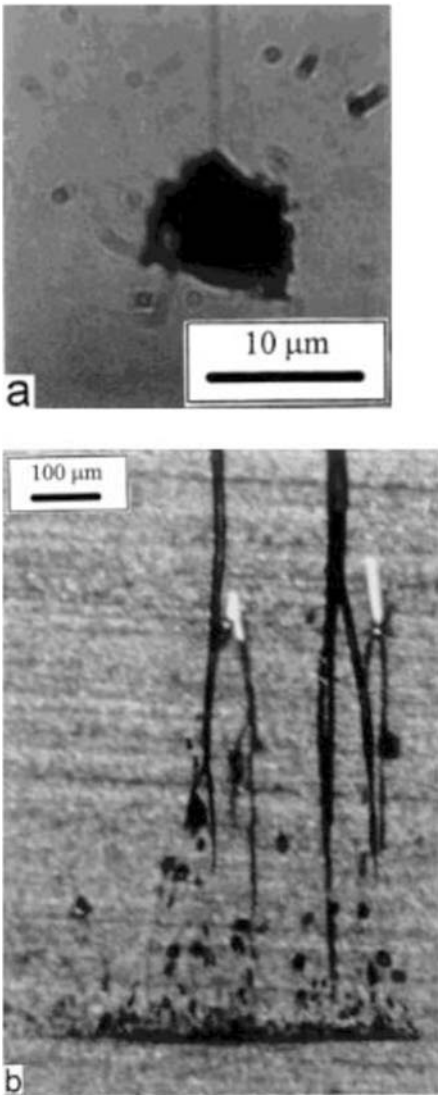

Fig. 2.19 (**a**) Graphite particle with resulting micropipe and (**b**) results of a process instability issue where constitutional supercooling has produced Si droplets on the growth surface leading to micropipe streaming

Li et al. [29] found that {0 1−1 2}, {0 1−1 3}, and {0 1−1 4} planes are the natural appearance faces for 4H-SiC. It implies that each of these planes has a low source free energy and can be used as seed face. By comparing the crystals grown on three seed faces, it was found that the quality of crystals grown on the {0 1−1 4} facet is much better than those of the crystal grown on other facets.

The above experiments confirmed that using non-*c*-face seed for SiC crystal growth is an effective method to eliminate micropipes in case of the existence of micropipes in seed. At present, micropipe-free wafers are commercially available from most suppliers.

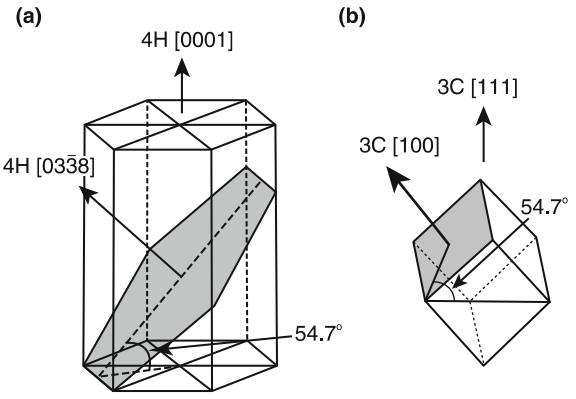

Fig. 2.20 Schematic illustration of unit cell: (**a**) 4H-SiC and (**b**) 3C-SiC

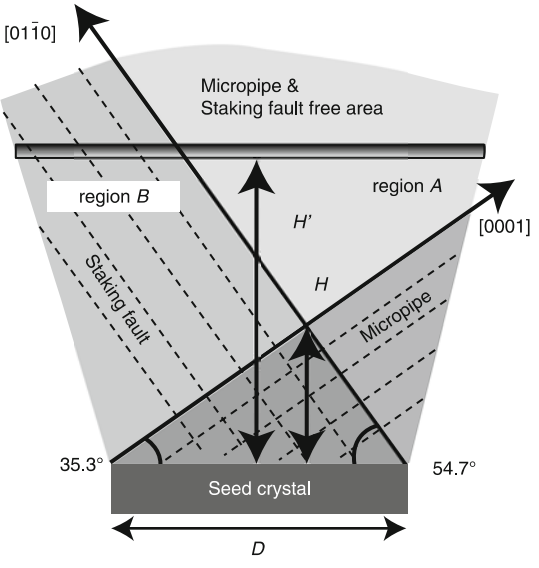

Fig. 2.21 Defect propagation on the 4H-SiC {0 3−3 8} seed

2.4.2 *Foreign Polytypes*

There are more than 200 polytypes for SiC materials. These polytypes have different characteristics. Because of nearly same stacking fault energy, several different polytypes such as 4H, 6H, and 15R are easily formed simultaneously in a crystal during crystal growth. Figure 2.23 shows a scanning image of a SiC wafer. In this image, we can see that 6H (green), 4H (yellow), and 15R (light yellow) coexist in a wafer. The mixing of the polytypes destabilizes growth and deteriorates the characteristic of SiC as an electronic material. Therefore, it is important to avoid the formation of foreign polytypes and keep the host polytype stability.

In the experiment, it was found that growth parameters such as the growth temperature, pressure in chamber, supersaturation, vapor-phase stoichiometry, impu-

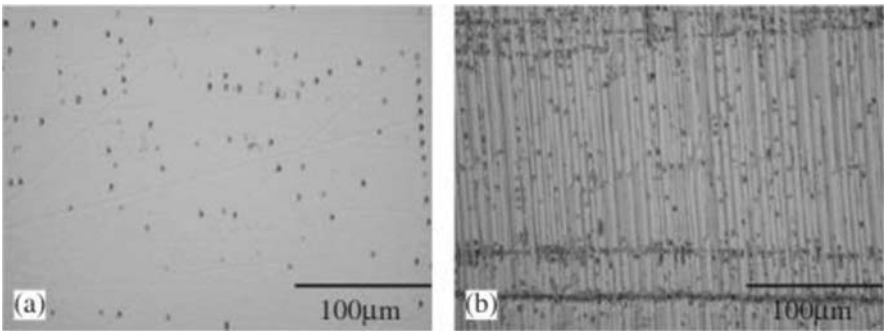

Fig. 2.22 Surface morphology of the 4H-SiC {0 3−3 8} wafer after molten KOH etching: (**a**) the micropipe and stacking fault-free area (region A) and (**b**) the micropipe-free area with stacking fault (region B)

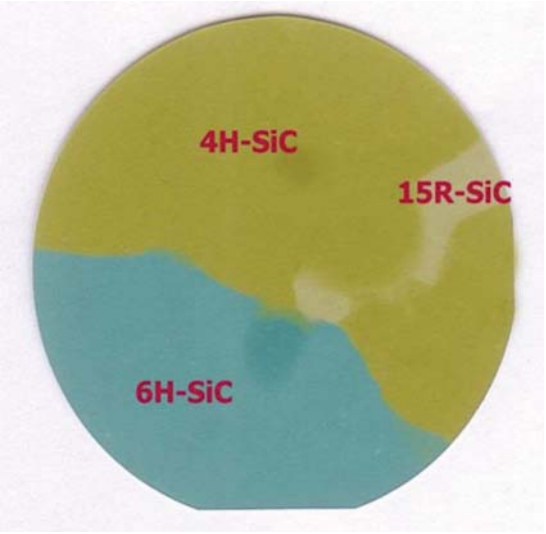

Fig. 2.23 Scanning image of a 4 in. SiC wafer in which 4H, 6H, and 15R polytypes coexist (Provided by Dr. Yang X L at Shandong University)

rities, and polarity of seed surface play important roles to influence the polytype stability. Therefore, the control of polytype is a complicated issue.

Knippenberg [30] reported empirical observation of the relative amount of individual polytype in SiC crystal growth as shown in Fig. 2.24. From this figure, we can see that the 3C is a metastable polytype, and 2H exists only at a low-temperature range. Above 2000 °C, 4H, 6H, and 15R are observed and sublimation growth can be performed. For SiC wafers to be used for electronic devices, 4H is the desired polytype. However, 4H is observed in a narrow temperature window and relative small amount. Thus, 4H-SiC crystal growth is more difficult than 6H.

Based on the classical thermodynamical analysis and crystal growth theory, Shiramomo et al. [31, 32] calculated the free energy of forming a critical nucleus in case of 2D nucleation as shown in Fig. 2.25. It can be expressed as follows:

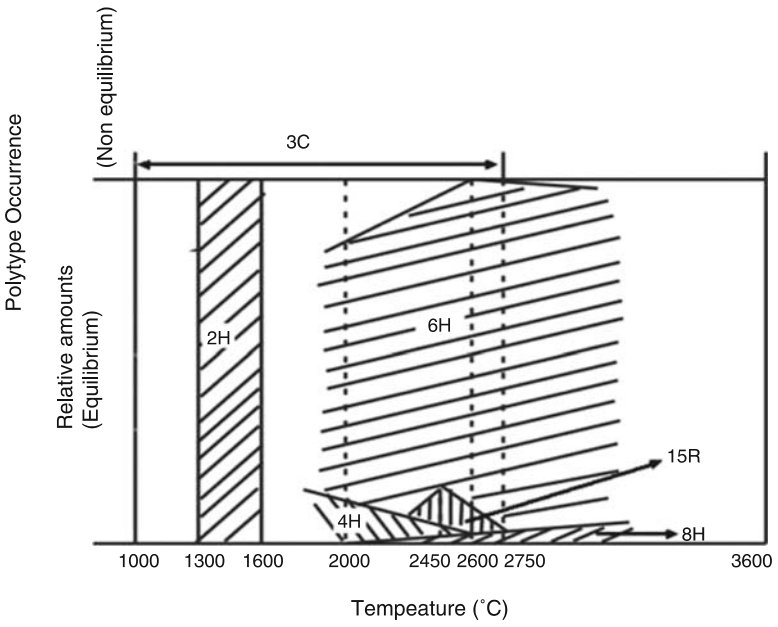

Fig. 2.24 Empirical observation of polytype occurrence in SiC crystal growth

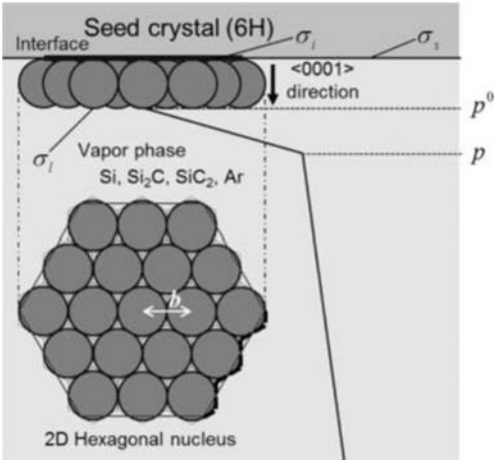

Fig. 2.25 Model of 2D nucleation theory for SiC crystal growth

$$\Delta G_2^* = \frac{b^4 \sigma_l^2}{\Delta\mu - \left(\frac{\sqrt{3}}{2}\right) b^2 \left(\sigma_l + \sigma_i - \sigma_S\right)} \tag{2.4}$$

where b is the first neighbor distance corresponding to the in-plane lattice constant. σ_s, σ_i, and σ_l are the surface energies of the substrate surface, the

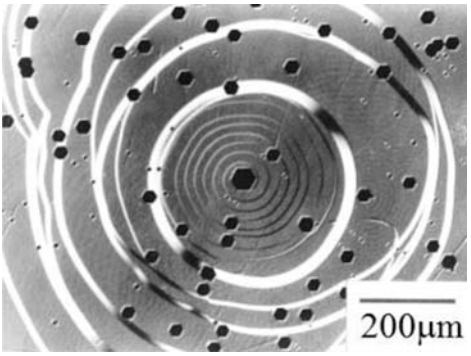

Fig. 2.26 Optical microscopic image of the growing surface of 6H-SiC after the chemical etching

layer/substrate interface, and the layer surface, respectively, as shown in Fig. 2.25. $\Delta\mu$ is the bulk chemical potential change associated with the molecular change from the vapor state to the condensed state.

To clarify which kind of polytype will be favored in the nucleation processes, the nucleation energies of 4H and 6H-SiC as a function of temperature and pressure which are the most easily generated polytypes in the sublimation method are calculated and compared. The calculation results indicated that when *c*-face was used as seed face, 4H-SiC 2D nuclei formation free energy is lower than that of 6H-SiC. This implies that the formation of 4H-SiC is more stable than that of 6H-SiC at nucleation stage in case of *c*-face seed. Additionally, the difference of nucleation energy between 4H-SiC and 6H-SiC decreased as the growth temperature increased and pressure decreased corresponding to increase of supersaturation of carbon species. This means that there is a large probability of the formation of a mixture of 4H and 6H polytypes in case of higher supersaturation, i.e., higher temperature of a seed and lower pressure in the growth chamber. In contrast, 6H-SiC is the most stable polytype for the growth on Si-face seed.

From the kinetic viewpoint, polytype replication through spiral growth around threading screw dislocations plays a critical role for the polytype stability. Figure 2.26 shows the typical surface morphology of a 6H-SiC crystal taken by optical microscope [33]. From this image, we can see that the outcrop of a threading screw dislocation on the surface provides an infinite step source. The spiral step will be kept through the whole growth procedure as long as the growth condition is stably maintained. At the step edges, the stacking information is provided, which ensures the replication of the polytype in the growth procedure.

2.4.3 Dislocations

SiC single crystal ingots and substrates contain a variety of dislocations. The Burgers vector, the extended direction, and the typical density are listed in Table 2.2.

Table 2.2 Main dislocation categories in SiC single crystals

Dislocation	Burgers vector	Extended direction	Typical density (cm^2)
Threading screw dislocation (TSD)	<0 0 0 1>	<0 0 0 1>	10^2–10^4
Threading edge dislocation (TED)	<1 1 −2 0>/3	<0 0 0 1>	10^2–10^4
Basal plane dislocation (BPD)	<1 1 −2 0>/3	In {0 0 0 1} plane	10^2–10^4

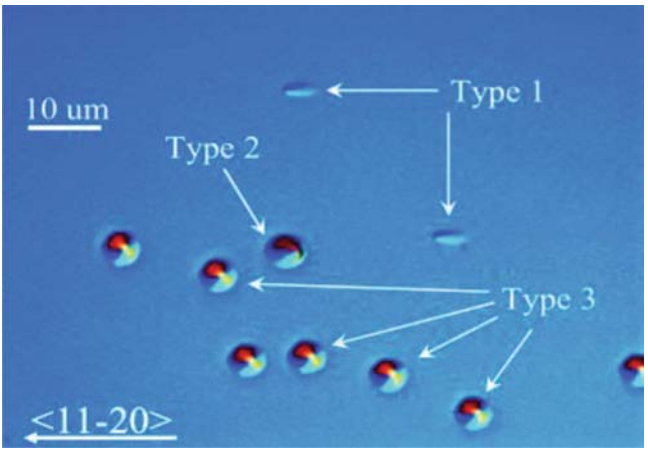

Fig. 2.27 The morphology of pits on SiC surface after oxidation

Figure 2.27 shows the typical surface morphology of SiC crystal after oxidation [34]. The oxidation pits are formed by oxidizing defects. Due to anisotropy of SiC structure, the oxidation rates of SiC are (0 0 0−1) > (1 1−2 0) > (0 0 0 1). Therefore, the oxidation pits were formed by the difference of the oxidation rate. In this figure, three kinds of pits were observed. Type 1, type 2, and type 3 correspond to basal plane dislocation, screw dislocation, and threading edge dislocation. The etch pits formed by molten KOH etching for SiC crystals have similar shapes.

As the device contains TSD, highly localized current may concentrate in the dislocation neighbor resulting in micro-plasmas. As a consequence, TSD causes the reduction of charge carrier lifetime [35]. BPDs are one of the troublesome defects in SiC materials. Stacking faults originating from the BPDs cause the increase of V_F under constant current for bipolar SiC devices, the increase of reverse-biased leakage, and the decrease of forward-biased current for unipolar SiC devices [36]. Diodes with higher TEDs densities have higher leakage current and slightly lower breakdown voltage compared to those without dislocations [37]. Among the three kinds of dislocations, the influence of TED on the performance of SiC device is relatively weak.

Since TED and BPD have the same Burgers vector, they can convert each other. To decrease the effect of dislocation on device performance, the conversions from BPD to TED are often controlled in CVD epitaxial growth by optimizing the growth parameters.

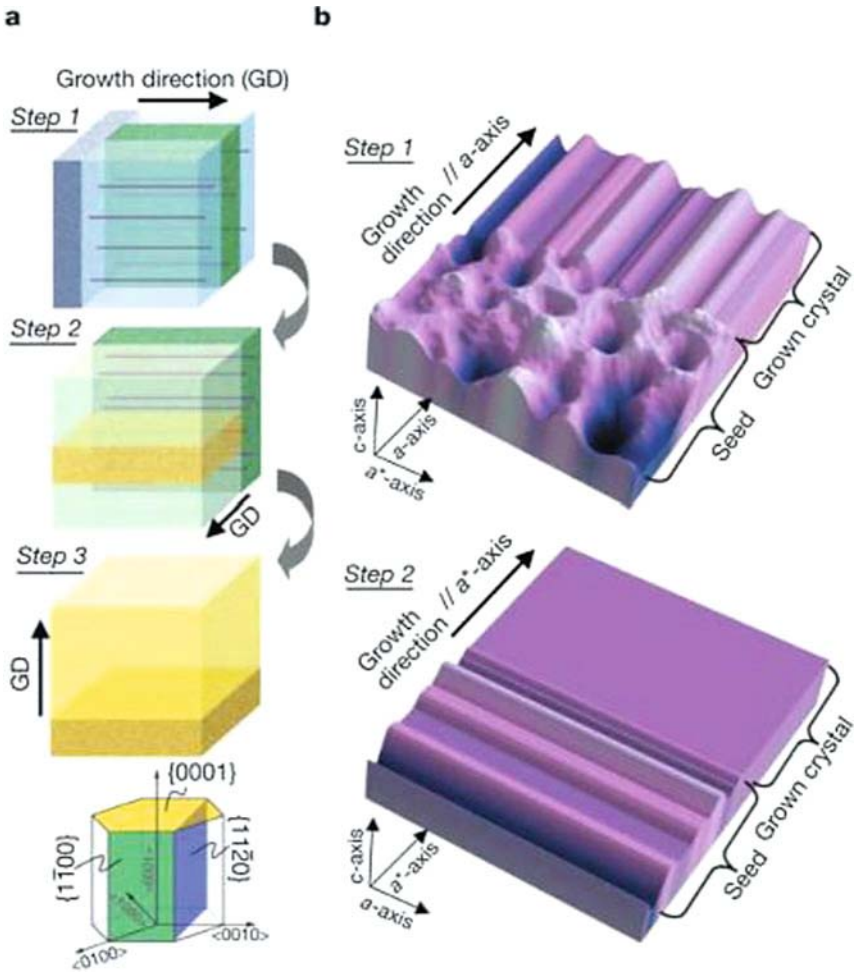

Fig. 2.28 Schematic diagram of the "repeated *a*-face" growth process. The growth sequences are as follows. Step 1: the first *a*-face growth. Step 2: the second *a*-face growth perpendicular to the first *a*-face (the seed was sliced from the first *a*-face growth crystal). Step 3: *c*-face growth with offset angle of several degrees (the seed was sliced from the second *a*-face growth crystal). (**a**) The first and second *a*-faces are {1 1−2 0} and {1−1 0 0}, respectively. (**b**) Top side view, showing {0 0 0 1} lattice plane irregularities of seed and grown crystal in steps 1 and 2. The a*-axis is perpendicular to both the *a*-axis and the *c*-axis

For conventional semiconductor materials such as Si and GaAs, dislocation-free crystals are generally grown from molten sources by means of the "necking" process. But "necking" process is not suitable for SiC crystals grown by PVT because rapid increase of crystal diameter is impossible. To reduce the dislocation density in SiC crystal, "repeated *a*-face" method was proposed by Nakamura et al. for the ultrahigh-quality SiC single crystal growth [38]. Figure 2.28 shows the "repeated *a*-face" growth process.

The process to eliminate dislocations is described as follows. Step 1: *a*-face ({1 1−2 0} or {1−1 0 0}) growth along the *a*-axis (<1 1 −2 0> or <1 −1 0 0>) direction, using a seed sliced from a *c*-face growth ingot. Step *N* (*N* = 2, 3, 4, ...): *a*-face ({1 −1 0 0} or {1 1 −2 0}) growth along the *a*-axis (<1 −1 0 0> or <1 1 −2 0>) direction, using a seed sliced from the *a*-face growth ingot of the previous step (step *N* − 1)—the seed surface orientation is perpendicular to both the previous step's growth and <0 0 0 1> directions. Step *N* + 1: *c*-face growth, using a seed sliced from the *a*-face growth ingot of the previous step (step N)—the seed surface is {0001} face, with several degrees off-axis toward the perpendicular to both the previous step's growth and <0 0 0 1> directions.

The principle for the reduction of the dislocation density is described as follows. In step 1, an *a*-face seed with a high density of dislocations, which are inherited from the crude *c*-axis SiC crystal, was used. In step 2, most of the dislocations are not exposed to the surface of the second seed, because they exit perpendicular to the first *a*-face growth direction, i.e., parallel to the second seed surface. In other words, the second *a*-face growth crystal inherits fewer dislocations.

It was found that the dislocation density could be reduced by increasing the repeating N counts. Etching experiment indicated that averaged etch pit density (EPD) in 4H-SiC decreased exponentially with increase in the repeat count of *a*-face growth. The average EPD and micropipe densities of a 20 mm diameter substrate, taken from the crystal grown on RAF seed with *a*-face growth performed three times, were 75 cm^{-2} and 0 cm^{-2}, respectively. The EPD value is lower by three orders of magnitude than that of conventional-grade SiC substrates.

Finally, the stacking fault was eliminated by the last step *c*-face growth because the stacking faults and partial dislocations are inherited only perpendicular to the *c*-axis. X-ray topographic observation shows that the stacking faults and partial dislocations are eliminated perfectly by the *c*-face growth since the stacking faults and partials lie on the {0 0 0 1} plane.

Figure 2.29 shows the quality assessment for the repeated *a*-face growth crystal by synchrotron topography. From Fig. 2.29a, we can see that crystal quality of the RAF substrate is very homogeneous, and there are very few macroscopic defects and dislocation. The long-range lattice warp is very small with the curvature radius of the lattice of about 800 m. In contrast, the conventional-grade substrate has many macroscopic defects and dislocation networks as shown in Fig. 2.29b.

Therefore, RAF is an effective method to eliminate dislocations and other defects in SiC single crystals.

2.5 Control of Electrical Characters of SiC Crystals Grown by Sublimation Growth

For the fabrication of vertical devices, low-resistivity wafers are needed to minimize the series resistance, while high-resistivity wafers are desired for the fabrication of lateral high-frequency devices, to reduce the parasitic impedance. In SiC

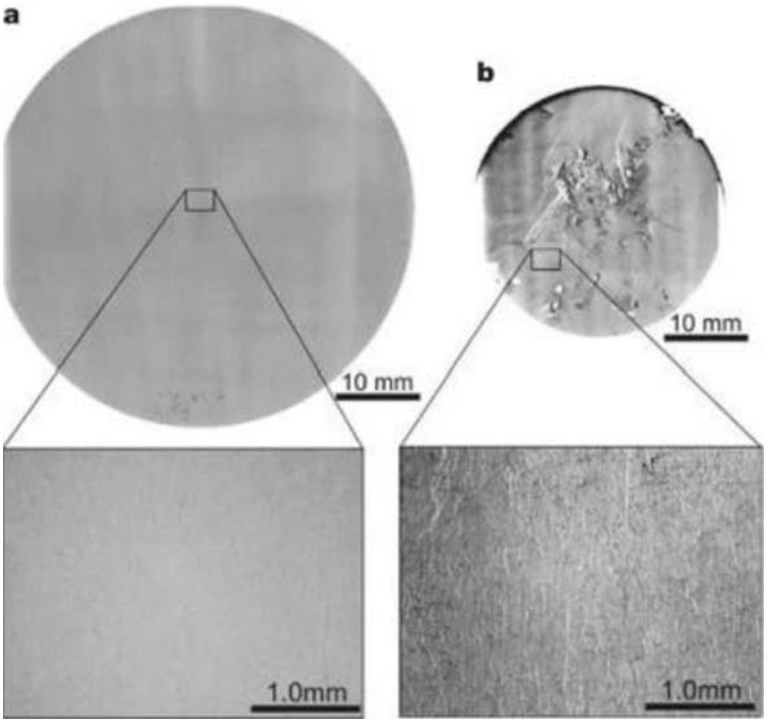

Fig. 2.29 Synchrotron monochromatic beam X-ray topographs. 4H-SiC (0001) 8° off-axis substrate, 2.0 in. in diameter, manufactured by the RAF process (**a**) and a 1.2 in. diameter specimen manufactured by the conventional process (only *c*-face growth (**b**). Averaged EPD and micropipe densities of the RAF growth crystal were about 250 cm^{-2} and 0 cm^{-2}, respectively, and those of crystal grown by the conventional method were about 3×10^4 cm^{-2} and 30 cm^{-2}, respectively. Magnified images are shown below. Dislocation networks are shown in the magnified image of (**b**)

single crystal, N and Al are generally the dopants for n-type and p-type boules, respectively. Semi-insulating characters of SiC crystals were realized by introducing deep levels compensating all shallow donors or acceptors.

2.5.1 n-Type Doping

In the procedure of SiC sublimation growth, nitrogen doping is generally conducted by introducing nitrogen gas into the growth chamber. In this case, carrier gases include Ar and N_2 with a suitable proportion. The nitrogen concentration in grown SiC crystal is approximately proportional to the square root of the nitrogen partial pressure during crystal growth and independent of growth rate. This implies that nitrogen incorporation is determined by the equilibrium between nitrogen in the gas phase and nitrogen adsorbed on the growing surface [39].

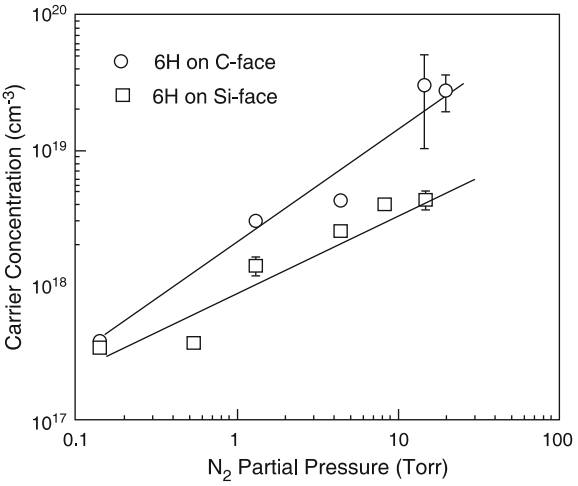

Fig. 2.30 N_2 partial pressure dependence of the carrier concentration in 6H-SiC grown on the (0 0 0 1) Si and the (0 0 0−1) *c*-faces

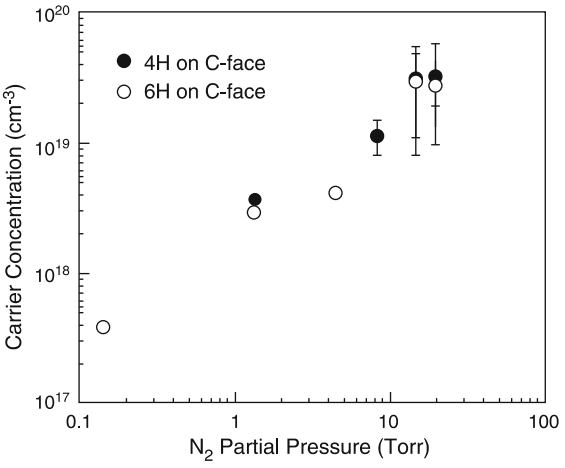

Fig. 2.31 N_2 partial pressure dependence of the carrier concentration in 4H and 6H-SiC grown on the *c*-face

Figure 2.30 shows the N_2 partial pressure dependence of the carrier concentration in 6H-SiC crystals grown on the (0 0 0−1) C and the (0 0 0 1) Si-faces [40]. The carrier concentration increased as the nitrogen partial pressure increased for both crystals. The crystals grown on the *c*-face always had higher carrier concentrations than those grown on the Si-face, and the difference became larger at higher carrier concentrations. The carrier concentration difference originated mainly from the large compensation of the impurity acceptor atoms in the low carrier concentration regime.

Figure 2.31 shows the N_2 partial pressure dependence of the carrier concentration in both 4H and 6H-SiC crystals grown on the *c*-face. Both crystals exhibited the similar concentration variation trend although 6H-SiC has larger nitrogen donor ionization.

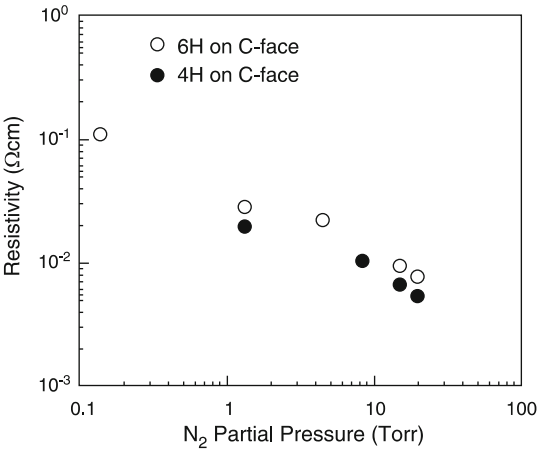

Fig. 2.32 N_2 partial pressure dependence of the resistivities of 4H and 6H-SiC crystals grown on the *c*-face

Figure 2.32 shows the resistivities of the 6H and 4H-SiC crystals as a function of the nitrogen partial pressure. The 4H-SiC crystal always exhibited lower resistivities at the same carrier concentration because of its higher electron mobility. At a nitrogen partial pressure of 20 Torr corresponding to the nitrogen concentration of 10^{20} cm^{-3}, bulk resistivities 7.6×10^{-3} Ω cm for 6H-SiC and 5.3×10^{-3} Ω cm for 4H-SiC were obtained. However, the resistivities of n-type 4H-SiC for the electronic devices were in the range of 0.01–0.03 Ω cm. Therefore, the electron mobility is rather low for 4H-SiC in the above experiment. In n-type SiC wafers, there are several kinds of deep levels or electron traps at a relatively high concentration of 10^{14}–10^{15} [41, 42].

It has been found that stacking faults were formed in highly nitrogen-doped 4H-SiC subjected to an oxidized or annealed in Ar at high temperature [43, 44]. When the nitrogen concentration exceeded 1×10^{9} cm^{-3}, the SF occurrence became distinct. Therefore, in order to decrease the resistivity of SiC, it is necessary to grow lightly nitrogen-doped 4H-SiC crystal and decrease the deep level impurity concentrations to very low level.

Recently, Kato et al. have grown low-resistivity n-type 4H-SiC crystals by sublimation using Al-N co-doping technique [45]. Figure 2.33 shows the schematic illustration of the Al-N co-doping 4H-SiC crystal growth. The furnace has two RF coils for heating SiC and Al source, respectively. N and Al doping levels were controlled in the range of 5×10^{18} cm^{-3} to 1×10^{20} cm^{-3} during growth.

It was found that the stacking faults (SFs) were suppressed in the n-type 4H-SiC grown by the co-doping technique. Figure 2.34 shows the etching morphologies of longitudinal cut SiC crystals after molten KOH etching treatment. In Fig. 2.34a, the etched surface shows morphology with line-shaped etch pits caused by a lot of SFs generated due to the high *N* doping of 3×10^{19} cm^{-3}. In contrast, the high N-Al co-doped crystal does not show any sign of SF generation in spite of the high *N* concentration of 8.8×10^{19} cm^{-3} as shown in Fig. 2.34b. Furthermore, the co-

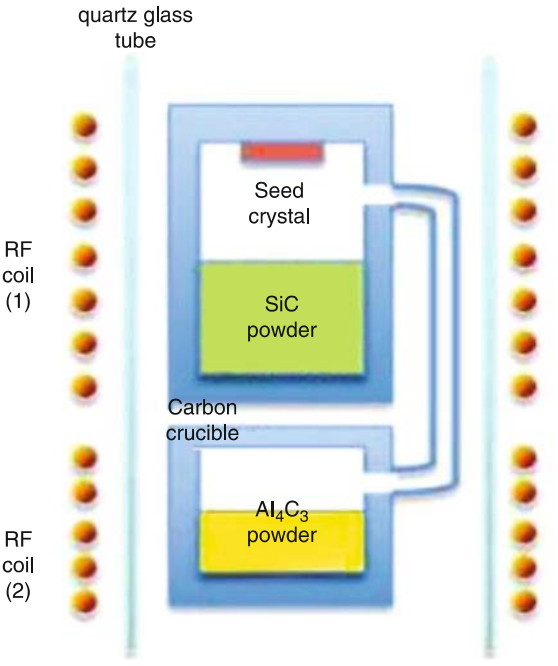

Fig. 2.33 Schematic illustration of Al-N co-doping 4H-SiC crystal growth

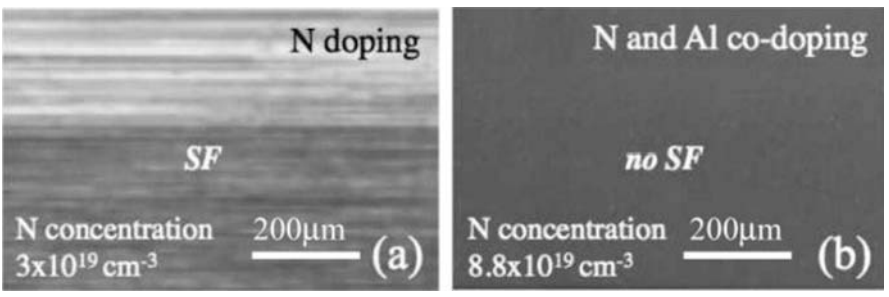

Fig. 2.34 The etching morphologies of longitudinal cut SiC crystals after molten KOH etching treatment. (**a**) Conventional sublimation-grown SiC with *N* concentration of 3×10^{19} cm^{-3}. (**b**) Co-doping-grown SiC with *N* concentration of 8.8×10^{19} cm^{-3} and Al concentration of 4.2×10^{19} cm^{-3}, respectively

doped 4H-SiC crystals show higher activation ratio of donor compared with the conventional nitrogen-doped crystals. When N and Al concentrations for co-doped 4H-SiC are 8.8×10^{19} cm^{-3} and 4.2×10^{19} cm^{-3}, respectively, the resistivity reaches 8.5 mΩ cm.

Therefore, low resistivity for n-type 4H-SiC could be achieved by N-Al co-doping technique. The SFs were suppressed until higher N concentration of 8.8×10^{19} cm^{-3} in the co-doped crystal. At the same time, the co-doped crystals showed higher activation ratio of donor compared with the conventional n-type 4H-SiC crystals.

2.5.2 *p-Type Doping*

For high-power SiC device application, substrates with low resistivity are required to reduce the unnecessary resistance of the devices. Especially for the fabrication of n-channel IGBTs, showing high performance compared to p-channel IGTs, p-type 4H-SiC substrates with low resistivity are required. Aluminum is often used as p-type dopant in SiC crystal. In general, aluminum doping is realized by adding aluminum or aluminum-containing compound into the SiC source. Aluminum doping is much more difficult than nitrogen doping during SiC crystal growth because severe depletion of the aluminum source occurs in the procedure of crystal growth at high temperature [46]. The Al concentration in crystal is almost proportional to aluminum vapor pressure in the growth chamber.

To realize the effective aluminum doping in 4H-SiC single crystals, Hens et al. have grown p-type SiC by using modified physical vapor transport (M-PVT) technique [47]. Figure 2.35 shows the schematic illustration of M-PVT SiC crystal growth method. In the left configuration of this figure, the Al source is located in the reservoir beneath crucible bottom, and the gas was flowed through the additional pipe only in small amount. If the additional flux is ten times larger than the conventional PVT, crystal growth will be disturbed in the center zone of the seed

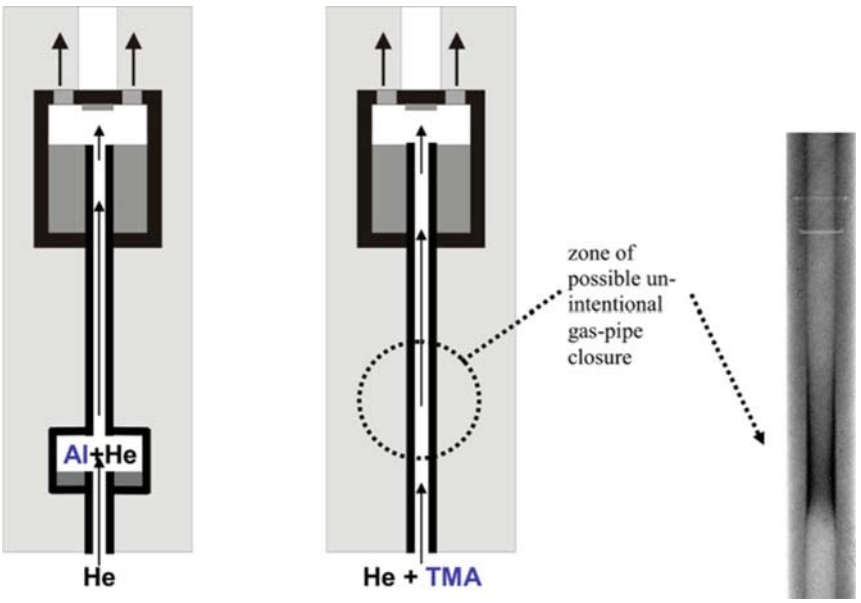

Fig. 2.35 Aluminum p-type doping SiC crystal growth by M-PVT technique. (Left) Regular setup with heated aluminum-containing reservoir. (Center) New setup with TMA source. (Right) X-ray image of gas pipe visible zone of unintentional deposition of carbon/graphite and related aluminum compounds due to decomposition of TMA

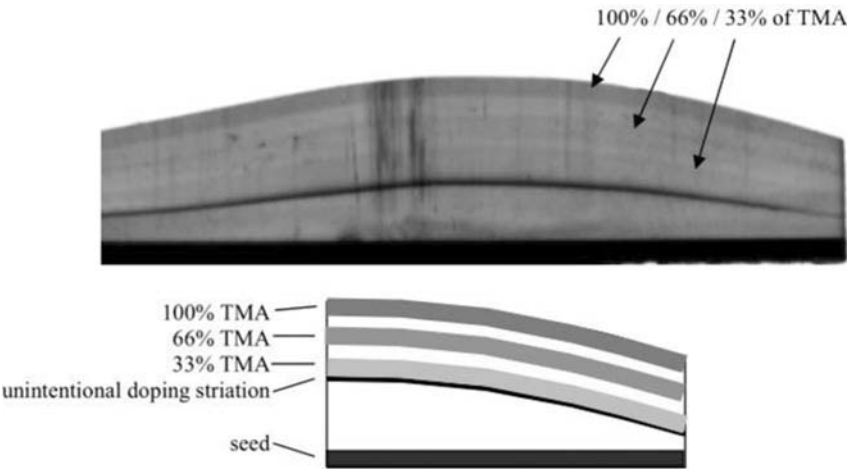

Fig. 2.36 Top: scanning image of longitudinal cut 6H-SiC crystal by M-PVT using TMA as Al source. Al doping concentration is indicated by the gray-level contrast. Bottom: schematic illustration of longitudinal cut of the highlighted doping stripes

crystal. If the additional flux is ten times smaller than the conventional PVT, the pipe will be closed by SiC deposition in the upper pipe zone at the entrance to the growth cell. Therefore, the use of solid Al source has the following disadvantages: (1) the additional pipe is easily blocked by the reverse transport of the SiC vapor species from the hot powder to the colder reservoir. (2) When the additional gas was flowed into the growth cell, it caused the temperature elevating of the central part of the gas room. It further possibly leads to the seed sublimation since the additional gas prevents the Si and C species from depositing on the seed. (3) The Al doping concentration is not easily controlled.

To improve the Al doping homogeneity, M-PVT p-type SiC crystal growth using tri-methyl-aluminum (TMA) as Al source is proposed as shown in the central configuration of Fig. 2.35. In this configuration, the feeding of TMA allows a more precise control of the Al flux into the growth cell. In addition, the use of high purity TMA can reduce the unintentional doping concentration. A major challenge during feeding of TMA into the hot growth cell is the pipe aperture narrowing or even blockade by graphite and related aluminum compound deposition on the walls after long run as shown in the right of Fig. 2.35.

Figure 2.36 showsan optical transmission image of a longitudinal cut of a 6H-SiC crystal grown on *c*-face 6H-SiC seed by M-PVT using TMA as Al source. The total gas flux was kept constant, and the relative values of TMA were varied in the following sequence: 0%, 33%, 0%, 66%, 0%, and 100%. The dark stripes correspond to 100%, 66%, and 33% of TMA, respectively. The black stripe is related to an unintentional high TMA flux when turning on the dopant supply for the first time. It was found that different Al incorporation levels from the low to

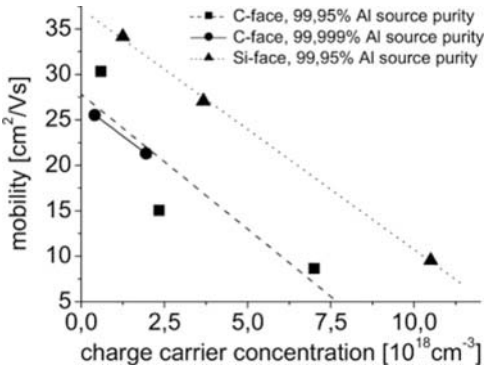

Fig. 2.37 Charge carrier mobility versus charge carrier concentration for a number of 6H-SiC crystals grown on *c*-face and Si-face SiC seeds

Table 2.3 Result of SIMS, Raman spectroscopy, and resistivity measurement of various crystals grown with Al-N co-doping

Growth no.	Al concentration (cm^{-3})	N concentration (cm^{-3})	Al/N	Dominant polytype	Carrier concentration	Resistivity (mΩ cm)
1	1.8×10^{-20}	1.5×10^{-20}	1.2	4H	3.0×10^{19}	86
2	3.1×10^{-20}	2.3×10^{-20}	1.3	4H	4.0×10^{19}	88
3	2.6×10^{-20}	1.8×10^{-20}	1.4	4H	4.0×10^{19}	97
4	1.5×10^{-20}	1.3×10^{-20}	1.5	6H	–	68

mid-10^{20} cm^{-3} could be achieved in SiC crystals by M-PVT using TMA as the Al source.

From a kinetic viewpoint, *c*-face is unfavorable for aluminum incorporation and favorable for nitrogen incorporation because the Al and N occupy the Si-lattice site and C-lattice site, respectively. The background N often causes the compensation of acceptors in p-type SiC. Even if the compensation is only in the range of 3–5%, it leads to a pronounced reduction of charge carrier mobility and conductivity. Figure 2.37 shows the influence of seed polarity on the compensation of acceptor. In case of Si-face seed, unintentional acceptor compensation of aluminum is much suppressed compared to the use of Si-face seed. From this figure, we can see clearly that the suppression of compensation causes the increase of the charge carrier mobility and further the conductivity increase by more than factor 2.

Recently, low-resistivity p-type 4H-SiC crystals were grown by sublimation using aluminum and nitrogen co-doping [48]. The crystal growth was performed by a two-zone heating furnace, which has two RF coils for heating high purity SiC source material and Al_4C_3. Table 2.3 shows representative results of SIMS, Raman spectroscopy, and resistivity measurement for the grown crystal. The lowest resistivities obtained for 4H and 6H-SiC were 86 mΩ cm and 68 mΩ cm, respectively.

The relation of Al and N concentrations of grown crystals is plotted in Fig. 2.38. It was found that Al/N = 1:1 line acted as a border of n-type and p-type. When the Al/N is larger than 1, the crystal exhibits the p-type electrical characteristics and vice versa.

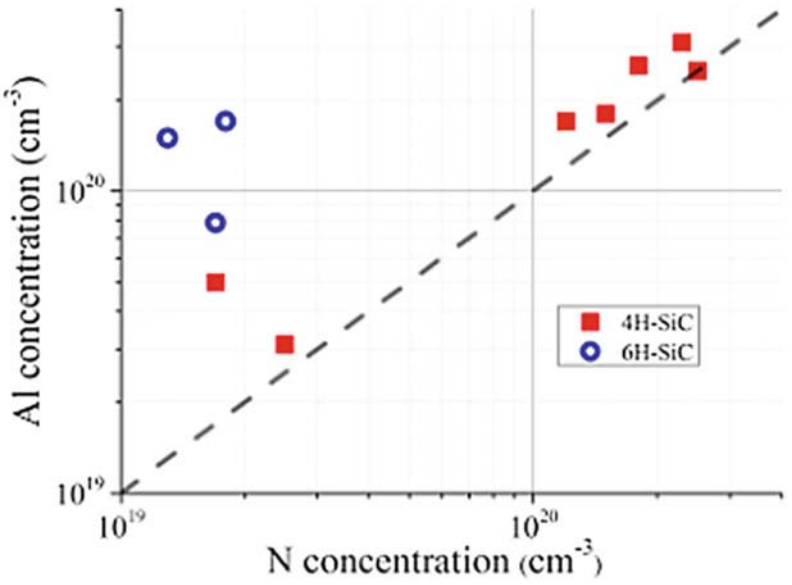

Fig. 2.38 Al and N concentrations measured by SIMS. The guide line show the Al/N = 1:1 line, as a border of n-type and p-type. Notation of 4H and 6H indicates the dominant polytypes of grown crystals

2.5.3 Semi-insulating

High-resistivity wafers are generally used fabrication of SiC- or GaN-based high-frequency devices to minimize the parasitic capacitances between the terminals, including the ground. Because it is very difficult to reduce the background dopant density below 10^{10} cm^{-3} by purification processes, compensation of dopants is often used to decrease the density of free carriers in the bands. In SiC, vanadium was the first element used as a compensation center to create semi-insulating wafers. Vanadium is an amphoteric impurity in SiC. It acts as an acceptor-like trap in n-type SiC and a donor-like trap in p-type SiC.

Vanadium deep levels in SiC have been identified by Schneider et al. [49]. Two deep levels are formed by vanadium in 6H-SiC: a V^{3+}/V^{4+} acceptor level about 0.8 eV below the conduction band and a V^{4+}/V^{5+} donor level approximately in the middle of the bandgap, i.e., about 1.5 eV.

Assuming that the donors (mainly nitrogen), acceptors (aluminum, boron, etc.), and vanadium are present simultaneously in the SiC crystals in electrically active concentrations N_D, N_A, and N_v, respectively, four compensation regimes can appear in 6H-SiC.

1. $N_V > N_D - N_A > 0$, vanadium compensates shallow donors which may be themselves partially compensated by acceptors.

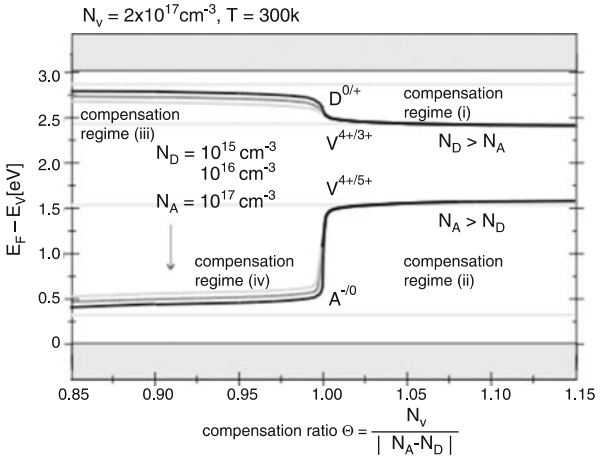

Fig. 2.39 Dependence of the Fermi level on the compensation ratio Θ for different shallow impurity concentrations N_A and N_D in vanadium-doped 6H-SiC

2. $N_V > N_A - N_D > 0$, vanadium compensates shallow acceptors which may be themselves partially compensated by donors.
3. $N_D > N_V + N_A$, domination of shallow donors lead to n-type conducting behavior, $\Theta < 1$.
4. $N_A > N_V + N_D$, domination of shallow acceptors leads to p-type conducting behavior, $\Theta < 1$.

Figure 2.39 shows the position of the Fermi level calculated from the charge carrier neutrality equation

$$n + N_A^- + N_{V(3+)} = p + N_D^+ N_{V(5+)} \tag{2.5}$$

as a function of $\Theta = N_V/|N_D - N_A|$ for different $N_D - N_A$ [50]. As long as vanadium compensates all other impurities as in regimes (1) and (2), semi-insulating SiC will be obtained. Another key condition for the preparation of semi-insulating SiC is that N_V cannot exceed the vanadium solubility limit.

V-doped semi-insulating 6H-SiC bulk single crystals have been grown by sublimation method from different research group. Bickermann et al. [50] found that if vanadium is added as a solid source to the SiC powder, it quickly exhausts during growth. Figure 2.40 is a scanning image of a longitudinal cut of a crystal grown with a vanadium content of 0.32 wt % in the source material. We can see that at the first stage, serious vanadium precipitation occurred. Following the crystal growth preceding, the vanadium concentration was gradually decreased, and the vanadium precipitation particles became smaller in size, but precipitation density does not change significantly. From GDMS measurements at the transition region

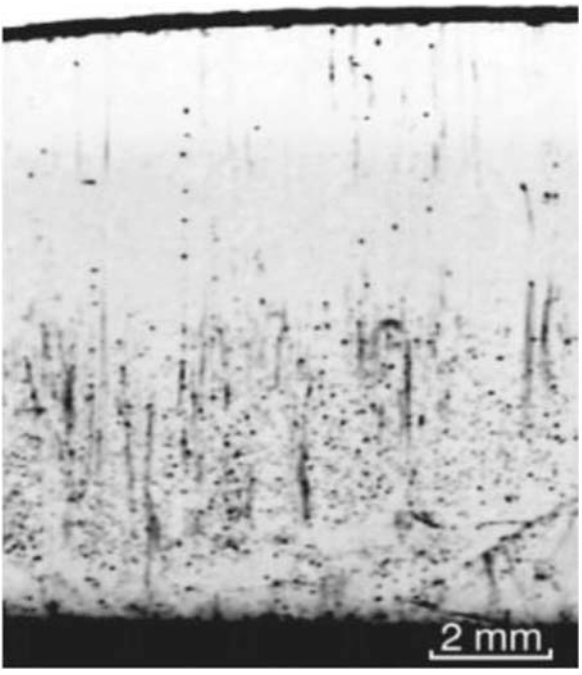

Fig. 2.40 The scanning image of a longitudinal cut 6H-SiC with vanadium doping. Semi-insulating 6H-SiC was grown by sublimation method using the solid vanadium source

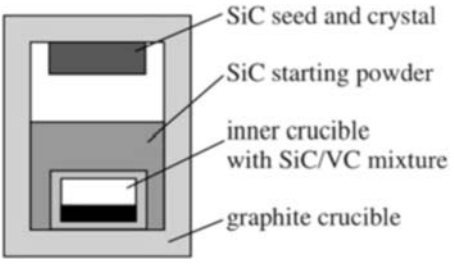

Fig. 2.41 Schematic illustration of the inner crucible located inside the growth container

from precipitated to non-precipitated areas, the vanadium solubility in SiC was confirmed to be about 4×10^{17} cm^{-3}.

In order to increase the semi-insulating yield of the grown crystals and avoid vanadium precipitation or depletion, vanadium concentrations in SiC crystals have to be lower than the solubility but higher than N_D in the whole crystal volume. To realize the vanadium uniform doping in SiC crystal, Bickermann et al. [50] used an inner crucible in which the SiC/VC mixture was filled as shown in Fig. 2.41. In this case, vanadium evaporation rate decreases as the container gets "sealed" in the early stages of growth due to SiC sublimation. A dense SiC/VC mixture sublimes at the top of the inner crucible and acts as an infinite vanadium source with nearly constant supply during SiC crystal growth. Therefore, semi-insulating, precipitate-free SiC crystals can be grown using the inner container doping method. Crystal volume yield is about 80%. The predominantly nitrogen-doped layer forming at the

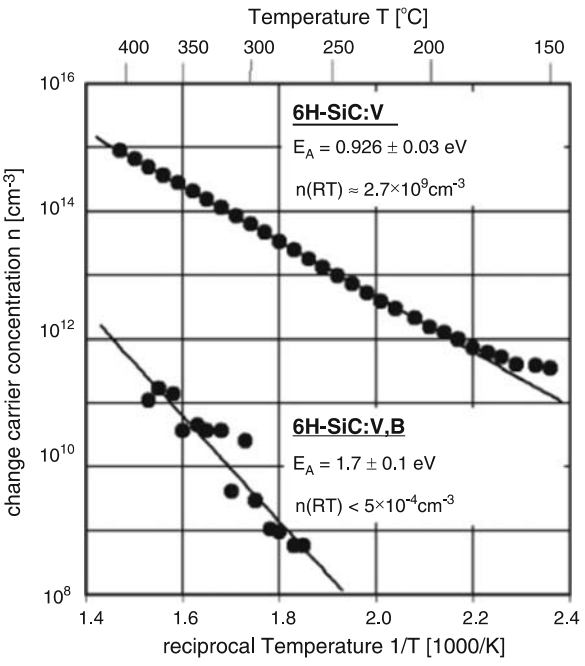

Fig. 2.42 Hall effect measurements of a V-doped and V-B co-doped 6H-SiC crystals

early stages of growth expanded to about 20% of the crystal volume. The vanadium concentration is about 5×10^{17} cm^{-3} near the seed and 2×10^{17} cm^{-3} at the end of growth, respectively. It implies that vanadium uniform doping has been realized. Similarly, V-B co-doping semi-insulating SiC crystals can be grown by using the inner container.

Figure 2.42 shows the Hall effect measurements of a V-doped and a V-B co-doped 6H-SiC crystals. For the V-doped crystal, the thermal activation energies are as high as 926 meV. It confirms that the vanadium compensates all shallow nitrogen donors. Extrapolation to room temperature gives the specific resistivities between 2×10^9 and 6×10^{10} Ω cm.

To overcome the difficulty in vanadium doping, semiconducting character could be also achieved by the use of intrinsic point defects. Therefore, high purity semi-insulating (HPSI) SiC was expected. The development of a semi-insulating SiC material requires two key components. First, a deep electronic level is necessary to trap either electrons or holes and to supply a large activation barrier to their subsequent release. Second, shallow levels are required to supply compensation to the deep electronic level so that the Fermi level can be pinned to the deep electronic level. In high purity SiC, the shallow electronic levels are mainly the boron and nitrogen. The deep electronic levels are vacancies.

The main difficulty for the growth of high purity SiC is the control of impurity incorporation in the crystal during growth. The metallic impurities can be easily eliminated by the high-temperature halogenation. But the nitrogen and boron are

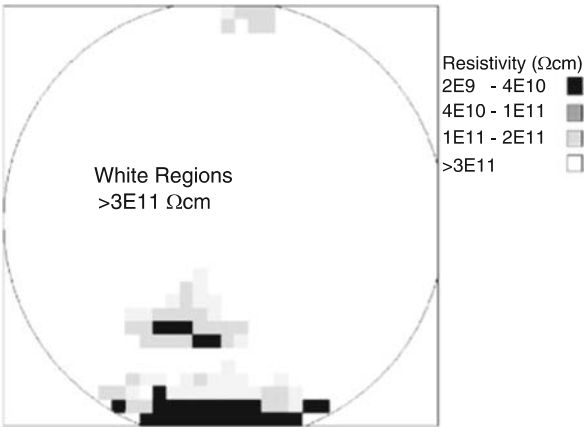

Fig. 2.43 High-resolution resistivity map of a 2″ diameter high purity semi-insulating 4H-SiC

difficult to reduce. Nitrogen comes from the absorbed air of the graphite parts and insulation. Boron is the accompanying product of the graphite. Therefore, the purification of graphite parts, insulation, and source is the critical technology for the growth of high purity SiC crystal. At early research work, Augustine et al. attempted to grow high purity SiC single crystals using sublimation method [51]. Unfortunately, the high purity SiC crystal did not exhibit semi-insulating electrical character due to the impurity contamination. Glow discharge mass spectroscopy (GDMS) measurements reveal that the metallic impurity concentrations are lower than the 1×10^{15} cm^{-3}, while the boron concentration is as high as 6.0×10^{16} cm^{-3}. Crystals exhibit resistivities in the 10^3 Ω cm range and are p-type due to residual high concentration of boron. It failed to obtain the high purity semi-insulating SiC crystals.

Jenny et al. [52, 53] reported the successful growth of high purity semiconducting 4H-SiC crystals by sublimation method. High-resolution resistivity map of a 2 in. diameter 4H-SiC was shown in Fig. 2.43. The entire wafer is semi-insulating with resistivity greater than 2×10^9 Ω cm. More than 80% of the wafer area has a resistivity $>3 \times 10^{11}$ Ω cm.

Secondary ion mass spectroscopy detection for the HPSI indicated that the only elements were nitrogen (2×10^{16} cm^{-3}) and boron (7×10^{15} cm^{-3}), and the concentrations of all other elements were below the SIMS detection limits or below the instrument background.

For examining electronic levels in semiconductors, Hall effect is an effect tool. Using the technique, we can determine several important electronic parameters, including the activation energy of the electronic level, the concentration of the principal defect, and the total net compensation. For the HPSI samples, the Hall effect is not suitable due to the extremely low mobility of the sample. Figure 2.44 shows the temperature-dependent resistivities of five HPSI samples. From the resistivity versus temperature, the obtained activation energies are 0.9, 1.1, 1.2,

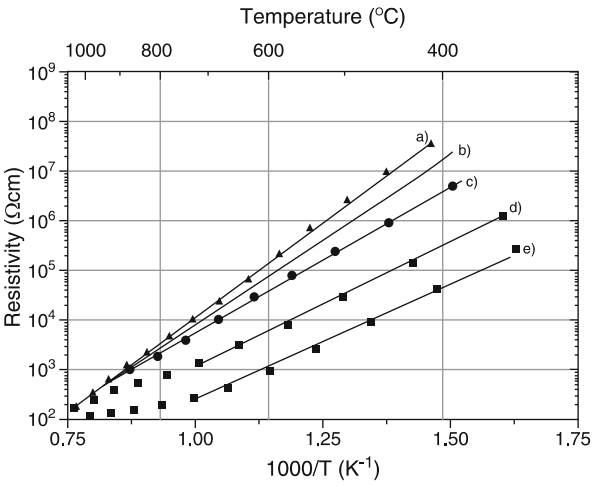

Fig. 2.44 Temperature-dependent resistivities for five HPSI samples whose activation energies are (**a**) 1.53 eV, (**b**) 1.33 eV, (**c**) 1.19 eV, (**d**) 1.06 eV, and (**e**) 0.90 eV

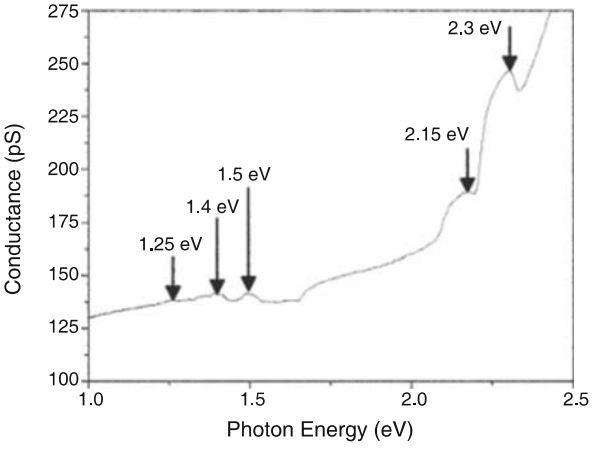

Fig. 2.45 Admittance versus photon energy plot that reveals the presence of five distinct energy levels

1.35, and 1.5 eV. Therefore, several defects are responsible for the semi-insulating character in the HPSI samples.

To further confirm the existence of multiple deep levels in HPSI, optical admittance spectroscopy (OAS) was used to measure the admittance of HPSI sample.

Figure 2.45 shows the OAS data of HPSI samples. It reveals that the activation energies for several deep levels are 1.25, 1.4, 1.5, 2.15, and 2.3 eV.

For activation energies greater than half of the bandgap, the bandgap energy (3.2 eV for 4H-SiC) has to be subtracted so that the data can be compared with the data obtained by other characterization techniques. Therefore, the actual activation

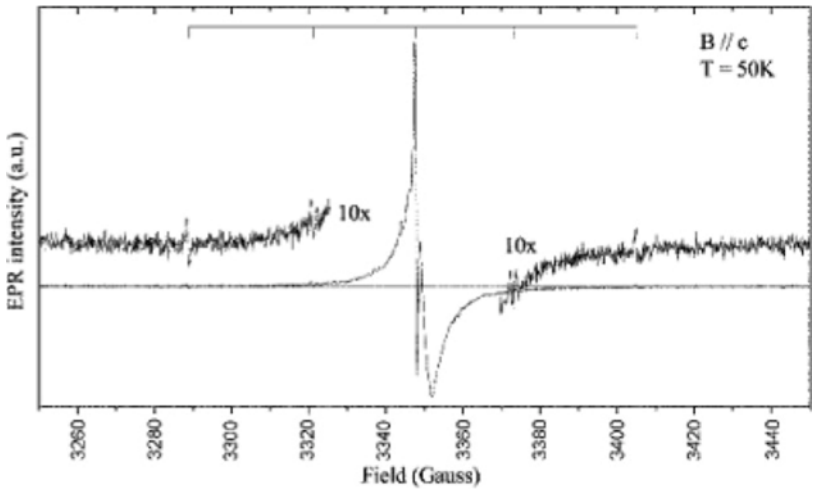

Fig. 2.46 The EPR spectrum of a 4H-SiC HPSI sample whose Fermi level was pinned to the 1.5 eV level and exhibits the carbon vacancy

energies are 0.9, 1.05, 1.25, 1.4, and 1.5 eV after the bandgap energy subtraction, which are very close to those obtained by temperature-dependent resistivity. The above two-group data proves that the source of the deep levels is probably to be intrinsic in nature.

Figure 2.46 is an electron paramagnetic resonance (EPR) spectrum of a sample exhibiting the activation energy of 1.5 eV. The large sharp peak with two hyperfine doublets is the main feature in the spectrum. It was identified as a carbon vacancy. The fact that defect is present in SI material suggests that it is electrically active and is responsible for at least one of the defects observed in the temperature-dependent resistivity measurements.

In addition, the SI material has a high thermal stability. After the HPSI wafers were subjected to 1650 °C annealing, for 90 min, no degradation in the SI character was observed in the annealed HPSI wafer. SI character preservation makes the HPSI wafers suitable for the application as ideal substrate for microwave devices.

2.6 Processing of Large-Diameter SiC Wafers

The processing from ingot to wafer for SiC is same as that for other semiconductors. SiC single crystal ingots are generally grown on {0 0 0 1} seed. The typical ingots are cylindrical in shape with a length of 20–30 mm. The crystallographic orientations of the ingots such as <0 0 0 1>, <1 1−2 0>, and <1 0−1 0> are determined by X-ray diffraction. Then the ingots are sliced into a number of wafers which were finally lapped, polished, and cleaned.

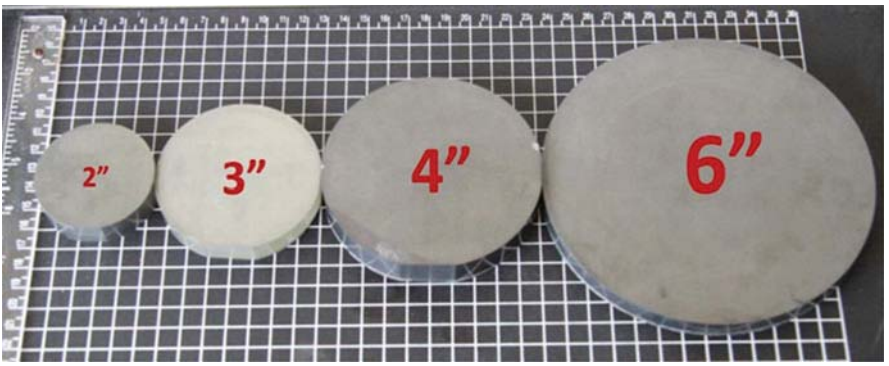

Fig. 2.47 As-grown SiC single crystal boules (Provided by Dr. Yan Peng at Shandong University)

SiC single crystal substrates are considered to be suitable for thin film growth of semiconductive GaN with wide energy bandgaps [54], because the lattice mismatch between SiC and GaN is quite small (3.5%) compared with sapphire substrates (16.1%) [55]. The quality of the deposition films is strongly dependent on the quality of substrates. Therefore, the processing of SiC wafers is extraordinarily important for film growth. However, the hardness of SiC is very closer to that of diamond, which makes it greatly difficult to process large-diameter SiC crystals. In addition, SiC substrate is very sensitive to surface defects resulting from lapping and polishing, which may propagate into an epitaxial layer and degrade device quality. Since MP achieves material removal through plastic deformation, scratches and subsurface damage layer containing dislocations are unavoidable [56]. Research on the epitaxial growth of 4H-SiC has shown that scratches are the primary contributors to polytype inclusions in the epilayers [57]. The polishing process of SiC substrates [51, 58–60] was investigated extensively. The removal mechanism of scratches in MP and physical and chemical process in CMP were analyzed. KOH etching and HRXRD were applied to evaluate the subsurface damage of SiC substrates. The effects of MP and CMP on the surface roughness were assessed. Three main procedures of SiC wafer processing were introduced. Variations of surface residual stresses during mechanical processing could be assessed by HRXRD.

SiC single crystals were grown by the sublimation method. Figure 2.47 is the image of as-grown SiC single crystals. The crystal boule was sliced into a number of wafers by diamond wires. Surface morphologies of polished wafers were observed by means of AFM and optical microscope. High-resolution X-ray diffractometer and KOH etching were used to assess the structural perfection of the wafer. Step profilometer and flatness measurement system were used to investigate the surface roughness and flatness. The SiC wafer processing includes the following steps.

2.6.1 Crystal Boule Slicing

It is very significant to slice high-quality SiC crystals into thin wafers with minimum warp, uniform thickness, and low kerf loss; otherwise it will bring great difficulty for succedent lapping and polishing. This has revitalized many interests in wire saw machining technology [58]. In general, diamond wire saw was used to slice SiC boule into wafers. The total thickness variation is less than 30 μm with warp about 20 μm for 2 in. wafers.

2.6.2 Lapping

Lapping is the second step for machining SiC in large-scale production. However, the lapping of silicon carbide is difficult because of its low fracture toughness, making it very sensitive to cracking [59]. Lapping process involves many parameters such as plate speed, pressure, grit size, abrasive density, etc. Thus, efficient lapping requires strict selection for operating parameters to maximize removal rate while controlling surface integrity.

Lapping plate is a cast-iron disk, its rotation speed is 40–70 rpm, and the applied pressure is 50–200 g/cm^2. The abrasive (B_4C) grain size is between 100 and 20 μm. The SiC material removal rate (MRR) is 5–20 μm/h owing to its high hardness and high wear resistance. MRR is increscent with the increasing of abrasive grit, density, plate speed, and pressure. However, a very high B_4C concentration is found to reduce the removal rate [60].

After lapping,the surface unflatness is 6 μm as shown in Fig. 2.48. Figure 2.49 shows the optical microscopic image of lapping surface. It can be seen that there exist lots of pits; the surface roughness R_a is about 100 nm after lapping. Due

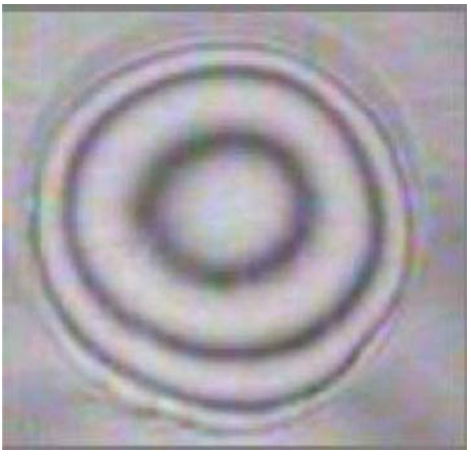

Fig. 2.48 Surface unflatness of SiC wafer after lapping (Provided by Dr. Yan Peng at Shandong University)

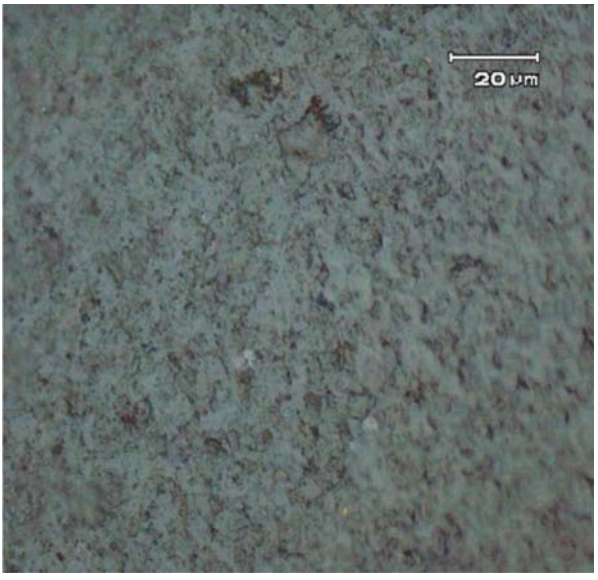

Fig. 2.49 Optical microscopic image of SiC wafer surface after lapping (Provided by Dr. Yan Peng at Shandong University)

to the great abrasive grit of lapping, it causes serious surface damage and large residual stresses. X-ray rocking curve measurement of (0 0 0 4) reflection for the wafer indicated that the full-width at the half-maximum (FWHM) is 122.4 arcs after lapping.

In the whole machining process, each step is very important for the successive processing. In order to reduce the total manufacturing time, it is preferable to obtain better ground surfaces, even if this takes longer lapping time [61].

2.6.3 Mechanical Polishing

MP is an important process aimed to remove the damaged layer caused by lapping to make a good surface and to amend the surface geometry exactly. The mechanism of SiC material removal by finer grit; harder abrasives, such as B_4C; and diamond in MP process actually includes the formation of mechanical microfractures and then the removal of these microfractures because of higher hardness of the abrasive and inherent hardness of the workmaterial [62].

The surface roughness after MP is $R_a = 3.1$ nm (measured by step profilometer). As shown in Fig. 2.50, the surface unflatness is 2 μm. Compared with surface quality after lapping, the surface unflatness decreased further after MP.

The polishing procedure was generally performed by diamond-based polishing slurries with decreasing grain size. A large number of scratches on the surface could be observed by AFM after MP. These scratches spread out in random directions with the depth in the range of 5–8 nm as shown in Fig. 2.51. This also indicates

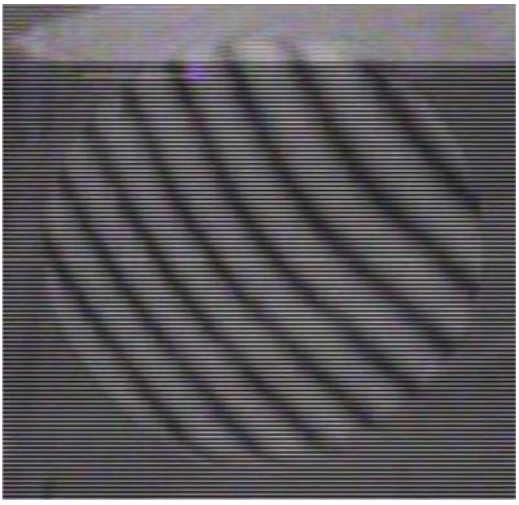

Fig. 2.50 Surface unflatness of SiC wafer after MP (Provided by Dr. Yan Peng at Shandong University)

that the material removal in MP procedure is dominant by the formation of brittle microfracture on a submicroscopic scale.

For both the mechanical lapping and polishing, subsurface damage was formed by harder abrasives. The subsurface damage has been found to extend in a depth range from one-half to one-seventy-fifth of the abrasive slurry particle size [63]. KOH etching was used to identify the subsurface damage as a part of the optimization of CMP process. Figure 2.52 displays the full-width at the half-maximum (FWHM) of (0004) reflection rocking curve of the SiC surface etched by KOH after MP with 2 μm diamond powder. It can be seen that when the etched depth reaches about 0.77 μm, the FWHM tends to keep constant. Thus, the damage depth of the surface can be considered to be about 0.77 μm.

2.6.4 Chemo-mechanical Polishing

CMP can be used to finish hard, brittle workmaterials with extremely smooth and damage-free surfaces. It depends on both chemical and mechanical effectiveness of the abrasive and the environment with respect to the workmaterial. In MP, diamond is harder than SiC; although the surface defects can be minimized by using very fine diamond particles, they cannot be completely eliminated [64]. Therefore, to produce extremely smooth and damage-free surface, further polishing process must be carried on. CMP was first demonstrated by Yasunaga et al. for polishing single crystal silicon using a soft abrasive ($BaCO_3$) [65]. Later on, this method was widely used to polish other crystal materials.

Theoretically any abrasive that can react with the workmaterial in a given environment and form a reaction product can be used for CMP [59]. For SiC CMP, the selected abrasive is SiO_2 which is much softer than SiC. The grit size of SiO_2 is 32 nm.

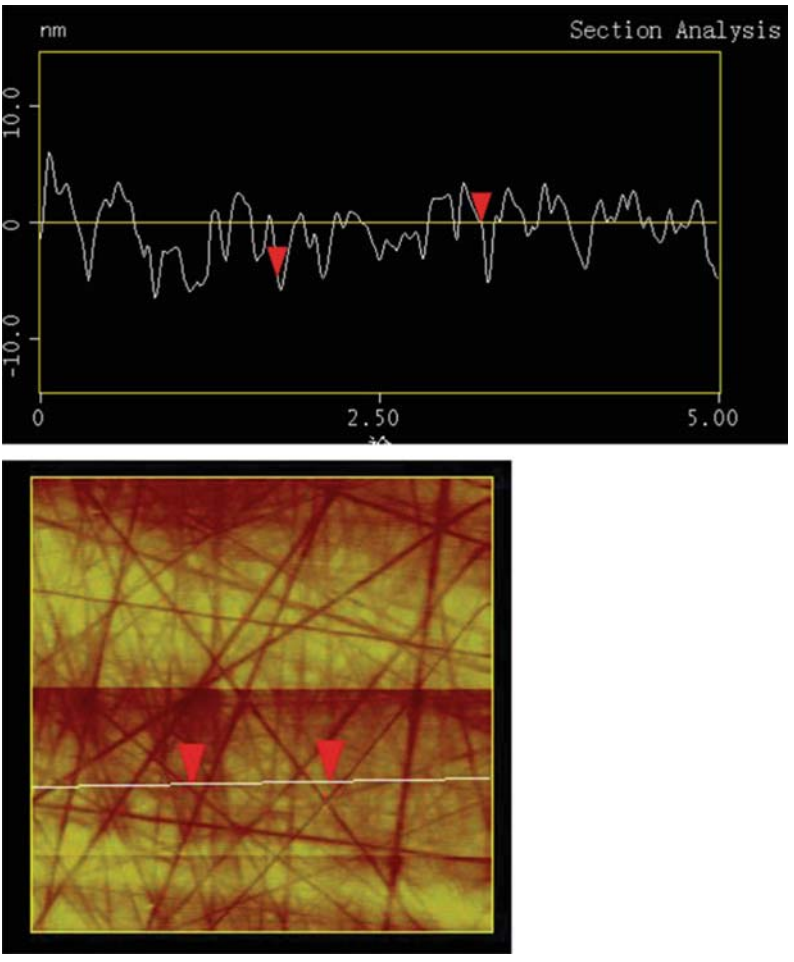

Fig. 2.51 AFM micrograph of the surface after MP ($5 \times 5\ \mu m^2$) (Provided by Dr. Yan Peng at Shandong University)

The wafer surface after CMP has a final surface roughness $R_a = 0.18$ nm (measured by AFM). Figure 2.53 is the AFM image of the surface finished by CMP, it reveals that the surface is extremely smooth, and there are no any scratches and other surface defects. Chemical reactions are performed between suspended silicon bonds in SiC and the alkaline (PH > 10) slurry of colloidal silica. The main chemical equation is as follows:

$$Si + 2\ NaOH + H_2O \rightarrow Na_2SiO_3 + 2\ H_2 \uparrow \tag{2.6}$$

The reaction product Na_2SiO_3 is soluble and can be removed easily from SiC surface by subsequent mechanical action by SiO_2. Chemical reaction will continue

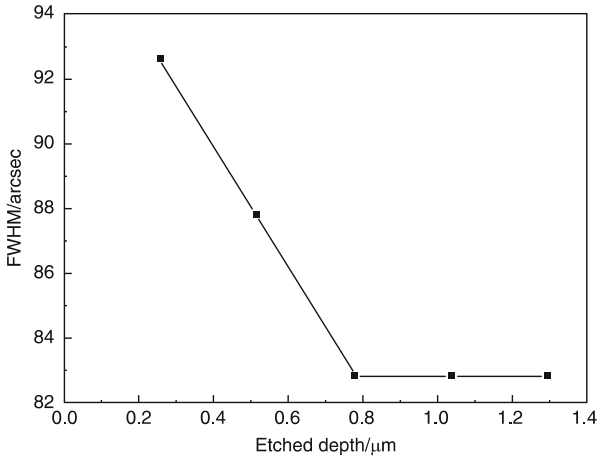

Fig. 2.52 The FWHM of (0004) reflection rocking curve of the surface etched by KOH after MP with 1 μm diamond powder (Provided by Dr. Yan Peng at Shandong University)

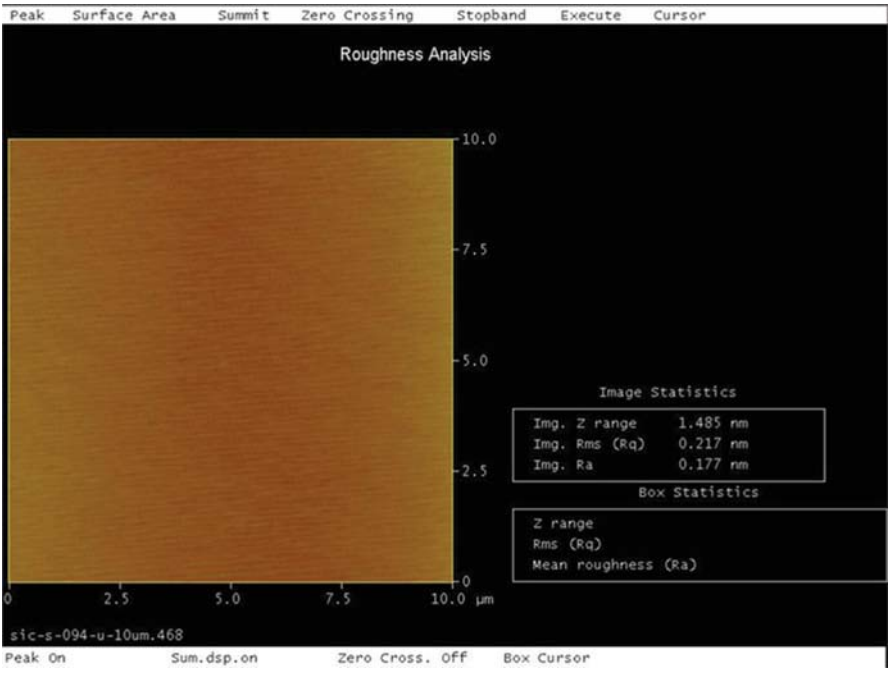

Fig. 2.53 AFM image of the SiC wafer surface finished by CMP (10 × 10 μm) (Provided by Dr. Yan Peng at Shandong University)

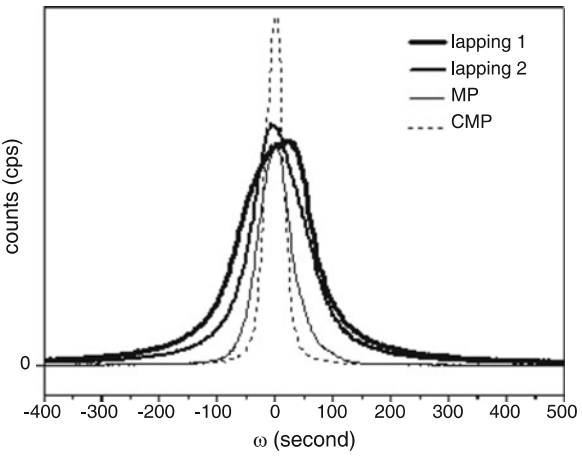

Fig. 2.54 Rocking curves of the SiC wafer surface in each machining process (Provided by Dr. Yan Peng at Shandong University)

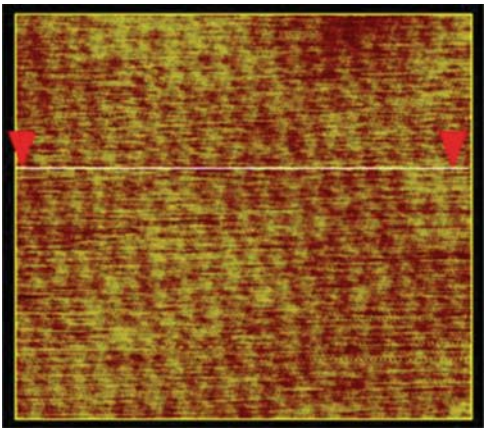

Fig. 2.55 AFM image of the CMP surface after KOH etching (Provided by Dr. Yan Peng at Shandong University)

after the passivating layers are removed [63]. Since material removal by this mechanism does not depend on the hardness but on the chemical potentials, it is possible to remove material by abrasives substantially softer than the workmaterial [63].

By HRXRD analysis shown in Fig. 2.54, the FWHM of (0004) reflection rocking curve of SiC wafer surface finished by CMP is 39.4 arcs which decreases much more than that after lapping. This indicates thin subsurface damage layer, good crystal lattice integrity, and low residual stresses in SiC wafer after CMP. From Fig. 2.54, it can be seen that FWHM falls down with each machining process. It proves that the damage layer and residual stresses have been minimized when the grain size of the abrasive decreases. The subsurface damage has been found to extend from depths ranging from one-half to one-seventy-fifth of the abrasive slurry size [64]. No scratches were visible on surfaces after KOH etching as shown in Fig. 2.55.

Three main machining processes of 2 in. SiC wafers were introduced. Slicing marks can be removed step by step by lapping and polishing. Lapping causes great residual stresses and deep damage layer which can be reduced gradually with subsequent polishing processes. Mechanical polishing produced smooth surface with a large number of scratches. These scratches can be effectively removed by CMP. After CMP, extremely smooth and low damage layer surface with roughness $R_a = 0.3$ nm was obtained. FWHM falls down with each machining process confirming that the surface damage layer and residual stresses minimize when the grain size of abrasive decreases. By the three main machining processes mentioned above, the final surface has low residual stresses and fine surface finish.

In summary, we introduce the SiC single crystal growth and substrate technologies in this chapter. It is difficult to reflect fully the status of SiC material research and development. Recently, new SiC growth technologies such as solution method and high-temperature chemical vapor deposition are well developed. However, we still hope that the contents in this chapter are helpful for SiC crystal grower and substrate processing technician.

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Chapter 3
Homoepitaxy of GaN Light-Emitting Diodes

Ke Xu, Miao Wang, Taofei Zhou, and Jianfeng Wang

3.1 Bulk GaN Substrates for Light-Emitting Devices

Crystal growth technologies are widely developed for the realization of GaN substrate with large size and high quality [1]. There are mainly three routes. The first one is improved from high-pressure high-temperature growth method. By adding sodium into the Ga melt for the enhancement of N concentration, the sodium flux growth method can grow GaN under temperature about 800 °C and lower pressure about 5 MPa [2]. The second route is referenced from hydrogen-thermal method, which is very mature for the growth of quartz. It is named as ammonothermal method by using ammonia as the solvent and KNH_4 or NH_4Cl as mineralizer; GaN crystal can be grown under low temperature about 600 °C and high pressure about 400 MPa [3]. The third growth method is HVPE, which is initially used in the growth of GaAs and InP [4]. With the advantage of high growth rate as several hundred micrometers per hour by HVPE method, GaN can be grown up to several millimeters, which is thick enough for the fabrication of bulk substrates. However, since there is a lack of GaN seed crystal, thick GaN films have to be grown on foreign substrates, such as sapphire, GaAs, and silicon. The big lattice and thermal mismatch between GaN film and the starting foreign substrate bring big challenge of strain control and dislocation reduction. On the other hand, separation of GaN from the foreign substrate is another challenge after the HVPE growth. Self-separation and laser lift-off technique are well developed to obtain crack-free GaN films.

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In this section, the progress in growth of bulk GaN by HVPE is introduced. The main challenges and solutions of HVPE growth method include dislocation reduction, strain control, and doping of GaN.

3.1.1 Growth Mechanism of HVPE System

Generally, HVPE reactor of GaN mainly includes two reacting zones. One is the source zone for providing chloride gas of gallium, and the other is deposition zone, in which the GaN is formed from the reaction of gallium source and nitride source (NH_3). Therefore, in the HVPE growth, main chemical reactions can be divided into two parts. One is in the source zone where the gallium is kept at a certain temperature and reacts with HCl gas, which is commonly used as reactive gas and introduced into the source zone over metal to form chloride gas of gallium. Then the gaseous species formed at the source zone are transported by carrier gas to deposition zone to further react with nitride source to form GaN. The carrier gases are generally H_2 and inert gas (N_2, He, Ar, etc.).

In the source zone, the gaseous species and their equilibrium partial pressures are very important for the formation of GaN in the deposition zone. Generally, the chemical reactions simultaneously happen in the source zone:

$$\mathrm{Ga\,(l) + HCl\,(g) = GaCl\,(g) + \frac{1}{2}H_2\,(g)} \tag{3.1}$$

$$\mathrm{Ga\,(l) + 2HCl\,(g) = GaCl_2\,(g) + H_2\,(g)} \tag{3.2}$$

$$\mathrm{Ga\,(l) + 3HCl\,(g) = GaCl_2\,(g) + \frac{3}{2}H_2\,(g)} \tag{3.3}$$

$$\mathrm{2GaCl_3\,(g) = (GaCl_3)_2\,(g)} \tag{3.4}$$

The equilibrium partial pressures in the source zone can be calculated by thermodynamic analysis [5]. In HVPE growth, the temperature of source zone is usually around 850 °C, at which the major gaseous species of gallium is formed by Eq. (3.1). It should be noticed that the input partial pressure of HCl should not be so high in order to make almost all the HCl introduced into the source zone react with gallium. Therefore, the equilibrium partial pressure of GaCl should be almost equal to that of HCl at source zone. From the thermodynamic analysis, if the temperature of the source zone is too low or the partial pressure of input HCl is too high, or the reaction area of gallium with HCl is too small, the reactions might be insufficient in the source zone, which means the reactions will be kinetically limited.

The GaCl formed at source zone and NH_3 are transported to the deposition zone separately by a carrier gas mixture of H_2 and inert gas. At the deposition zone, the source species are mixed, and the following chemical reactions occur simultaneously.

$$\mathrm{GaCl\,(g) + NH_3\,(g) = GaN\,(s) + HCl\,(g) + H_2\,(g)} \tag{3.5}$$

$$\mathrm{GaCl\,(g) + HCl\,(g) = GaCl_2\,(g) + \frac{1}{2}H_2\,(g)} \tag{3.6}$$

$$\mathrm{GaCl\,(g) + 2HCl\,(g) = GaCl_3\,(g) + H_2\,(g)} \tag{3.7}$$

$$\mathrm{2GaCl_3\,(g) = (GaCl_3)_2\,(g)} \tag{3.8}$$

Then, gaseous species at the growth zone include GaCl, $GaCl_2$, $GaCl_3$, $(GaCl_3)_2$, NH_3, HCl, H_2, and inert gas. The partial pressures of these gaseous species at the growth zone as a function of temperature at deposition zone have been calculated by Koukitu et al. [6]. The partial pressures of $(GaCl_3)_2$ and $GaCl_2$ are very small under typical growth conditions. The equilibrium constants for these reactions can be calculated from the equilibrium equations [7]. $GaCl_3$ also reacts with NH_3 to form GaN, whose equilibrium constant is close to zero at usual growth temperature. Though the equilibrium constants are close for both reactions using GaCl and $GaCl_3$, the partial pressure of $GaCl_3$ is far lower than that of GaCl. Therefore, Eq. (3.5) is the dominate reaction.

The driving force for the deposition can be obtained from the difference between the number of Ga atoms put in and the amount of Ga atoms remaining in the vapor phase, which can be written as [6]:

$$\Delta P = P^0_{\mathrm{GaCl}} - \left(P_{\mathrm{GaCl}} + P_{\mathrm{GaCl_3}}\right) \tag{3.9}$$

where P^0_{GaCl}, P_{GaCl}, and $P_{\mathrm{GaCl_3}}$ are the input partial pressure of GaCl, the partial pressure of GaCl, and $GaCl_3$ in the vapor phase in deposition zone, respectively. From the calculation [6], the growth temperature has an important influence on the driving force. One point should be noticed that the influence of H_2 on the decrease of the driving force is more significant at high growth temperatures and the driving force decreases with the increase of H_2 in the carrier gas [8].

3.1.2 Progress in HVPE Growth of GaN Substrate

3.1.2.1 Dislocation Reduction and Strain Control

To obtain high-quality and crack-free bulk GaN substrate, dislocation reduction and strain control are the most important issues during HVPE growth. Epitaxial lateral overgrowth (ELOG) is an effective and traditional method to bend the dislocation line and form void structure in GaN films simultaneously, which helps to enhance the dislocation annihilation for dislocation reduction and release the growth and thermal stress [9, 10].

A standard ELOG process is as below: (a) depositing mask film such as SiN, SiO_2, etc. on GaN film; (b) etching dielectric film to expose GaN as window area; and (c) growing GaN layer from the window and then laterally overgrowing to cover the mask. By carefully adjusting the mask/window shape, the growth parameters for the overgrowth, reasonable lateral overgrowth rate, and smooth surface can be achieved [10–13]. Other technologies base on ELO have been proposed like double-layer ELO [14, 15] and three-step ELO [16] in order to further eliminate the remaining TDs in the coalescence region.

By improvement of ELOG technology, some special technologies have been developed in HVPE system for the growth of high-quality and crack-free GaN layers, such as dislocation elimination by the epitaxial growth with inverse-pyramidal pits (DEEP), TiN-based nano-mask, and photoelectron-chemical-etched nanowires.

DEEP was reported by Kensaku Motoki from Sumitomo Electric [17]. During the growth of GaN layer, there are numerous large hexagonal inverse-pyramidal pits constructed mainly by {11 −22} facets appearing on the surface. While GaN growing, dislocations are collected to the center of the hexagonal pits parallel to (0001) in the <11 −20> or <1 −100> direction, and therefore dislocations are eliminated within the hexagonal pits except for its center. DEEP method can produce a high-quality GaN layer, but the dislocation distribution on surface of GaN is no uniform. Far away the center of pits possesses low DDs; on opposite, the center of pits gathering dislocation possesses very high DDs [18, 19].

Besides ELOG and DEEP, nano-mask is recognized as a good approach that not only reduces the DDs but also easily separates the freestanding GaN from sapphire. Yuichi Oshima et al. developed a novel technique for preparing large-scale freestanding GaN wafers called VAS (void-assisted separation) by thin TiN film [20].

ELOG, DEEP, and nano-mask are using dielectric film as mask for the overgrowth of GaN; another unique method without dielectric film as mask is developed in our institute [21]. By the electrode-less photoelectron-chemical (PEC), long and straight GaN nanowire arrays are obtained, which have a density about 10^7 cm^{-2}, diameters ranging from 150 to 500 nm, and corresponding lengths ranging from 10 to 20 μm. It is found that GaN nanowires are almost dislocation and strain free (Fig. 3.1a, b), because PEC etching is beginning from the dislocation core. Based on these GaN NWs, we can get high-quality and crack-free GaN layer (Fig. 3.1c, d), with thickness about 400 μm and dislocation density about 10^4–10^6 cm^{-2}.

In addition to the abovementioned methods, increasing thickness of GaN is another effective approach to decrease the defect density of GaN substrate. The dislocation density reduced to 10^6 cm^{-2} as the thickness increased to 5 mm [22]. According to the same research from our group, it is found that the dislocation density is declining sharply from 10^8 to 10^4 cm^{-2} when the thickness is from several micrometers increasing to several millimeters (Fig. 3.2a–h). The related panchromatic CL images of different thickness GaN are shown in Fig. 3.2i.

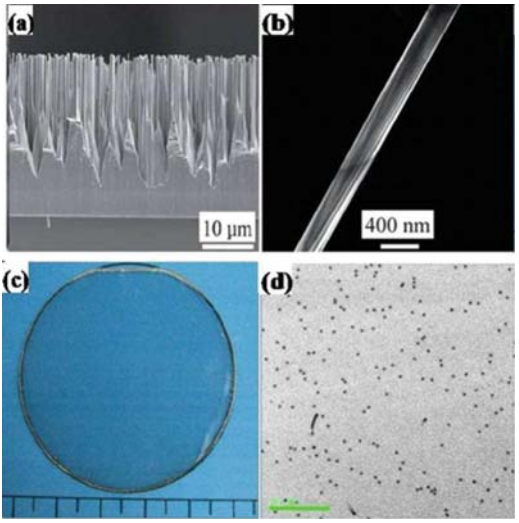

Fig. 3.1 (**a**) SEM image of GaN NW array [21]. (**b**) Weak-beam dark-field TEM image with $g = 11–22$, revealing that the GaN-NW does not possess dislocations [21]; Reproduced by permission of The Royal Society of Chemistry. (**c**) The photo of a 400 μm GaN base on the PEC GaN NW arrays template. (**d**) Panchromatic CL images show that the DDs of (**a**) are 3×10^6 cm^{-2}

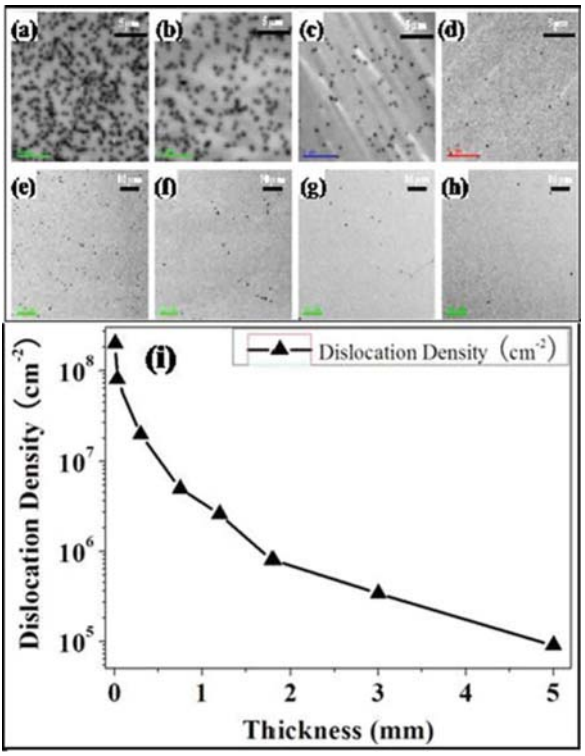

Fig. 3.2 Thickness from 5 μm to 5 mm and panchromatic CL images: (**a**) 5 μm, 2×10^8 cm^{-2}; (**b**) 20 μm, 5×10^7 cm^{-2}; (**c**) 200 μm, 2×10^7 cm^{-2}; (**d**) 0.7 mm, 5×10^6 cm^{-2}; (**e**) 1.2 mm, 3×10^6 cm^{-2}; (**f**) 1.8 mm, 8×10^5 cm^{-2}; (**g**) 3 mm, 3.4×10^5 cm^{-2}; (**h**) 5 mm, 8.0×10^4 cm^{-2}; (**i**) the relation between thickness and DDs

3.1.2.2 Si-Doping for n-GaN Substrate

The growth of *un*-doped GaN is simple but not suitable to make LED, LD, or high-power electronic devices, because its resistivity is relatively high with the typical value about 1 Ω cm. In order to control its electrical properties, a flexible and reproducible doping during HVPE growth of GaN is necessary and important.

SiH_4 is mostly used as the n-type doping source in MOCVD [23], but it is not suitable in HVPE, most of which is a hot-wall system with typical growth temperature of about 1040 °C. SiH_4 will decompose into silicon and hydrogen before it is transported to the growth zone of HVPE system, contributing less to the doping process. Great efforts have been made to find a proper doping source. Undoped single crystalline Si was used to react with HCl gas to produce dopants [24], but it is difficult to realize the precise control of the doping level. Dichlorosilane (SiH_2Cl_2) was a suitable choice for HVPE growth of Si-doped GaN because of its higher thermal stability.

The free carrier concentrations increase linearly in a semilog plot with SiH_2Cl_2 flow rates from 5 to 25 sccm [25]. This is different from the case in MOCVD growth of Si-doped GaN with SiH_4, where the free carrier concentrations increase linearly with SiH_4 flow rates [23].

The growth rate of GaN in HVPE is about tens to hundreds microns per hour, higher than that in MOCVD, so HVPE could easily realize growth of GaN with different dislocation density. The influence of dislocation density on the electron mobility is carefully studied. It is found that the mobility of FS GaN is higher than that of the GaN template at the same carrier concentration, with the dislocation density about 10^6 cm^{-2} for the freestanding GaN and 10^8 cm^{-2} for the GaN template, respectively. Edge dislocation introduces acceptor centers along the dislocation line, which could capture electrons and make the dislocation lines negatively charged. When electrons travel across the dislocations, it will be scattered, thus reducing the mobility [26].

3.1.2.3 Fe-Doping for High-Resistivity GaN Substrate

Semi-insulating (SI)-GaN substrate is very important for the performance of GaN-based HEMT device. However, *un*-doped GaN grown by HVPE in general shows n-type conductivity due to the residual donor impurities such as O and Si, which may give rise to the degradation of device performances. By compensation of the residual carriers from electron trapping centers, SI crystal is obtained by doping with Fe, Cr, or Zn [27–29]. Among these different doping elements, Fe-doping is wildly used for the reproducibility and controllability. With a Fe concentration above 10^{15} cm^{-3}, it is sufficient to compensate unintentionally incorporated donor impurities (oxygen and silicon) and native defects in GaN for the SI property [30, 31]. Although the formation energy and concentration of the point defect and/or the complex structure will be changed during the annealing process, the SI property of GaN:Fe bulk films grown by HVPE is thermal stability up to 1050 °C [32]. The resistivity

decreases with the temperature with an activation energy about 0.5–0.6 eV which is attributed to Fe deep acceptor [30, 33]. Fe-doped bulk SI GaN (SI-GaN:Fe) grown by HVPE has been commercialized and resulted in a significant improvement of the device performance and reliability of the AlGaN/GaN heterostructure field effect transistors [34, 35]. Besides the SI property, the other properties of the GaN:Fe also have been widely interested, such as a diluted magnetic semiconductor to realize future spintronic applications [36, 37].

Compensation mechanisms of GaN:Fe have attracted much more attention, since these are important to the optical, electrical, and magnetic properties of the crystal [28, 38]. The Fe atoms incorporated in GaN matrix substitute Ga sites and introduce the charge transfer level $Fe_{Ga}^{3+/2+}$ in the midgap, which are crucial to carrier-mediated ferromagnetism and to predict band offsets in heterostructures on the basis of the internal reference rule [36, 39]. Since the charged state of $Fe_{Ga}^{3+/2+}$ is transferred from Fe^{3+} to Fe^{2+} by capturing an electron, the Fe atom acts as a compensating deep acceptor in GaN [28, 32]. The Fermi level is pinned approximately 0.5–0.6 eV below the conduction band minimum (CBM), which will change the formation energies of native point defects of GaN. The Fe^{3+} on Ga site will split into the ground state $^6A_1(S)$ and the excited states $^4T_1(G)$, $^4T_2(G)$, and $^4E(G)$ [28, 38]. A series of characteristic IR luminescence with a sharp zero-phonon line (ZPL) at 1.299 eV due to the spin-forbidden $^4T_1(G) \rightarrow {}^6A_1(S)$ transition will be observed at low temperature, as shown in Fig. 3.3a. The additional lines above ZPL are attributed to the splitting of the excited $^4T_1(G)$ state of Fe^{3+} under the combined effects of spin-orbit coupling, Jahn-Teller coupling, and the axial distortion of the trigonal crystal field in C_{3v} of the wurtzite lattice structure [28, 40]. The luminescence appears at energies less than 1.3 eV which are attributed to the local vibrational modes and phonon mode. Besides the IR part emissions, the blue and red broad bands which are attributed to the defect structures related to the doped Fe ion are generally observed, while the common yellow band is nearly unobserved due to the ionizing of the shallow donor involved in the related defect level. On the other hand, since the carrier-lifetime-killer actor of the doped transition metal impurities, quenching of the intensity of near band-edge excitonic emissions in the UV region is expected, as those shown in Fig. 3.3b [32, 38]. Raman investigation on the GaN:Fe bulk crystal confirms a strain-free incorporation of iron. Besides the normal Raman mode, an additional Raman mode at 670 cm^{-1} is usually observed in Fe-doped samples, which was assigned to a kind of phonon mode originated from VN. But, as those shown in Fig. 3.3c, unlike the familiar point-defects, this mode is thermal stability after annealing up to 1050 °C. Hence, a Fe-VN complex structure-related Raman mode is considered [41].

3.1.2.4 Minority Diffusion Lengths in Bulk GaN

The dislocations strongly affect the carrier properties in GaN including minority diffusion lengths and surface recombination velocities which are important for device performance. For example, in photovoltaic detectors, due to a large

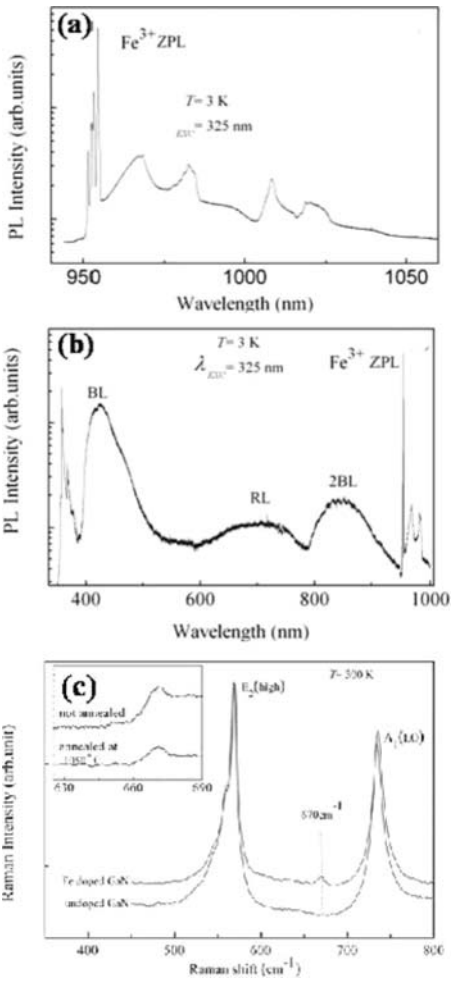

Fig. 3.3 (**a**) A series of characteristic IR luminescence with a sharp zero-phonon line (ZPL) at 1.299 eV at low temperature. (**b**) Quenching of the intensity of near band-edge excitonic emissions in the UV region. (**c**) A kind of phonon mode originated from VN

absorption coefficient of GaN, carriers are generated close to the surface and recombine. A sufficiently long minority diffusion length and the suppression of surface recombination velocity are helpful in the realization of high sensitivity [42]. However, for the most of characterization methods, such as photoluminescence [43], surface photovoltage [44], and photocurrent [45] measurements, the spatial resolution of as-measured carrier properties is low, which makes it difficult to reveal the relationship between the experimental results and the local dislocation structures. Electron-beam-induced current (EBIC) method is capable of achieving the inhomogeneity of minority diffusion length along a depth gradient, but a p-n junction or a Schottky barrier has to be made at cross section [46]. Recently, a combination of surface photovoltage spectroscopy (SPS) method and kelvin probe force microscopy (KPFM) was reported for the simultaneous measurement of the

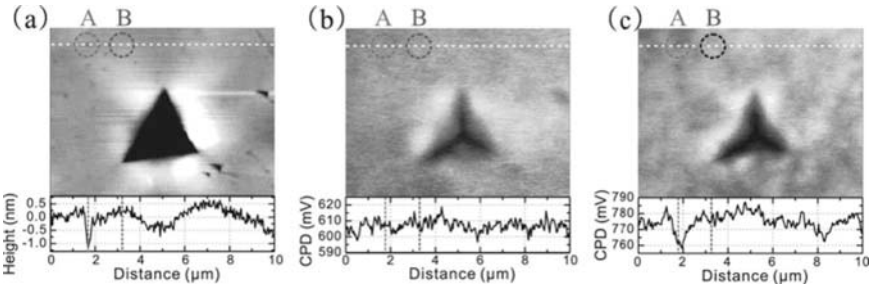

Fig. 3.4 (**a**) The topographic image around a nanoindentation with a scan area of 10 × 10 μm. A V-pit of thread dislocation is marked with A, and a nearby plane position is marked with B. (**b**) and (**c**) are the CPD images of the same area acquired under dark condition and under UV illumination with wavelength of 360 nm, respectively. The curves in the images are the profiles along the white lines

topography, the local minority diffusion length, and the surface recombination velocity at a single thread dislocation [47]. The contact potential difference (CPD) at nanometer scale varying with the incident photon energy was measured with corresponding topography image. SPS responses at single thread dislocations near a nanoindentation on a HVPE-grown GaN surface can be distinguished. As shown in Fig. 3.4a–c, the thread dislocations introduced by a nanoindentation were observed as V-pits, where the photovoltage was lower than that on plane surface under ultraviolet illumination. Compared with those on plane surface, the calculated hole diffusion length is 90 nm shorter and the surface electron recombination velocity is 1.6 times higher at an individual thread dislocation.

3.2 Structural Characterization in Homoepitaxial GaInN/GaN Light-Emitting Diode Growth

Group III-nitride device development still suffers from mismatched heteroepitaxial growth. Mismatch in lattice constants and thermal expansion coefficients between substrate, mostly sapphire or SiC, and epitaxial layer inhibits perfect crystal formation, resulting in high densities of threading dislocations [48]. Low-dislocation-density bulk GaN has therefore long been sought for as the ideal substrate for homoepitaxial growth. It was found that the performance of LEDs could be improved by a reduction of the threading dislocation (TD) density, especially for green LEDs [49]. Different techniques have been used to reduce the TD density, such as lateral epitaxial overgrowth [50]. These methods, however, reduce the TD density only in parts of the wafer, leaving the rest useless. With the recent advances in hydride vapor-phase epitaxy (HVPE), bulk GaN substrates with a TD density as low as 10^5 cm^{-2} provide an ideal template for homoepitaxial

growth [51]. Moreover, V-defects have often been reported in the active region of GaInN/GaN LEDs [52], especially with high In composition.

The main challenges are (1) to obtain epitaxial production worthy-sized bulk crystals of such high qualities and (2) to replicate the bulk performance in epitaxial overgrowth [53].

One very promising approach is to grow thick layers of GaN by hydride vapor-phase epitaxy (HVPE) [54–58]. In such material, threading dislocation densities, as judged by cathodoluminescence (CL) of the top surface [59], can routinely reach values as low 10^6 cm^{-2} and even 10^5 cm^{-2}. Wafers up to the dimensions of 2 inch are commercially available [60, 61]. The second challenge now calls for metalorganic vapor-phase epitaxy (MOVPE) to replicate the low dislocation density in homoepitaxial films on these substrates [62].

Here, two types of GaN templates were used for the analysis of the structural characterization of homoepitaxial GaN/GaN light-emitting diode: (1) 300 mm thick freestanding HVPE GaN and (2) 2 mm thick MOVPE GaN on 330 mm thick c-plane sapphire. HVPE GaN and MOVPE GaN templates were n-type doped with Si donor concentrations of 1×10^{18} and 1×10^{19} cm^{-2}, respectively. The surface of HVPE GaN was polished to atomic layer flat level via a proprietary chemical mechanical polishing (CMP) process. The root mean square (RMS) of the surface roughness of the HVPE GaN templates was 0.1–0.2 nm which was comparable to those of as-grown MOVPE GaN on sapphire. From (0004) X-ray rocking curve measurements, the full-widths at half-maximum were about 90 arcsec, while those for MOVPE-GaN were about 200–250 arcsec. An AIX-200RF MOCVD reactor was employed for homoepitaxy of GaInN-based light-emitting diodes (LED) consisting of (1) 0.5 mm thick n-GaN, (2) 5 periods of 3 nm thick GaInN quantum well and 6 nm thick GaN barrier, and (3) 0.2 mm thick *p*-GaN. Both templates were loaded into the growth chamber side by side. In order to prevent thermal decomposition of the templates, NH_3 was introduced into the chamber while raising the templates' temperature to growth temperature of *n*-GaN (1100 °C). The homoepitaxy growth proceeded immediately once the growth temperature was reached. Typical dopants of Si and Mg were utilized for the growth of *n*- and *p*-GaN with doping concentration of 3×10^{18} and 1×10^{20} cm^{-3}, respectively. Optimized growth conditions on the sapphire wafer were exploited for all epitaxial layers.

After the growth, both types of samples were evaluated for optical performance, crystalline quality, and surface morphology via photoluminescence (PL), X-ray diffraction (XRD), atomic force microscopy (AFM) techniques, and transmission electron microscopy (TEM), respectively. As shown in Table 3.1, the roughness of the *p*-layer due to heavy Mg doping was a factor of 2 higher on the sapphire-based structure than that of the GaN template.

Then typical LED fabrication processes such as reactive ion etching (RIE), e-beam evaporation, and photolithography were introduced to form mesa, transparent contacts, and electrodes on the LED devices. The size of the LED device was 350 μm × 350 μm with an effective mesa area of 300 μm × 300 μm. Transparent contacts on the mesa were formed by 5 nm of Ni followed by 5 nm of Au. A metal stack of Ti/Al/Ti/Au was formed on MOVPE-grown n-GaN layer for the electrical

Table 3.1 Reported performances of nonpolar and semipolar LEDs prepared on bulk-GaN substrates

Orientation	Structure	Wavelength (nm)	Radiant flux (mW)	Voltage (V)	Peak shift due to current increase	Reference
a	7-nm 5QW, no EBL[a]	450	...	4.4	None	[63]
a	3-nm 5QW	522	0.07	...	Red shift due to thermal effect	[64]
m	8-nm 6QW, 2.2-20 nm	407.4	23.7	5.2	Negligible blue shift	[65, 66]
m	3-nm 5QW	435	1.79	5	Blue shift	[67]
m	8-nm 6QW	468	8.9	6.4	Less than c-plane LEDs	[68]
m	2–4 nm 3QW	460–506	Max. 6	...	Red shift to be investigated	[69]
$(10\bar{1}\bar{1})$	2.5-nm 6QW	412	20.58	3.93	Minimal due to piezofield reduction	[70]
$(10\bar{1}\bar{1})$	3-nm 6QW	443.9	13.41	8.29	Minimal due to piezofield reduction	[71]
$(11\bar{2}\bar{2})$, $(11\bar{2}\bar{2})$	3-nm SQW	425, 530, 580	1.76, 1.91, 0.54	3.4, 3.8, 3.0	Blue shift due to state filling	[72]
$(11\bar{2}\bar{2})$	4-nm 6QW	522.4	5.0	6.9	Low-energy localized state filling	[73]
$(11\bar{2}\bar{2})$	3.5-nm SQW	562.7	5.9 (pulsed)	...	Localized energy state filling	[74]

Shown data were taken at 20 mA, unless mentioned otherwise. In the column for structures are the thickness and number of InGaN QWs [75]
[a]Electron-blocking layer

contact. Electroluminescence (EL) was employed to evaluate the optical output performance for LED on quasi-bulk HVPE GaN and LED on thin MOVPE GaN template on sapphire, named hereafter "LED on GaN" and "LED on sapphire," respectively. (0002) XRD curves confirmed the superlattice periods of 8.5 and 8.8 nm for GaInN/GaN active regions in LED on GaN and LED on sapphire as designed, respectively. A higher number of satellite peaks as well as one order of magnitude higher satellite peak intensities derived from the active region of the LED on GaN samples suggested superior crystalline quality and sharper interface of the GaInN quantum well (QW) and GaN barrier compared to those of the LED on sapphire samples. Fitting of the (0002) XRD curves assuming that the GaInN QW layers were pseudomorphically grown on GaN yielded indium contents of 13% and 9% for LED on GaN and sapphire, respectively. Though the difference in indium incorporation could be explained by compressive strain and/or template temperature, it will require further systematic study to clarify this discrepancy.

As shown in Fig. 3.5, PL peak wavelengths observed for as-grown LED on GaN and sapphire were 440 and 420 nm, respectively. The PL results agreed with (0002) XRD results and reconfirmed that indium incorporation was higher in GaInN QW layers in LED on GaN compared to that of the LED on sapphire. Moreover, the peak intensity of the LED on GaN was 20 times as strong as that that of the LED on sapphire. This big difference cannot be solely explained by the difference of the indium content.

The results of the optical output power of fully fabricated LED dies show that electroluminescence intensities of the LED on GaN were much stronger than those of the LED on sapphire when operating under the same driving current. At driving current of 0.5 A, the radiation power of the LED on GaN could reach 7 mW. Also, the LED on GaN's driving current could achieve values as high as 600 mA, which is much higher than the LED on sapphire. The latter reached the voltage limit of 7 V in the testing system at the driving current of only 80 mA. This result suggests the

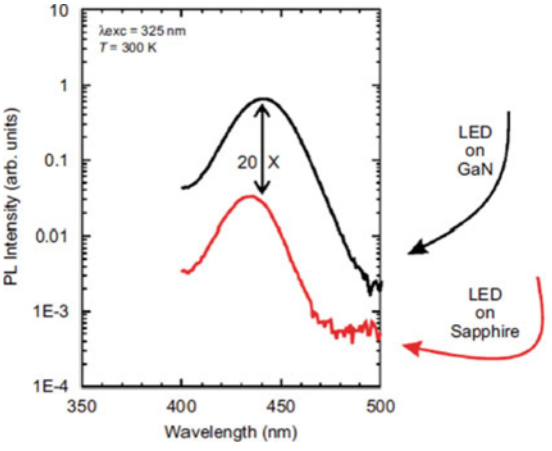

Fig. 3.5 Photoluminescence spectra of as-grown LED on GaN and LED on sapphire [53]

suitability of bulk GaN as a homoepitaxial template for high optical output power LEDs and hence solid-state lighting applications.

3.2.1 Evaluation of Threading Dislocation Density

Threading dislocation densities in the heteroepitaxial GaN on c-plane sapphire were as low as mid-10^8 cm^{-2} [6], while the threading dislocation densities on HVPE GaN were found to be about mid-10^6 to lower than 10^7 cm^{-2} [76]. After the homoepitaxial growth, threading dislocation densities in both samples increased to lower than 10^8 and lower than 10^9 cm^{-2} for the LEDs on GaN and sapphire, respectively. Jasinski et al. [77] reported that the threading dislocations on MOVPE-grown GaN and GaInN layers on quasi-bulk GaN templates were propagated directly from the template. The resulting threading dislocation densities of the homoepitaxial layers hence were of the same order of magnitude as those of the quasi-bulk GaN itself. The heavily doped Mg might initiate microstructural defects in p-GaN and lead to formation of additional dislocations. However, the process of newly formed dislocations which increased the threading dislocations densities in both samples by one order of magnitude was unknown. Investigations by transmission electron microscopy will be required to further investigate the nature of dislocations formed in the homoepitaxial layers. Nevertheless, this result suggests that existing dislocations could play a major role in the expansion of dislocation densities in the homoepitaxial growth.

Using scanning electron microscopy (SEM), the number of epitaxial defects, i.e., hexagonal pits, could be determined (Fig. 3.6). These defects appeared as dark spots in CL images taken at the peak wavelength of each sample. In the CL image of the LED on GaN, there were bands of low-intensity areas, while there were high densities of low-intensity spots scattered randomly over the mesa area. It was very difficult to identify dislocation-related dark spots on either sample. The pit densities were 7×10^4–3.6×10^5 cm^{-2} for the LED on GaN which were almost one order of magnitude smaller than those found on the LED on sapphire where defect densities were approximately 1–2×10^6 cm^{-2}.

However, when observing the LED on GaN at lower temperatures, i.e., 77–150 K, an additional number of dark spots besides those pits was observed as shown in Fig. 3.7. These additional dark spots represented dislocations formed in the regrown epitaxial layers. The corresponding dislocation densities were found to be about 2×10^6 and 5×10^6 cm^{-2} at 438 and 385 nm, respectively. At 385 nm, there was strong emission observed from pits. The emission at 385 nm was attributed to donor–acceptor pair recombination. On the other hand, it was difficult to estimate more accurate densities of the dark spots for the LED on sapphire due to its high dislocation density.

For comparison, the CL images at 367 nm were collected from an etched *n*-GaN area. For the LED on GaN sample, there were a number of dark spots that clearly related to threading dislocations. The density of those dark spots was

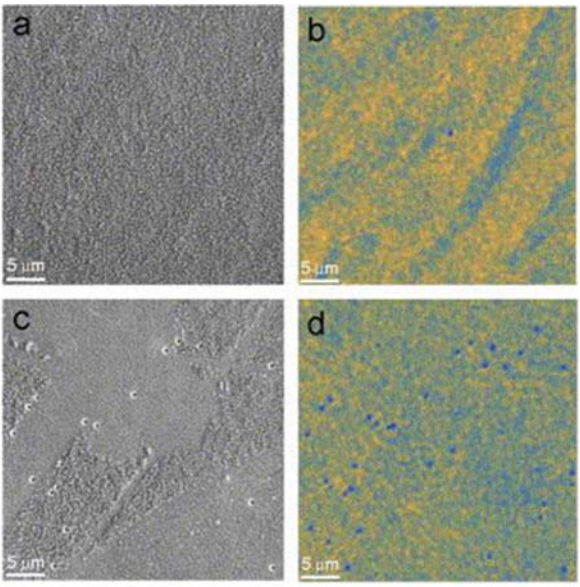

Fig. 3.6 SEM (a, c) and CL (b, d), micrographs of mesa area on the LED on GaN (a, b) and the LED on sapphire (c, d). The CL micrographs were collected at 440 and 420 nm for LED on GaN and sapphire, respectively. Markers represent 5 μm. Rugged surface of both samples were formed during LED fabrication process. Pits can be clearly identified as dark spots in CL images [53]

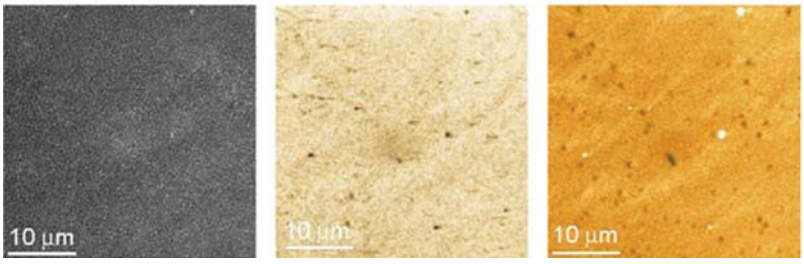

Fig. 3.7 SEM (left) and CL (middle and right) micrographs of mesa area on LED on GaN at 79 K. The central and right images were taken at 438 and 385 nm, respectively [53]

4.5×10^6 cm^{-2}. This number was similar to those found for the LED on GaN at low temperature. There are still a number of control parameters such as template cleaning procedure and growth conditions to optimize in order to further reduce the dislocation density in the homoepitaxial layer on such quasi-bulk HVPE GaN templates.

A cross-sectional TEM micrograph is shown in Fig. 3.8. It reveals the set of five QWs between n-type and p-type layers. No growth boundary is observable at the homointerface of the bulk GaN template and the epitaxial GaN layer. The contrast variations in the multiple quantum well (MQW) stack may be the result of radiation damage, ion-milling damage, or local charge or strain buildup. It was also suggested that phase separation in the GaInN QWs might be possible. Furthermore, no defects are observed along a lateral length of the QWs for over 1.2 μm. This suggests a low density of structural defects and good crystalline quality of the epitaxial material [78].

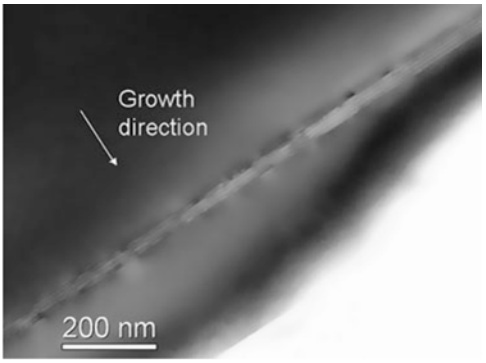

Fig. 3.8 Bright-field image of the QWs recorded along the $[1\bar{1}00]$ zone axis. The narrow darker lines are the QWs. Note that there is no defect along a lateral distance of more than 1.2 μm [78]

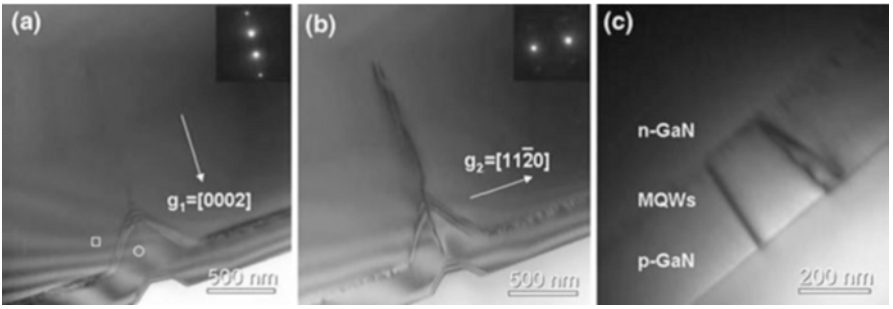

Fig. 3.9 Bright-field images at $g1 = [0002]$ (**a**) and $g2 = [11\bar{2}0]$ (**b**). The insets are the corresponding diffraction patterns. A large inverted pyramid with a diameter of 650 nm and depth of 480 nm is seen. The TD connected with the inverted pyramid is determined to be edge-type by the $g \cdot b = 0$ invisibility criterion. Subfigure (**c**) was taken along the $[1\bar{1}00]$ zone axis. It shows TDs that originate in the QWs [78]

It was also observed that large inverted pyramid defects were initiated by TDs, as shown in Fig. 3.9. The $g \cdot b = 0$ invisibility criterion was used to determine the defect type. In Fig. 3.9a, the TD reveals no contrast when the sample was tilted to $g1 = [0002]$. This indicates a Burgers vector of $b = 1/3\langle 11\bar{2}0\rangle$ and identifies it as an edge-type TD. The length of these TDs is usually 1.5 μm or more, while the epitaxial layer is only 0.75 μm thick. These TDs should therefore originate from the bulk GaN template and not from the epitaxial growth.

These large inverted pyramids have diameters from 600 to 650 nm at the top, and their depths range from 460 to 480 nm. Their origin beneath the QW region corresponds very well to the thickness of the overgrown n-layer. It can be concluded that they should form at the beginning of the homoepitaxial growth. During the growth of the n-type GaN, there must have been no or only very little growth of GaN around the vicinity of the TDs. However, after the deposition of five periods of QWs, the p-type material begins to fill in the V-shaped gap. Since the p-type GaN cannot fill in the gap entirely, pits with diameter from 300 to 500 nm remain at the surface and can be observed in the scanning electron microscopy (SEM) images

[53]. Thus the density of such large inverted pyramids was determined to be around 3×10^5 cm^{-2} by counting the pits in the SEM images. The TDs themselves continue to propagate until they reach the sample surface.

Inversion domains are known to exist in the homoepitaxial layer of GaN [79] and could lead to the formation of pits on the surface [80]. Therefore, in order to make sure that whether there are any inversion domain inside of the inverted pyramids, convergent beam electron diffraction (CEBD) is used to determine that patterns recorded inside (circle in Fig. 3.9a) and outside (square in Fig. 3.9a) the inverted pyramid, respectively. Both of them were taken along the $[1\bar{1}00]$ zone axis. Figure 3.10b and d are simulated patterns of Ga polarity at thickness of 210 nm and 180 nm, respectively. From left to right, the indices of each disc are [0002], [0000], and $[000\bar{2}]$. The different contrast within the [0002] and $[000\bar{2}]$ discs is caused by the polarity. By comparing the experimental patterns with the simulated ones for both polarities, we find that the material both inside and outside of the inverted pyramid has the same Ga polarity. Consequently, the inverted pyramids are not inversion domains. Besides TDs connected with inverted pyramids, TDs originating in the QWs are observed as well, as shown in Fig. 3.9c. The total TD density is estimated to be 2×10^8 cm^{-2} or less from cross-sectional TEM images. Those additional defects suggests that there is a need for further growth optimization of the QW region. For the heteroepitaxial LEDs, the TD density was determined to be 6×10^9 cm^{-2} by plan-view TEM. These TDs are mainly of edge and mixed type. No generation of V-defects is observed when TDs go through the QWs. Despite

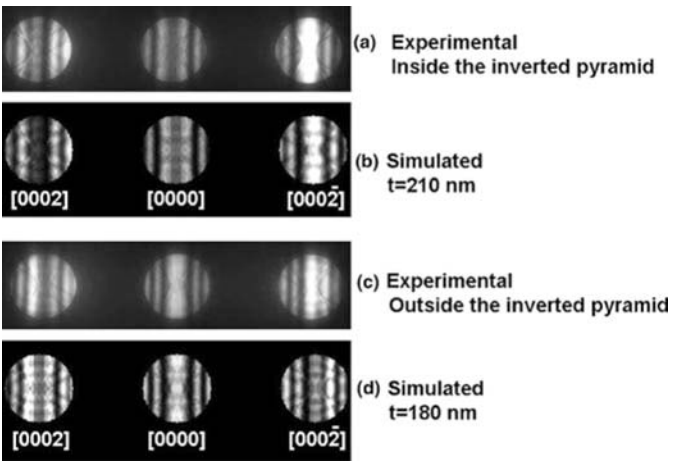

Fig. 3.10 CBED patterns of the GaN thin films recorded (**a**) inside the inverted pyramid (circle in Fig. 3.9); (**c**) outside the inverted pyramid (square in Fig. 3.9). Both of them were taken along the $[1\bar{1}00]$ zone axis. (**b**) and (**d**) show simulated CBED patterns for Ga polarity at thicknesses of 210 nm and 180 nm, respectively. The different contrast within [0002] and $[000\bar{2}]$ discs is due to the polarity. Comparisons between the experimental patterns and simulated ones suggest both materials have the same Ga polarity [78]

the existence of large inverted pyramids, the TD density has been reduced in the homoepitaxial LED to 1/30 of that in the heteroepitaxial one. This must be the reason for the 20-fold stronger photoluminescence intensity in the homoepitaxial material, as described in Ref. [53].

3.2.2 Electrical Characterization and Optical Characterization of Homoepitaxial InGaN/GaN Light-Emitting Diodes

InGaN/GaN-based light-emitting diodes (LEDs) grown heteroepitaxially on sapphire or SiC substrates contain a high density of threading dislocations ($\sim 10^8$–10^{10} cm^{-2}) due to large lattice and thermal expansion mismatch between the substrate and III-nitrides. It has been found that the high density of dislocations has limited adverse effects on the optical performance of the LEDs, especially at blue and green wavelengths, due to strong carrier localization effects in InGaN alloys [81, 82]. However, the dislocations, particularly those threading through the active region, may have a pronounced influence on the electrical characteristics of the LEDs by enhancing carrier tunneling [83, 84], dopant diffusion [85–87], and contact metal migration [88]. Anomalously high leakage currents are generally observed in commercially available GaN-based LEDs, which in many cases are grown on sapphire substrates. The high junction leakage raises concerns about device reliability, particularly under high-power operation conditions [89].

InGaN/GaN MQW LEDs on a freestanding GaN substrate can substantially reduce the defect density. As a consequence, the LEDs show a marked reduction in reverse leakage current, forward tunneling current, and improved injection efficiency under low bias compared to their counterparts on conventional sapphire substrates.

Cao et al. compared the electrical characteristics of InGaN/GaN multiple-quantum-well (MQW) LEDs grown on bulk GaN and sapphire substrates [90, 91]. The bulk GaN substrates with a thickness of 300 μm were produced by the HVPE technique [92, 93]. The materials were unintentionally doped and had a room-temperature resistivity of ∼0.076 Ω cm. The dislocation density in the bulk GaN is $\sim 2 \times 10^7$ cm^{-2}, several orders of magnitude lower than those in the heteroepitaxial GaN. Homoepitaxial growth was conducted on the Ga-face of the GaN substrates by low-pressure metalorganic chemical vapor deposition at 1050 °C using trimethylgallium (TMGa) and ammonia precursors. Silane and bis-cyclopentadienyl-magnesium (Cp_2Mg) were used for n- and p-type doping, respectively. Hydrogen was used as the carrier gas.

LEDs with peak wavelengths ∼405 nm were grown on both GaN and sapphire substrates in the same growth run. The LED structure consisted of a 10-period $In_xGa_{1-x}N$/GaN ($x = 0.1$–0.21) multiple-quantum-well (MQW) active region sandwiched between a 2 μm *n*-GaN layer (Si 5×10^{18} cm^{-3}) and a 0.1 mm p-type AlGaN cladding layer and a 0.2 μm *p*-GaN contact layer (Mg$\sim 1 \times 10^{19}$ cm^{-3}).

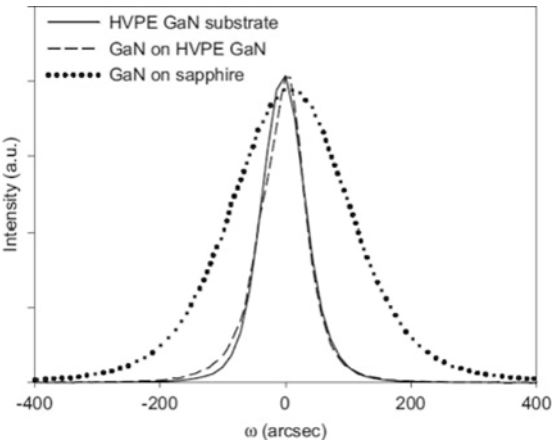

Fig. 3.11 HRXRD rocking curves of the (0002) reflection of an HVPE GaN and GaN epilayers grown on GaN and sapphire [91]

Top-emitting LEDs with a size of 300 μm × 300 μm were fabricated using standard photolithography and dry etch techniques [94]. For direct comparisons, identical devices were also grown on 2 in. sapphire substrates with a 100 nm GaN buffer layer under the same epitaxy conditions.

The homoepitaxial GaN epilayers exhibited a smooth, defect-free surface with a clear step structure, as revealed by AFM measurements, indicating good 2D step-flow growth. Second ion mass spectrometry (SIMS) measurements showed that the C, H, and O concentrations in the homoepitaxial structures were lower than those in heteroepitaxial GaN by a factor of 2–4 and are close to their SIMS detection limits. The reduced impurity incorporation in the homoepitaxial GaN is likely a result of reduced microstructural defects which may act as impurity segregation sites [95]. High-resolution X-ray diffraction (HRXRD) characterization showed that the rocking curve FWHM of the (0002) reflection of the GaN substrates, the epilayers on GaN, and the epilayers on sapphire are in the range of 85–129, 79–119, and 224–245 arcsec, respectively. Figure 3.11 compares the HRXRD rocking curves of a GaN substrate before and after homoepitaxial growth of a 3 mm GaN and a typical GaN epilayer on sapphire. The rocking curve FWHM of the homoepitaxial GaN is 79 arcsec, which is slightly smaller than that of the substrate (85 arcsec) and much smaller than that for GaN grown on sapphire (230 arcsec). Since the FWHM of the (0002) peak reflects the degree of lattice distortion from dislocations, the smaller FWHM of the homoepitaxial GaN confirms that the threading dislocation density is substantially reduced.

Figure 3.12 compares typical *I*–*V* characteristics of the LEDs measured at increasing temperatures. At low and moderate forward biases, two main exponential segments with different slopes can be distinguished for the LED on sapphire. The *I*–*V* characteristics can be represented by $I = I_0 \exp(qV/E)$. The temperature-independent energy parameter E has values of 190 and 70 meV in the voltage ranges 0–2.0 and 2.0–2.8 V, respectively. No realistic ideality factors can be extracted. These behaviors are characteristic of tunneling current in a semiconductor diode [83,

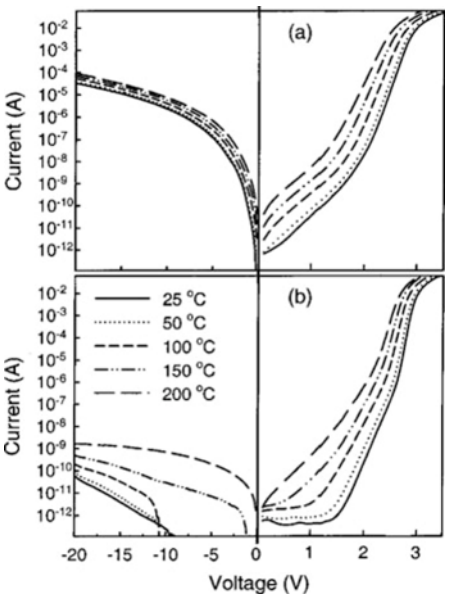

Fig. 3.12
Temperature-dependent $I-V$ characteristics of the LEDs grown on (**a**) sapphire and (**b**) GaN [90]

84]. The forward I–V characteristics of the LED on GaN also divide into two distinct linear sections with different slopes (see Fig. 3.12b). However, the slopes appear to be a function of temperature. At low injection levels, tunneling may still dominate, but the slope change suggests the involvement of thermally activated currents. As the forward current increases, diffusion and recombination currents start to dominate over the tunneling component. In fact, the forward current at bias >2.6 V can be described by the conventional drift-diffusion model as $I = I_0 \exp(qV/1.5kT)$ until series resistance in the diode dominates. The dominance of diffusion-recombination current reflects the high material quality of the homoepitaxial LED, where defect-assisted tunneling current is greatly suppressed.

The reverse-bias current in the LED on sapphire is much higher than conventional diffusion and generation currents, which are unobservably small in wide bandgap semiconductor diodes. The strong field dependence but low-temperature sensitivity of the leakage current is indicative of carrier tunneling. In sharp contrast, the LED on GaN shows a dramatic reduction in reverse current by more than six orders of magnitude. The remaining leakage current is a function of both applied bias and temperature, suggesting a combination of tunneling current and thermal generation current. In particular, as temperature increases from 100 to 150 °C, there is a sudden jump in the low-bias current, probably arising from thermal ionization of carriers from deep traps and trap-assisted tunneling process. An activation energy of ~0.5 eV is extracted from the $\log(I) - 1/T$ plot at −12.5 V where the change of the current as a function of temperature is roughly an exponential function.

The defect density in the homoepitaxially grown InGaN/GaN MQW LED is remarkably reduced compared to the similar device grown on sapphire, leading

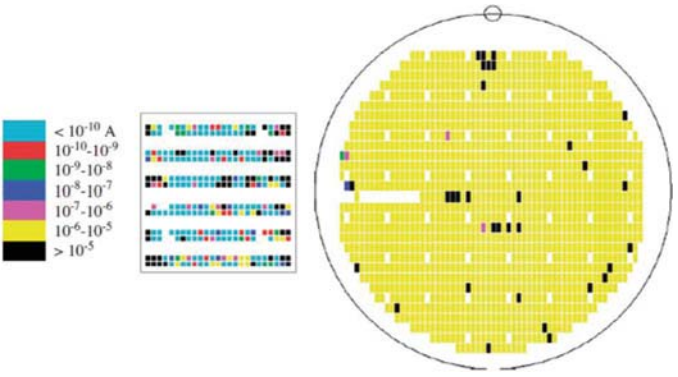

Fig. 3.13 The distribution of reverse currents at −10 V in LEDs grown on 1 × 1 cm^2 GaN and 2 in. sapphire substrates [91]

to much improved electrical characteristics. In contrast to the strong tunneling behaviors observed in the LED on sapphire, thermally activated currents were found to be dominant in the LED on GaN. An inhomogeneous distribution of reverse current in the LED on sapphire provides evidence that V-defects and the associated screw and mixed dislocations are electrically active and behave as leakage current pathways.

To investigate the distribution of leakage current in the LEDs, wafer mapping was carried out. Figure 3.13 shows the maps of leakage current measured at −10 V. The current is relatively high (∼3 μA) in the LEDs on sapphire but very uniform across the 2 in. wafer. Only 2% of the LEDs have leakage current >10 μA at −10 V. While most LEDs on GaN have extremely low reverse leakage (<10^{-3} μA), ∼20% of the LEDs are quite leaky. Interestingly, most leaky devices are located near the wafer edges, where the density of macroscopic defects in the GaN substrate is higher. This finding supports the above assumption that major defects originating from the substrate surface cause the low yield and poor scalability of the homoepitaxial diodes. Figure 3.14 shows the mapping results of the forward voltage at 50 mA. The average value for the LEDs on GaN is 3.9 V, lower than 4.2 V for the LEDs on sapphire. Approximately 5% of the LEDs on GaN, mainly along the wafer edges, have a forward voltage lower than 3 V. These devices are essentially shorted in both forward and reverse directions.

The superior electrical characteristics of most homoepitaxial LEDs are consistent with their improved optical properties. At 20 mA, the LEDs on GaN are twice more efficient than the LEDs on sapphire. The performance improvement is even more pronounced at low injection currents. This can be ascribed to the high structural quality of the MQW structures where nonradiative recombination rates are greatly reduced.

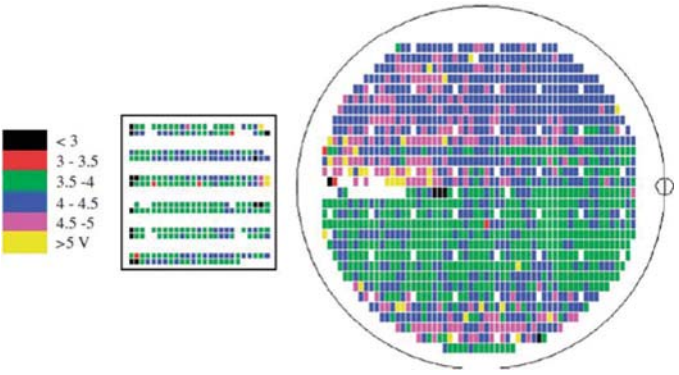

Fig. 3.14 The distribution of forward voltages at 50 mA of LEDs grown on 1 × 1 cm^2 GaN and 2 in. sapphire substrates [91]

3.3 Nonpolar and Semipolar Orientations GaN LED Grown on Bulk GaN Substrates

3.3.1 Problems with Conventional c-Plane LEDs and Motivation for Nonpolar and Semipolar Orientations

As the spectral range of light emission was extended from blue to green, we encountered a problem in luminescence efficiency, which is strongly related to InGaN material quality and QW structure. The material issue is that InGaN alloys tend to show spinodal decomposition [96, 97]. Furthermore, underlying GaN layers cause pseudomorphic growth of InGaN, thus, high In content is difficult and tends to introduce misfit dislocations and other types of defects. This problem is related to thermodynamics and growth kinetics; hence growth techniques and optimization will improve the materials. This aspect of the problem is common to all crystallographic orientations; nevertheless, different orientations may have different degrees of tolerances. The empirically found trend of high In incorporation into $(11\bar{2}2)$-oriented InGaN films may be related to this aspect. Further investigations are expected [75].

The QW structure-related challenge is due to the quantum-confined stark effect (QCSE, LEDs with thick active layers were dimmer than those with thin active layers) (Fig. 3.15). This effect is inevitable as long as strained QW structures are used in the polar orientation. In this case, a crystallographic solution may be given: employment of nonpolar orientation to have the polarization vectors lie in the plane, thus in the device direction, so no strain-induced electric fields appear. This is the main reason for the nonpolar orientation. Once we eliminate the QCSE, thicker active layers, as thick as the critical thickness, can be employed, which offer advantages, e.g., a larger active region volume. In addition to nonpolar orientations, it has been found by computation that semipolar orientations can provide similar

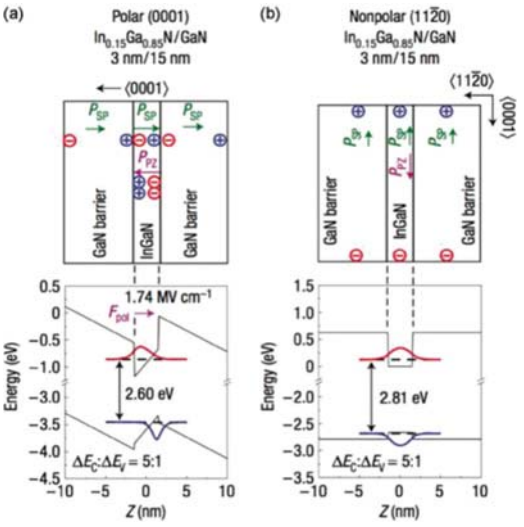

Fig. 3.15 QW structures on (**a**) polar and (**b**) nonpolar orientations and their band diagrams. Polarization charges appear at interfaces of the polar-oriented QW and induce electric fields that spatially separate electrons and holes in the QW. In nonpolar orientations, polarization charges do not affect the band structure. Because of the internal electric fields in the polar-oriented QW, transition energy occurs to be smaller than that of the nonpolar-oriented QW (QCSE). When the QW is embedded in the common +c-oriented LED structure, the internal electric fields are increased as LED positive bias is increased. After Chichibu et al. [98]

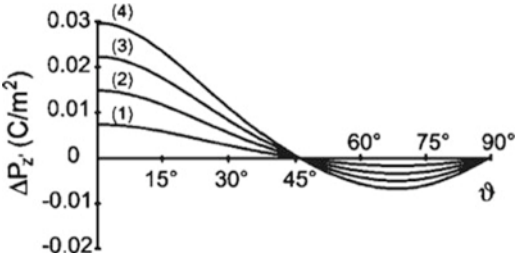

Fig. 3.16 Computed polarization charge (spontaneous and piezoelectric) density in InGaN/GaN QWs as a function of tilt angle of the growth plane with respect to the c-plane. Internal field strength becomes zero around $\theta = 45°$. After Romanov et al. [100]

effects in eliminating the QCSE. These calculations depend on material parameters such as elastic constants. Some of the necessary parameters are not well known to date, particularly those of InN [99]. These uncertainties introduce variations in the calculated results; Fig. 3.16 is an example result of these studies [100, 101]. Nevertheless, it has been believed that the advantage will be obtained for angles around 45°–60°. These angles include $(10\bar{1}1)$ and $(11\bar{2}2)$ orientations.

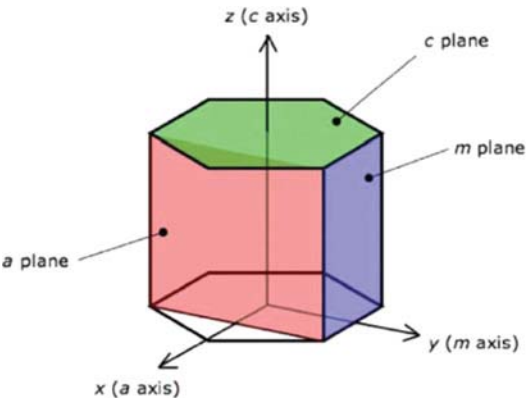

Fig. 3.17 Hexagonal prism representing a GaN crystal unit cell with common nomenclature of planes and axes. Coloring of the planes is for clarity and does not indicate any physical significance [75]

In addition, extra properties such as optical polarization are considered to be advantages over c-plane devices in some applications.

3.3.2 Crystallography and Piezoelectricity

A significant difference in nitride semiconductors from other conventional optoelectronic semiconductors is the crystal structure. Nitride semiconductor materials crystallize in wurtzite structures, while other typical optoelectronic semiconductor materials crystallize in zinc blende structures under normal conditions. Hexagonal lattices are expressed by using the Miller-Bravais index [102, 103]. Figure 3.17 shows a hexagonal prism representing a GaN crystal. The (0001) plane is the conventional growth plane and is called the $+c$ plane. All the current commercial products are fabricated via the c-orientation growth. The c axis [0001] is an electrically polar axis in wurtzite crystals. The $(000\bar{1})$ plane is often called the $-c$ plane; the zinc blende equivalence is considered to be the {111} B plane. Vertical planes are parallel to [0001], thus electrically nonpolar, and they are called nonpolar planes. Low-index nonpolar planes are $\{11\bar{2}0\}$ and $\{1\bar{1}00\}$, called a and m planes, respectively. It is a convention that the z axis of a 3-D spatial coordinate system is defined to be parallel to the c axis. It is a common practice that the x and y axes are defined to be parallel to the a and m axes, respectively. Note that Cartesian coordinates are conventionally used in wurtzite crystals. In some literature, the x and y axes are defined to be parallel to the m and a axes, respectively, as these two crystallographic axes are chemically different but equivalent in the sense of continuum mechanics [104]. Planes that make angles with respect to the c axis are called semipolar planes. Figure 3.18 shows three low-index semipolar planes in relation to the two nonpolar planes, which are important in InGaN LEDs. Semipolar planes are seldom atomically flat planes containing atomic steps. Detailed discussions are given in [105].

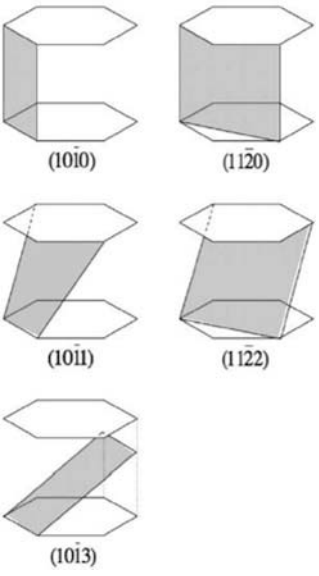

Fig. 3.18 Important semipolar planes (bottom three, painted in gray) shown along with the low-index nonpolar planes (top two). $\{10\bar{1}1\}$, $\{10\bar{1}3\}$, and $\{11\bar{2}2\}$ planes are at 62°, 32°, and 58° from the basal plane for GaN, respectively [75]

It is calculated from the closely packed structure of spheres that the ideal wurtzite structure possesses a *c/a* ratio of 1.633, where *c* and *a* are the conventional lattice constants in the *c* and *a* crystallographic directions, respectively. In reality, GaN, for example, has a ratio of 1.627, which implies that the crystal is compressed in the *c* direction under standard conditions (room temperature, 1 atm). Consequently, the centers of positive and negative charges from the ionicity of the Ga–N bond are displaced from each other, and electric charges theoretically appear at the opposite surfaces of the crystal. This is called spontaneous polarization. It is also possible to intentionally stress crystals (e.g., coherently grown heteroepitaxial films). The *c/a* ratio changes from the unstrained state, and additional polarization charges will result, which is called piezoelectric polarization. In any case, semiconductor crystals are not able to sustain voltages larger than their bandgaps, as carriers start shifting within the crystal to neutralize polarization charges (Fig. 3.19a), or ions in the atmosphere may adhere to the crystal surface to neutralize the polarization charges [106]. As a result, electric fields induced by spontaneous/piezoelectric polarization are irrelevant in large homogeneous materials (Fig. 3.19b). However, in heterostructures, this is not the case. There will be polarization-charge discontinuities at the interfaces, and net polarization charges induce internal electric fields. These electric fields are relevant in small-size heterostructures, e.g., QWs, resulting in the QCSE (Fig. 3.15). The strength of the internal electric fields is determined by the projection (i.e., cos θ) of the polarization vector (i.e., strain state, *c/a* deviation from 1.633) onto the plane of interest. Nonpolar orientations utilize cos $\theta = 0$, and semipolar orientations try to attain $c/a = 1.633$ (although strained semipolar crystals do not necessarily remain wurtzite, rigorously speaking; see [100] for details).

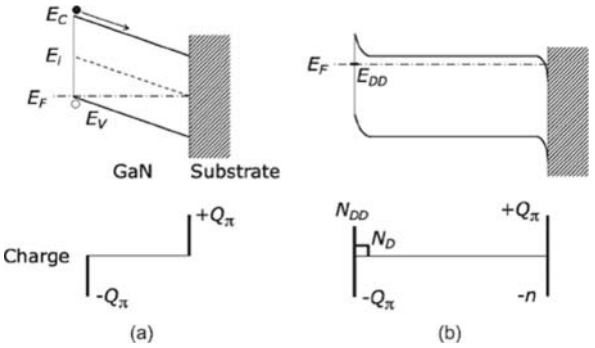

Fig. 3.19 Effects of polarization fields on carrier generation and field screening. (**a**) Idealized case of intrinsic semiconductors described by the band diagram and charge distribution. As a crystal grows on an insulating substrate, E_V meets E_F as a result of polarization fields. Holes are created at E_V, and electrons are swept toward the substrate by the polarization fields. Polarization charges ($+Q_\pi$ and $-Q_\pi$) are located at the interface and growth surface and are screened by carriers as the film grows. (**b**) More realistic case of thick n-type semiconductor films. Generated electrons have gathered at the substrate interface ($-n$) and neutralized the polarization charges. At the film surface, E_F is pinned at a deep donor level (E_{DD}), and a space charge layer is created where donors are charged (N_D). Polarization charges at the surface are neutralized by the charged donor and deep donors (N_{DD}) [75]

3.3.3 *Performance of Nonpolar and Semipolar-Oriented LEDs Using Homoepitaxial Substrates*

Several heteroepitaxial approaches implement *m*-axis or *a*-axis growth orientations [107, 108] yet result in very high densities of threading dislocations ($\sim 10^{10}$ cm^{-2}) and stacking faults ($\sim 10^5$ cm^{-1}) likely limiting LED performance [108]. The use of low-dislocation-density bulk GaN substrates sliced from boules recently resulted in better nonpolar homoepitaxial growth [72, 109]. UV and blue GaInN LEDs on the *m*-plane [67] and green and yellow LEDs on semipolar $(11\bar{2}2)$ substrate [73] have been demonstrated, the best of which show properties superior to those of c-plane growth [67, 72, 73, 110].

Bulk GaN substrates became available commercially in 2006. By that time, c-plane GaN wafers were commercially available but were limited in supply at a high cost. By making *c*-oriented hydride vapor-phase epitaxy (HVPE) GaN grow thick enough ($\sim$5 mm), it is possible to slice it in other orientations, thereby obtaining nonpolar and semipolar GaN substrates [111]. Hence, the size of the sliced wafers depends on how thick *c*-oriented GaN crystals were grown, and the current HVPE growth technology enables to provide approximately 10-mm-thick crystals. Although harvested nonpolar/semipolar substrates are small in view of commercial LED production, they are large enough to carry out basic research to investigate the potential of nonpolar- and semipolar-oriented LEDs. The performance of homoepitaxial LEDs is summarized in Table 3.1.

Most nonpolar LEDs reported to date have been fabricated on the m orientation. LED performances were drastically improved by two research groups via homoepitaxy [66, 67, 112]. Kim et al. [68] claimed an advantage of growing thick QWs due to the absence of the QCSE. The external quantum efficiency was determined to be ~40% in the early study [67]. The current desire is to achieve luminescence of longer wavelengths [69], as only one report can be found on LEDs beyond 500 nm with reasonable optical output power [113]. We may be able to have an optimistic view on achieving green light emission from m-plane LEDs, as a similar obstacle was confronted by c-plane LEDs during the 1990s. Other problems include hillock formation on epitaxial m-plane films. The mechanism of hillock formation and their effects on LED characteristics are still unknown. Hillock formation can be avoided by employing vicinal substrates [112, 114, 115]. Tsuda et al. [116] reported smooth film growth without hillocks. Although a study by Yamada et al. [63] indicated that the m-orientation had a higher potential for light-emitting devices than the a-orientation, recent accomplishments on a-plane LEDs emerged in 2008 have demonstrated competitive performances [64, 72]. Green light emission was achieved, yet output power was comparable to heteroepitaxial LEDs.

Despite the advantage of arbitrary slicing GaN crystals, experimental studies on semipolar LEDs have been limited to $(10\bar{1}1)$ and $(11\bar{2}2)$ orientations [117]. These two low-index planes share a tilt angle of approximately 60° with respect to the *c*-plane; thus, they are considered to be advantageous in terms of the QCSE. Green, yellow, and amber light emission has been realized on $(11\bar{2}2)$ with reasonable optical output [70, 73, 74]. The $(11\bar{2}2)$-oriented InGaN yellow LEDs were reported to have more stable performances against changes in ambient temperature than AlInGaP yellow LEDs [70]. $(10\bar{1}1)$-oriented LEDs have exhibited strong blue light emission [71, 118] with 34% external quantum efficiency, and longer wavelength emission has now been sought. As far as green emitters are concerned, the $(11\bar{2}2)$ orientation seems to have advantages among reported nonpolar/semipolar orientations to date. An important achievement on laser diodes to be mentioned here was reported by Enya et al. [119] in July 2009. Pure green laser diodes were demonstrated on the $(20\bar{2}1)$ plane, which has not been used for LEDs.

It is not intuitive that if the m-plane is preferred to the a-plane in device fabrication, why does the $(11\bar{2}2)$-plane (an inclined a-plane) seems to have advantages over the $(10\bar{1}1)$-plane (an inclined m-plane). We do not know yet whether these are inherent properties of these crystallographic planes or if it is only a matter of growth techniques and conditions.

3.4 Efficiency Droop and Efficiency Enhancement of Homoepitaxial InGaN/GaN Light-Emitting Diodes

The development of high-brightness LEDs suffers from the nonthermal rollover of internal quantum efficiency (IQE) at high current density known as the efficiency droop [120–122]. For the best commercial LEDs, the IQE peaks at a current density

of a few A cm^{-2} but is reduced by ~25% at high current density J ~100 A cm^{-2}. Several mechanisms for efficiency droop have been proposed, including carrier leakage [120] and carrier delocalization from In-rich regions [121–124]. Great progresses have been made to mitigate this efficiency droop: semiempirical modeling [125], compressive stressed substrates [126], InGaN barriers for active region [127], etc.

Katsushi Akita et al. characterized InGaN-based blue LEDs on GaN substrates with low TDDs and on c-plane sapphire substrates and revealed the advantages of using GaN substrates [128]. GaN substrates were grown by HVPE, and their TDDs were less than 1×10^6 cm^{-2}. The detail fabrication flows of LEDs were provided in Ref. [128]. The LEDs with 3-nm-thick QWs and 5-nm-thick QWs were fabricated and characterized. The indium compositions of these two types of QWs were designed to be 14% and 10%, respectively, so as to obtain the same emission wavelength of 450 nm. The conditions for the carrier localization of the QWs are expected to be different between the two LEDs.

Figure 3.20a, b shows the output powers and the EQEs of the LEDs with 3-nm-thick QWs (sample (a)) and 5-nm-thick QWs (sample (b)) on sapphire substrates as a function of forward current. Figure 3.20c, d shows the output powers and the EQEs of the LEDs with 3-nm-thick QWs (sample (c)) and 5-nm-thick QWs (sample (d)) on GaN substrates as a function of forward current. As shown in Fig. 3.20a, the output power of sample (a) does not increase linearly with increasing forward current. The EQE of sample (a) was 8.8% at 20 mA but decreased with increasing forward current and dropped to 5.6% at 200 mA. This phenomenon is typically observed in blue LEDs on sapphire substrates and indicates that the carrier localization is in play. In contrast, the EQE of sample (b) dropped drastically at 20 mA. The EQE increased gradually with increasing forward current, but it was lower than that of sample (a) at 200 mA. As shown in Fig. 3.20c, the current dependence of the output power of sample c was almost the same as that of sample (a). The EQE of sample (c) was as high as 8.3% at 20 mA. It decreased with increasing forward current and dropped to 4.9% at 200 mA. This phenomenon indicates that the carrier localization is in play in LEDs also on GaN substrates with low TDDs as well as on sapphire substrates and that nonradiative recombination centers (NRCs) unrelated to threading dislocations (TDs) exist in the active layers. In contrast, the output power of sample (d) increased almost linearly with increasing forward current. The EQE of the LED was as high as 7.9% at 20 mA and diminished only slightly with increasing forward current to 6.6% at 200 mA. The decrease of the EQE of the LED was suppressed in the case of sample (d). This suggests that the concentrations of NRCs are lower for QWs with smaller indium compositions. This is supported by the fact that the large decrease of the EQE at high current densities is not observed in the near-UV LED with QWs with smaller indium compositions in Ref. [129]. The output powers were 17 mW at 20 mA (12.5 A/cm^2) and 148 mW at 200 mA (125 A/cm^2) when sample (d) was mounted p-side down and molded with epoxy. The EQEs were 30% at 20 mA and 26% at 200 mA. This value is considerably high at such a high current density. On the sapphire substrate, the

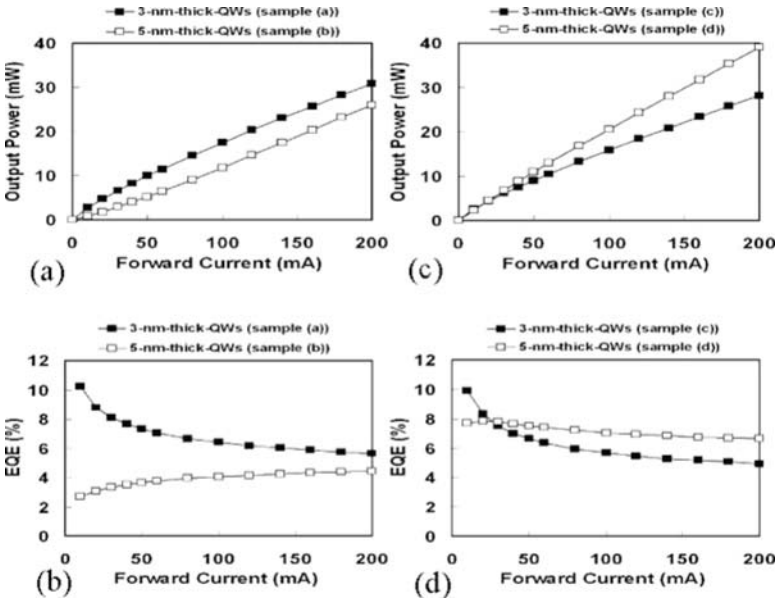

Fig. 3.20 (**a**) The output power and (**b**) the EQE of LEDs on sapphire substrates as a function of forward current; (**c**) the output power and (**d**) the EQE of LEDs on GaN substrates as a function of forward current [128]

EQEs were estimated 30% at 20 mA and 19% at 200 mA when sample (a) was mounted p-side down and molded with epoxy. Therefore, the use of GaN substrates in conjunction with thick QWs is a promising approach for fabrication of high power LEDs.

3.5 Light Efficiency Extraction

The total device efficiency of an LED is usually described as the external quantum efficiency (EQE). This figure of merit describes the efficiency of turning electrical carriers into photons. EQE can loosely be broken into internal quantum efficiency (IQE), injection efficiency, and extraction efficiency. The injection efficiency and IQE are largely a function of the crystal quality and electrical optimization of the LED structure. The extraction efficiency of a device describes the efficiency of the LED structure and packaging at removing photons generated in the active region of the device from the semiconductor material. It is known that the extraction efficiency of LEDs is limited by high refractive index contrast between the GaN (2.4) and air (1.0). The angle of the light escape cone is only 23°, which leads to a light extraction efficiency as low as 4.18% per crystal face [130]. For conventional LED on sapphire, smaller refractive index (1.78) and higher transparency of sapphire

compared to bulk GaN are favor of light extraction. In contrast, a considerable amount of downward light in homoepitaxial LED is absorbed by the FS-GaN substrate. Thus, the problems about extraction efficiency for the LEDs on FS-GaN are more serious than the counterpart on sapphire. Currently, it has been demonstrated that several methods are used to improve extraction efficiency in GaN based on FS-GaN substrate, such as etching roughness of N-Face GaN [131, 132], geometric die shaping [133–135], and photonic crystal (PhC) structures [136].

3.5.1 Surface Treatment Methods

The critical angle for photons to escape from GaN film is determined by Snell's law. The angle is crucially important for the light-extraction efficiency of LEDs. It has been demonstrated that changing surface of the backside GaN can be used to improve light-extraction efficiency in InGaN-based LEDs on GaN substrate. This can be understood that the effective index of the GaN film has been decreased. It means more photons which should be total reflected can escape from GaN film for improving the total light efficiency.

Yi-Keng Fu et al. fabricated nitride-based LEDs with a roughed backside GaN substrate by chemical wet-etching process. The results show that they can enhance the 20 mA output power by 95% and 29% from the near-UV LED and blue LED, respectively, compared with standard LEDs [132]. Hong Zhong et al. used ICP etching to pattern the backside of semipolar LEDs, and a substantial increase (100% before packaging and 33% after) in output power was observed at 20 mA drive current in comparison with a smooth backside reference sample [137]. Yuji Zhao et al. fabricated the first 30-mW-class semipolar blue light-emitting diode (LED) on a freestanding $(10\bar{1}1)$ GaN substrate by using microscale periodic backside structures [131]. The schematic structure of the device with the roughened backside is shown in Fig. 3.21a, while SEM images of the backside of the GaN substrate before (Fig. 3.21b) and after (Fig. 3.21c) backside roughening are also presented. A schematic graph (left) and an optical micrograph (right) of a working blue LED using this packaging method are shown as insets in Fig. 3.22. Room temperature (RT) electroluminescence (EL) measurements under pulsed conditions with a duty cycle of 1% were performed in an integrating sphere. Figure 3.22 shows the light output power vs current and external quantum efficiency vs current curves of the LED. At a forward current of 20 mA, the semipolar LED has an output power of 31.1 mW and an EQE of 54.7%. At 350 mA, the LED has a slightly lower EQE of 45.4% and an output power of 458 mW. The roughened devices demonstrated a better performance by having a sixfold increase of the output power after packaging, compared with a fourfold increase in the case of conventional devices mainly due to the dramatic enhancement of photon extraction from the backside of the substrate.

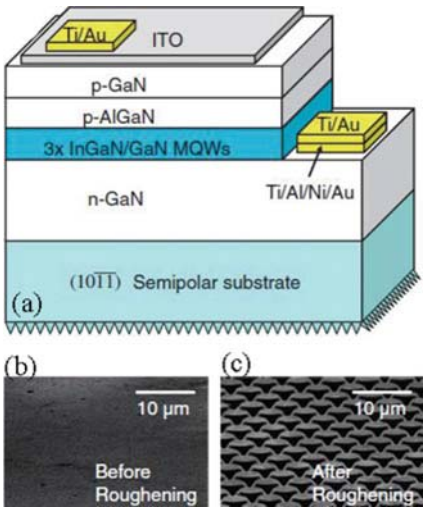

Fig. 3.21 (**a**) Schematic views of the semipolar $(10\bar{1}1)$ LED device with backside roughening structures. (**b**) SEM images of the backside of the GaN substrate before roughening and (**c**) after roughening, from a 10-tilted angle [131] (Copyright (2010) The Japan Society of Applied Physics)

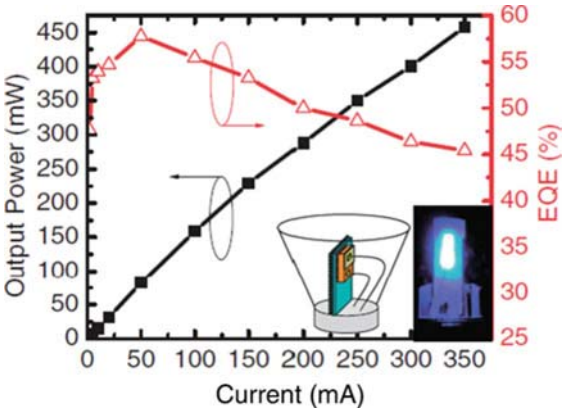

Fig. 3.22 Light output power vs current and external quantum efficiency vs current curves for a packaged $(10\bar{1}1)$ LED with backside roughening under pulsed conditions. Insets: Schematic graph (left) and optical micrograph (right) of a working blue LED using a transparent packaging method [131] (Copyright (2010) The Japan Society of Applied Physics)

3.5.2 Chip Shaping Method

Chip shaping is a method that has proven successful for material systems that are more fully mature than the nitrides [138]. Carefully designing the chip geometry of bulk GaN-based LEDs structure can improve the chances of light extraction for photons incident on device sidewalls. By breaking the lateral symmetry in a LED, conditions can be created such that each total internal reflection moves the photon path closer to being within the critical angle.

Bo Sun et al. realized a light extraction efficiency enhancement of bulk GaN light-emitting diodes (LEDs) in the shape of truncated pyramid. Compared with the reference LEDs, an enhancement of up to 46% on the light output power from rectangle-shaped LEDs chip with the inclination angle (~44°) has been observed. Compared with the common triangle-shaped and hexagon-shaped LEDs, large size

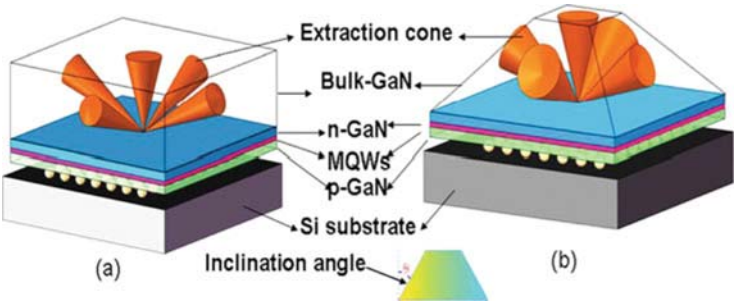

Fig. 3.23 Schematic diagrams of conventional flip-chip bulk-GaN LEDs (**a**) and truncated pyramidal-shaped flip-chip bulk-GaN LEDs (**b**) [134]

of conventional rectangular LEDs shaped with truncated pyramid shows more obvious enhancement in light extraction efficiency [134]. The schematic diagram of bulk-GaN LEDs with a truncated pyramidal shape was shown in Fig. 3.23.

Bulk-GaN LEDs have a relative large windows layer for light extraction in which the horizontal and vertical dimension is comparable. That means photons generated from multiple quantum wells have more chances to be scattered by sidewalls compared to conventional sapphire-based LEDs. However, for rectangular-shaped LED chip, the efficiency is still limited as light totally internally reflected at a semiconductor-to-ambient interface cannot change its incidence angle upon any of the facets. In case of a truncated pyramidal-shaped LED chip as shown in Fig. 3.23b, when light reflected from one facet to another, its incidence angle is changed. It means that light has several chances to escape from the LED chip which can then be extracted through top surface as well as the tilted sidewalls after considering Fresnel losses. The tilted sidewall also increases the light escape cones associated with the sidewalls and the same to the light escape cones related to the top surface. According the simulations, the light escape cones associated with the sidewall gradually enlarge with increasing the inclination angle. When the inclination angle was increased to 44°, the light escape cones associated with top surface and sidewalls start to overlap. Photo source emitted from QWs can be regarded as a dipole emitter, of which the normalized radiation patterns, given by the power per unit of solid angle, were a lambert-shaped (defined by $\sin^2\theta$ or $\cos^2\theta$). About 74% of dipole light power was confined in the 60° light cone, which means that the light extraction efficiency from sidewalls can be greatly enhanced if the light escape cone associated with the sidewall more merged in the dipole radiation patterns.

The L-I characteristics of truncated pyramidal-shaped bulk-GaN LEDs with different inclination angle and reference LEDs are shown in Fig. 3.24. The light output power of LEDs increased as the inclination angle enlarged from 0° to 30°; however, the light output power reached its maximum when the inclination angle increased to 44°; furthermore, a slight power reduced was found after the inclination angle enlarged to 50°. The experiment results are consistent with the simulation results. Compared with the reference LEDs, the LEDs with an inclination angle of

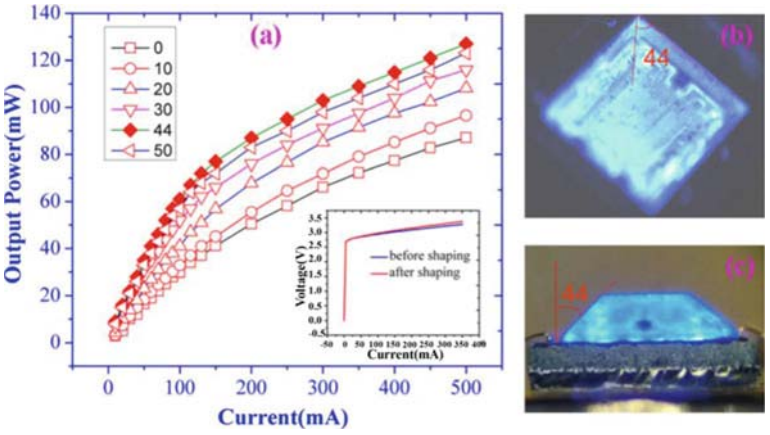

Fig. 3.24 (**a**) L-I characteristics of the truncated pyramidal-shaped LEDs (from inclination angle 0°–50°, respectively) and reference LEDs, and the insets show the $I-V$ curve of LEDs before and after laser shaping, (**b**) tilt view, and (**c**) cross-sectional view of optical micrographs of truncated pyramidal-shaped LEDs (with inclination angle 44°) at 5 mA injection current [134]

~44° have reached a larger enhancement of light extraction efficiency, up to 46%. The inset of Fig. 3.24 shows $I-V$ curve of LEDs before and after laser shaping. It can be found that the laser-shaping process does not cause undesirable damage to the LED chip. Figure 3.24b, c also shows the tilt view and cross-sectional view of optical microscopic images of the LED with an inclination angle of ~44° operated at an injection current of 5 mA. Light extracted among the four sidewalls can be easily observed.

In addition, it was found that compared to triangle-shaped and hexagon-shaped LEDs, large size of conventional rectangular LEDs shaped with truncated pyramid showed more significant improvement in light extraction efficiency. This could make the conventional rectangular bulk-GaN LEDs have a better improvement of external quantum efficiency even up to very high current densities just using the standard fabrication process.

3.5.3 Photonic Crystal Method

To enhance extraction of LEDs, photonic crystal (PhC) structures have drawn much attention, which could lead to efficiently coupling light from the dielectric-guided modes into air [139–142]. In addition to increasing the extraction efficiency of LEDs, periodic PhC structures have the ability to enhance the directionality, especially along the vertical orientation. Recently, Weisbuch et al. demonstrated two air-gap embedded PhCs, which created a waveguide with highly confined and

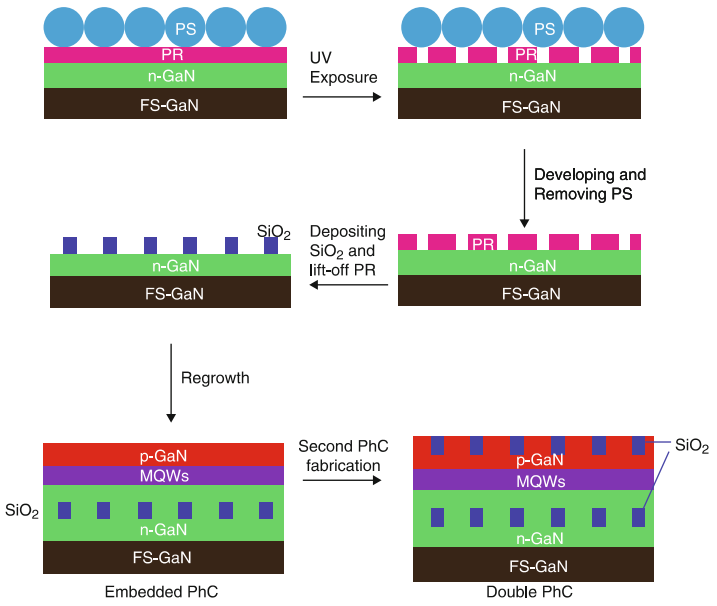

Fig. 3.25 Schematic illustration of the process for the fabrication of embedded PhC and double PhC LEDs. Reprinted with permission from Ref. [136], Optical Society of America

well-extracted mode while exhibiting no significant deleterious effects on the LEDs [143, 144].

Tongbo Wei et al. reported homoepitaxially grown InGaN/GaN light-emitting diodes (LEDs) with SiO_2 nanodisks embedded in *n*-GaN and *p*-GaN as photonic crystal (PhC) structures by nanospherical-lens photolithography. The introduction of SiO_2 nanodisks doesn't produce the new dislocations and doesn't also result in the electrical deterioration of PhC LEDs. The light output power of homoepitaxial LEDs with embedded PhC and double PhC at 350 mA current is increased by 29.9% and 47.2%, respectively, compared to that without PhC. The corresponding light radiation patterns in PhC LEDs on GaN substrate show a narrow beam shape due to strong guided light extraction, with a view angle reduction of about 30° [136].

Figure 3.25 shows the fabrication process flow for embedded and double SiO_2 PhC LEDs.

Figure 3.26a demonstrates the scanning electron microscope (SEM) image of cross-sectional view of the *n*-GaN laterally reovergrown over the SiO_2 nanodisks in the embedded PhC LED. It is noted that the SiO_2 nanodisks are fully surrounded by the GaN layer, without leaving the voids. The diameter, period and height of the embedded SiO_2 nanodisk are 400, 900 and 200 nm, respectively. According to the top view of PhC structure, there is a uniform hexagonal-lattice distribution of SiO_2 nanodisks as shown in Fig. 3.26b. Selectively regrowth of p-GaN with a thickness of 150 nm is carried out to fill the space between SiO_2 nanodisks. Furthermore, transmission electron microscopy (TEM) is employed to investigate

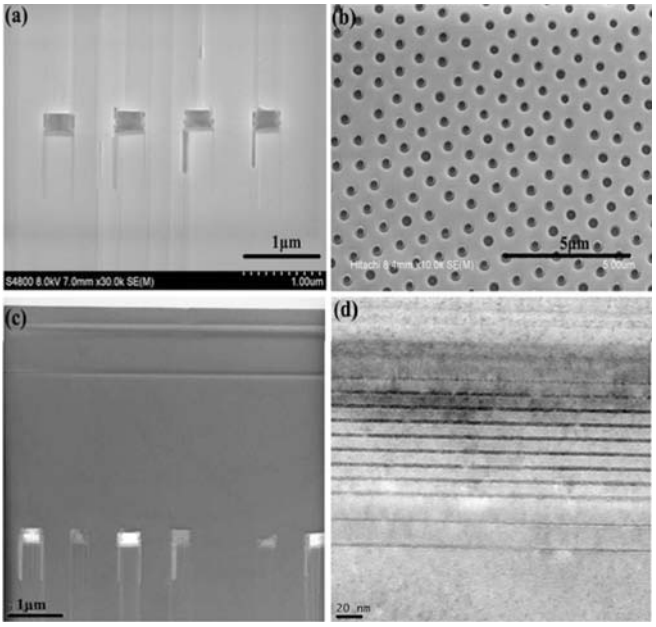

Fig. 3.26 (**a**) Cross-sectional view of embedded PhC of SiO_2 nanodisks surrounded by n-GaN and (**b**) tilted top view of p-GaN surface with top SiO_2 PhC structure. (**c**) Cross-sectional TEM image of the LED with embedded SiO_2 PhC (**d**) is the magnified region of MQWs from PhC LED in (**c**). Reprinted with permission from Ref. [136], Optical Society of America

the crystalline quality of GaN layers that are homoepitaxially grown on the SiO_2 PhC structure. As shown in Fig. 3.26c, d, almost no threading dislocations can be observed in both n-GaN and MQWs structures, implying the high-quality growth of GaN on FS-GaN substrate. In the epitaxial lateral overgrowth (ELOG) on sapphire, Wuu et al. reported the SiO_2 array could block the dislocation propagation, but new dislocations may be introduced in the lateral coalescence region during the second growth [145]. Unlike the heteroepitaxial growth, there are also no new dislocations formed on the SiO_2 nanodisks in the grown process.

The far-field emission patterns from the PhC LEDs show much smaller view angles but obvious enhancement in the overall integrated emission intensity. The light is further redirected to the top escape cone through the twice transmission of embedded and top SiO_2 arrays, resulting in the most significant focusing effect and more photon capable of escaping from the chips.

Bulk-GaN-based LEDs are attracting more and more attention since the first LEDs grown on bulk GaN substrates were reported by the UCSB group in 2005, due to the potential to fabricate high-power and high-efficiency devices. Over the past decade, many approaches to further improve the performance of native bulk-GaN-based LEDs have been demonstrated. Even though the developing technologies of GaN substrates are still on the way, their applications to LEDs have attracted much interest of community. Although these freestanding substrates still have

relatively high densities of dislocations and stacking faults, GaN-based LEDs were successfully realized by homoepitaxy on polar, nonpolar, and semipolar substrates, with the progresses in the improvements of internal quantum efficiency, engineering of light extraction, and suppressing the efficiency droop. The achievements in GaN LEDs will more and more clearly prove the great advantages and irreplaceability of GaN substrates. Along with the advance of GaN-freestanding substrates in decreasing the density of defects and lowering the cost of production, wider applications of GaN substrates in high-efficiency and high-power LEDs for solid-state lighting can be desirable, on condition that homoepitaxy technology is well developed and widely used.

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Chapter 4
GaN LEDs on Si Substrate

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4.1 Epitaxy of GaN LED on Si Substrate

4.1.1 Overview of GaN Epitaxy on Si

Substrate is the basis of GaN epitaxial growth, which has great impact on the crystal quality, the strain, the luminescence behavior, and the light extraction mode. To some extent, Si is not considered to be an excellent choice as the substrate for GaN epitaxy. Such a sense is mainly attributed to the mismatch in the lattice constant and the thermal expansion coefficient. As shown in Fig. 4.1, the lattice mismatch and thermal mismatch between GaN and Si (111) substrates are 16.9% and 57%, respectively, which are much larger than that of GaN/sapphire and GaN/6H-SiC. These factors lead to high dislocation density, film cracking, and wafer bending, bringing great challenge to the epitaxial growth of GaN.

There is great challenge but also great potential to grow GaN on Si substrate. Leaving the weak point aside, Si substrate gets many other attractive advantages. Firstly, the availability of Si wafers makes the substrate relatively cheap, and the cost goes down when the diameter gets larger. Benefiting from the development of microelectronic in semiconductor industry, the processing technology of Si-related materials is very mature, which makes the fabrication of LED device very flexible. And the LEDs can be also integrated into the microelectronic devices. Besides, the Si substrate has good thermal and electric conductivity, which is good to the

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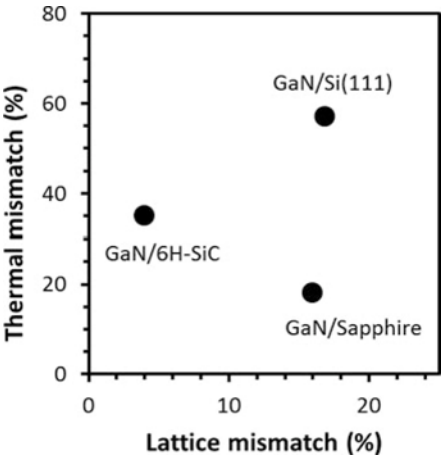

Fig. 4.1 The lattice and thermal mismatch of GaN epitaxy on different substrates

device reliability. Moreover, the large lattice and thermal mismatch between Si and GaN bring great opportunity to grow high-quality InGaN quantum wells. Once dislocation density and film cracking are under-controlled, the tensile-type thermal strain and lattice strain raised by the Si substrate will become positive factors for indium incorporation. Growth temperature can be enhanced to improve the quality of InGaN quantum wells (QWs).

Since the 1970s, when the first GaN on Si substrate was reported [1], great efforts on GaN/Si technology have been made by various researchers in order to industrialize the GaN LEDs on Si. But it took until 2009 for the first bright LED on Si substrate to be present [2]. And nowadays, the LEDs on Si substrate have already been commercially available and widely spread in our lives.

Then, what are the crucial technologies for GaN LEDs growing on Si substrates? Firstly, film-cracking problem must to be solved; otherwise the GaN epitaxy cannot be processed to devices. One of the approaches is to pattern the substrate into small grids via etching off grooves or growing dielectric strips. During the growth process, the region of the grooves or strips will not grow GaN, which acts as "cracks" on the wafer and helps to release stress. Moreover, the grid boundaries can localize the stress within small parts; even if there is a crack initiate at one of the grids, it will be isolated within the grid and not propagated to the entire wafer. Another approach to avoid cracking is to balance the thermal strain by lattice strain with the assistance of buffer. The buffer consists of multiple AlGaN layers with Al content gradually decreased from 100% to 0%. Lattice constant of AlGaN will increase as the Al content decreased, and compressive strain will accumulate within AlGaN film. Once the buffer layers grow thick enough, the compressive stain can compensate the tensile strain raised by the thermal mismatch and avoid film cracking.

Dislocation density in the GaN film also has great impact on the performance of LEDs. Direct growth of GaN on Si substrate results in high threading dislocation density up to 10^{10} cm^{-2}, which is useless for LED device. Epitaxial lateral overgrowth (ELOG) can be applied to reduce the dislocation density in GaN on Si substrate. An AlN layer was normally deposited on the Si substrate as the buffer. Upon that, island growth mode (3D) of GaN can be formed with the help of lattice

strain between GaN and AlN. And then lateral overgrowth can be conducted to coalescent the islands. The 3D-ELOG growth mode can effectively reduce the dislocation density to a magnitude of 10^8 cm^{-2}, which is comparable to that of GaN grown on sapphire substrate.

In this chapter, we will focus on the technologies of GaN LEDs on Si substrate, including substrate preparation, epitaxial growth, device fabrication, and device characterization. The unique techniques of GaN on Si will be introduced in detail, whereas the generic techniques will be briefly mentioned.

4.1.2 Buffer Technology

Among the planes in the lattice of Si, (111) plane is most suitable for GaN film growth because of its hexagonal symmetry favoring epitaxial growth of the GaN (0001) plane with wurtzite structure. The epitaxial relationship is GaN (0001) parallel to Si (111), GaN [11−20] parallel to Si [−110], and GaN [−1100] parallel to Si [11−2] [3].

The large difference in the lattice constants of GaN ($a_{GaN} = 0.3189$ nm) and Si ($a_{Si(111)} = 0.3840$ nm) yields a lattice parameter mismatch (16.9%) resulting in a high threading dislocation density (TDD) of 10^{10} cm^{-2}. Another severe problem is the large thermal dilatation mismatch between GaN and Si. The in-plane thermal expansion coefficient of GaN is 5.59×10^{-6} K^{-1} [4] as compared to 2.59×10^{-6} K^{-1} of Si, which leads to a large tensile stress during cooling from the growth temperature (about 1000 °C) to room temperature. The stress can be determined via the curvature of the sample which is proportional to the stress value [5]. Under typical MOCVD growth conditions, the stress amounts to 0.9 GPa μm^{-1} GaN [6]. The great tensile stress will cause cracking and a concave bending of the GaN/Si epi-wafer, which cause problems to device applications.

In order to obtain low TDD and crack-free GaN film on Si substrate, a suitable buffer layer is needed.

4.1.2.1 Thin AlN Buffer on Grid-Patterned Si Substrate

The challenges in using Si as the substrate are as great as the benefits. At the very beginning, it is necessary to appropriately treat the Si substrates to obtain the optimum state for growing high-quality GaN layer. The results presented in this section are based on Si (111) substrate.

The substrate orientation is usually oriented by an X-ray diffractometer; in the process of determining substrate orientation, cutting, and subsequent polishing, the error is introduced, so that the real surface of the Si substrate with the expected crystal surface has a certain deviation, and the degree of deviation is usually defined by the miscut angle. Research shows that the miscut angle of Si (111) substrate has a significant influence on the optical properties of GaN-based LED grown on it [7]. Of

course, the miscut angle closer to 0° is better, but taking the control of the substrate production into account, it is usually controlled within 0.3° [7].

The thickness of substrates has evident effect on the growth of GaN film and LED structure on Si. Usually, the thicker the substrate, the smaller is the amount of deformation of the epitaxial wafer during the entire epitaxial growth and cooling process, which will favor the control of the wavelength uniformity of LED structure. However, the increase in substrate thickness will add to the cost of the Si substrates and at the same time is not conducive to lift-off of the Si substrate when the vertical structure chip is fabricated, and therefore, the thickness of the substrate should not be too thick. For a 2 in.-patterned Si (111) substrate with a thickness of 0.43–1 mm, an epitaxial wafer with good wavelength uniformity can be obtained, whereas for a 6 in.-patterned Si (111) substrate, the thickness is typically chosen to be 1–1.5 mm. For un-patterned Si substrates, thicker substrates are often required in order to obtain LED films with crack-free and good wavelength uniformity.

Grid-patterned Si substrate (GPSS) fabrication is one of the key technologies for the selective area growth (SAG) on GPSS. The size of the unit patterns usually depends on the size of the chips to be obtained. Figure 4.2 shows a schematic view of a GPSS, in which Fig. 4.2a is a vertical view, and it can be seen that the Si substrate is divided into separate unit patterns by pattern boundary. There are two different approaches for pattern boundary, one is obtained by growing layer of dielectric film (such as SiN_x, SiO_2) and the other by means of photolithography to obtain the dielectric film boundary, as shown in Fig. 4.2b, and another method is etching trenches on the Si substrate by photolithography as shown in the sectional view of Fig. 4.2c. Since such a boundary is amorphous, no oriented crystalline seed layer can be grown on it during the process of growing GaN; the GaN thin film is also divided into separate cell patterns, which greatly reduces the thermal stress between the GaN thin film and the substrate. By using the above two types of boundary, a high-quality GaN film can be obtained.

Before loading the substrates, it is necessary to clean the Si substrate, which typically consists of two parts. The first part refers to the wet cleaning prior to being placed in the MOCVD reaction chamber. This process is usually done using the typical Si substrate cleaning technology widely used in the IC industry and will not be repeated here. The second part refers to the dry cleaning in the MOCVD reaction chamber. The purpose of this process is to remove the native oxide layer on the surface of the Si substrates and obtain a flat surface suitable for epitaxial growth. Figure 4.3 shows two atomic force microscope (AFM) images of the Si (111) substrate after being polished, wet cleaned, and dry cleaned in the MOCVD reaction chamber. As can be seen from Fig. 4.3a, large amount of scratches present on the surface of the Si (111) substrate after polished and wet cleaned. Such a surface is not suitable for obtaining a high-quality epitaxial film. The scratches on the surface of the Si (111) substrates disappear, and the step flow occurs as a result of dry cleaning in the reaction chamber (usually at a substrate temperature (1100 ± 100) °C in H_2 atmosphere); the root mean square (RMS) of surface roughness is also reduced from 0.583 to 0.178 nm (10 μm × 10 μm range), which creates good surface conditions for subsequent epitaxial growth.

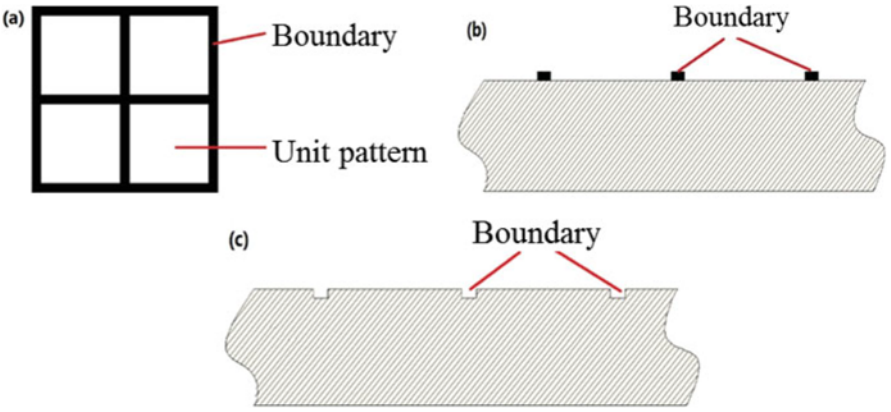

Fig. 4.2 Scheme for patterned Si substrate in (**a**) vertical view, (**b**) sectional view of Si substrate with dielectric film boundary, and (**c**) sectional view of Si substrate with trench boundary

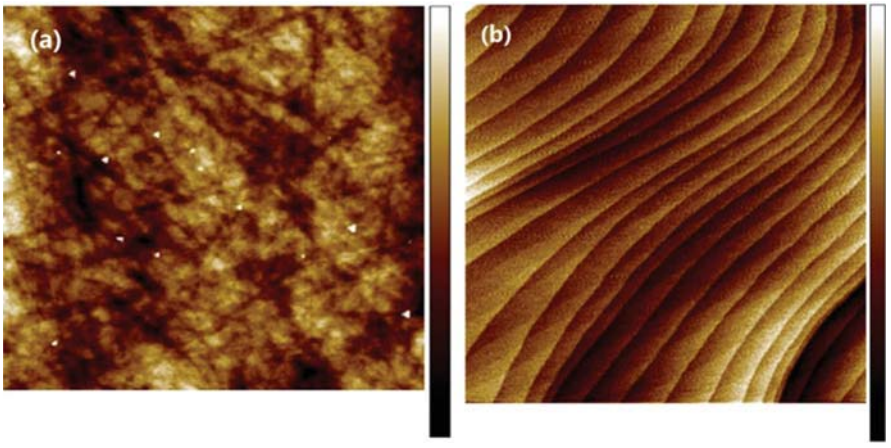

Fig. 4.3 AFM images of polished and wet-cleaned Si (111) substrate surface (10 μm × 10 μm scanning area). (**a**) Before dry cleaning in MOCVD, RMS = 0.583 nm; (**b**) after dry cleaning in MOCVD, RMS = 0.178 nm

When GaN is grown on Si substrates directly, Si surface easily reacts with NH_3 to form SiN_x. GaN single crystal cannot grow on this layer [8], and the Si substrate reacts with metal Ga to form so-called Ga melt-back etching phenomenon [9], resulting in macroscopic defects on the surface of the epitaxial wafer as shown in Fig. 4.4. In order to overcome the above problems, researchers introduced an intermediate layer or buffer layer between the GaN and the Si substrate to prevent the GaN from directly contacting with the Si substrate or to avoid the formation of SiN_x on the surface of the Si substrate by employing an intermediate layer without NH_3. These buffer layers include 3C-SiC [10], AlAs [11], γ-Al_2O_3 [12], BN [13], and so on. Although these buffer layers can solve the problems, these usually require

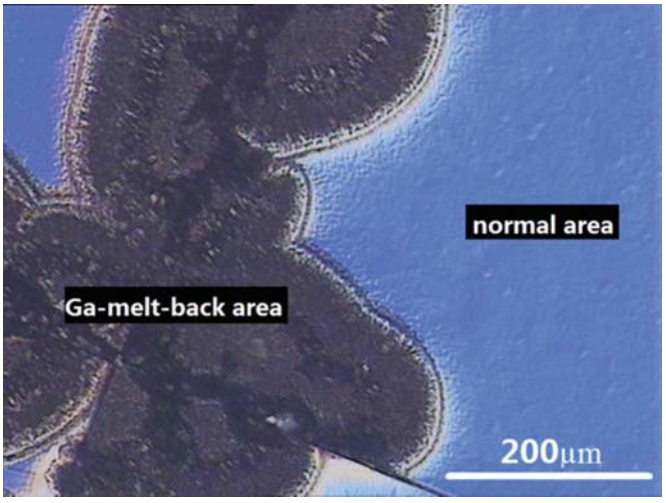

Fig. 4.4 Ga melt-back defects formed by reaction between Ga and Si substrate

a two-step epitaxy growth, which complicates the growth process. In contrast, AlN is an ideal intermediate material; a good coverage of AlN on the Si substrates surface cannot only serve as seed layer or nucleation layer to prevent the melt-back etching but also facilitate the subsequent growth of GaN [14]. Al and Ga belong to the group III, which can grow GaN without two-step epitaxial growth. Moreover, in comparison with the bond formation of Si–N, Al and N atoms tend to bond together much easier, which can avoid the formation of SiN_x polycrystalline layer.

As early as 1993, H. Amano et al. succeeded in using AlN as the intermediate layer to obtain a single crystal GaN film [15]. However, it was not mentioned in Amano's report how he solved the problem of NH_3 reaction with Si substrate (AlN growth required NH_3). It was not until 2000 that Khan clearly stated in his study that a few monolayers of metallic aluminum (Al) were deposited on the Si substrate prior to the growth of the AlN intermediate layer, which is believed to be useful for accelerating the subsequent AlN growth mode transferring from three-dimensional (3D) island growth to two-dimensional (2D) film growth [16, 17], thereby cleverly addressing the reaction of NH_3 with the surface of the Si substrate and Ga melt-back etching problem. This is very necessary to the following growth of high-quality GaN [14]. It was proved in both MBE [14, 17, 18] and MOCVD systems [16, 19, 20]. Much work had been paid in studying AlN growth temperature, V/III ratio, and suitable thickness [15, 21–23].

As mentioned above, GaN grown on Si shows a large mismatch dislocation density, usually $>10^{10}$ cm^{-2} (edge, screw, and mixture), due to the large lattice mismatch between the two materials. Therefore, reducing the dislocation density is a key technology for growing GaN films on Si substrates. Epitaxial lateral overgrowth (ELOG) is an important technique to reduce the dislocation density and

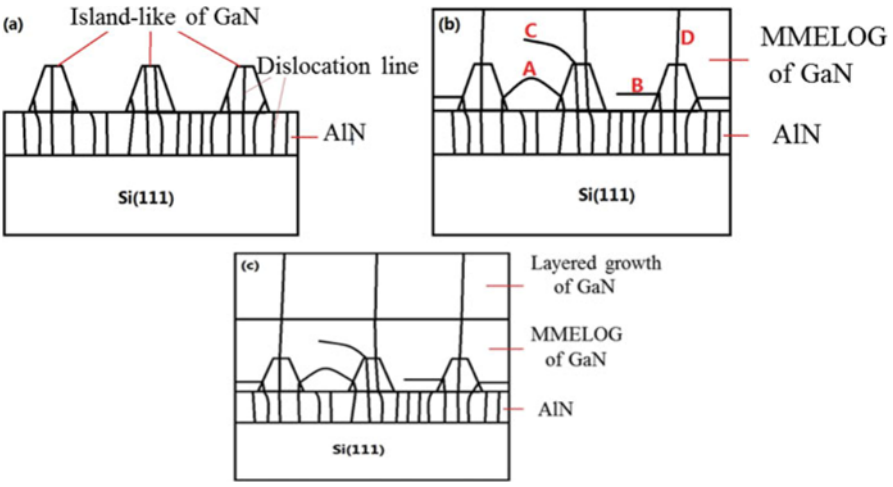

Fig. 4.5 Scheme for reducing the dislocation density of GaN film on Si substrate achieved by MMELOG in which the black lines represent dislocation lines. (**a**) Formed island-like GaN nucleation layer, (**b**) island-like GaN by means of MMELOG and then combined into a whole, (**c**) layered growth of GaN film with low dislocation density

is widely used in the growth of GaAs, InP, GaN, and other materials [24]. Threading dislocations can be blocked at the hetero interface. In 1999, Kung grew GaN on Si substrates by using ELOG technology [25, 26]. Honda et al. [26] and Dadgar et al. [27] also successfully grew GaN films on Si substrates by SAG technique and ELOG technique, respectively.

Jiang et al. [7] proposed a method to reduce the dislocation density of GaN films on Si substrates by referring to ELOG technology, which is called "maskless micro epitaxial lateral overgrowth technology (MMELOG)." Here, "maskless" refers to the fact that there is no need to growing masks (conventional ELOG needs to be fabricated before growth), while "micro" means a much smaller lateral epitaxial scale than the conventional ELOG. This method is described in detail below. Figure 4.5 shows a schematic representation of this technique: (1) growing AlN buffer layer on Si (111) substrate; (2) forming a "GaN island-like nucleation layer" on the AlN buffer layer; (3) the "nucleation layer" keeps on growing up, called the 3D GaN layer; and (4) growth combine layer, through the ELOG process 3D GaN layer, will be merged into a GaN layer with flat surface.

As shown in Fig. 4.5a, in the vertical direction, only a portion of the threading dislocations (TDs) extends from the AlN buffer layer to GaN island, thus reducing the dislocation density within GaN layer. Notably, the density of the GaN island (the number of islands per unit area) and the size (the area where the GaN island is in contact with AlN) have a significant effect on the TDs extending from the AlN buffer layer to the GaN island. The smaller the density and size of GaN is, the lower the dislocation density in the GaN island will be. However, the density of GaN is

too small and will not be conducive to the subsequent merge of ELOG into a whole. Therefore, proper GaN density and size are needed to be controlled. The distance between the GaN islands is usually controlled in the range of 0.5–2 μm, and the size of the islands is in the range of 1–5 μm. In addition to the growth conditions of the GaN island layer itself, the state of the AlN layer is also an important factor in the control of the GaN island. Generally, the smoother the surface of the AlN is, the higher the qualities of the crystal are, and in the island-like pattern, GaN is easier to grow. In general, small V/III ratio (usually <500), high pressure, and high temperature easily make GaN to grow in accordance with island-like patterns.

It is possible to achieve MMELOG on the island of GaN, mainly due to the large lattice mismatch (2.47%) between AlN and GaN, just because the existence of large lattice mismatch that provides a high surface energy prevents GaN from growing on AlN. Therefore, subsequent GaN will choose to grow on homogeneous GaN islands, and then coupled with the appropriate GaN growth conditions, ELOG of GaN can be achieved. At this point, the most important condition for ELOG is the large V/III ratio, usually reaching more than 2000. In the process of ELOG, the dislocations in the island of GaN will change or interact with each other. For example, two dislocations react with each other and disappear (shown in red letter A in Fig. 4.5b), dislocation lines turn parallel to the growth surface (shown in red letter B in Fig. 4.5b), dislocation lines divert in a certain direction (shown in red letter C in Fig. 4.5b), and dislocation lines extend along the growth direction (shown in red letter D in Fig. 4.5b). In this case A, B, and C correspond to the decrease of the dislocation density in the subsequent layer, and as shown in Fig. 4.5c, only the dislocation of D case will remain in the GaN epitaxial layer. The evolution mechanism is based on the results observed by transmission electron microscope (TEM), and the results will be given later. With regard to the evolutionary mechanism of dislocations in the ELOG process, previous study of GaN ELOG has been reported [24–30], thus no longer go into much detail here.

Figure 4.6 shows TEM photographs of GaN film with crack-free and low dislocation density obtained on Si (111) substrate, using a 100-nm-thick AlN buffer layer. As can be seen from Fig. 4.6a, in the AlN layer, there exist a large number of dislocations where white lines in the figure represent dislocation lines (dislocation density $>10^{10}$ cm^{-2}), and after island-like growth and MMELOG, GaN dislocation density is reduced, 10^8 cm^{-2} order of magnitude. Figure 4.6b–d are partial enlarged views of Fig. 4.6a, where the red letters of A, B, and C in the figure represent three kinds of dislocation evolution of A, B, and C given in Fig. 4.5b, respectively. In order to show the reduction of GaN dislocation density by the island-like growth and MMELOG mode more intuitively, we have prepared a sample of GaN grown directly on AlN layer. The TEM photograph was shown in Fig. 4.6e. The dislocations in AlN buffer layer in Fig. 4.6e extend extensively to the upper GaN layer, so that the dislocation density within the GaN layer is quite high compared to the large drop in the AlN/GaN interface in Fig. 4.6a.

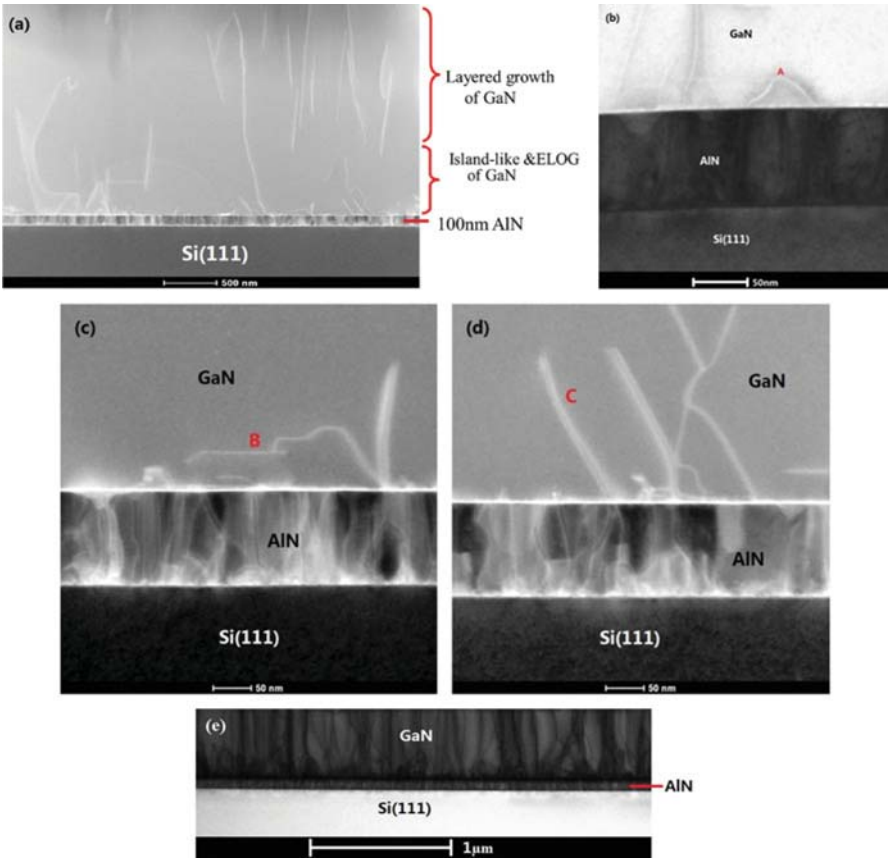

Fig. 4.6 TEM image of GaN film on Si substrate with a 100 nm AlN buffer layer. (**a**) High-quality, low dislocation density GaN film grown on the AlN buffer layer using island-like growth and MMELOG technology, (**b**) example of evolution mechanism of A class dislocation in Fig. 4.5, (**c**) example of evolution mechanism of B class dislocation in Fig. 4.5, (**d**) example of evolution mechanism of C class dislocation in Fig. 4.5, (**e**) high dislocation density GaN film grown directly on the AlN buffer layer

After the first reduction of GaN island-like growth model and the second reduction of MMELOG process, the dislocation density decreased by two orders of magnitude, from 10^{10} to 10^{8} cm^{-2}. Using this technique, GaN with (002) and (102) plane double-crystal rocking curve are obtained at half peak width of 230 arcsec and 330 arcsec, respectively. The GaN film is further flattened by subsequent layered growth (also known as 2D growth), which provides a good surface condition for the subsequent growth of the LED structure. Figure 4.7 shows the AFM morphology of the GaN surface after the growth of the layered GaN. The surface roughness RMS was 0.148 nm.

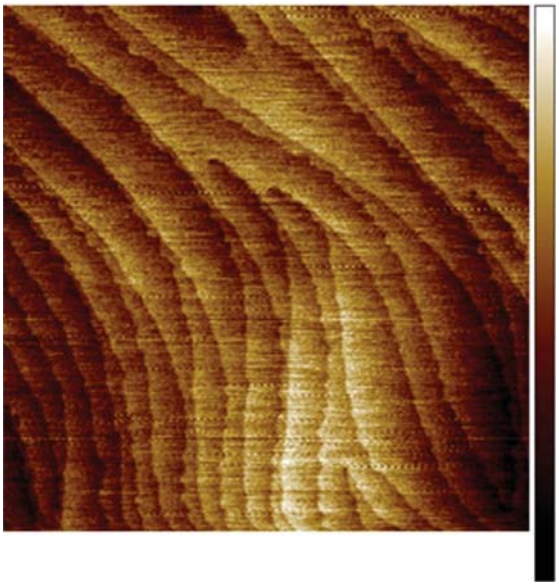

Fig. 4.7 AFM image of GaN film on Si substrate achieved by MMELOG with a 100 nm AlN buffer layer RMS = 0.148 nm (2 μm × 2 μm scanning area); the thickness of GaN film is 3.2 μm

4.1.2.2 Graded AlGaN Buffer on Bare Si Substrate

Despite the lattice mismatch of GaN with sapphire substrates, the two-step growth technique [31] can realize a high-quality GaN film normally under a compressive strain because the coefficient of thermal expansion (CTE) of sapphire is larger than that of GaN (Fig. 4.8a), giving a relatively broad process window with little risk in micro-crack formation. Epitaxial growth of GaN-based LEDs on large diameter Si substrates has a great potential in significantly reducing the LED manufacturing cost for energy-efficient solid-state lighting. This epitaxial integration, however, was hindered by two major technological challenges. The 16.9% lattice mismatch between GaN and Si normally causes a high density (10^9–10^{10} cm^{-2}) of threading dislocations (TDs), often working as non-radiative recombination centers and hence deteriorating the LED efficacy [32]. Due to the huge CTE misfit (57%), Si substrates after the epitaxial growth lag behind GaN in wafer shrinking during the cooldown from growth temperature and effectively stretch the GaN film, which may lead to tensile stress, wafer bowing, and micro-crack network formation in the GaN layer (Fig. 4.8b) [33]. It should be mentioned that even the strong residual tensile stress in the nominally crack-free GaN-on-Si LED epitaxial wafers right after the growth still can often induce micro-cracks under device operation over time, causing carrier leakage, light output decay, and other reliability issues.

In order to avoid the formation of micro-crack network in GaN epitaxial film grown on bare Si substrates, various buffer and/or AlN interlayers have been inserted between GaN and Si. The positive lattice mismatch of +2.4% between GaN ($a = 0.3189$ nm) and AlN ($a = 0.3112$ nm) can be utilized in the Al-composition-graded AlGaN/AlN buffer layers to build up enough compressive strain in the GaN

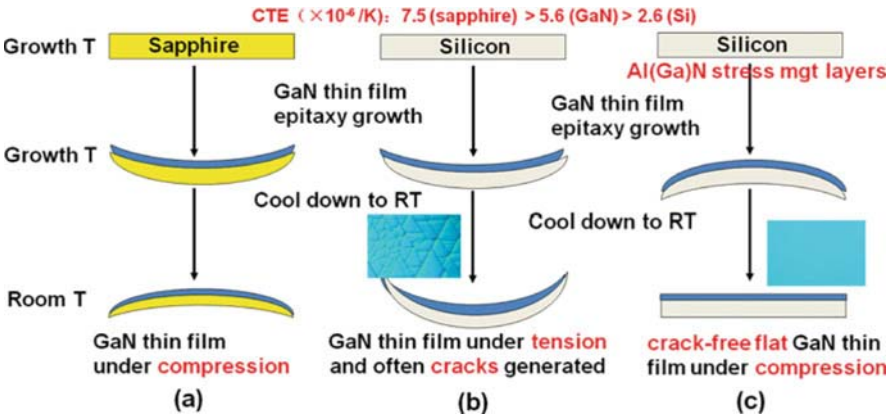

Fig. 4.8 Schematic diagram of the stress evolution during growth and cooldown of GaN film grown on sapphire (**a**), and Si substrates without (**b**) and with (**c**) Al-composition-graded AlGaN/AlN buffer layers

film at epitaxial growth temperature, for the compensation of the tensile stress induced by the CTE difference during the cooldown process [34, 35]. With a five-step-graded AlGaN/AlN multilayer buffer (Fig. 4.10a), crack-free GaN film (Fig. 4.9d) with an edge crack length shorter than 0.5 mm was obtained on Si (111) substrates.

It was found that the compressive strain built up within the Al-composition-graded AlGaN/AlN buffer layers could not only be used to compensate the tensile stress due to the CTE mismatch during the cooldown but also induce the inclination and annihilation of threading dislocations (TDs) at the interfaces according to the cross-sectional TEM observation (Fig. 4.9a, b). The full width at half maximum (FWHM) of GaN (0002) and (10-11) double-crystal X-ray rocking curves (XRCs) for the as-grown 2-μm-thick crack-free GaN film on Si (111) with a five-step-graded AlGaN/AlN multilayer buffer were 475 and 1147 arcsec, respectively (Fig. 4.10c, d), which, however, were still substantially larger than those of GaN grown on sapphire substrates. It should be mentioned that the large difference between the GaN (0002) and (10-11) XRCs FWHMs reflected a high density of edge-type dislocations, which are normally non-radiative recombination centers in LEDs. It is essential to reduce the edge-type TD density for the realization of high-efficacy LEDs grown on Si substrates.

Meanwhile, it was noted that there was a strong interplay between the defect engineering and the stress management for GaN growth on bare Si substrates. The inclination of existing edge TDs (Fig. 4.9c) effectively generates in-plane misfit dislocation segments, which result in a partial relaxation of the built-up compressive strain within the AlGaN/AlN multilayer buffer and the GaN overgrown layer [35–37]. A partial strain relaxation of the AlGaN/AlN multilayer buffer and the GaN epitaxial layer was clearly revealed by the displacement of their reciprocal lattice points (RLPs) along the Qx direction (not exactly aligned along the Qz

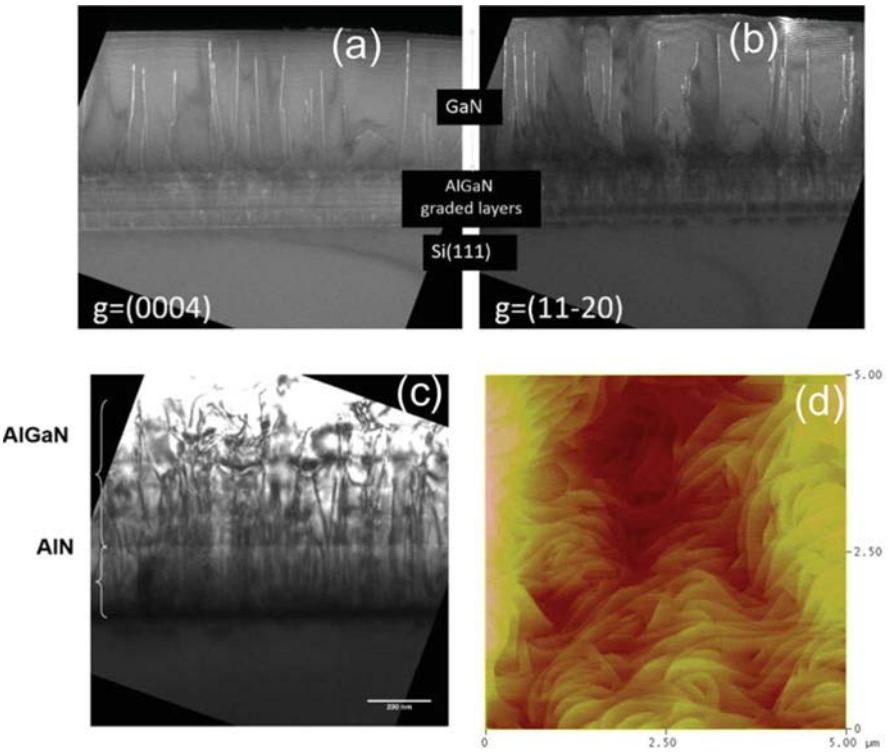

Fig. 4.9 Dark-field two-beam cross-sectional TEM images of GaN grown on Si (111) with a five-step-graded AlGaN/AlN buffer under a diffraction condition of (**a**) $g = 0004$ and (**b**) $g = 1120$, (**c**) bright-field TEM of the five-step-graded AlGaN buffer layers, (**d**) AFM image of the as-grown GaN surface with a root mean square roughness of 0.56 nm

direction) [35] in the (1124) X-ray reciprocal space mapping (RSM) (Fig. 4.10b). The inclination of TDs cancels out some compressive strain and may facilitate the formation of micro-cracks, which renders a limited thickness for crack-free GaN film grown on Si substrates. Therefore, it is also critical to reduce the edge-type TD density during the growth of GaN on Si for stress control.

It was observed that in AlGaN/AlN material system, greater lattice-mismatch compressive strain promotes larger angle bending of TDs [36, 37]. In the aforementioned five-step-graded AlGaN/AlN buffer structure [35] and other groups' reports [34, 38], typically a series of high Al-composition AlGaN layers (having a limited lattice mismatch with the underlying AlN layer) were firstly deposited on AlN/Si but gave little contribution to the TD bending/reduction and compressive strain accumulation. For instance, there is only 0.48% lattice mismatch between AlN and $Al_{0.80}Ga_{0.20}N$, which makes the TD bending at a small angle, and most of the TDs still propagate into the upper layers, contributing a broad XRC for GaN (10-11) diffraction.

Based on the understanding about the lattice mismatch, TD reduction, and strain relaxation, Sun et al. revised and simplified the design of the AlGaN/AlN

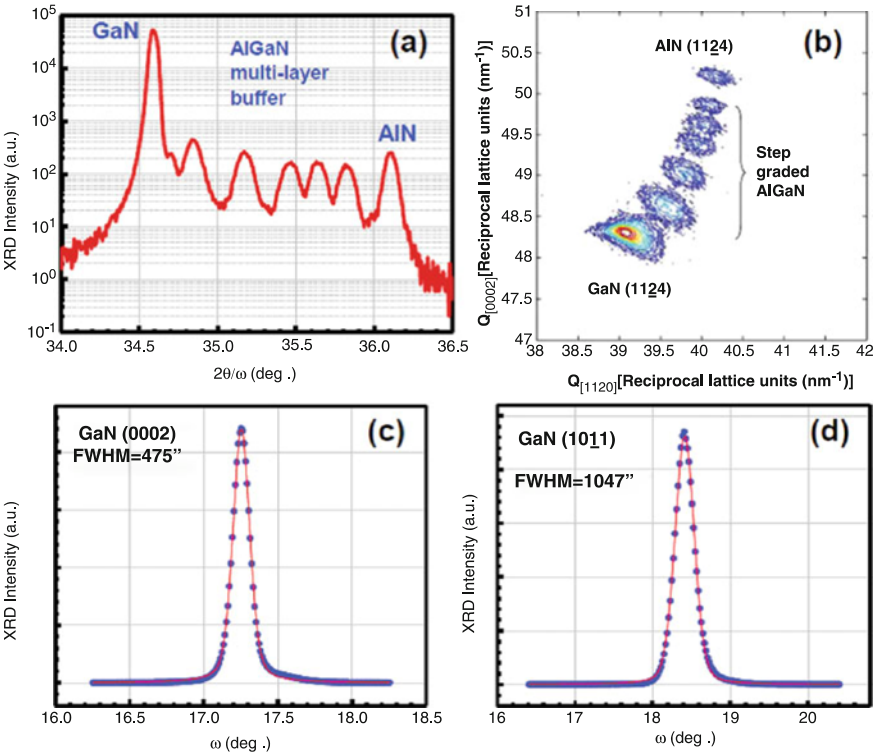

Fig. 4.10 (**a**) (0002) $2\theta/\omega$ scan of GaN grown on Si(111) with a five-step-graded AlGaN/AlN buffer, (**b**) reciprocal space mapping of the as-grown structure measured in an off-axis (1124) configuration, (**c**) double-crystal X-ray rocking curves of GaN (**c**) (0002) and (**d**) (10-11) diffractions

multilayer structure for the growth of crack-free high-quality GaN on Si substrates [39]. By eliminating the high Al-composition AlGaN layers, Sun et al. grew $Al_{0.35}Ga_{0.65}N$ as the first AlGaN layer in direct contact with AlN on Si. An increased compressive strain within the AlN/$Al_{0.35}Ga_{0.65}N$ structure, induced by the 1.6% lattice mismatch, facilitates the TDs bending at a larger angle, as well as their annihilation through dislocation interaction. With a greatly reduced TD density, compressive strain can be built up more effectively during the subsequent growth of $Al_{0.17}Ga_{0.83}N$/GaN for the compensation of tensile stress due to the CTE mismatch during the cooldown, resulting in a crack-free high-quality GaN film on Si. According to the TEM observations (Fig. 4.11a, b), from the AlN nucleation layer, through the $Al_{0.35}Ga_{0.65}N/Al_{0.17}Ga_{0.83}N$ buffer layers, to the GaN thick layer, a substantial portion of TDs were filtered out, and the crystalline quality was improved remarkably (Fig. 4.11c). And the as-grown high-quality GaN film on Si showed an atomically smooth surface featured with a step-flow morphology (Fig. 4.11d), which was distinctly different from that of the defective GaN grown on Si

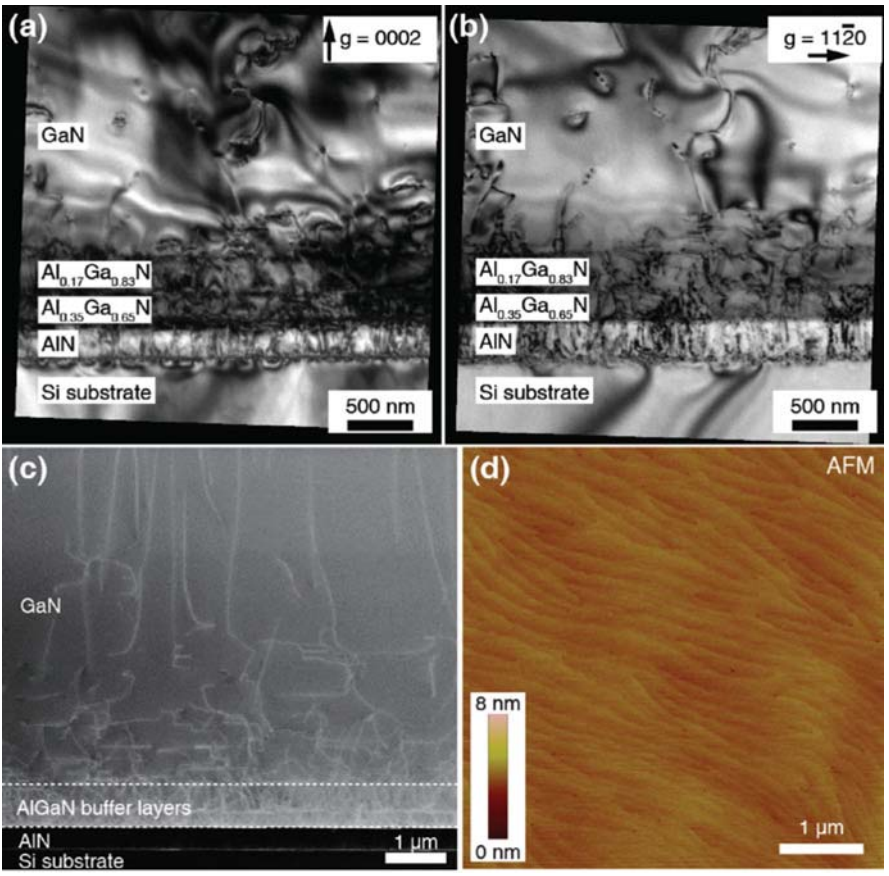

Fig. 4.11 Cross-sectional weak-beam bright-field TEM images of GaN grown on Si with an Al0.17Ga0.83N/Al0.35Ga0.65N/AlN buffer, obtained with (**a**) $g = 0002$ and (**b**) $g = 1120$, revealing TDs with screw and edge components, respectively. (**c**) Cross-sectional high-angle annular dark-field scanning TEM image of GaN grown on Si. (**d**) AFM image of the surface of this GaN film grown on Si, showing a step-flow surface morphology with a root mean square roughness of 0.19 nm

with a five-step-graded AlGaN/AlN buffer (Fig. 4.9d). The surface step pinning by the TDs was substantially suppressed for the high-quality GaN with a reduced TD density.

The crystalline quality of the as-grown GaN film on Si with an $Al_{0.17}Ga_{0.83}N/Al_{0.35}Ga_{0.65}N$/AlN buffer was also evaluated by DCXRC measurements in a skew symmetric geometry. The full width at half maximum (FWHM) of (0002), (2021), (2023), and (101 m) ($m = 1$, 2, 3, 4, and 5) DCXRCs for 3.6-μm-thick n-type GaN (Si doping 8×10^{18} cm^{-3}) grown on Si was all below 300 arcsec (Fig. 4.12a, b), indicating a low density of edge TDs [40, 41]. It's noted that edge TDs as NRCs are more detrimental to IQE than screw and mixed ones [42]. The TD density

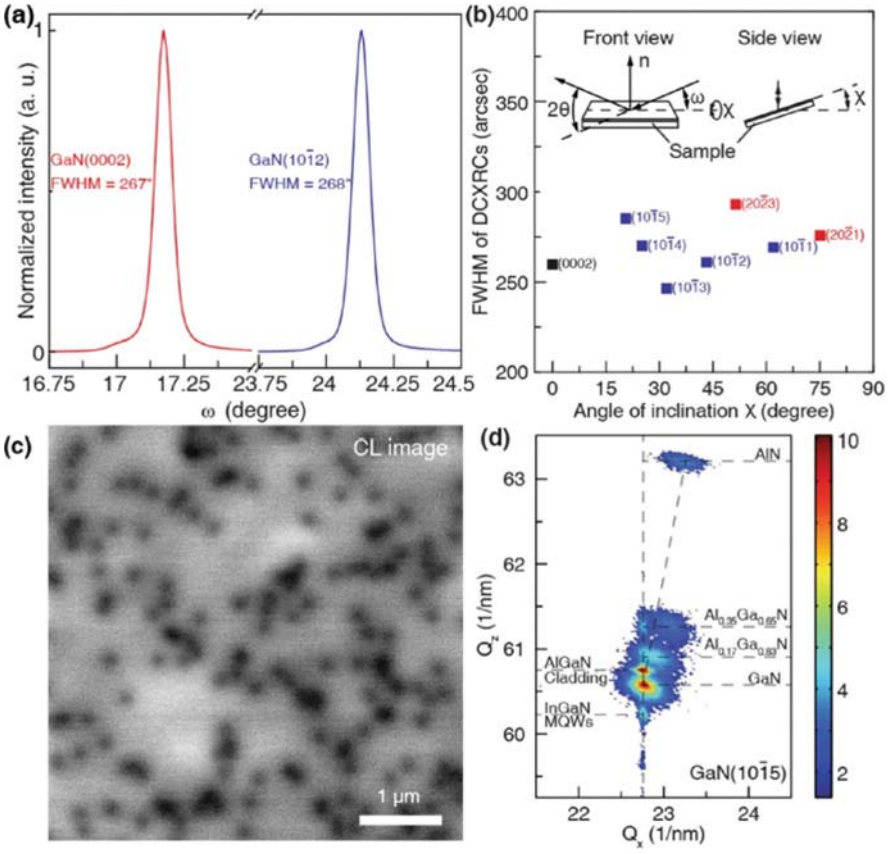

Fig. 4.12 (**a**) Double-crystal X-ray rocking curves of the high-quality GaN grown on Si around the (0002) and (10-12) diffractions. (**b**) FWHM of DCXRCs taken from a series of skew reflections at an increasing angle χ with respect to the (0001) plane for a 3.6-μm-thick n-type GaN (Si doping at 8×10^{18} cm^{-3}) grown on Si. The insets are schematic diagrams illustrating the inclination angle χ. (**c**) Panchromatic CL image of the high-quality GaN film grown on Si. The density of the dark spots, representing the TD density in the GaN film grown on Si, is about 5.8×10^{8} cm^{-2}. (**d**) RSM of GaN heterostructure grown on Si measured around (1015) asymmetric reflection

in the as-grown GaN-on-Si film was estimated to be around 5.8×10^{8} cm^{-2} based on the dark spot density in the panchromatic cathodoluminescence (CL) image (Fig. 4.12c). The as-grown GaN-on-Si template provides a high-quality material platform for the subsequent coherent growth of highly efficient InGaN/GaN multiple quantum well (MQW) active region, as evidenced by their vertically aligned RLPs along the Qz direction with respect to the GaN RLP in the (1015) RSM (Fig. 4.12d).

4.1.3 Quantum Well Strain Engineering

Similar to the growth of GaN on Si substrate, growth of the quantum well (QW) encounters the same problem, as there exists lattice mismatch between the InGaN well and GaN barrier. The lattice parameter of InN a-axis is 0.3548 nm, which has 10% lattice mismatch compared with GaN. For InGaN QW, the value of mismatch is 2–3%.

The large lattice mismatch will directly lead to the decrease of the crystal quality, such as producing new dislocations and causing indium segregation. On the other hand, it will introduce huge compressive stress to the quantum wells. X-ray diffraction measurement shows that InGaN quantum well (3 nm) is almost completely strained along the a-axis, so that the InGaN would suffer from the compressive stress of GaN. The asymmetry of the wurtzite structure of GaN in the c-axis direction leads to the existence of spontaneous polarization and piezoelectric polarization electric field; according to the strain of InGaN, one can calculate the QW which exists in the huge pressure field, up to 1 MV/cm, and the electric field will distort the band structure and cause serious band bending.

If the band is bent and the carrier is injected into the quantum well, it is separated rapidly by the piezoelectric field. The electrons are concentrated and trapped near the p side, and the hole is concentrated near the n side. Carrier separation occurs, and the overlap of the wave functions becomes smaller, which leads to the increase of carrier radiative recombination lifetime and lowers the radiative recombination rate and the efficiency of LED. Reduction of radiative recombination efficiency will make the carrier accumulation in quantum wells, as the carrier depletion rate is lower than the injection rate, thereby further causing carrier overflow and Auger recombination and reducing the luminous efficiency of LED. In addition, the presence of stress will also affect the indium incorporation during the epitaxial growth.

To summarize, the key issue to enhance the efficiency of LED is to reduce the stress in the QWs, which is beneficial to both material growth and device performance. One of the approaches is to grow AlInN or AlInGaN as the barrier to make its lattice parameter the same as InGaN well. As illustrated in Fig. 4.13, despite the bowing factors, for a blue LED with $In_{0.2}Ga_{0.8}N$ QW, if we grow $In_{0.2}Al_{0.8}N$ as the barrier, the lattice constant of a-axis is the same as the QW, while the barrier potential is higher than that of GaN as the barrier.

Using $Al_xGa_yIn_zN$ quaternary alloy as the barrier which can also achieve the effect, Table 4.1 lists the different composition and corresponding bandgap energy (without considering the bowing factors) of $Al_xGa_yIn_zN$ barrier matched with $In_{0.2}Ga_{0.8}N$ well to achieve the same lattice constant. Considering the carrier localization effect not worse than GaN, the Al composition must be set to at least 30%. Theoretically, these are good methods to release stress, but it is difficult for material growth, mainly attributed to opposite growth behavior of AlN and InN. For AlN which is easy to pre-react, the suitable growing conditions are low pressure, small V/III ratio, and high temperature, whereas InN, which is easy to decompose,

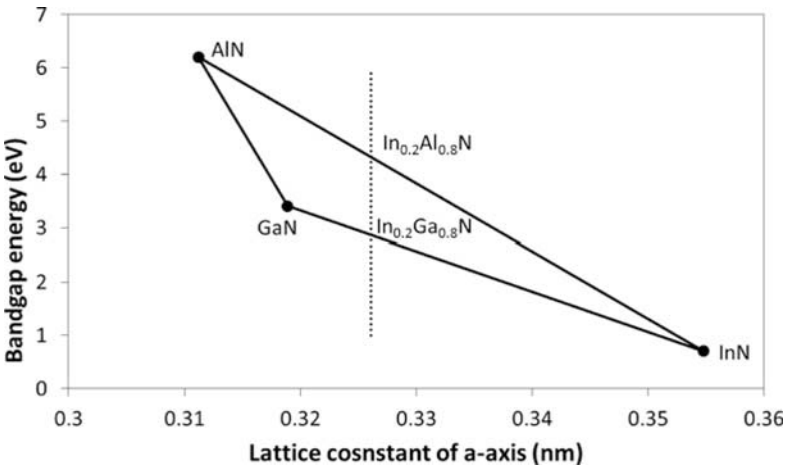

Fig. 4.13 Schematic diagram of lattice-matched InGaN and InAlN

Table 4.1 Calculated composition and bandgap energy of $Al_xGa_yIn_zN$ barrier matched with In0.2Ga0.8N well

x	y	z	Bandgap energy (eV)
0.10	0.68	0.22	3.08
0.20	0.56	0.24	3.30
0.30	0.44	0.26	3.53
0.40	0.31	0.29	3.75
0.50	0.19	0.31	3.97

is suitable to grow under high pressure, high V/III ratio, and low temperature. The antagonistic growth conditions of the two materials bring great difficulty in growing high-quality AlInN or AlGaInN materials. Thus to grow lattice-matched barrier is not a practical way to relax strain within the QWs.

A common way to relax strain of QW is to insert a layer or multiple layers of InGaN with relatively low indium content, after n-GaN and before the QWs. Such a layer is often called as pre-strain layer. The purpose of growing pre-strain layer is to partially relax the strain form n-GaN with the help of its indium content, which makes InGaN accommodate the lattice of QWs.

To grow the pre-strain layer, one should be concerned not only on the effect of strain relaxing but also on the quality of the material. If we bring too much negative effect to the QW crystal quality, then the strain relaxing becomes worthless. Thus the content of indium should be properly controlled. Too much indium will result in quality deterioration, and too little indium will not generate enough strain relaxation. Normally, the indium content in the pre-strain layer is set to be one third of that in the QW. Instead of growing a single layer of InGaN as the pre-strain layer, InGaN/GaN superlattices (SLs) are preferred when the pre-strain layer is thick. It is known that the crystal quality gets worse when growing InGaN: it is necessary to repair up the crystal with the help of GaN before InGaN grow too thick. And repeating of the InGaN/GaN SLs will form pre-strain layer which gives consideration to both

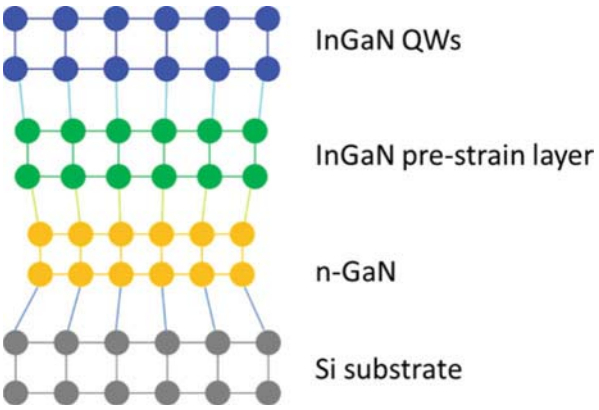

Fig. 4.14 Schematic illustration of strain evolution in a LED structure with pre-strain layer grown on Si substrate

strain relaxing and QW quality. As illustrated in Fig. 4.14, a pre-strain layer inserted between n-GaN and QWs makes the lattice evolved more gently, which is helpful to buffer the compressive stress in InGaN QWs.

The large lattice and thermal mismatch between Si and GaN bring great challenge in material growth, but also the opportunity to grow high-quality InGaN quantum wells. Once dislocation density and film cracking are under control, the tensile-type thermal strain and lattice strain raised by the Si substrate will become positive factors for indium incorporation. Growth temperature can be enhanced about 20 degrees to improve the quality of QWs.

4.1.4 V-Pits of GaN LED

There is a high density of threading dislocations (TDs) in InGaN/GaN LED grown on foreign substrates, due to the poor matching between the epi-layer and substrate in the lattice parameter and the thermal expansion coefficient. The density of TDs is about 10^8–10^9 cm^{-2} for LED grown on sapphire or SiC substrate and 10^9–10^{10} cm^{-2} for LED grown on Si substrate. The TDs are regarded as the non-radiative recombination centers [43] but seem to be insensitive to the luminous efficiency of GaN-based LEDs, unlike that of the traditional semiconductor materials. Two mechanisms have been proposed to explain this phenomenon. The traditional theory considers that most of carriers in the InGaN wells are localized in the In-rich regions and recombined before they reach the TDs [44, 45]. The recent theory proposed that the reason behind this phenomenon ascribes to the V-shaped pits (V-pits). The V-shaped pits with six {10-11}-oriented sidewalls, induced from dislocations, are the inverted hexagonal pits embedded in MQW structures [46]. Figure 4.15 shows the structure of V-shaped pits.

As a typical characteristic in GaN-based LEDs, the V-pits had been paid attention as early as 1998 [47, 48]. These works mainly focused on the formation mechanism

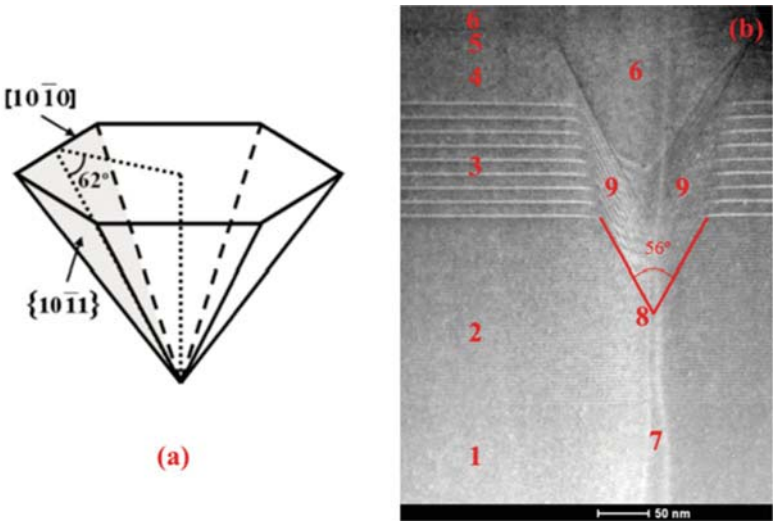

Fig. 4.15 Schematic structure of the V-shaped pits (**a**). STEM images of V-shaped pits in GaN-based LEDs grown on Si substrate (**b**). The numbers represent (1) n-type GaN, (2) InGaN/GaN SLs, (3) c-plane MQW, (4) HIL, (5) P-AlGaN EBL, (6) p-type GaN, (7) threading dislocation, (8) the position of pit generation, (9) the sidewall QW of V-shaped pits

of V-pits. Over time, the researchers began to follow the influence of the V-pits on the performance of LED. In 2000, Takahashi [49] examined the relations between the TD densities and the photoluminescence intensities of the SQW in which V-pits were intentionally formed, comparing them with the relations for a normal SQW under strong excitation conditions. The results indicated that the intentionally formed V-pits increase the luminescence intensity and reduce the dependence of photoluminescence intensity on the TD density of underlying GaN. In 2005, Hangleiter found that the TDs can be self-screened by the formation of V-shaped pits, and a physical model is proposed to explain this effect [50, 51]. The thickness and In concentrations in the sidewall structure of V-shaped pits were found to be much lower compared to those of the flat region, which provides an energy barrier around each dislocation. Consequently, V-shaped pits induced from dislocations can effectively screen the dislocations themselves and prevent carriers from non-radiative recombination. Here, we call this physical mode as "V pits screening TD" model.

Subsequently, tremendous efforts have been exerted to study the influences of V-shaped pits on the performance of InGaN/GaN MQW LEDs [52–60]. In our previous work [61], we observed the electroluminescence of sidewall MQWs at cryogenic temperatures. A broad short-wavelength EL peak with strong relative intensity to the main emission was observed at cryogenic temperatures in the LED with the unintentionally doped (UID) EBL but absent in the heavily doped (HD) EBL sample with identical epitaxial layer structure. Figure 4.16 shows the EL

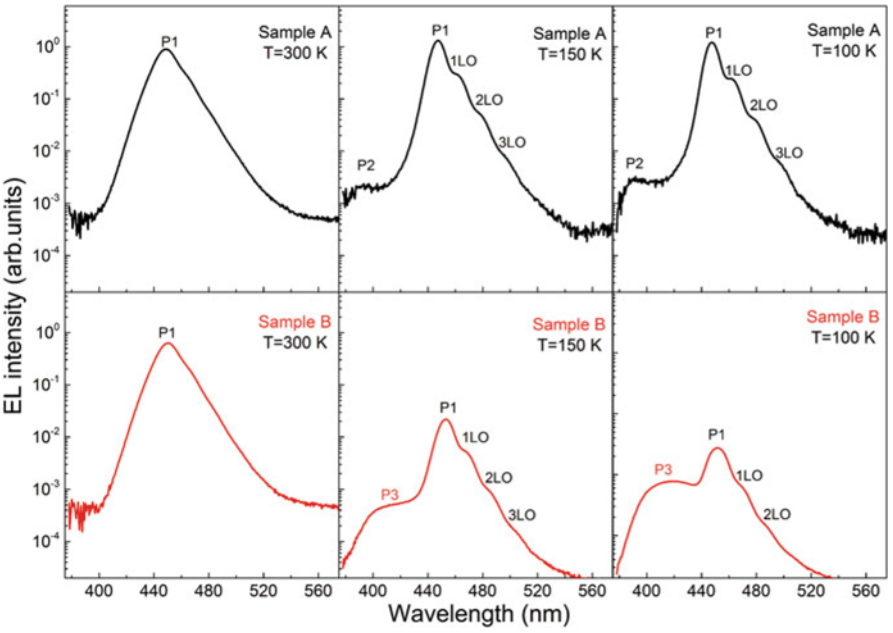

Fig. 4.16 EL spectra of the experimental samples at typically 35 A/cm^2. The spectra of the same sample are comparative in intensity. The emission intensity of Sample B decreases seriously as temperature drops, which is in sharp contrast to that of Sample A. In addition, P3 appears from 150 K in Sample B and increases in intensity as temperature further drops to 100 K

spectra of Sample A with the UID EBL and Sample B with the HD EBL at typically 35 A/cm^2. The main emission peak (P1) originates from the *c*-plane MQWs, and the emission peak (P2) involves to the Mg-related transition. After a careful analysis, we identify the sidewall MQWs in the V-pits as the emitter of P3. The peak wavelength of P3 is shorter than that of P1. It can lead to the conclusion that In concentrations in sidewall structure of V-shaped pits were much lower compared to those of the flat region. This conclusion is consistent with the "V pits screening TD" model and provides a solid proof of the existence of the self-screening effect.

In recent years, the "V pits screening TD" model is accepted by many researchers that the unexpectedly high emission efficiency of InGaN-based LEDs with high dislocation density attributes to the V-shaped pits. In the model, the role of V-pits is only screening TD. However, Li [62] reported an experimental phenomenon irrelevant to screening TD. In the research, it was demonstrated that the V-shaped pits have a significant influence on the hole injection depth.

In our previous work [63], a physical model, called the "V pits enhancing hole injection" model, has been established by using numerical simulation. In the model, screening dislocations is just one of the roles of V-shaped pits on the improvement of quantum efficiency, and V-shaped pits also play an important role on the hole injection into the MQWs. Due to the lower polarization charge densities in the

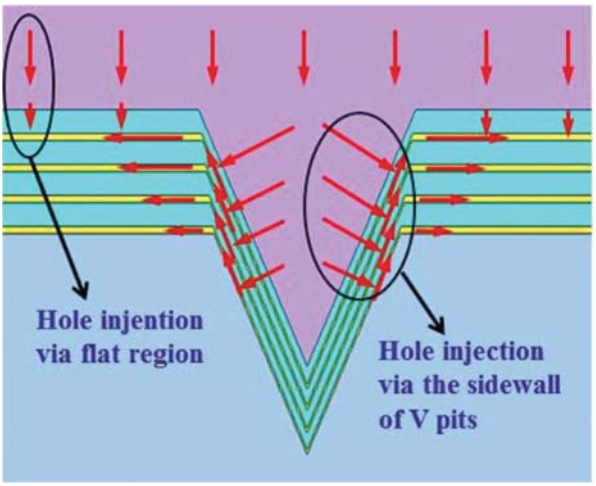

Fig. 4.17 The diagram about the process of hole injection into c-plane QW. The red arrows denote the direction of hole transport

sidewall structure with lower In concentration and {10-11}-oriented semi-polar facets, the injection of holes into the MQW via the sidewalls of the V-shaped pits is easier than via the flat region. It is helpful to reduce the efficiency droop and then improve the quantum efficiency of the LED. Therefore, InGaN/GaN MQW LEDs with high dislocation density still have high emission efficiency. Figure 4.17 illustrates clearly the process of hole injection into c-plane QW. There are two ways for hole injection into c-plane QW. One way is hole injection via flat region, in which holes are directly injected from p-type layer into c-plane QW. Another one is hole injection via the sidewall of V-pits, in which most of the holes in the V-shaped pit are injected into sidewalls QW laterally rather than vertically from p-type layer, run along the sidewall QW and then flow into c-plane QW.

Based on the "V pits enhancing hole injection" model, it can be well understood that the V-shaped pits have a significant influence on the hole injection depth [62]. The model is also used to explain the experimental results, in which LED with the larger size of V-shaped pit has higher quantum efficiency but lower forward voltage [64]. In the work, a careful simulation calculation is conducted, whose numerical models simultaneously include the screening dislocations and enhancing hole injection of V-shaped pits. It shows good agreement between the experimental data and the simulated results. The larger the V-shaped pit size is, the better it is for screening TDs and the injection of holes. It is revealed that screening TDs is the dominant role of V-shaped pits only at the small injection current density and has no effect on forward voltage. Yet the enhancing hole injection is the more significant function of V-shaped pits at the normal work current density and reduces the forward voltage. So, LED with the larger size of V-shaped pit having higher quantum efficiency but lower forward voltage is largely due to more hole injection via larger V-shaped pits.

In addition, we also experimentally demonstrate that the V-pits act as paths of hole injection into the c-plane MQWs at cryogenic temperatures [65]. It is evidenced

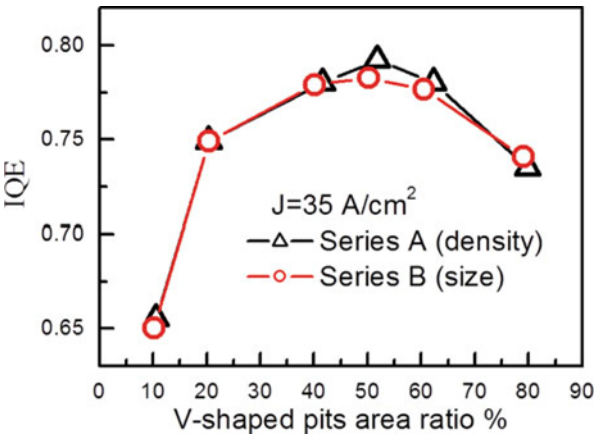

Fig. 4.18 The dependence of IQE on the area ratio of pits from the calculated results of Series A (density) and Series B (size) at the current density of 35 A/cm^2. The area ratio of pits here means the area ratio of the V-shaped pits accounting for the last QW

by the unusual broadening and blueshift of the emission of the c-plane MQWs, which occurs when the proportion of hole current flowing via the V-pits is increased.

It is confirmed that the V-shaped pits can promote the injection of holes in addition to screening the dislocations and then improve the quantum efficiency of the LED. According to this model, the density and size of pits are closely related with the hole injection, thereby affecting the quantum efficiency of LED. Hence, it is important to investigate the effect of the density and size of pits on improving the performance of LED. Two series of calculations are performed [66]. The one is the calculation for different density of pit with fixed size (Series A). Another is the calculation for different size of pit with fixed density (Series B). The calculated IQE curves show that the IQE is firstly enhanced and then reduced with an increase in both density and size of pits. The calculated results are in good agreement with the experimental results of the reported paper [67, 68]. The IQE displays the similar variation trend for different series of calculations. It implies that there is the same key factor for the dependence on both density and size of pits. The dependence of IQE on the area ratio of pits from the calculated results of Series A and Series B at the current density of 35 A/cm^2 is presented in Fig. 4.18. The area ratio of pits here means the area ratio of the V-shaped pits accounting for the last QW. As described in Fig. 4.18, the dependences of the calculated IQE on area ratio are almost the same for both two series of calculations. It indicates that the area ratio is the key factor. The calculated results show that the optimal value of area ratio is about 50% at the current density of 35 A/cm^2. For there lies an optimal value for pits density and the V-pits are induced from dislocations, there lies an optimal value for the density of dislocations, which is a new concept contrary to conventional viewpoints. It is the reason for the unexpectedly high emission efficiency of InGaN-based LEDs with high dislocation density, especially for LED grown on Si substrate.

It should be noted that the above results are obtained from the models based on two hypotheses in the simulation. The one is that the V-shaped pits are uniformly distributed. Another is that all of the pits have the same size. It is very difficult to

realize the two hypotheses for a real LED. Therefore, the enhancing effect of V-pit on hole injection will be weakened in the real devices, which resulting in the real optimal data is much smaller than the theoretical value (<50%). However, the results will point out the future development direction for boosting the blue LED performance: how to get the same size and uniformly distributed V-pits in the device.

In conclusion, the V-shaped pits can promote the injection of holes in addition to screening the dislocations and then improve the quantum efficiency of the LED. At present, a lot of researches are focused on the role of V-shaped pits screening the dislocations, but the effect of V-shaped pits on hole injection has only recently begun to get attention. It is significant to the device performance, which deserves intensive study.

4.2 Device Processing of GaN LEDs on Si Substrate

Most GaN-based LEDs are grown on sapphire, SiC, or Si substrates. The substrates of sapphire and SiC are chemically stable and mechanically tough; thus they are difficult to be removed and often be processed to lateral structure. For GaN on Si substrate, as the substrate can be easily removed by wet etching, it can be processed to a vertical thin film structure.

The chip fabrication process of vertical LEDs grown on Si substrate can be simply described in Fig. 4.19. After the growth of (a) GaN LED epi-structure on Si substrate is finished, (b) we deposited metal layers on the p-surface of the wafer

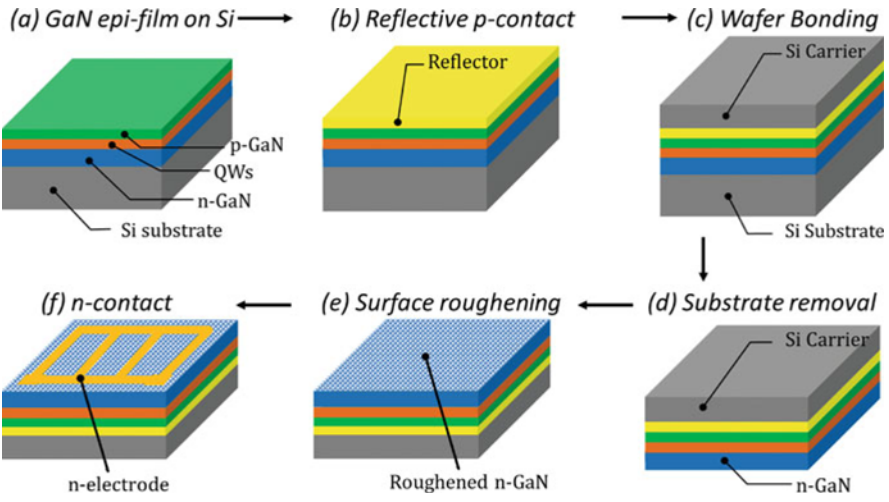

Fig. 4.19 Device fabrication processes of vertical LEDs grown on Si substrate, (**a**) growing Epi-film on GaN, (**b**) making reflective p-contact, (**c**) bonding the wafer to a new Si carrier, (**d**) removing the original Si substrate, (**e**) roughening n-GaN surface and (**f**) making n-contact

which act as p-contact and light reflector; (c) then the p-surface is bonded to a new electric conductive carrier via metal bonding technique; (d) the original Si substrate is etched off by wet etching, leaving the n-surface exposed to the air; (e) the n-surface is then roughed by wet etching to enhance light extraction; and finally, (f) n-contact is prepared [69], completing the chip process.

The chip fabrication process of vertical LEDs adopts many common techniques used in lateral LEDs fabrication, which are not needed to be described in detail. Some specific techniques used in vertical LED fabrication process will be focused below.

4.2.1 Reflective P-Type Ohmic Contact

The efficiency of a LED comprises not only internal quantum efficiency but also extraction efficiency. As Si can absorb a large amount of visible light emitted from the QWs, a reflective mirror is often placed between p-GaN and Si carrier to enhance the light extraction efficiency. In a vertical structure LED, current flows vertically through the Si carrier; thus the mirror layer between p-GaN and Si carrier functions not only as a reflecting layer but also as a p-contact layer.

Despite high reflectivity, it is difficult to make low resistivity p-contact as the hole concentration of p-GaN is low and the work function of p-GaN is high (7.1 eV). It becomes more difficult to select a suitable material as the reflective contact layer when we need to consider both reflectivity and resistivity. Ag is the most promising reflection metal for visible light, but its work function is only 4.3 eV, which makes it very hard to produce good ohmic contact to p-GaN. To overcome this problem, a bilayer structure of Ni/Ag reflector is developed. An ultrathin Ni layer with a few angstroms thick is deposited on the p-GaN surface; ohmic contact can be easily formed due to a high work function of Ni (5.2 eV). Ag layer is laid above the Ni layer acting as the reflection layer.

The thickness of Ni layer must be properly controlled. If the Ni layer is too thin, ohmic contact is hard to be formed, resulting in high resistivity; and if it is too thick, the Ni layer will absorb the light, reducing reflectivity. The Ni layer is often deposited by electron beam evaporation, and the required Ni thickness is a few angstroms which is very hard to be precisely controlled. An improved technique, so-called Ni sacrifice, is introduced to improve the practicality of making high reflectivity and low resistivity reflector [70]. The "sacrifice" can be understood through the procedures of depositing, annealing, and removing of Ni layer. Firstly, a relatively thick Ni layer is deposited on p-GaN surface and annealed in N_2 ambient to form ohmic contact; then the original Ni layer is removed by wet etching; and finally Ag reflector is deposited. During the "Ni sacrifice" process, a small amount of Ni atoms will be diffused into p-GaN and form ohmic contact during annealing process, and the extra Ni atoms are removed to ensure high reflectivity.

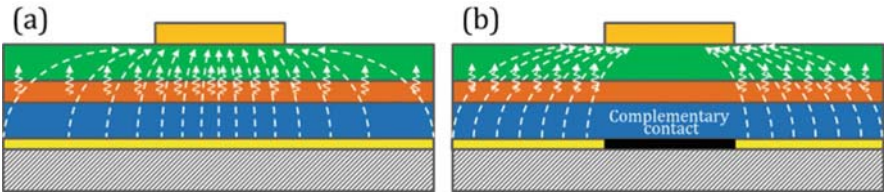

Fig. 4.20 Light extraction and current spreading in vertical LED (**a**) without complementary contact and (**b**) with complementary contact

4.2.2 Complementary Contact

Because of large tensile strain existing in GaN on Si, the thickness of epi-layer cannot be too thick, normally 2–3 μm. Compared with the width and length of LED chip of several hundred μm, the sidewall emission can be neglected. Majority of light will be emitted from the n-GaN surface. When n-contact is deposited on n-GaN surface, it will raise two problems: current crowding and light blocking. As illustrated in Fig. 4.20a, in a conventional LED structure, current prefers to flow following the path with lowest resistance; thus most of the current will be concentrated under n-contact, which is known as current crowding. Since most current crowd under n-contact, most light will emit from the region of QWs under n-contact, but the light from that region will be scattered by the n-contact, and this is called light blocking. Current crowding and light blocking will largely affect internal quantum efficiency as well as light extraction efficiency, distorting the performance of vertical LEDs.

We design a complementary contact structure to solve the problems of current crowding and light blocking [71]. As illustrated in Fig. 4.20b, we form a high-resistive contact on p-GaN surface with the same geometry of n-contact, which is the so-called complementary contact. The high-resistive contact can be achieved by deposition of dielectric materials like SiO_2 or Si_3N_4, forming a high-resistive media between p-GaN and p-contact, but not affecting light reflection. Current is forced to flow away from the region under n-contact and is distributed more uniformly across the junction, relieving current crowding. And because no current is flowing through the region under n-contact, no light will be emitted from the junction area under n-contact, and thus almost no light will be blocked by n-contact.

Experimental results of LED devices show that the complementary contact is effective to improve light extraction efficiency. With complementary contact, light extraction efficiency can be enhanced by 10–40%; the actual value depends on the coverage ratio of n-contact.

4.2.3 Film Transferring of GaN to New Substrate

The epi-structure of GaN LED grown on Si substrate is the same as that grown on sapphire substrate. But it cannot be processed to lateral structure like LEDs on sapphire substrate. Without film transferring, the light extraction efficiency can be very low due to light absorption of Si substrate. If we can transfer the epi-film to a new carrier with a reflector, the light extraction efficiency can be largely enhanced.

After the complementary p-contact with high reflectivity is prepared, film transferring process can be carried out. The film transferring comprises two main steps: firstly, the as-prepared wafer is attaching to a new carrier, and then, the original Si substrate is removed by wet etching.

The as-prepared wafer can be attached to a new carrier via thermal bonding or electrical plating. In thermal bonding, bonding media is deposited on both the wafer surface and carrier surface, and by applying high pressure under high temperature, bonding media diffuse into each side to form a continuous phase and join the wafer and carrier together. Both the bonding media and the carrier should have some special features such as good mechanical properties to sustain the structure, high thermal conductivity and electrical conductivity to conduct heat and electricity, good chemical stability to resist chemicals during chip fabrication, and matched thermal expansion coefficient with GaN films to lower thermal strain. And for the bonding media, good adhesivity is a must to attach the film to the carrier. Si is an outstanding carrier candidate with acceptable electrical conductivity, good thermal conductivity, high chemical stability, and matched thermal expansion coefficient. Metals are also used as carrier for LED transferring due to the excellent thermal conductivity and low price. Au is a promising bonding media with excellent properties in the aspects of adhesivity, thermal and electrical conductivity, and chemical stability. Indeed Au was widely used as the bonding media in semiconductor manufacturing, although the cost is high. Instead of pure Au, Au-Sn alloy with Au weight percentage from 10 to 90% is used as the bonding media to reduce the production cost. The Au-Sn alloy brings another advantage: by utilizing alloy composition to the eutectic point of Au-Sn system, bonding temperature can be dramatically reduced. Although Au-Sn alloy can reduce production cost to some extent, the price of it is still too high. A diffusion bonding technique is developed by using base metals as bonding media. The principle of diffusion bonding is based on diffusion of miscible metals: if two pieces of metals with smooth surface are laid together and sustain compressive force at high temperature, their atoms will diffuse into each other and form a continuous interface. As illustrated in Fig. 4.21, after Ag reflector is prepared, three layers of metals are deposited above the reflector sequentially, namely, diffusion barrier layer, bonding layer, and diffusion layer, respectively. The barrier layer above the Ag reflector is to prevent diffusion from the bonding layer to the Ag reflector. The bonding layer, normally in the form of high melting point metals like Cu, Mo, or Au, is acting as solvent; and the diffusion layer, normally in the form of low melting point metals like In or Sn, is acting as solute. A new Si carrier with surface covered by bonding layer is attached to as-prepared wafer. Under compressive stress and a

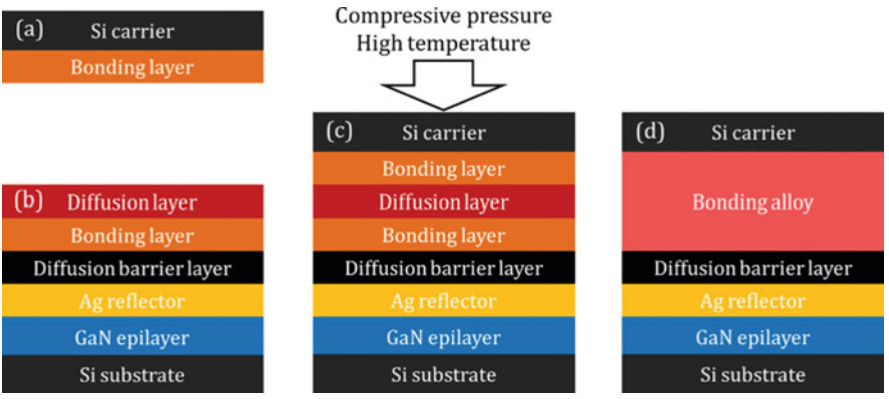

Fig. 4.21 Schematic illustration of diffusion bonding process, (**a**) depositing bonding layer on a Si carrier, (**b**) depositing reflector layer, diffusion barrier layer, bonding layer and diffusion layer on epi-wafer, (**c**) joining the two parts together under high pressure and high temperature and (**d**) the diffusion layer and the boding layers will form a continuous ally phase

proper high temperature, the atoms in the diffusion layer and bonding layers will diffuse into each other and finally form a continuous alloy phase.

After completing the bonding process, the original Si substrate can be removed by wet etching. Wet etching of Si is a very mature technology in IC industry; both anisotropic and isotropic etching modes have been developed. Anisotropic wet etching of Si is designed to create shapes like corners, grooves, or trenches, which will be used and discussed in later process of surface roughing. In the Si substrate removal process, isotropic etching of Si with aqueous HNO_3/HF is often used. The etching mechanism includes two steps: firstly oxidize Si to SiO_2 by HNO_3 and then dissolve SO_2 by HF. Related reactions are listed below:

$$\mathrm{Si} + 4\mathrm{HNO_3} \rightarrow \mathrm{SiO_2} + 4\mathrm{NO_2} + 2\mathrm{H_2O}$$
$$\mathrm{SiO_2} + 6\mathrm{HF} \rightarrow \mathrm{H_2SiF_6} + 2\mathrm{H_2O}$$

With surface covered by Au thin film, new Si carrier can be protected during etching, and the original Si substrate will be removed. The GaN film is then carried by the new Si substrate. The position of n- and p-GaN is upside down with p-GaN on the bottom and n-GaN exposed to the air.

4.2.4 Surface Roughening of N-Polar N-Type GaN

In GaN-based LEDs, light is very hard to escape from the bulk to the air as the total reflection angle of GaN is very small. Although a reflector is prepared at the backside of p-surface, it is still not enough to have high light extraction efficiency with a flat n-surface. A normal method is to make the n-surface rough to enhance the opportunity of light to escape [72, 73].

Normally, GaN epi-film grown on Si substrate is of Ga-polarity. As mentioned above, during the chip fabrication process, the epi-film is transferred to a new carrier with n-surface exposed to the air, indicating the top surface is of N-polarity. The polarity change provides a good opportunity to surface roughening. Ga-polarity surface is resistive to most chemicals at room temperature. But N-polar GaN can be selectively etched by water with the help of alkaline:

$$2GaN + 3H_2O \overset{OH^-}{\rightarrow} 2Ga_2O_3 + 2NH_3$$

According to the reaction above, the reaction of GaN with water should have no polarity dependence. But in fact, the truth is that Ga atoms are firstly attacked by hydroxyl (OH-) group and then reacted with water to form Ga_2O_3 and hydroxyl group. The polarity dependence of wet etching can be attributed to the difference in bond structure [74]. As illustrated in Fig. 4.22, in N-polar GaN, each nitrogen atom has one dangling bond perpendicular to the surface, and hydroxyl groups are free to attack Ga atoms, forming hexagonal pyramid-shaped etching surface, while in Ga-polar GaN, each nitrogen atom stretches out three dangling bonds covering

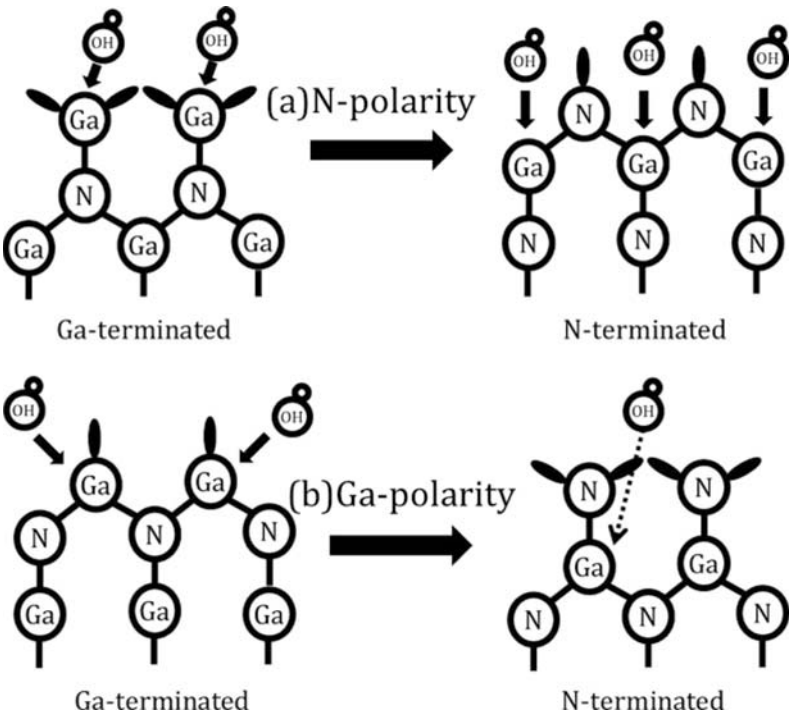

Fig. 4.22 GaN etching of different polarities: (**a**) N-polar GaN can be etched by alkaline, and (**b**) dangling bonds of N atoms prevent Ga atoms from attacking by alkalizing in Ga-polar GaN

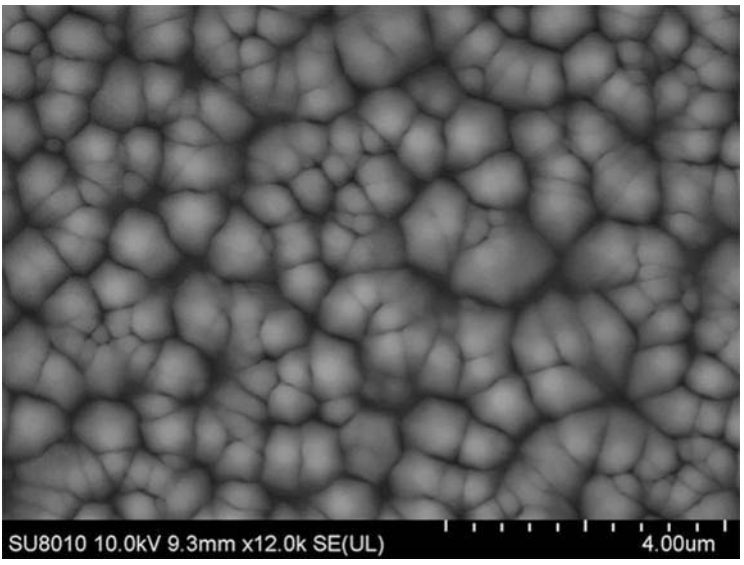

Fig. 4.23 SEM image of roughened N-polar surface by wet etching in KOH solution

the Ga atoms below them. Hydroxyl groups are repelled away from Ga atoms by the negatively charged dangling bonds; thus Ga-polar GaN is resistant to etching by alkaline.

As shown in Fig. 4.23, after wet etching in KOH solution, the N-polar GaN surface is roughened with hexagonal-shaped pyramids covering the whole surface. The facets of the hexagonal pyramids are of $\{10\bar{1}0\}$ orientation.

One can observe that the pyramids are not very uniform with different sizes. That can be attributed to the nonuniform defect distribution as the pyramids are initialed from dislocations.

With a roughened surface, the light can have a high probability to escape from the pyramid to the air after a few rounds of reflections. In vertical LEDs on Si substrate with a reflector, light extraction efficiency can be enhanced by 30–50% percent if surface roughening is applied; the value can be higher without a reflector.

4.2.5 Ohmic Contact on N-Polar N-GaN

The polarity change brings merit to surface roughening but also brings difficulty to n-contact making. In lateral LEDs, making ohmic contact on Ga-polar n-GaN is very easy using Al- or Ti-based metals, while in vertical LEDs, ohmic contact on N-polar n-GaN is difficult to obtain because of the formation of V_{Ga}-O_N complex on the surface of N-polar GaN [75]:

$$O + V_N \rightarrow O_N$$
$$V_{Ga} + O_N \rightarrow V_{Ga} - O_N$$

The formation of V_{Ga}-O_N not only consumes V_N but also acts as acceptors and compensates donor-like defects V_N, lowering electron concentration and leading to a poor ohmic contact. A surface treatment before n-contact deposition with Ar plasma can help to improve the stability of ohmic contact on N-polar n-GaN. With Ar plasma treatment, V_N concentration can be dramatically increased, and the existence of V_{Ga}-O_N will no more affect the electron concentration on the surface. Therefore, ohmic contact on N-polar n-GaN with high stability can be easily obtained with the help of Ar plasma treatment [76].

4.2.6 Device Passivation

Reliability is very important to a commercial LED. The most effective way to improve reliability of an electronic device is to do passivation. With the protection of passivation layer, LED can be protected from surface recombination and foreign-atom diffusion.

Figure 4.24 lists four vertical LEDs with different types of passivations. (a) Without passivation, surface recombination occurs when electrons and holes travel via the surface of the device, reducing the radiative recombination efficiency [77]; foreign ions such as Na + may diffuse into the active region, causing current leakage; and H atoms may diffuse into p-GaN [78], resulting in degradation of p-GaN. (b) Passivation of sidewalls with SiO_2 dielectric material can help to protect key region of the device – the QWs. (c) Passivation of sidewalls and n-surface and passivation of the entire surface can provide better protection. But the quality and the thickness of the passivation layer should be properly controlled to avoid light extraction impediment [79]. (d) Beyond n-surface and the sidewalls, p-surface is also partially passivated [80] near the edge. With such a design, current is forced to flow away from the surface of the sidewall, further preventing recombination of carriers at the interface of GaN/SiO_2. And leakage current can be dramatically reduced.

4.3 Device Characterization of Vertical Thin Film LEDs Based on GaN/Si Technology

For the LED grown on Si substrate and be fabricated into vertical thin film structure, it gets some unique features which are different from the conventional lateral LEDs. These features, specifically uniform current flow, excellent heat conduction, and single-face light emission, will bring many merits to the performance of LED.

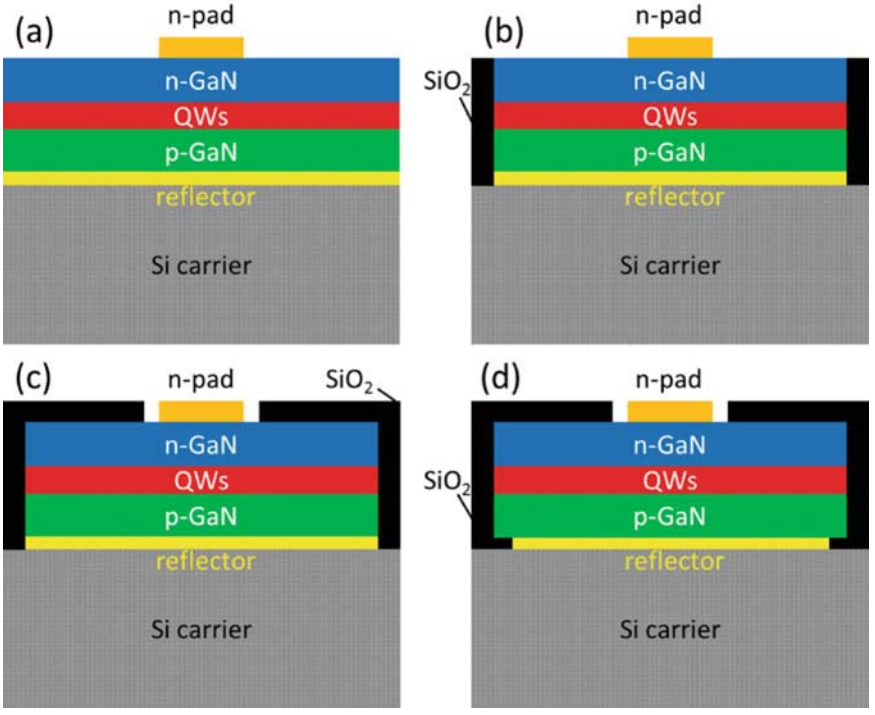

Fig. 4.24 Schema of a vertical LED (**a**) without passivation, (**b**) with sidewalls passivated, (**c**) with entire surface passivated, and (**d**) with double side passivated

As illustrated in Fig. 4.25a, for a typical lateral LED structure with both n-pad and p-pad on the same sides, the current flows downward through the QWs and then travels laterally to the n-side; the current is very crowded under the n-pad. Nonuniform current flowing will largely affect the performance of LED; it raises the operation voltage, causes regional over temperature, and reduces the reliability of LEDs. Under high current density, the status becomes even worse. In a vertical structure LED with n-pad and p-pad laid on two opposite sides, current flows directly through the QWs to n-pad. The current flowing path is symmetrical. With proper n-contact, current distribution can be very uniform across the whole QW region, and current crowding can be avoided. A simple way to justify the current spreading performance of a LED is to measure its I-V characteristic. Normally, a better current spreading will result in a lower forward voltage under high current density.

The dependences of voltage on current density of the two types of LEDs are plotted in Fig. 4.26. The solid line represents lateral LED on sapphire substrate, and the dash line represents vertical LED on Si substrate. Obviously, the vertical LED has a lower voltage at every current density, and the gap becomes bigger

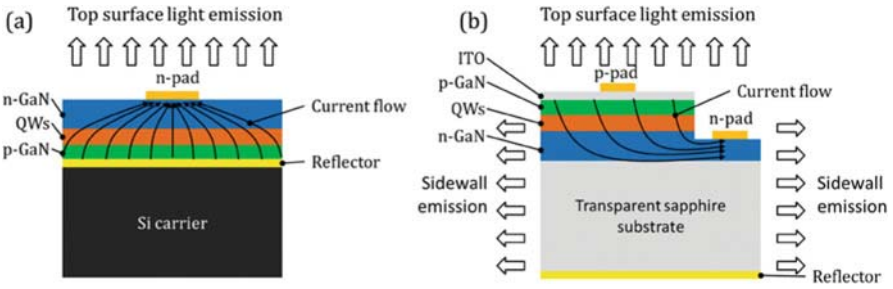

Fig. 4.25 Comparison of LED with (**a**) vertical structure and (**b**) lateral structure

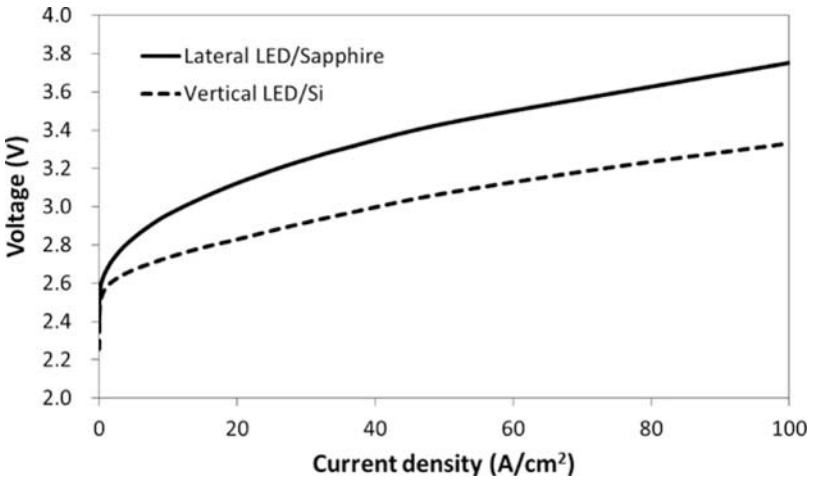

Fig. 4.26 Comparison of V-I characteristics between vertical thin film LED and conventional lateral LED

when current density increases. This phenomenon can be mainly attributed to the difference of current spreading. Commonly, the better current spreading of a LED, the lower the operation voltage will be.

The thermal conductivity is a very important feature for LED devices. Although the efficiency of LEDs is relatively high, still ten percent of the energy is lost in the form of heat. If the heat cannot be conducted away rapidly, it will accumulate inside the device and heat up the junction. Under a high temperature, the device will suffer thermal droop, that is, the efficiency of a LED drops down when temperature is increased. Besides, the reliability of the LED will also be largely affected; the LED devices will degrade faster under a higher temperature. Therefore, it is very important for a LED to maintain a relatively low temperature, which required good thermal conductivity. As in Fig. 4.25b, a conventional lateral LED has a thick sapphire substrate at the backside, and heat needs to be conducted away from the substrate. The thermal conductivity of sapphire is relatively low (45 W/mK). Under

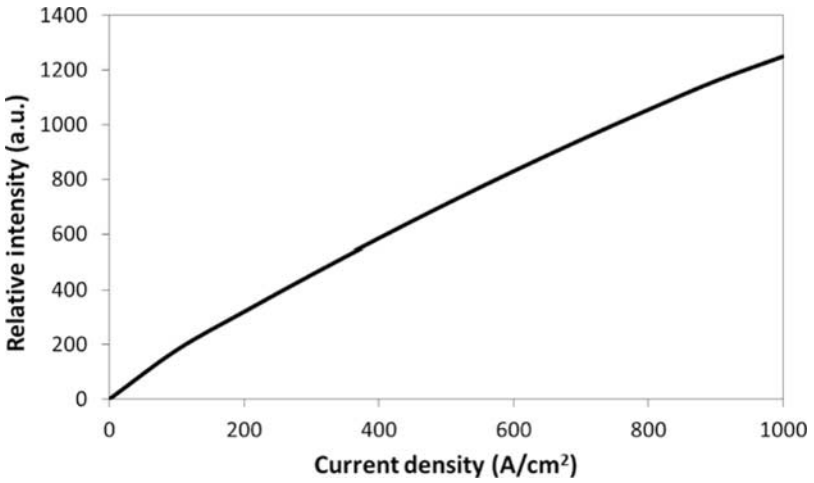

Fig. 4.27 Emission intensity versus current density of a vertical thin film LED

high current density, the junction temperature will rise up to very high level and lead to a very poor reliability. The nonuniform current distribution will aggravate the status. For the vertical structure, the heat is flowing through the Si carrier. Thus a conventional lateral LED structure is not suitable for high power application. A solution to this is to mount the top face instead of the bottom face on the sink, which is called as "flip chip" structure. The flip chip structure reduces the thermal diffusion length and directly contacts GaN to the sink, which can largely reduce the junction temperature. With flip chip structure, LEDs grown on sapphire can be used in high power application.

The Si carrier has a much better thermal conductivity (150 W/mK) which is two times higher than that of sapphire, resulting in a lower junction temperature. Combined with the good current spreading behavior, very high current density can be applied to the vertical thin film LEDs. Figure 4.27 demonstrates a vertical thin film LED chip in the size of 0.1 mm^2 working under various current densities. The emission intensity of the device shows no obvious decay up to a current density of 1000 A/cm^2.

The junction temperature is measured to compare the heat conduction capability between the lateral and vertical LEDs. The measuring is based on I-V testing method [81]. Figure 4.28 plots the junction temperatures of a lateral LED and a vertical LED at various current densities under a same ambient temperature of 30 °C. At 5 A/cm^2, the junction temperature of the vertical LED on Si is 40 °C, which is slightly lower than that of the lateral LED. As current density increases, the junction temperature of both samples increases. When current density increased to 100 A/cm^2, for vertical LED the junction temperature is 85 °C, whereas the junction temperature for lateral LED is 102 °C.

Another advantage for vertical thin film LED is on the light extraction mode. As illustrated in Fig. 4.25b, because the sapphire substrate is transparent and the

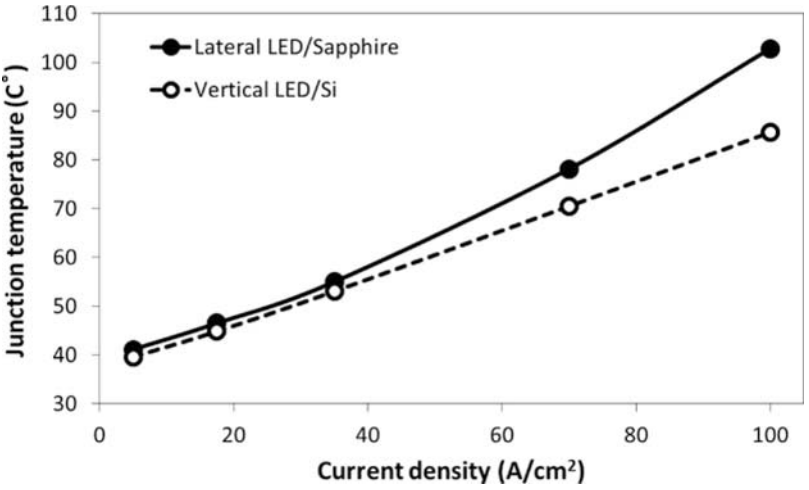

Fig. 4.28 Comparison of junction temperature between vertical thin film LED and conventional lateral LED

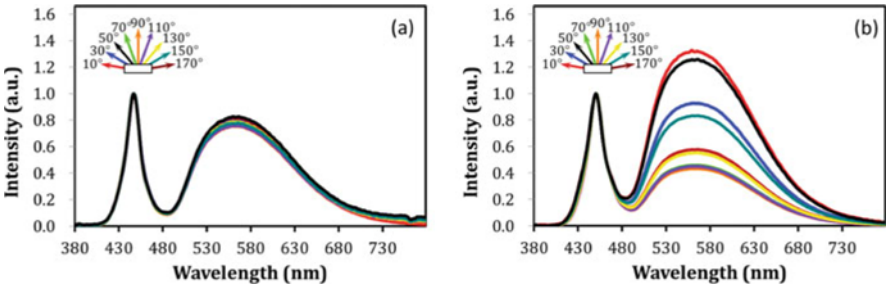

Fig. 4.29 The spectra of white LEDs of (**a**) vertical thin film structure on Si and (**b**) lateral structure on sapphire in different viewing angles

thickness is 70 μm, a large amount of light will be emitted from the sidewall of the sapphire. Excluding the bottom surface, there are five surfaces that can be the faces for light emission. It is difficult to manipulate the light emission, for instance, in white light application, as there are too many faces where light can come out, it is hard to apply the phosphor to the LED. As in Fig. 4.29b, the spectra of a phosphor which converted white LED based on lateral structure on sapphire substrate are measured in different viewing angles. The portion of yellow light is different in different viewing angles, which will lead to nonuniform color temperature. For the thin film vertical structure with epi-film thickness of only 2 μm, almost all the light comes out from the top surface. Thus it is very easy to control the light in LED applications. As shown in Fig. 4.29a, the light emitted from a vertical thin film phosphor-converted white LED has almost the same spectra in any direction.

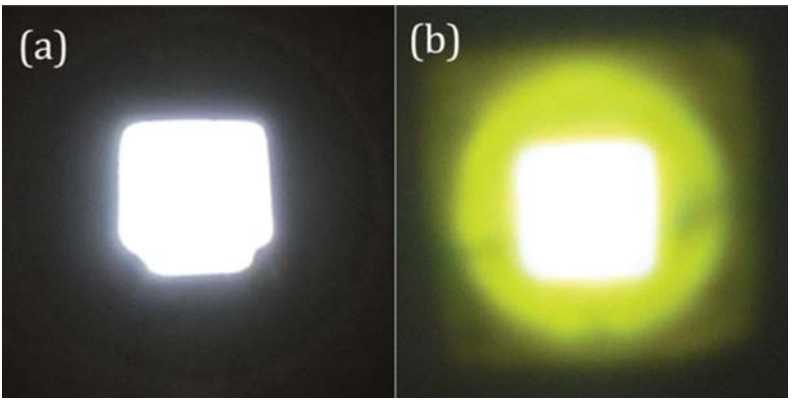

Fig. 4.30 Projection of white light of (**a**) vertical thin film LED on Si and (**b**) lateral LED on sapphire

The light emitted from the vertical thin film LED is highly directional. With simple light path design, it can propagate parallel in a long distance. As illustrated in Fig. 4.30a, the projection of a vertical thin film white LED in a distance of 5 m is recorded by a camera. It can be seen that the facula is very uniform, and the border of which is very sharp. By comparison, the facula of a lateral LED is less uniform with blurry border (Fig. 4.30b).

In conclusion, the thin film vertical LED on Si substrate has its unique features. In combination with good current spreading and excellent heat conductivity, LEDs on Si can be applied in high power application under high current densities. Because of one face emission behavior, LEDs on Si have high directional emission light, and it can be applied in directional lighting applications such as projectors, headlights, and car lamps.

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Chapter 5
The AlGaInP/AlGaAs Material System and Red/Yellow LED

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5.1 AlGaInP/AlGaAs Material System Lattice and Bandgap Energy

AlGaInP/AlGaAs is the material of choice for the long-wavelength part of the visible spectrum, namely, for red, orange, yellow, and yellow-green wavelengths. Both of them are zinc blende structure as shown in Fig. 5.1.

$Al_xGa_{1-x}As$ for Al mole fractions $x < 0.45$ are direct-gap semiconductors. For Al mole fractions $x < 45\%$, the Γ conduction-band valley is the lowest minimum, and the semiconductor has a direct gap. For $x > 45\%$, the X valleys are the lowest conduction-band minimum, and the semiconductor becomes indirect.

AlGaAs lattice nearly matches with GaAs for whole Al content [1]. And AlGaAs is a high-efficiency material suitable for infrared and red wavelengths. However it is unsuitable for orange and shorter wavelengths due to the direct-indirect transition of the $Al_xGa_{1-x}As$ bandgap at x of 0.45 corresponding to a wavelength of 624 nm [2].

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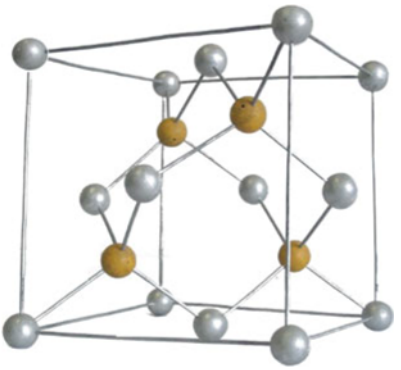

Fig. 5.1 AlGaInP zinc blende structure: gray ball, Al, Ga, In; yellow ball, As, P

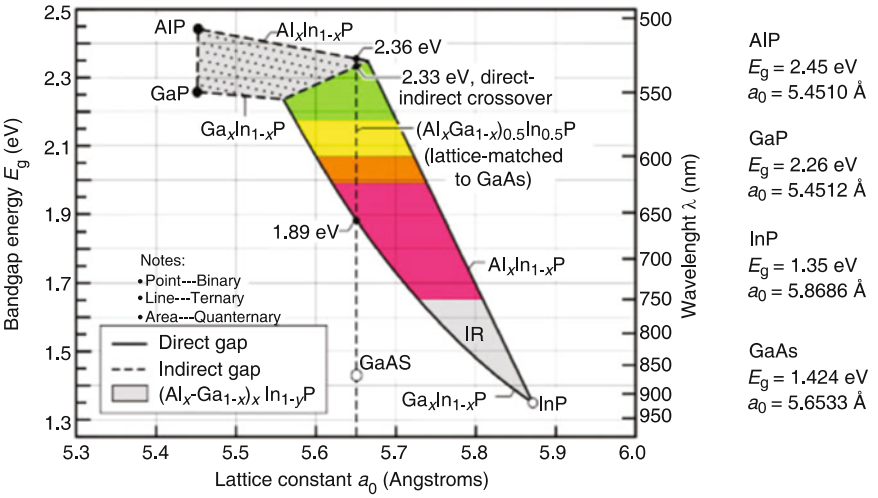

Fig. 5.2 AlGaInP zinc blende structure, gray ball: Al, Ga, In and yellow ball: As, P

$(Al_xGa_{1-x})_{1-y}In_yP$ alloy lattice constant varies with indium content linearly but changes very slightly as shown by Eq. (5.1), and the lattice mismatches with GaAs as shown by Eq. (5.2).

$$a_{(Al_xGa_{1-x})_{1-y}In_yP} = 5.45 \times (1-y) + 5.8688 \times y \tag{5.1}$$

$$\frac{\Delta a}{a_{GaAs}} = -0.03567 + 0.0379 \times y \tag{5.2}$$

At the molar indium composition of 50%, $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ is lattice matched to GaAs as shown in Fig. 5.2 [3], which can be calculated by Vegard's law [4, 5].

Such long-wavelength visible-spectrum devices will play an important role in solid-state lighting applications. In Fig. 5.2, the least squares fit to this data

(indicated by the dashed lines) and give us the bandgap of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ alloy range at 2 K by Eqs. (5.3) and (5.4), and at 300 K by Eqs. (5.5) and (5.6).

$$\mathrm{Eg}\,(\Gamma) = 1.985 + 0.610 \times x \tag{5.3}$$

$$\mathrm{Eg}(X) = 2.282 + 0.0852 \times x \tag{5.4}$$

$$\mathrm{Eg}\,(\Gamma) = 1.900 + 0.610 \times x \tag{5.5}$$

$$\mathrm{Eg}(X) = 2.204 + 0.085 \times x. \tag{5.6}$$

Similar to AlGaAs, AlGaInP suffers from a direct-indirect transition of the bandgap. However, the direct-indirect transition in AlGaInP occurs at a higher energy compared with AlGaAs, which occurs at the energy of 2.23–2.33 eV corresponding to 556–532 nm.

Besides direct-indirect transition, AlGaInP exact bandgap energy suffers from order and disorder effect with In atoms and Ga and Al atoms, at which the direct-indirect transition occurs depending on the degree of randomness of the quaternary alloy semiconductor; generally it is lower for AlGaInP with a high degree of order [6].

The first-principles pseudopotential method with the virtual crystal approximation is used to calculate the band offsets at (001) $Ga_{0.5}In_{0.5}P/Al_xGa_{0.52-x}In_{0.5}P$ heterostructures. The valence-band offset VBO varies with x as VBO = 0.433x eV, while the inferred conduction-band offset CBO at Γ minima varies in x as CBO = $0.787x$ eV. The values for $CBO^{\Gamma}/\Delta Eg$ are around 0.65. And as shown in Fig. 5.3, the results are in very good agreement with the experimental data [7].

5.2 AlGaInP/AlGaAs Material Epitaxy by MOCVD

AlGaInP materials and devices have led to major advances in high-brightness LEDs. The fabrication of AlGaInP-based light emitters dates back to the mid-1980s. It is closely related to the development of metal-organic vapor phase epitaxy (MOVPE) because the standard growth technologies for conventional LEDs like liquid-phase epitaxy (LPE) or hydride vapor phase epitaxy (HVPE) were not suitable for the growth of AlGaInP. The first light-emitting AlGaInP-based devices were semiconductor lasers developed in Japan [8]. High-efficiency LEDs grown by MOVPE were reported a few years later [9, 10]. Despite the difficulties in epitaxial growth, the new material system was attractive, because it combined the possibility to achieve high efficiency with the flexibility to tune the emission wavelength over half of the visible spectrum from green to red. Continuous progress in epitaxial growth, processing technology, and the design of structures for effective

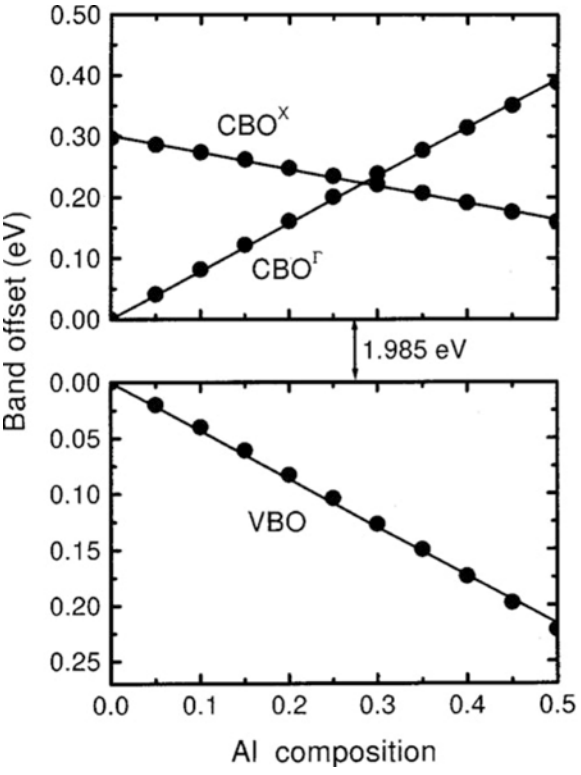

Fig. 5.3 Composition dependence of the valence- and conduction-band offsets at $Ga_{0.5}In_{0.5}P/Al_xGa_{0.52-x}In_{0.5}P$ (001) heterostructures

light extraction enabled the fabrication of AlGaInP LEDs with record high external efficiencies above 50%. The possibility to efficiently generate light in frequently used colors like yellow, orange, or red accelerated the use of AlGaInP LEDs in many applications such as interior and exterior automotive lighting, traffic lights, full-color displays, or all kinds of indoor and outdoor signs.

As a metastable phase material without its own substrate, AlGaInP usually has been grown on the GaAs substrate. Thus the lattice matching between AIGaInP and GaAs substrate is the most important. Commonly before the epitaxy of AlGaInP layer, GaInP and AlInP materials were firstly deposited on GaAs substrates, respectively, according to the linear interpolation method. At the molar In composition of 50%, $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ lattice matched with GaAs at room temperature; however, the difference of thermal expansion coefficient between AlGalnP and GaAs should be also considered. And the molar In composition x is usually set slightly larger than 0.5, which benefits for better crystal quality.

P-type and n-type doping are crucial for AlGaInP/AlGaAs material. And the control of doping concentration, uniformity, and repeatability plays a key role in the improvement of yield and performance of devices. Si_2H_6 and Cp_2Mg are commonly used as n-type and p-type dopants, and the doping concentration is controlled by adjusting the dopant flux. In addition, the doping of Mg is more complicated than

that of Si. From the larger range of growth conditions, the hole concentration of materials is nonlinear with the flow of Cp_2Mg and is affected by temperature and growth speed, so the significant change of growth conditions should be avoided.

High-quality A1GaInP/AlGaAs bulk layers as well as quantum well (QW) structures have been grown by LP-MOVPE on (100) offset 6°–15° toward (111)B-oriented GaAs substrates. TMGa, TMAl, and TMIn were used as MO sources, and Cp_2Mg and SiH4 were used as p-type and n-type doping precursors. 100% arsine and phosphine as the group V element sources, the growth temperature was around 700 °C, with the reactor pressure of 50 mbar and the V/Ill ratio in the gas phase around 300 in hydrogen atmosphere. Especially emission wavelength blue shifting of AlGaInP epitaxial layers, including MQW structure, were observed on GaAs substrate orientation offset from (100) toward (311)B, this phenomenon is caused by the (111) ordering on the group III sublattice [11]. Now by the state of the art (311)B or (511)B orientation GaAs substrate were used widely for AlGaInP LED.

5.3 AlGaInP/AlGaAs LED Structure Design and Manufacture

Owing to the high refractive index of semiconductors, light incident on a planar semiconductor-air interface is totally reflected, if the angle of incidence is sufficiently large. As a result of total internal reflection, light can be "trapped" inside the semiconductor. Light trapped in the semiconductor will eventually be reabsorbed, e.g., by the substrate, active region, cladding layer, or metallic contact.

The external quantum efficiency (EQE) of an LED is the product of the internal quantum efficiency (IQE), η_{iqe}, and the light extraction efficiency (LEE), η_{lee}, i.e.,

$$\eta_{\text{eqe}} = \eta_{\text{iqe}} \times \eta_{\text{lee}}$$

The LEE plays an important role in increasing the power efficiency of LEDs.

5.3.1 Bragg Reflector and Textured Chip Surfaces

Subsequent to the AlGaInP laser development that occurred in the early 1980s, AlGaInP LED development started at the end of the 1980s and early 1990s [9, 10, 12, 13]. These LEDs were grown in a p-side-up configuration on conductive n-type GaAs substrates. Except to the AlGaInP lasers, LED structures employ current-spreading layers. The effect of the current-spreading or light attractive window layer is shown in Fig. 5.4a [14].

Without a current-spreading layer, the current is concentrated under the center of the top contact. Because most of the light is generated in the region below the opaque

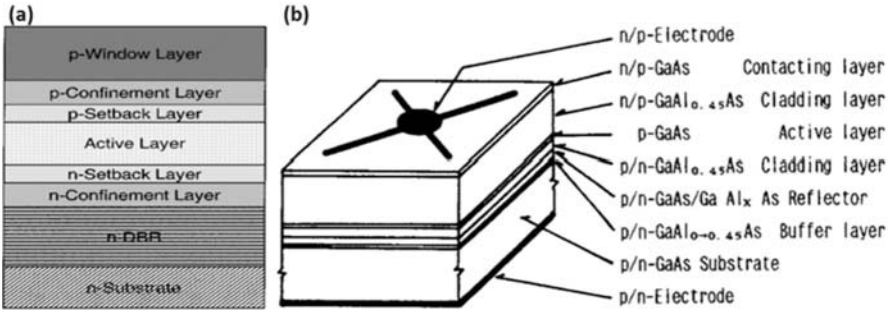

Fig. 5.4 (**a**) Schematic drawing of the layer structure of a typical high-brightness LED, (**b**) structure of DH-LED with Bragg reflector [14]

top contact, the light extraction efficiency of AlGaInP LEDs without a current-spreading layer is very low. For a sufficient thick and conductive current-spreading layer, the entire p-n junction plane of the LED chip lights up and not just the region below the top ohmic contact. It is desirable to spread the current beyond the contact area by a distance larger than the contact radius. However, spreading the current all the way to the edge of the chip could result in unwanted surface recombination.

In order to improve the extraction efficiency of AlGaInP LED based on absorbing GaAs substrate (referred as AS-substrate), a distributed Bragg reflector DBR is included between the substrate and the lower cladding layer shown as in Fig. 5.4b [15].

As shown in Fig. 5.5, a new structure of high-brightness light-emitting diodes (LED) is experimentally demonstrated. The thin window layer is composed of a 300-nm-thick indium-tin-oxide layer and a 500-nm-thick GaP layer for both current spreading and light antireflection. The two coupled distributed Bragg reflectors (DBRs) with one for reflecting normal incidence light and the other for reflecting inclined incidence light which is emitted to the GaAs substrate are employed in the LED fabrication. The coupled DBRs in the LED can provide high reflectivity with wide-angle reflection. With the injection current increasing, the luminance intensity of device A shows the substantial superiorities over device B; the luminous flux of device A is about 1.79 lm and of device B is 1.32 lm with the saturation currents 130 mA and 110 mA, respectively. The luminance efficiency of device A is larger than that of device B, and the curve of device A is slowly declining with the current increasing, which indicates that light generated inside device A would emit outside much more than device B. This is mainly attributed to the thin window layers and the coupled DBRs, which have the advantages of less optical absorption, better current spreading, and larger antireflection for the light emitting outside [16].

As shown in Fig. 5.6, metal-organic chemical vapor deposition (MOCVD)-based aluminum gallium arsenide (AlGaAs) used as the bottom window (BW), which was inserted between the light-emitting diode (LED) structure and the absorbing substrate, has been proposed to improve the extraction efficiency of 630 nm AlGaInP LEDs. In an AlGaInP LED with this AlGaAs BW, enhanced light

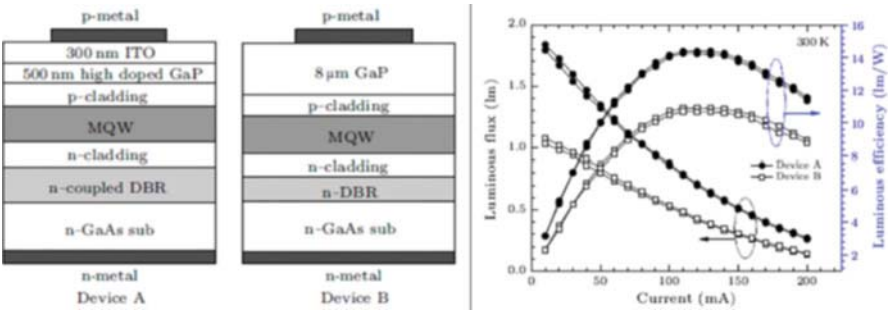

Fig. 5.5 Schematic view of cross sections of the AlGaInP LED studied, luminance intensity and luminance efficiency versus dc current for the LEDs studied [16]

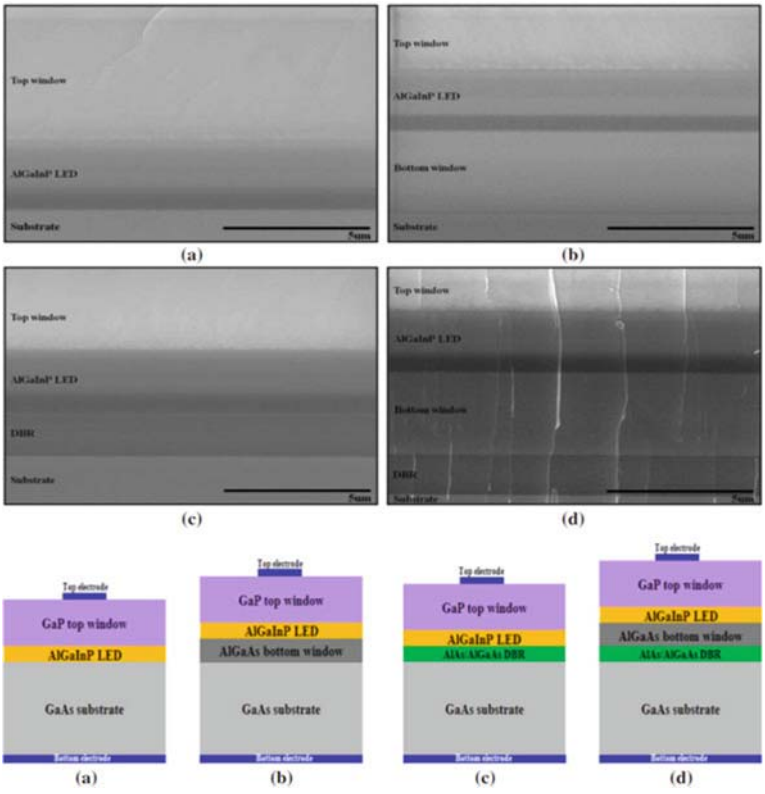

Fig. 5.6 (Color online) SEM images (upper panels) and schematics (lower panels) of structures of (**a**) conventional AlGaInP LED and AlGaInP LEDs with (**b**) BW only, (**c**) DBR only, and (**d**) both BW and DBR [17]

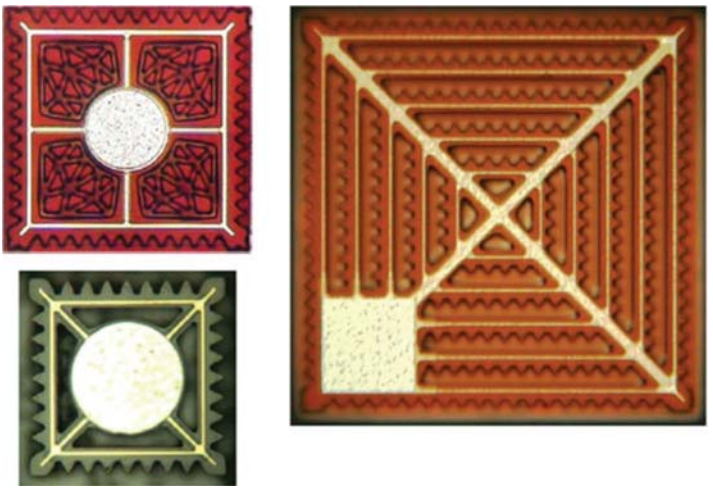

Fig. 5.7 Top-view images of surface-structured OSRAM chips. Various chip sizes have been fabricated with similar luminous efficiencies, demonstrating the scalability of the concept [19]

extraction efficiency was observed, as some of the light emitted from the active region to the absorbing substrate could pass out of the LED through the BW. In addition, it was found that an output power of 8 mW was obtained from an AlGaInP LED with both a BW and a distribution Bragg reflector (DBR), a nearly twofold improvement of over 4.2 mW that was obtained from a conventional one at an injection current of 80 mA [17].

Chip surfaces may be textured in order to increase the light extraction efficiency. An advantage of this approach is that it leads to a scalable chip design as opposed to the chip-shaping techniques discussed above. A possibility of structuring consists of randomly roughening the upper window layer. This can be achieved, e.g., using polystyrene spheres and dry etching [18]. In this case, incident photons at the roughened surface are either scattered isotropically and can escape from the chip or reflected with a random distribution of the reflection angles. As a result, the probability of light extraction is increased on multiple round trips between the surface and substrate assuming the substrate is covered by a highly reflective DBR mirror.

In Fig. 5.7, top-view images of surface-structured LEDs are shown. Contact frames are used to distribute the current across the device since current spreading in the window layer is strongly suppressed underneath the etched structures. Also, current densities are increased in the light extraction structures, enhancing the efficiency further. One advantage of the concept is that it leads to a completely scalable chip design, whereas other advanced extraction mechanisms require certain ratios between chip size and thickness for maximum efficiency. Larger chip sizes can simply be obtained by adding more contact frames with attached light extraction structures.

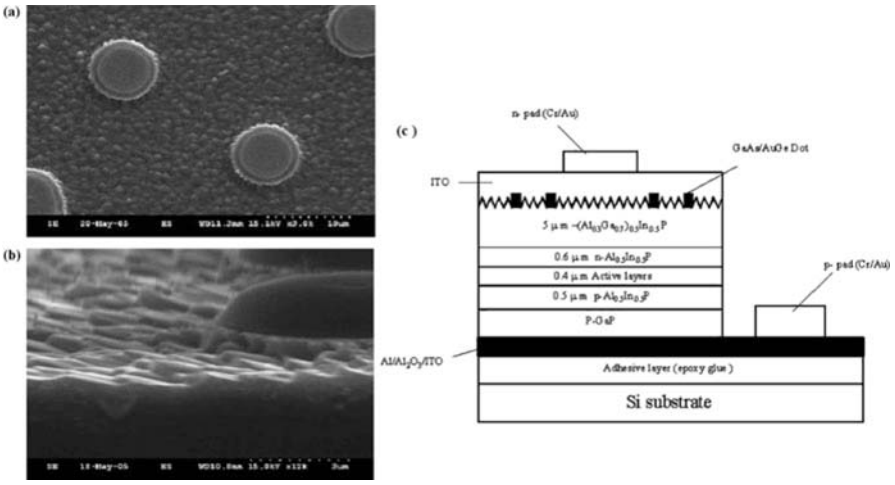

Fig. 5.8 SEM images of an n-side roughened-surface AlGaInP LED. (**a**) Top view and (**b**) cross-sectional side views. (**c**) Schematic cross section of a AlGaInP LED with n-side surface roughening

An n-side-up AlGaInP-based light-emitting diode (LED) with a triangle-like surface morphology was fabricated using the adhesive layer bonding technique, followed by wet etching to roughen the surface. The light output power of the roughened-surface LED was 1.6 times higher than that of a flat-surface LED at an injection current of 20 mA, i.e., a significant improvement attributed to the ability of the roughened surface to not only reduce the internal reflection between the rear mirror system and the semiconductor-air interface but also to effectively scatter the light outside the LED device. Figure 5.8c schematically depicts a cross-sectional image of AlGaInP LED with n-side surface roughening. Figure 5.8a shows scanning electron micrograph (SEM) images of the top and cross-sectional side views of the AlGaInP LED after H_3PO_4:HCl = 5:1 for 40 s of etching time. According to Fig. 5.8b, the roughened-surface morphology of the n-side-up AlGaInP-based LED displays a triangle-like feature, which tilts toward a specific direction associated with the lattice orientation. This feature could be related to the surface polarity of AlGaInP since this roughening feature can only be observed through wet etching only on the n-side-up surface of AlGaInP material after the GaAs substrate is removed. Our laboratory is currently investigating the detailed mechanism of forming the roughened surface [20].

5.3.2 Transparent Substrate

As shown in Fig. 5.9, to further eliminate the absorbed GaAs substrate affect, the transparent substrate (TS) was employed [21]. In this letter, they report the develop-

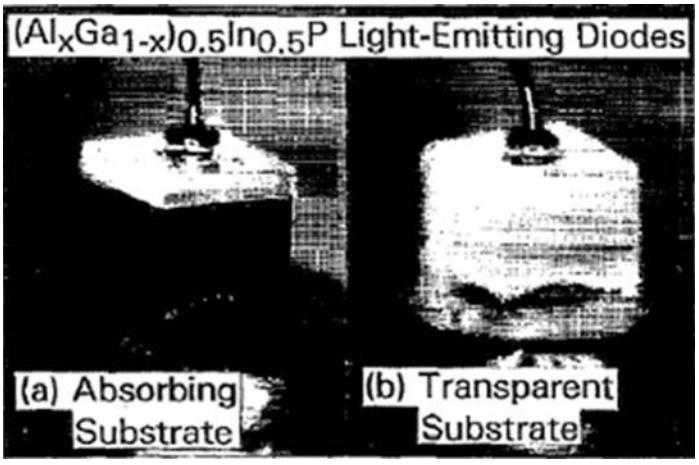

Fig. 5.9 Photomicrographs of (**a**) absorbing-substrate (GaAs) and (**b**) transparent-substrate (GaP) AlGaInP LED chips operating at 50 mA (dc) with an emission wavelength of $\lambda \sim 600$ nm [21]

ment of a new family of transparent-substrate (TS) $(Al_xGa_{1-x})_{0.5}In_{0.5}P$/GaP LEDs whose luminous performance exceeds that of all other current LED technologies in the green to red (560–630 nm) spectral regime by at least a factor of 2. The maximum luminous efficiency of these devices is 41.5 lm/W at $\lambda \sim 604$ nm (20 mA, direct current). These devices are fabricated by semiconductor wafer bonding a "transparent" n-type GaP substrate to a p-n $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ double heterostructure (DH) LED after selective removal of the n-type GaAs-absorbing substrate employed for lattice-matched growth. And in 1996, visible-spectrum transparent-substrate GaP-AlGaInP/GaP light-emitting diodes fabricated with large-area wafer-bonding technology operating at 635.6 nm exhibit low voltage (<2.1 V at 20 mA) and high external quantum efficiency (23.7%) [22].

In a conventional transparent-substrate chip, external quantum efficiency is limited by internal optical losses within the LED structure [23]. These losses include the finite reflectivity of ohmic contact metallization, reabsorption by the active layer, and free-carrier absorption. For AlGaInP LEDs, a trade-off exists between active layer reabsorption and electron confinement which results in an optimum active layer thickness depending on the emission wavelength [24]. This effect is pronounced for shorter-wavelength devices ($\lambda_p < 630$ nm) wherein the required thickness for sufficient electron confinement results in appreciable photon reabsorption in the active region. Consequently, light extraction techniques that require long photon path lengths may be inferior in realizing high-efficiency devices for such material systems where significant internal loss mechanisms are present. In order to maximize extraction efficiency in such structures, techniques are required which reduce the photon path length for extraction. These improvements can be realized by modifying the geometry of the LED chip. M. R. Krames et al. reported a truncated-

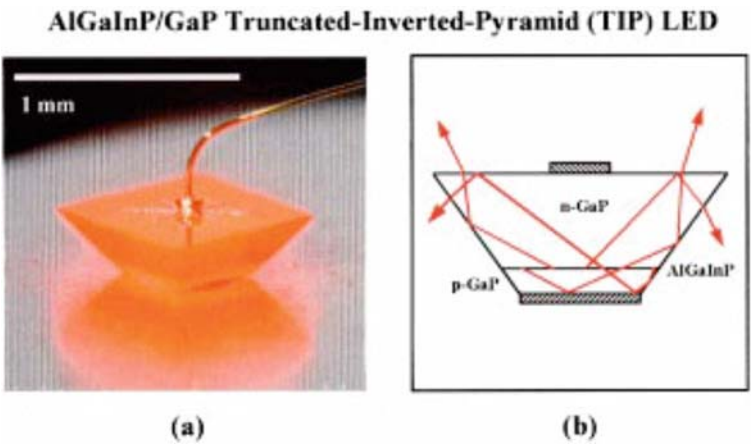

Fig. 5.10 Geometry of the truncated-inverted-pyramid LED: (**a**) photomicrograph of a TIP LED under forward bias; (**b**) schematic cross section showing means by which photons are redirected by total internal reflection [25]

inverted-pyramid (TIP) chip geometry, which provides substantial improvement in light extraction efficiency over conventional AlGaInP/GaP chips. The TIP geometry decreases the mean photon path length within the crystal and thus reduces the effects of internal loss mechanisms. In orange-emitting ($\lambda_p < 610$ nm) devices, peak efficiencies exceed 100 lm/W. And in the red ($\lambda_p < 650$ nm) wavelength regime, peak EQE of 55 and 60.9% are measured under direct current and pulsed operation, respectively. Photographs and schematic structures of the device are shown in Fig. 5.10a, b [25].

5.3.3 Thin-Film Structure

For traditional LEDs with AlGaInP structure, the epilayer is at first deposited on GaAs wafers, but the absorbing GaAs is subsequently removed in the fabrication process. Transfer to a new carrier can be facilitated either on chip or wafer level and usually involves an intermediate metal layer for soldering. Since the final result is a device in which the thin film of AlGaInP active material has been transferred from one wafer to another, the devices are frequently named "thin-film" LEDs. Compared to TS-LEDs with a basically isotropic emission pattern, thin-film LEDs are more directional top emitters which might be an attractive feature for many applications.

S. Illek et al. demonstrated a TF AlGaInP LED with an array of buried cone-shaped microreflectors. The LED structure is shown schematically in Fig. 5.11a–f. The cones are etched through the active layer and covered by a metal and a thin dielectric layer. Small openings in the dielectric provide for electrical conductivity

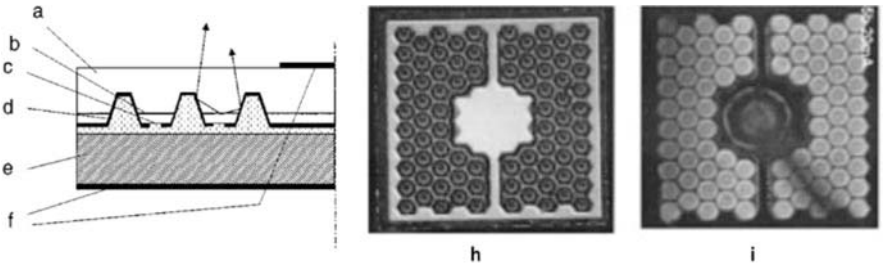

Fig. 5.11 Schematic cross section of a thin-film LED with buried microreflectors, (**a**) AlGaInP LED structure with removed GaAs substrate, (**b**) active layer, (**c**) electrical contacts, (**d**) microreflector with dielectric/metal mirror, (**e**) carrier, and (**f**) electrodes. Top view (**h**) and illumination pattern (**i**) of a 615 nm thin-film LED

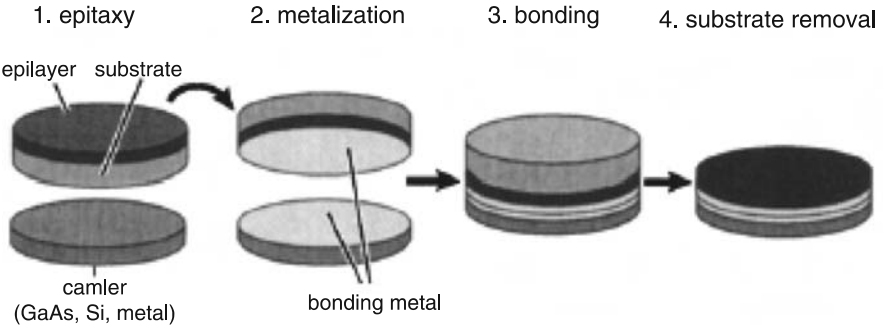

Fig. 5.12 Wafer-bonding processing steps for thin-film LED technology utilizing metal-to-metal bonding by means of soldering

and localize current injection and light generation to the center of the cones. The shape of the microreflectors is designed such that totally reflected light is guided upwards. As a result, the TF-LED with buried microreflector is predominantly top emitting. In contrast to TS-LEDs, very thick window layers in order to increase sidelight extraction are not required. Figure 5.11h shows the top view of a 615-nm device with a structured interface. Although the array of microreflectors is located underneath the planar top layers, it is clearly visible from the top. As shown in Fig. 5.11, the illumination pattern light is generated and extracted around the microreflectors, confirming the principle of operation.

Thin-film LEDs (TF-LEDs) as an alternative to TS-LEDs, offering high extraction efficiency, are made possible by TF technology. Here the epitaxial layer is removed from the original GaAs substrate and transferred to another carrier by means of metal-to-metal bonding. Stringent semiconductor-to-semiconductor wafer-bonding process parameters such as ultraflat surfaces and crystallographic orientation matching are not required for TF-LEDs shown as in Fig. 5.12 [14].

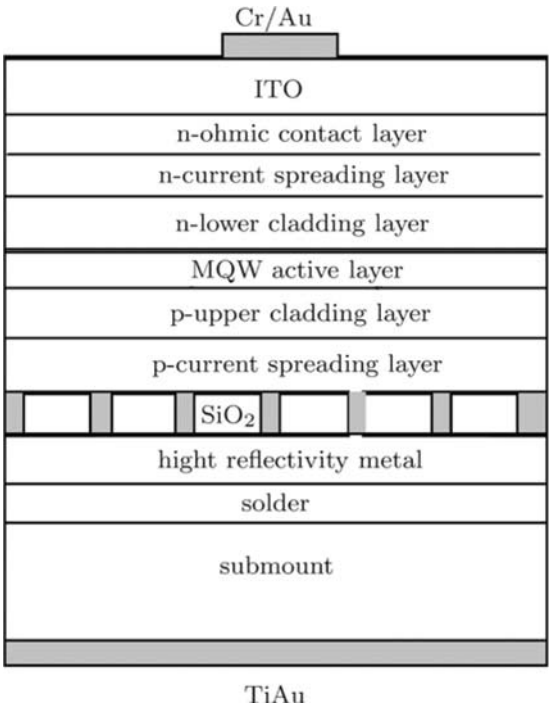

Fig. 5.13 Schematic structure of the ODR-LED [26]

High-brightness AlGaInP thin-film LED with ODR- and transparent-conducting ITO n-type contact has been fabricated by [26]. The schematic structure of the ODR-LED is shown in Fig. 5.13. The normal incidence reflectivity of ODR is 92.7% at $\lambda = 630$ nm (above 92.7% for 620–770 nm). It is found that the sheet resistance of the ITO films (95 nm) is of the order 23.5/□ with up to 92% transparency for 590–770 nm of the spectrum. ITO n-type contact can improve to spread current uniformly and enhance light output power for antireflection. The light output from the ODR-LED with ITO at forward current 20 mA exceeds that of AS-LEDs and ODR-LED without ITO by about a factor of 1.63 and 0.16, respectively. A favorable luminous intensity of 218.3 mcd from the ODR-LED with ITO could be obtained under 20 mA injection, which is 2.63 and 1.21 times higher than that of AS-LED and ODR-LED without ITO, respectively.

Bergenek et al. investigate the use of photonic crystals for light extraction from high-brightness thin-film AlGaInP light-emitting diodes with different etch depths, lattice constants, and two types of lattices (hexagonal and Archimedean). Both simulations and experimental results show that the extraction of high-order modes with a low effective index n_{eff} is most efficient. The highest external quantum efficiency without encapsulation is 19% with an Archimedean A7 lattice with reciprocal lattice constant $G = 1.5\ K_0$, which is 47% better than an unstructured reference device [27].

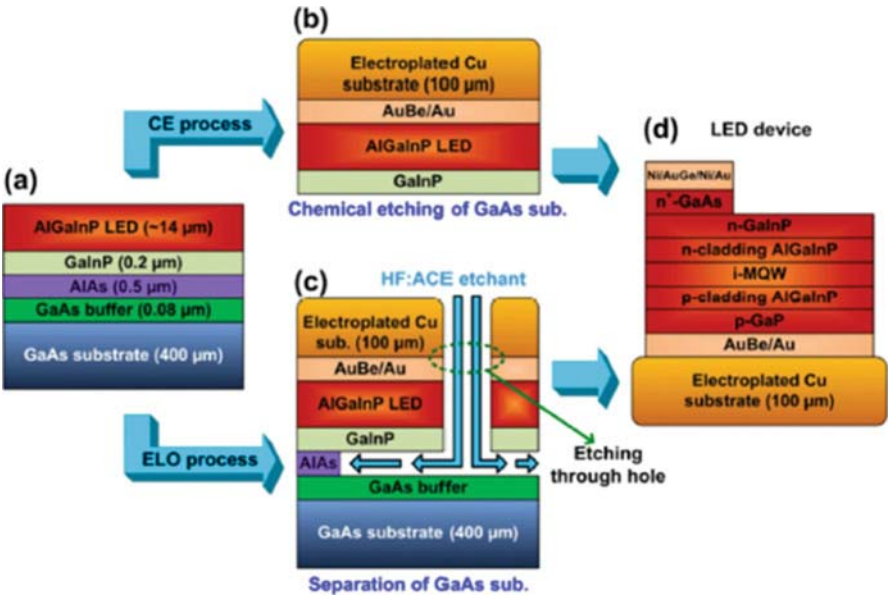

Fig. 5.14 Schematic diagrams of (**a**) epitaxial growth on the GaAs substrate, (**b**) chemical etching process to remove the GaAs substrate, (**c**) ELO process to separate the GaAs substrate, and (**d**) vertical-type AlGaInP LED fabricated on the Cu substrate [28]

Fan-Lei Wu et al. fabricated a thin-film vertical-type AlGaInP LEDs on Cu substrates. By performing the epitaxial lift-off (ELO) process, the LED device can be transferred from GaAs to Cu substrate, as shown in Fig. 5.14. It confirms that the design of patterned Cu substrate is very helpful to obtain the thin-film vertical-type AlGaInP LEDs. Additionally, via the ELO process, the separated GaAs substrate can be reused for production cost down [28].

A twice wafer-transfer technique can be used to fabricate high-brightness p-side-up thin-film AlGaInP-based light-emitting diodes (LEDs) with an indium-tin-oxide (ITO) transparent conductive layer directly deposited on a GaP window layer, without using postannealing. The ITO layer can be used to improve light extraction, which enhances light output power. The p-side-up thin-film AlGaInP LED with an ITO layer exhibited excellent performance stability (e.g., emission wavelength and output power) as the injection current increased. This stability can be attributed to the following factors: (1) refractive index matching, performed by introducing ITO between the epoxy and the GaP window layer enhances light extraction; and (2) the ITO layer is used as the current spreading layer to reduce the thermal accumulation in the epilayers. Figure 5.15 presents a flowchart illustrating the fabrication of thin-film p-side-up AlGaInP-based LEDs by using twice wafer-transfer technology [29]. A substantially higher output power of up to 181 mW at 1000 mA and high wall plug efficiency are obtained.

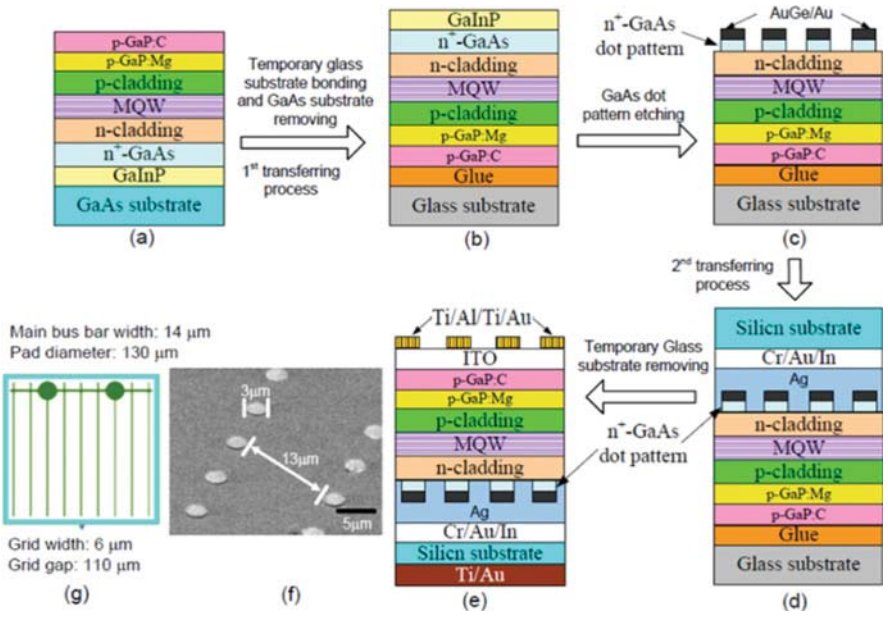

Fig. 5.15 (**a**)–(**e**) Schematic diagrams of fabrication process for p-side-up thin-film AlGaInP-based LED with ITO contact layer, (**f**) top-view image of dot-patterned GaAs on n-cladding surface for the thin AlGaInP-based LED after removing GaAs substrate, (**g**) overall macro schematic of device with detail layout

5.3.4 Flip-Chip Structure

Flip-chip light-emitting diode with a geometric sapphire shaping structure (GSSFC) [30] also was employed to eliminate absorbed GaAs substrate affect shown as in Fig. 5.16.

5.4 AlGaInP/AlGaAs Red/Yellow LED Application in Solid-State Lighting, Display, and Communication

5.4.1 Application in Solid-State Lighting

There are three common architectures for generating white light; the simulated optical power spectra for these three architectures are shown in Fig. 5.17. The phosphor-converted LED (pc-LED) is based on a blue LED to pump yellow-green and red wavelength optical downconverters (typically phosphors), thus producing white light. The hybrid LED (hy-LED) is based on a blue LED used to pump a yellow-green wavelength downconverter, and then the blue and yellow-green light

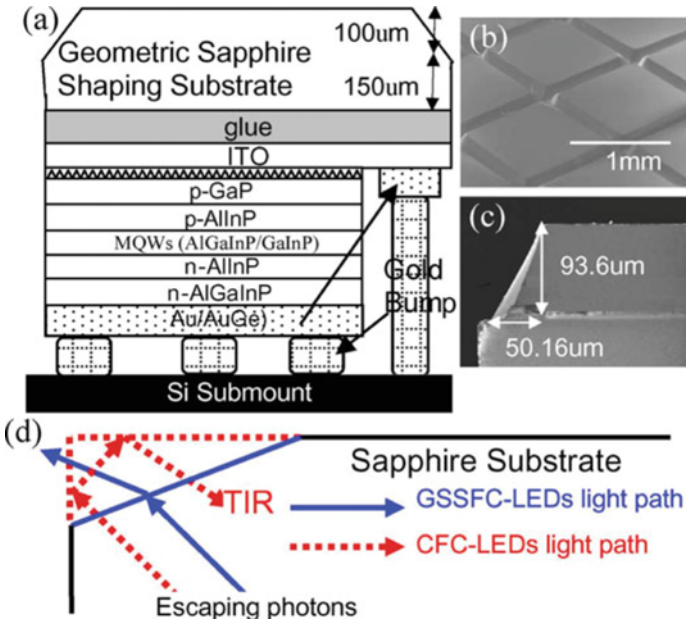

Fig. 5.16 (**a**) Schematic diagram of the AlGaInP GSSFC-LEDs structure. (**b**) SEM figures of the top view of geometric sapphire shaping substrate profile and (**c**) cross-sectional profile. (**d**) Described with the possible photons paths inside the structure of the GSSFC-LEDs and the CFC-LEDs

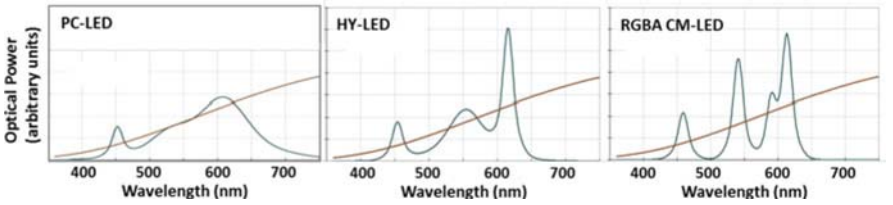

Fig. 5.17 Typical simulated optical power spectra for the three white light LED package architectures considered

is mixed with light from a red LED to again produce white light. The primary colors that compose a red, green, blue, and amber (RGBA) color-mixed LED combine to produce white light.

The current state-of-the art commercial pc-LED, with a luminous efficacy of approximately 137 lm/W, is about 33% efficient. Because of the fundamental Stokes efficiency loss associated with this architecture, 100% efficiency is not possible. Even if all other losses were eliminated, the current pc-LED with its current spectral distribution of optical power can at most have luminous efficacy of approximately 220 lm/W (LER $\times$ Stokes losses). This upper pc-LED potential can be considered approximately equal for warm and cool white. The current 100 nm FWHM wide red

phosphor emission linewidth causes a significant spillover of light into the deeper red, where the human eye is less sensitive, and is a significant contributor to the spectral inefficiency of current pc-LED white light.

Optimization of the lighting quality was aimed at maximizing either luminous efficacy of radiation (LER) or color rendering index (CRI). In this case, people operated with the emission spectra only and did not account for the efficiencies of individual emitters, which could depend strongly on their emission wavelengths. Already in earlier studies, a trade-off between LER and CRI has been revealed, i.e., LER could be maximized at the expense of CRI and vice versa shown as in Fig. 5.17 [31, 32].

Figure 5.18a shows that the white light source comprising of two LEDs and the YAG-phosphor enables achieving the efficacy of ~215 lm/W at CCT = 2400 K and CRI 70–75. At higher CRI values of ~90–95, the efficacy slightly decreases down to ~195–200 lm/W. It should be noted that a very similar solution for the color mixing but with the use of a different phosphor has been suggested earlier at Osram within the Brilliant Mix concept. So high efficacy predicted for the warm white light is achieved due to a rather high "phosphor efficiency" of ~55% compared to WPE of LEDs emitting at the wavelengths close to 560 nm, i.e., deep in the "green gap." At that, the optimal emission wavelengths of two LEDs lie beyond the "green gap" of the LED efficiency (see Fig. 5.18c). Similar phosphor-converted sources, being optimized for generation of cool white light (CCT > 5000 K), provide remarkably lower values of efficacy and CRI (see Fig. 5.18a). In the case of white light source consisting of LEDs only, the transition from three optimized LED emitters (CRI < 92) to four ones (CRI > 92) was found to occur at CRI ≈ 92 irrespective of the correlated color temperature (CCT) of white light [33].

Optimal number of four for individual emitters with almost monochromatic emission spectra and their optimal emission wavelengths was recommended [34, 35] to maximize LER of white light sources at rather acceptable CRI values of ~80–90. Similarly to optimal LER, there is a distinct transition from the optimal number of LEDs of three (two nitride and one phosphide LEDs) to four (three nitride LEDs and one phosphor) occurring at CRI ≈ 92. However, the general behavior of efficacy difference considerably from that of LER is there is a maximum of the efficacy achieved at CRI of ~88–91. At CRI > 92, where four LEDs come into play, the efficacy drops down dramatically. The reason for the drop can been understood from the SPD spectra of the white light sources (Fig. 5.18c).

Quite different results have been obtained by optimization of the light sources consisting of three LEDs and the YAG-phosphor (Fig. 5.18b). In the case of a warm white light (CCT = 2400–3000 K), the maximum efficacy of ~180 lm/W is lower than in combination of two LEDs and phosphor. The reason for this is a lower WPE of the additional LED having the emission wavelength situated inside the "green gap." In the case of the neutral white light (CCT = 4000 K), however, the efficacy of ~190–195 lm/W at extremely high CRI of ~97 can be obtained. In this case, the optimal wavelength of the additional LED moves to the periphery of the "green gap" (Fig. 5.18d), thus increasing the efficacy of the white light source. Comparison of the optimization results obtained for the white light sources consisting entirely of

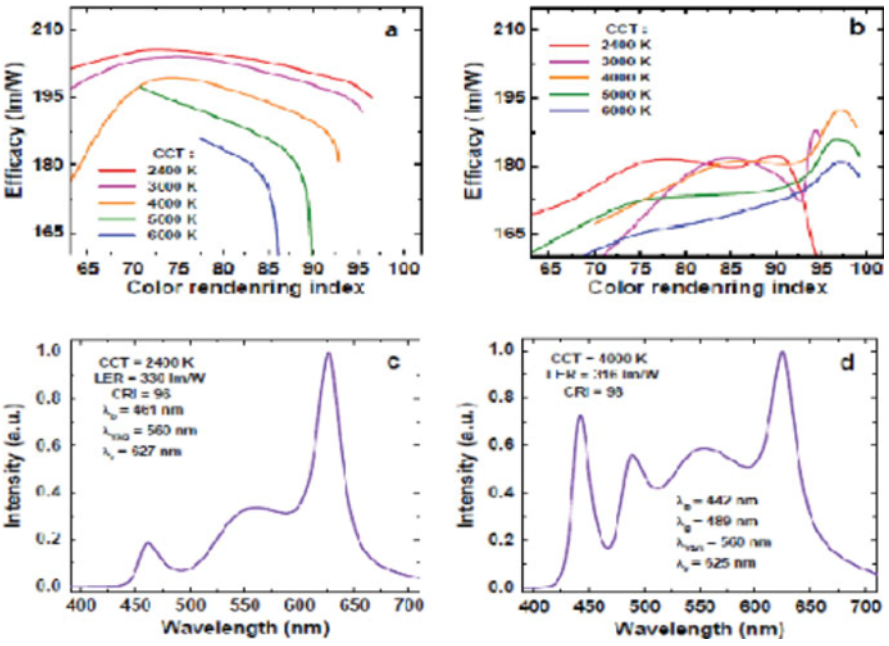

Fig. 5.18 Optimized efficacy of a light source comprising of a YAG:Ce^{3+} phosphor pumped by a blue LED and two (**a**) or three (**b**) LEDs as a function of CRI. Total emission spectra of optimized white light sources comprising of two LEDs and the YAG-phosphor (**c**) or three LEDs and the YAG-phosphor (**d**)

LEDs and those utilizing partial light conversion by a YAG:Ce^{3+} phosphor enables one to conclude that the latter scheme of the color mixing provides at the moment a systematically higher, by ~10%, efficacy at higher CRI values (~90–97 versus ~86–90). The major reason for this benefit is a high overall "phosphor efficiency," which exceeds remarkably WPEs of both nitride and phosphide LEDs in the "green gap" shown as in Fig. 5.19a [33]. In Fig. 5.19b, dashed lines are guides to the eye, illustrating the "green gap": the decrease in efficiency from the blue to the green-yellow and from the red to the green-yellow [36].

One can see that in the case of three LEDs, only the optimal wavelength $\lambda_g = 532$ nm gets deep into the "green gap" of LED efficiency, whereas in the case of four LEDs, both $\lambda_g = 514$ nm and $\lambda_y = 566$ nm are situated inside the gap. Because of a low efficiency of the green-gap LEDs, the latter leads to a dramatic efficacy reduction when four LEDs are utilized in the white light source.

Therefore, the phosphor-converted LEDs will be advantageous over the light sources mixing light from LEDs only, until the "green gap" problem is cardinally resolved. One more conclusion following from the optimization results is that the efficacy of ~200 lm/W at an excellent color rendition (CRI ~ 95) is feasible for phosphor-converted LEDs. So for the high-quality lighting source, AlGaInP LED now gives the most important contribution of low CCT application at the wavelength

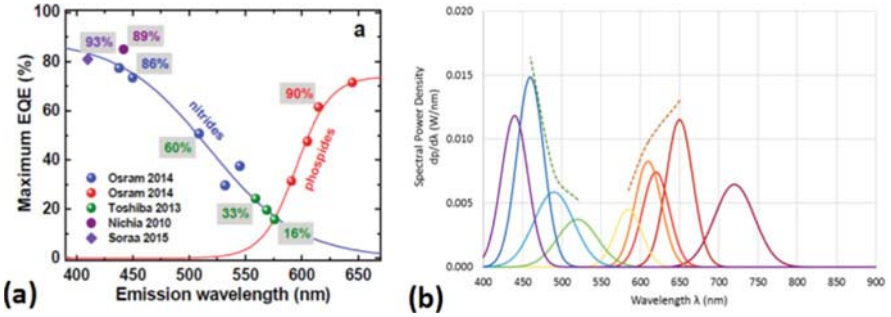

Fig. 5.19 (**a**) Green gap between the GaN and AlGaInP base LEDs as the state of the art, (**b**) spectral power densities of state-of-the-art commercial LEDs vs. wavelength

of 630 nm and for the excellent color rendition (CRI) to solve the green gap problem with the wavelength 566 nm.

As shown in Fig. 5.20a, relative LER is higher with narrower red linewidth, increasing by 15%, from 80% to 95%, as the linewidth decreases from the current 100 nm FWHM to 35 nm FWHM. It is important to note that the improvement continues as linewidth continues to narrow to even less than 35 nm, with no penalty in color-rendering quality. The challenge is thus to develop new red downconverters—phosphors, quantum dots, etc.—with narrower emission linewidth while maintaining high (greater than 90%) internal radiative quantum efficiency. As narrower linewidth red wavelength downconverters are explored, their center emission wavelength is also important. As can be seen in Fig. 5.20b, relative LER is higher the closer the center emission wavelength is to 614 nm. A center wavelength of 623.5 nm would incur a 5% efficiency penalty, and a center wavelength of 630 nm would incur a 10% efficiency penalty.

The hy-LED has a significant efficiency advantage over the more standard pc-LED architecture because the red LED incurs no Stokes deficit in generating red light, and red LEDs have intrinsically narrow linewidths with little spillover into the deep red where the human eye is relatively insensitive. A luminous efficacy of about 280 lm/W, or an efficiency of around 68%, is considered to be the hy-LED upper potential. In contrast, the pc-LED upper potential is only 255 lm/W and could be closer to 220 lm/W if narrower red-phosphor linewidths are not achieved. However, the hy-LED also has two major disadvantages, both associated with the AlInGaP technology used for the red LED. First, the thermal efficiency droop associated with these AlInGaP-based red LEDs is much greater than that associated with InGaN-based blue LEDs. Their different thermal behavior requires a control system to maintain a consistent color point, which adds complexity and cost to the lighting system. Second, AlInGaP-based red LED efficiencies decrease the shorter their red wavelengths, as illustrated in the spectral power densities for various LEDs in Fig. 5.20b. At 614 nm, which can be considered the ideal red peak for lighting as it is just long enough to provide good color-rendering quality but just short enough for good

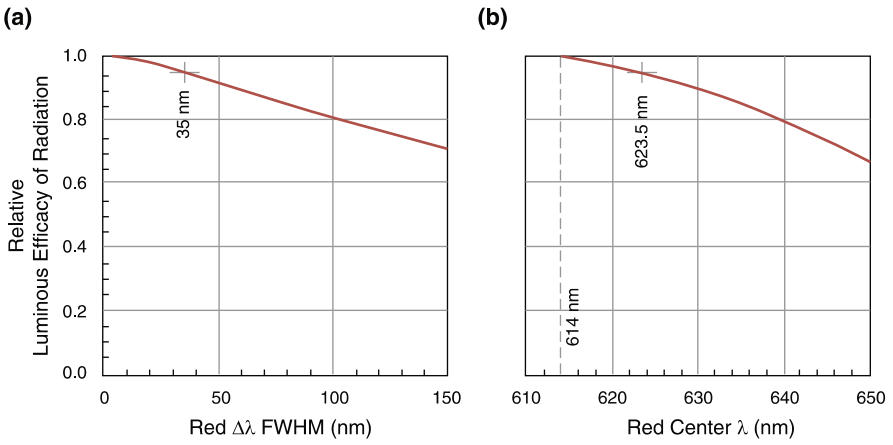

Fig. 5.20 Relative white light luminous efficacy of radidation (**a**) as the FWHM linewidth of the red phosphor increases, for a given red center wavelength of $\lambda = 614$ nm, and (**b**) as the red center wavelength increases, for a given FWHM linewidth of $\Delta\lambda = 7$ nm

sensitivity by the human eye (reasonably high LER), state-of-the-art research LED external quantum efficiencies (EQE) are only about 25%. This architecture faces the challenge of improving the red LED.

Red LED efficiency improvement is an important but tough challenge. Replacing even an ideal narrow linewidth red phosphor in a pc-LED architecture with high-efficiency red LED at 614 nm in a hy-LED architecture would enable approximately 10% improvement, and replacing a non-ideal wide-linewidth red phosphor in a pc-LED architecture would enable approximately 25% improvement. The key challenge is to overcome what appear to be fundamental limits associated with AlInGaP materials: an unfavorable band structure in the shallow red both for carrier transport/confinement and radiative carrier recombination (due to a direct to indirect bandgap crossover). A novel variant of AlInGaP, or a different material system entirely (e.g., InGaN), may provide a solution. The full exploitation of composition and band-structure engineering in semiconductor materials is often limited by strain issues associated with lattice mismatches to common substrates; however, recent research breakthroughs may have overcome these issues including metamorphic epitaxy and nano-compliancy. The development of novel substrates that are lattice-matched to material compositions of interest for 614 nm red LED emission may also reap benefits [38].

5.4.2 Application in Display

The first true all-LED flat panel television screen was possibly developed, demonstrated, and documented by James P. Mitchell in 1977. Inorganic light-emitting

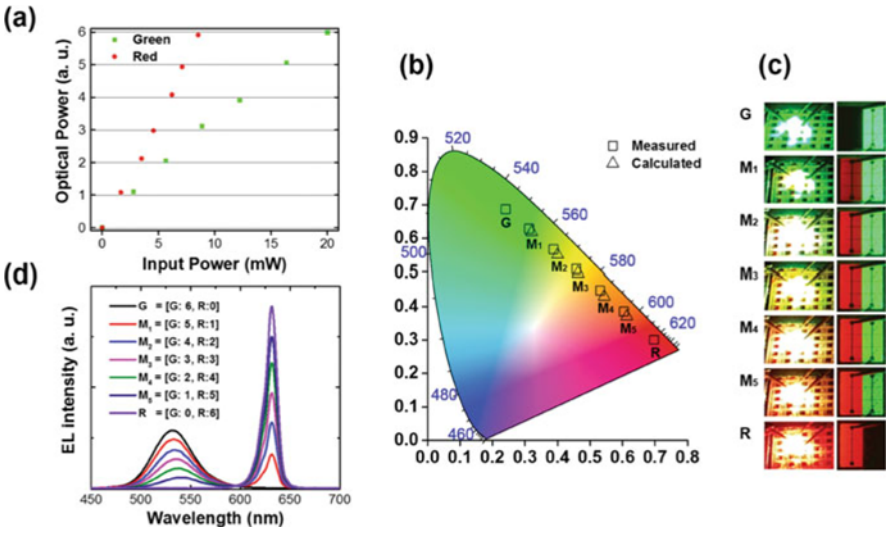

Fig. 5.21 Performance of additive color mixing on the dual color LEDs having a LAS-type array structure realized by adhesive bonding: (**a**) optical output and input powers tuned in the green and red LED subpixels, and (**b**) CIE color coordinates, (**c**) photographs (left) and microscope images (right), and (**d**) EL spectra of the dual color LEDs for the seven color modes. For reference, the CIE coordinates for the seven color modes were calculated using equation

diodes (LEDs) are the brightest and most efficient and stable light source for displays [39–41]. In the current display industry, inorganic LEDs are mainly used as backlights for thin-film-transistor liquid-crystal displays or red-green-blue (RGB) subpixels for outdoor LED displays. From 2016, as the interest in microdisplays such as the ones used in smartphones, smart watches, and head-mounted displays (HMDs) has increased, much effort has been made to apply highly efficient inorganic LEDs as their micro-display light source.

Chang-Mo Kang et al. introduced adhesive bonding and a chemical wet etching process to monolithically integrate two materials with different bandgap energies for green and red light emissions. As shown in Fig. 5.21, the structure can emit various colors by integrating both AlGaInP-based and InGaN-based LEDs onto one substrate which could be a solution to achieve full color with high resolution; the dual-color LEDs integrated by the bonding technique were tunable from the green to red color regions (530–630 nm) as intended [42].

5.4.3 Application in Communication

Visible light is the more suitable for indoor optical wireless communication (OWC) compared to the popular IR band which is preferable for long-haul communication.

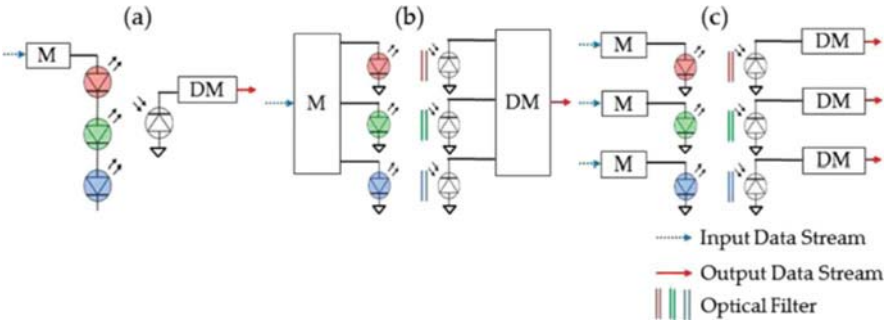

Fig. 5.22 (**a**)–(**c**) Configurations for utilizing multiple light sources in VLC

The high switching capability of LEDs along with other important features such as energy efficiency and longer lifetime makes them the most favorable light source that can be incorporated into visible light communication (VLC). At present, the arrangement of various types of LED is available, each having its own characteristics and unique properties. Based on the features, they can be used in different types of lighting applications. The potential market growth of LED lighting technology is foreseen to be very strong in the coming years, which creates a strong case for this lighting technology to be integrated into VLC [43].

The "multi-chip" approach utilizes three or more LED chips emitting different colors, typically red, green, and blue (RGB), to produce white light. Depending on the light intensities of the different chips, color control can be achieved. Multi-chip WLEDs have lower color rendering index (CRI) than pc-LEDs. pc-LEDs are cheaper and less complex compared to these multi-chip LEDs; however, they have a bandwidth limitation due to the low phosphor conversion efficiency. When using multi-chip LEDs in VLC, there are three ways to utilize the chips: connecting the pins in series to modulate all sources at the same time (Fig. 5.22a), independently modulating each chip for a single communication channel (Fig. 5.22b), and independently modulating each chip enabling parallel communication channels (Fig. 5.22c).

These methods are depicted in Fig. 5.22; the figure "M" denotes modulation and "DM" denotes demodulation. In the first method, we see a considerable bandwidth enhancement compared to pc-LEDs, since there is no slow phosphor component in the generated light. Optical filtering is used in pc-LED systems to suppress the slow phosphor decay and extract the much faster blue response, but this comes at the cost of losing a considerable portion of the received signal power. However, in multicolored sources, almost the entire optical power of the emitted spectrum for each channel can be harnessed by optical filtering. This is because no phosphor wavelength converters are present. The second method is utilized in the newly introduced color shift keying (CSK) modulation by IEEE. The intensity of each color channel generates a specific color point in the CIE 1931 color coordinates. This can be utilized as constellation points for modulation purposes. Optical filters are required at the receiver to extract the intensities of each color channel to generate

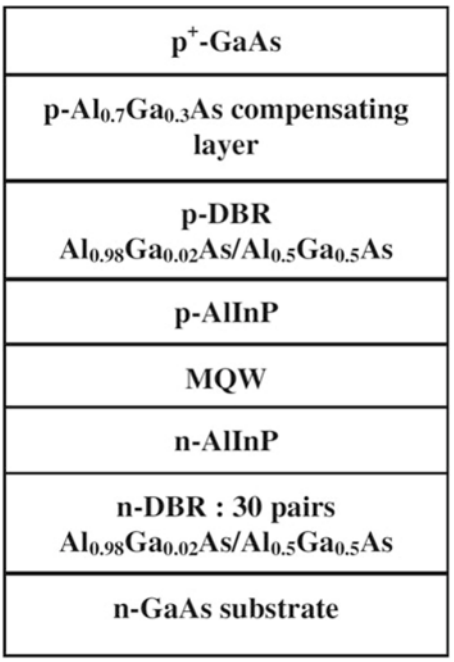

Fig. 5.23 Schematic diagram of AlGaInP-based LEDs for VLCs [46]

the color coordinate. This method is discussed elaborately in Section IV-F. In the third method, each color can be modulated independently, provided white color balancing is maintained. At the receiver, optical filtering is used to extract data from each color channel. This system has the potential for wavelength division multiplexing (WDM) [44, 45].

In 2008, Oh et al. investigated the effects of reflectivity of p-DBR and the number of QWs in active layers on the spectral characteristics and optical power of RCLEDs, in order to develop high-power RCLEDs appropriate for VLCs. The schematic diagram for the AlGaInP-based LED structures for VLC application is shown in Fig. 5.23. As the reflectivity of p-DBR increased, the FWHM of EL spectrum was reduced from 12.3 to 3.6 nm, whereas the relative integrated intensity decreased from 1.0 to 0.37, which was attributed to the improvement of spectral purity of the peaks with the inphase condition. As the number of QWs decreased, the optical power increased owing to the reduction of the optical loss of the recycling light in the active region. Using the optimized structural conditions, we demonstrated RCLEDs having a modulation speed up to 130 MHz in free space, which clearly showed that the optimized RCLED structure is a promising candidate for VLCs [46].

5.5 III-Nitrides Red/Yellow LED

5.5.1 GaN-Based Yellow Light-Emitting Diodes

AlGaInN-based LED, the wavelength of the light, can cover up all visible range. Same for GaN-based LED, GaN-based LED can basically cover all the visible light wavelength range. But there is a huge deficiency for this kind of material which is for GaN-based LED, the lighting efficiency is extremely unsatisfactory when the wavelength of the light is in long range (yellow light or red light). GaN can reach an acceptable efficiency when the wavelength of the light is short. For example, the efficiency of GaN-based blue light emitter can reach 70% [47]; for green light emitter, the efficiency can also reach 30% and above [48]. This phenomenon is called "green gap," in which the efficiency of LEDs has a huge drop when the wavelength of the light emitted is beyond the green light wavelength (550 nm to 600 nm especially) [49]. That does not only happen with GaN-based LED; that phenomenon has also happened with AlGaInN-based LED.

Unlike GaP or GaAs materials, the efficiency of the GaN-based light emitter has less sensitivity to slab staggering [50]. The increase of the GaN-based yellow light emitter efficiency can bring us significant improvement in many ways. The first improvement is white light illumination industry. This improvement is revolutionary which means fluorescent powder can be removed from the lighting system by using true yellow light which can create real white GaN-based light. On the other hand, the light quality of display and white illumination can be greatly enhanced by improving the efficiency of yellow light to overcome the "green gap". Also this can be used as the reference for blue and green light emitter to boost the efficiency even further. Furthermore, the highly efficient yellow light emitter can be used as a bedding for GaN-based red light emitter to accomplish full visible light spectrum in GaN LED [51].

Figure 5.24 shows that the efficiency varies with light wavelength changes, in which there is a gap showing when the wavelength is at green light [52].

LED efficiency reduces as current increases. This can be explained by several different reasons. The first reason is that when the density of the current pass through the diode gets increased, charge carriers will leak out from the active area (lighting area) [53]. This will lower the working efficiency. The second reason is auger recombination, which is a non-radiation recombination. The rate of recombination is proportional to the cube of the charge carrier concentration. When the charge carrier becomes more concentrated, the auger recombination will happen more frequently even in a domination condition; in that case the LED efficiency will drop [54].

LED efficiency reduces as temperature rises. When the temperature of the LED increases, the internal quantum efficiency will drop. Some studies claim that the reason for the efficiency drop as temperature rises is quite complicated, which include many factor and reasons such as defect, charging the carrier, thermal stress, heat dissipation, etc. [55]. Currently the drop of efficiency as temperature of the device rises has been treated as normalcy, but GaN-based yellow light emitter has

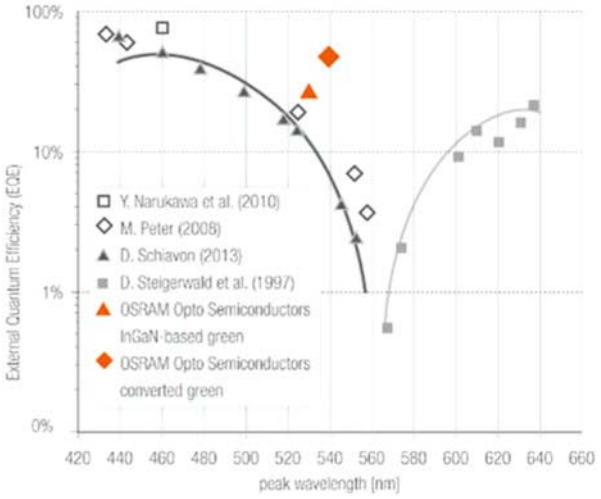

Fig. 5.24 Green gap, there are several factors that will reduce the efficiency of the GaN-based LED [52]

relatively lower temperature sensitivity compared with AlGaInP-based LED, which means the efficiency drop for GaN-based diode is less than AlGaInP-based diode if they have the same amount of temperature increase [56].

LED efficiency reduces as wavelength increases [57]. The wavelength of GaN-based LEDs can be changed by using different indium composition in the InGaN/GaN multiple-quantum-well (MQW). The higher the indium level, the longer the wavelength will be. But the problem is that the structure of InN and GaN has a significant difference in lattice constant, which means when the concentration level of indium increases, the lattice mismatch of quantum well of InGaN and GaN will be greater; this will cause an increase in stress. In this case, the piezoelectric effect of InGaN will reduce the overall efficiency. On the other hand, since both InN and GaN are non-dissolvable solids, when the concentration of In excesses a certain amount, InN will separate out that will reduce the crystalline quality and LED working efficiency. So the key point to optimize the efficiency of the long-wavelength light-emitting diodes is to reduce the stress force acting on quantum well and optimize the crystalline quality [58]. This makes the study on efficiency with wavelength droop considerably valuable and meaningful.

5.5.2 Progress on GaN-Based Yellow LED

The research of GaN yellow LED has begun very early by Nakamura in the 1990s [59]. And he successfully produced GaN-based yellow LED. But the epitaxial structure of the yellow LED is the same as both blue and green LEDs, in which

yellow light is accomplished by reducing the growing temperature to increase the mixture concentration of indium. So the product he got was extremely inefficient in which the efficiency is only about 1%. And the efficiency for blue and green LEDs is 7.3% and 2.1%, respectively. For the next several decades, the efficiency of both blue and green LEDs has increased more than ten times. But the development of yellow LED technology is very limited. Also the facilities that yellow LED needs are not developed [56]. At present there are two directions to study GaN-based yellow LED. The first one is based on semipolarized or nonpolarized GaN. The main idea is to reduce piezoelectric field to increase lighting efficiency. The indium composition is relatively high in InGaN QW of Yellow LED. However, there is larger lattice mismatch between high indium composition InGaN QW and GaN carrier, which will bring compression stress to QW and leads to piezoelectric field. And piezoelectric field will separate carrier and make carrier overflow, which will reduce the efficiency. The second theory is based on low-dimensional structure of InGaN-like quantum dot or quantum wire. Using quantum dot of InGaN creates concentrated indium localized state, in which the localized state can restrict carrier effectively and polarization inside the localized state is comparatively less.

For the first theory, Funato and his colleague have successfully produced GaN-based yellow LED on (11–22) semipolar plane template in 2006 [60]. They believe that the mismatch between GaN well and GaN base should be very small, which can strongly reduce the stress inside the quantum well in order to reduce the negative effect created by piezoelectric field. But sadly the result is unsatisfactory, in which the efficiency of the new LED does not have much improvement compared with the previous LED. Then in 2008, Sato and his colleagues improved that technology by increasing the crystalline quality and reducing the dislocation density inside the quantum well [61]. The high power yellow InGaN LEDs with a peak emission wavelength of 562.7nm grown on low extended defect density semipolar (11–22) bulk GaN substrates by metal organic chemical vapor deposition. The report says when the LED is under a pulse current at 200 mA, the light intensity reaches 30 mW, which means the external quantum efficiency is nearly 6%. That is a significant improvement comparing with the previous result (1% efficiency). But the problem is that the wavelength for the light is only about 550 nm which is a bit short comparing with proper yellow light. After that, Yamamoto and his colleagues produced GaN green-yellow LED with a wavelength of 552 nm that grew at GaN (20–21) semipolarized substrate in 2010. The external efficiency for the new product can reach 12.6% in low current density condition [62]. There are several advantages for this kind of theory (produce yellow LED by using semipolarized or nonpolarized substrate). First is that the product given by homoepitaxy substrate usually has better crystalline quality. Second, the stress can be decreased since quantum well reduced when LED grows. Also the piezoelectric on the quantum well p-n junction is nearly zero. Those advantages can help boost LED efficiency. But the drawback is that the substrate is very difficult to get and the problem can be hardly avoided. The polarized c-GaN substrate is very hard to produce already, for semipolarized or nonpolarized substrate is even harder. This drawback makes the theory only be used

in laboratory study. Applying the theory into scale production is hardly going to happen [56].

Since the limitation of the first theory, people are trying to find some solution by the second theory, by using quantum dot or quantum wire. In 2005, Seong-Ju Park et al. investigated the enhancement of phase separation in the InGan layer grown on a GaN layer with a rough surface, in order to form self-assembled In-rich quantum dots in the InGaN layer [63]. InGaN films were grown on both smooth and rough GaN surfaces with a root mean square (rms) roughness of 2.5 and 23.5 Å, respectively. The cross-sectional transmission electron microscopy (TEM) images of InGaN layers grown on smooth and rough GaN surfaces was analyzed by authors. The images show that the rough GaN layer induces phase separation in InGaN film even though the thickness of the InGaN layer is less than the critical layer thickness and the InGaN with a low In composition. For the sample that grew from rough surface substrate, obvious segregation of quantum well can be easily observed. By using that character, they can produce LED with obvious segregation indium in InGaN quantum well. This is a valuable beginning of the quantum dot technology; the theory provides both technological means and direction for further work.

With the progress before, Soh and his colleagues create nanometer-scaled pattern on a GaN template by etching method; then they produce InGaN/GaN quantum well on the GaN template [64]. The produced quantum well has lower edge dislocation density and less stress; also the InGaN quantum dot density can reach 4.5E9. LED with this specific structure can emit yellow light, and comparing with ordinary quantum well structure, the new structure can provide higher light intensity and less wavelength drift. After they observe the phenomenon, they create a structure to describe and explain the benefit (as shown in Fig. 5.25), which when the concentration of the InGaN is not equally distributed inside the quantum well, the area with more concentrated indium will have less energy gap in which charge carriers will be trapped in, also since the density of indium is relatively higher around the quantum well, which can create a good buffer against stress. So quantum well is a qualified lighting area.

By using this idea, Lv and his colleagues optimized the growing method by creating better growing condition for the quantum base [65], which includes using higher temperature when the base is growing and using hydrogen instead of nitrogen that can produce better base quality. That method successfully produced InGaN quantum well-based green-yellow LED with longer wavelength. But the efficiency for the device was not clearly recorded.

From previous papers, the most difficult part of InGaN quantum dot-based LED is that quantum dots need to be distributed uniformly inside the material and the crystalline quality needs to be ensured at the same time. On the other hand, the size of lighting quantum dot is limited which can hardly suffer huge current density. Also the material-generating craft is hard to control with bad stability.

The development of GaN-based yellow LED needs to utilize well-developed machines, tools, and growing crafts and use blue LED and green LED as references to innovate new material and crafts. This is a very feasible way to increase the efficiency of GaN-based yellow LED in the future [56].

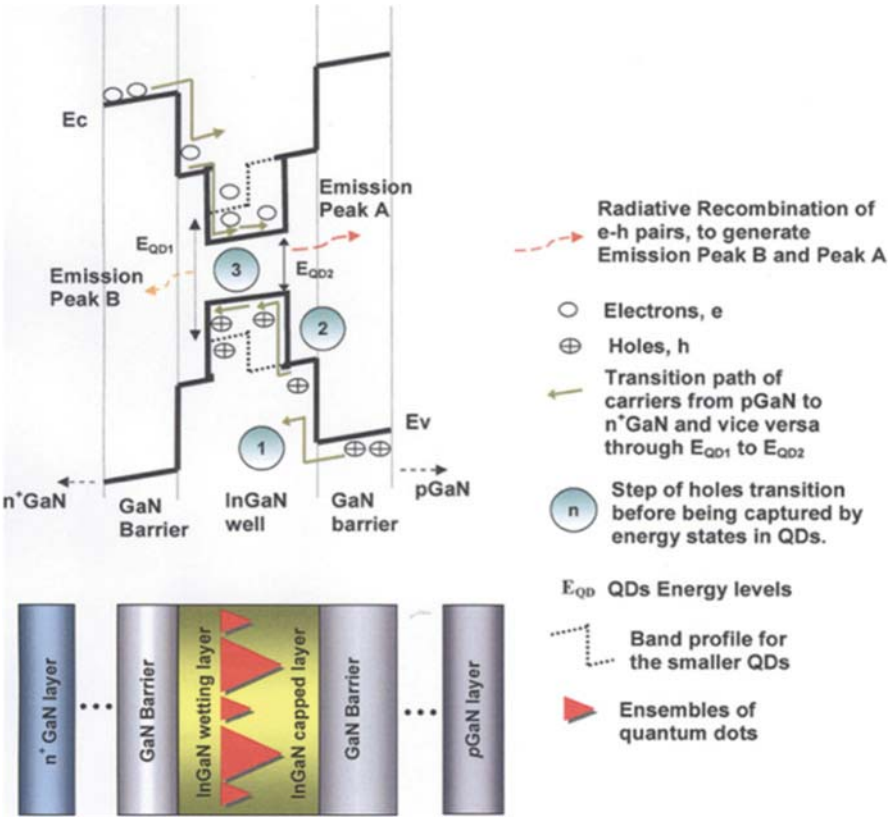

Fig. 5.25 Color online schematic band diagram of bimodal distribution of QDs embedded in the InGaN well layer of LEDs with illustration of their carrier transport kinetic [64]

5.5.3 Substrate Technique

Substrate is the fundamental of LED epitaxy growth, which will influence the quality of the crystalline quality, stress situation, and lighting method. There are several factors that need to be considered: the lattice mismatch between substrate material and epitaxy material, the chemical stability of substrate material, and the cost of substrate material. Currently the substrate material can be chosen from sapphire (Al2O3), silicon carbide (SiC), and silicon itself (Si). Also there are some other choices like GaN and AlN, but those materials are rare and have not been used in scaled production [66].

Currently the most common material for substrate is sapphire; most GaN-based LEDs on the mark were using sapphire as substrate. This is because sapphire has been used as substrate for a very long time which makes the craft technique well

developed. Also sapphire has very good chemical stability. But the problem for this material is that the heat conduction is comparatively lower.

As for SiC, the lattice constant and the dilatation coefficient for SiC are similar with GaN, and also SiC contains good heat conduction and good optical properties (index of refraction is high); those advantages make SiC a quite competitive material for making substrate for GaN-based LED. But the problem is SiC is hard to produce which means the cost for SiC is comparatively higher. So this material is not currently widely used [67].

Si is a substrate material with huge potential; this is because silicon substrate is easy to produce. Due to the development of semiconductor, silicon-related material craft technique is quite mature (cheap). Also, silicon substrate is good at both heat and electric conduction and easy to assemble to electronic devices. But the problem is silicon has significant lattice mismatch and heat mismatch with GaN. At present, people are finding solutions to solve those problems. Some researchers use AlN buffer layer technology to reduce the negative influence caused by lattice mismatch [68]. As for heat mismatch problem, some designed pattern will help reduce epitaxy layer fracturing pheromone caused by heat mismatch between those two materials [69].

Since silicon as substrate has been successfully used to produce high-quality blue and green light LEDs, if the white light technique wants to be accomplished, using silicon as substrate for yellow LED seems the most suitable choice [70].

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Chapter 6
The InGaN Material System and Blue/Green Emitters

Ning Zhang and Zhiqiang Liu

6.1 Blue LEDs

6.1.1 Buffer Layer for the Growth of GaN and Growth of High-Quality GaN Materials

III-nitrides can be of wurtzite (Wz), zincblende (ZB), and rocksalt structure. For bulk AlN, GaN, and InN, wurtzite is the thermodynamically stable structure under ambient conditions, which has a hexagonal unit cell and thus two lattice constants c and a. The space grouping for the wurtzite structure is $P6_3mc$ in the Hermann-Mauguin notation. The Wz structure consists of two interpenetrating hexagonal close-packed sublattices with different types of atom, offset along the c-axis by 5/8 of the cell height (5c/8), (0001) planes of Ga and N pairs stacked in an ABABAB sequence. Atoms in the first and third layers are directly aligned with each other. Three surfaces are of special importance in nitrides, which are (0001) c-planes, (11–20) a-planes, and (1–100) m-planes. Other surfaces could also be observed in nitrides nanostructures, i.e., (1–102) r-planes and (11–23) n-planes. For epitaxy GaN thin film or single crystals, determining the orientation is not straightforward and will depend on growth conditions, substrates, or doping.

Because bulk gallium nitride crystals are still not commercially available now, gallium nitride materials are mainly grown on substrates of another material such

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as sapphire, silicon carbide, silicon, etc. Normally, the lattice constant mismatch is the most important factor for a material as a suitable substrate for gallium nitride crystals heteroepitaxy. Moreover, properties other than the lattice constants including the material's crystal structure, surface finish, composition, reactivity, chemical, thermal, and electrical properties can also influence quality of the gallium nitride epitaxial layer; those properties of a substrate for gallium nitrate crystals should be considered roundly.

Sapphire, single-crystal aluminum oxide, was the original substrate used in Maruskas and Tietjen's pioneering study of GaN epitaxy by hydride vapor-phase epitaxy (HVPE) in 1969 [1]. GaN epitaxy on c-plane sapphire result in c-plane oriented films but with a 30° rotation of the in-plane GaN crystal directions with respect to the same directions in the sapphire. The rotation of the (0001) nitride plane with respect to the sapphire (0001) occurs to reduce the lattice constant mismatch, and the mismatch would be 30% without this rotation. However, the large lattice constant mismatch still reaches 16% [2] between the substrate and the epilayer to lead to high dislocation density in the GaN epitaxial film [2]. In order to improve the surface morphology and crystalline quality of epitaxial film, two-step growth process is widely adopted to reduce problems caused by lattice mismatch in growing gallium nitride (GaN) with metal-organic chemical vapor deposition (MOCVD) on a sapphire substrate. In 1986, Amano et al. used low-temperature AlN buffer layer to significantly improve the optical and electrical properties of the GaN layers grown on sapphire [3, 4]. And later, Wickenden et al. [5] and Nakamura [6] independently developed the use of low-temperature GaN buffer layer. Usually, before the growth of a LT buffer layer, the nitridation of sapphire is carried out to reduce the defect density, enhancing the electron mobility, and reducing the yellow luminescence in subsequently deposited films. Sapphire is nitridated by exposure to ammonia/hydrogen gas mixtures in MOCVD. After nitridation, a LT GaN or AlN buffer (usually about 500–550 °C for MOCVD) dramatically improves the surface morphology and crystalline quality of GaN sequentially deposited at HT (usually about 1100 °C for MOCVD) on sapphire. Annealing at a high growth temperature crystallizes the amorphous buffer layers into films with preferential orientation ([0001] for c-sapphire) and reduces the density of low-angle grain boundaries.

Generally, sapphire is commonly used as the substrate for III-nitride LEDs. However, the large lattice mismatch and thermal expansion coefficient mismatch between GaN and sapphire substrate cause high TDD in the range of 10^8 to 10^{10} cm^{-2} [7]. TDs are very harmful to electronic and optoelectronic devices because they act as non-radiative electron-hole recombination centers [8]. Thus, it is always desirable to reduce the number of TDs in GaN. There are several different growth approaches to reduce TDD in GaN films recently. Epitaxial lateral overgrowth (ELOG) [9] and its derivatives can significantly reduce TDD, but it inevitably needs to interrupt the growth process. Meanwhile, growing on PSS is another alternative way, and it can also reduce TDD efficiently [10]. Different ELOG techniques with ex situ substrate patterning are widely used to reduce the TDD and grow high-quality GaN layers [11–13] which have also been adapted to AlGaN layers [14, 15]. But, there are some drawbacks for ex situ ELOG because of

long ex situ masking procedures and the presence of localized TTDs in the window regions. Moreover, a relatively thick overgrowth of the mask is essential to coalesce the wing area. In order to overcome the drawbacks of ex situ ELOG, in situ ELO techniques are developed, especially in small scales. In situ ELOG techniques are effective to improve the quality of GaN epilayers comparing to the ex situ ELOG techniques. Tanaka' work [16] shows that SiNx intermediate layers deposited in situ are an effective tool to grow high-quality GaNe pi layers. However, Engl et al. [17] observed that SiNx interlayers do not reveal any visible improvement in crystal quality of AlGaN layers, since AlGaN does not grow as selective as GaN [18]. Forghani et al. use the implementation of SiNx for AlGaN layers with 20% Al content and developed an appropriate model for the effect of SiNx interlayers on the reduction of edge-type TD in AlGaN [19].

Extensive research on growth conditions for high-quality gallium nitride crystals growth on sapphire has been done to reduce TDD, 3D-2D growth process [20] was applied, and cone-shaped patterned sapphire substrates were used as substrates. During the 3D growth process, growth condition was to adjust to control the facets including {1$\underline{1}$01} inclined facets and top (0001) plane. The thickness of 3D layer should be near to the height of cone-shaped patterns on which there were little GaN deposited. At the end of the process, cone-shaped patterns were surrounded by 3D layer. In the following 2D growth process, inclined side facets coalesce quickly, and the interaction of TDs with the side facets causes the TDs to bend over. Some samples of GaN films on PSS were grown by a Thomas Swan close-coupled showerhead (CCS) MOCVD where a 633 nm laser interferometer was used to monitor the growth. Trimethylgallium (TMGa) and ammonia (NH3) were used as precursors, and pure hydrogen was used as the carrier gas. At the onset, the PSSs whose specification was 2 um (bottom) $\times$ 1 um (space) $\times$ 1.5 um (height) were annealed at 1060 °C in H_2 atmosphere, then cooling down the reactor to 530 °C, and an about 30-nm-thick GaN nucleation layer was deposited. Three-dimensional layer was grown on the nucleation layer which is recrystallized by ramping up the temperature to 1045 °C with the rate of 1.5 °C/s and holding the temperature for about 90 s. During this period, low temperature (about 1010 °C) and V/III ratio (about 670) were set to encourage the 3D growth. Besides, in order to optimize the parameters of 3D layer growth, the pressure was varied from 4.5×10^4 Pa to 6.5×10^4 Pa, and the growth time was adjusted from 1000 s to 850 s and 750 s. After the 3D layer, 2D growth process for merging quickly was recommended. Then raising the temperature (1060 °C) and V/III ratio (about 1200), a pressure was set to 2.0×10^4 Pa. Furthermore, another sample was grown with normal process to compare with the 3D-2D process. After growth, morphologies were examined by SEM at different stages of sample A. Moreover, TDD was assessed by etch-pit density (EPD) measurements, and XRD was used to support the results.

Morphological evolution of GaN layer growth with the 3D-2D process can be obviously observed in Fig. 6.1. The growth temperature and reflectance transient are taken from the sample and the morphology at different stages of growth. As shown in inset (1), amorphous GaN is deposited uniformly on the PSS after the nucleation. And the thickness of nucleation layer is about 30 nm. In the duration,

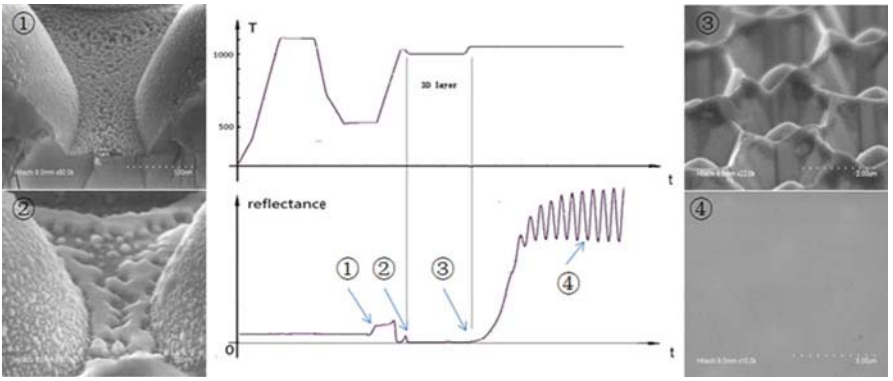

Fig. 6.1 3D-2D growth temperature and reflectance transient taken from sample (4.5×10^4 Pa, 1000 s 3D layer growth time). SEM insets show the morphology at different stages of growth as the nucleation before (1) and after recrystallization (2), at the end of 3D layer (3), and after coalescence (4) [12]

the reflectivity increases with the nucleation layer growing because the reflectivity is in proportion to the thickness of nucleation layer. As nucleation layer recrystallize under a high temperature, the materials are redistributed. GaN grains are formed, and then they gain or lose particles from one grain and transport to another; thus smaller grain shrinks, while larger grain grows. Finally the platelet-shaped islands are mainly left on the space of PSS, as can be seen in the inset (2). In the 3D layer growth, growth conditions are adjusted to achieve that vertical growth rate is much higher than lateral growth rate. 3D layer surrounds the cone-shaped pattern, and the thickness of 3D layer is near to the height of cone-shaped pattern. Furthermore, the hexagonal recesses have {1$\underline{1}$01} incline facets and narrow (0001) plane. In the following 2D process, lateral growth rate is much higher than vertical growth rate; thus the incline facets coalesce quickly, and the interaction of TDs with the side facets causes the TDs to bend over. However, TDs in the (0001) surface will not bend over. The phenomenon can be observed in Fig. 6.2, and dislocations above the patterns bend over (in circle 1), while those among the patterns extend to the surface (in circle 2).

The condition of 3D layer is critical to reduce the TDD. Pressure and growth time are changed for the samples. All samples are etched in hot H_3PO_4/H_2SO_4 (3/1) solution, and then EPD is examined by the AFM. And XRD is used to calculate TDDs. For XRD, the measurements of rocking curves of (002) and (102) are carried out, and the XRD (002) and (102) rocking curves of sample (4.5×10^4 Pa, 1000 s 3D layer growth time) reach 211 arcsec and 219 arcsec, respectively.

And the densities of screw-type dislocation D_S and edge-type dislocation D_E can be estimated from the XRD FWHM values based on the following formulas [21]:

$$Ds = \frac{\beta_S^2}{4.35 \times |b_S|^2} = \frac{\beta_{002}^2}{4.35 \times (b_s \cdot \cos\alpha)^2} \tag{6.1}$$

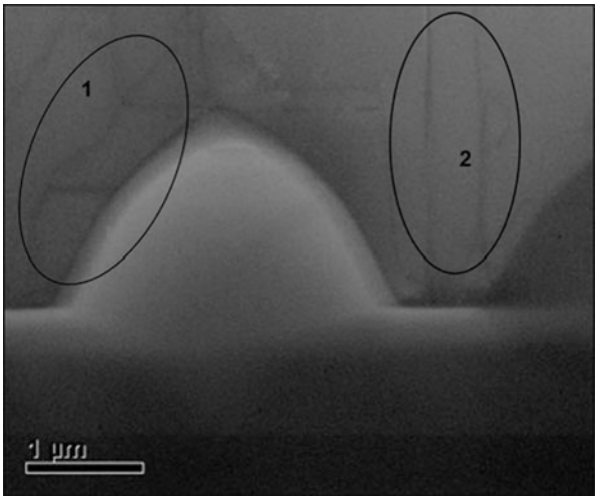

Fig. 6.2 Bending-over TDs and unbending-over TDs [12]

$$D_E = \frac{\beta_e^2}{4.35 \times |b_e|^2} = \frac{\beta_{102}^2 - \beta_{002}^2}{4.35 \times (b_e \cdot \sin\alpha)^2} \tag{6.2}$$

where $|b_S|$ and $|b_e|$ are the Burgers vector sizes of the screw-type dislocation ($|b_S| = 0.5185$ nm) and edge-type dislocation ($|b_e| = 0.3189$ nm), respectively, and β_{002} and β_{102} are XRD FWHM values of (002) and (102). And α is the angle between the reciprocal lattice vector (K_{hkl}) and the (001) surface normal. With the FWHM of (002) and (102) rocking curves of sample (4.5×10^4 Pa, 1000 s 3D layer growth time), the dislocation density is 1.685×10^8 by calculation, and it meet the EPD 9.80×10^7 of the sample, which is shown in Fig. 6.3, AFM image (5 um × 5 um) of sample (4.5×10^4 Pa, 1000 s 3D layer growth time) after wet chemical etching.

TDDs of the samples which grew with the 3D-2D process are much less than that of the sample of normal process which grew with normal process. Besides, TDDs increase as the pressure increases. And TDDS increase as the growth time decreases. Since the pressure also effects on the growth rate, both pressure and growth time relate to the thickness of 3D layer. Thus, the thickness is critical parameter for reducing the TDDs. Three-dimensional layer has the incline facets {1$\underline{1}$01} and (0001) plane; TDs in the (0001) surface will not bend over, so small area of (0001) plane is good for reducing TDDs. Generally, the thickness of 3D layer is recommended to be near to the height of cone-shaped pattern to further reduce TDDs.

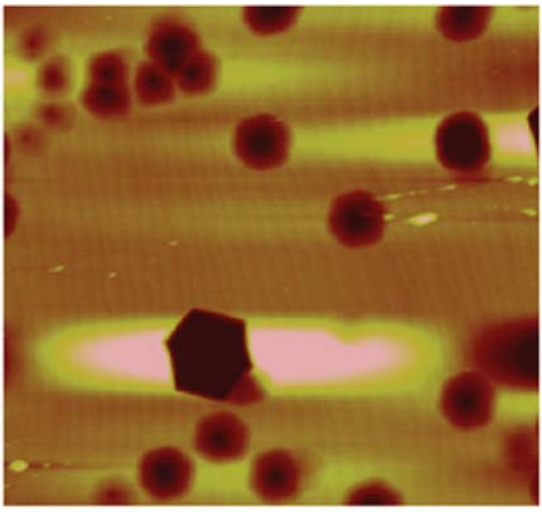

Fig. 6.3 AFM image (5 um × 5 um) of sample (4.5×10^4 Pa, 1000 s 3D layer growth time) after wet chemical etching [12]

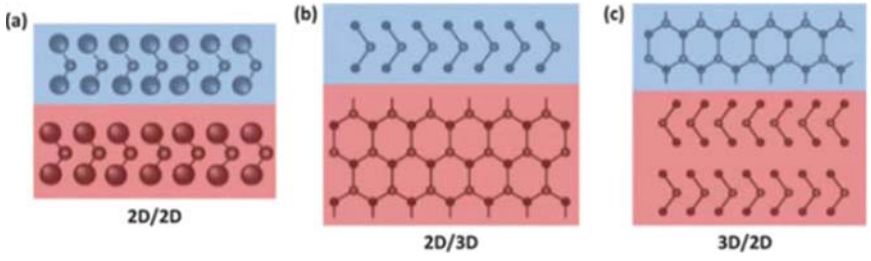

Fig. 6.4 The principle of vdWE. (**a**) 2D material grown on 2D material. (**b**) 2D material grown on 3D material. (**c**) 3D material grown on 2D material

6.1.2 New Buffer Layer for High-Quality GaN Materials

Since the native substrate of GaN is very expensive, we usually use Si [22], sapphire [23], and SiC [24] as the substrate to grow GaN films, which is called heteroepitaxial growth. In this way, there are many strong chemical bonds at the interface to connect the epilayer and the substrate, so that it can lead to many defects and dislocations during the epitaxial process because of the mismatch, so the quality of the GaN films reduced. To solve this problem, a buffer layer like AlN or GaN grown at a lower temperature was introduced, and it can decrease the defects to below 10^8 cm^{-2}. Recently, another growth mechanism was reported to improve the heteroepitaxial growth of GaN. That is van der Waals epitaxy (vdWE) [25], which means the connection between the substrate and the epilayer is weak in van der Waals interactions rather than strong chemical bonds, as shown in Fig. 6.4, so we can ignore the mismatch in this way.

For vdWE, graphene is a perfect candidate, for it is a 2D material without darling bonds on the surface, and it is hexagonal structure like GaN in plane. Besides, it is van der Waals interactions between different graphene layers, so it is easy to separate them. Since then, what can we do by using graphene?

Firstly, we can use graphene as a buffer layer.

As we said before, graphene acting as a buffer layer can prevent the dislocations caused by mismatch and then improve the crystal quality. However, there is an obstacle we need to face with; it is the nucleation on the graphene surface. Indeed, without the dangling bonds, there is less mismatch, and also it cannot provide the sites for Ga or N atom to nucleate. So we need to adopt some other methods to promote the nucleation process.

The first way is ZnO nanowalls, which is mainly adopted by Chung et al. in 2010 [26]; they grew GaN films and LED structure on graphene/SiC substrate using this method. And then in 2012 [27], GaN grown on graphene/SiO_2 was achieved successfully, with the flat surface. It is a big progress in nitride growth since we can grow single crystal on amorphous substrates.

Another way is using the steps on SiC substrates. It is known that we can get graphene on SiC directly by a high-temperature sublimation process, and the step on it can act as the nucleation sites. Balushi et al. [28] studied the nitride nucleation on such substrate. It is found that GaN nucleated at the step-edge priorly and little at the terrace, the nucleation sizes will become larger as the temperature rises, and it is easier to nucleate at few-layer graphene surface. Jee et al. [29] grew GaN films using this method and got good-quality films with the RMS for only 3 Å, and the full-width half maximum (FWHM) of the GaN (0002) peak was 0.06°.

The third way is plasma treatment. We destroyed the graphene surface in this way indeed, even though we can get lots of nucleation sites. Chae et al. [30] grew GaN films on graphene/SiO_2 using this method, and the film quality is good without yellow luminescence band.

And also, we can use some other ways, like pulsed sputtering. Shon et al. [31] used this method to grow GaN films on graphene/amorphous SiO_2 substrate; they got the good-quality film and LED successfully.

Secondly, we can use graphene as a release layer.

Graphene is a 2D material without dangling bonds on the surface, so the connection between graphene layers is very weak, so that it is easy to release the epitaxy layer on graphene. In this way, we can transfer the grown material onto other substrates and make more kinds of devices. Exactly, the first GaN film grown on graphene was transferred to foreign substrates successfully. In 2010 [26], Chung et al. reported that they grew GaN LED on ZnO-coated graphene/SiC substrate using ZnO nanowalls as an intermediate layer, and then the LED was transferred to glass, metal, and plastic substrates, which was found that they all exhibit good performance. In 2014 [29], Jee et al. grew graphene on SiC directly by a high-temperature sublimation process and then grew GaN LED on it. They use the kind of SiC substrate with vicinal steps which can facilitate nucleation. It is needed to mention that they release the GaN films by a 2-mm-thick Ni stressor, and after transferring the released GaN/Ni/tape stack on a host substrate, the SiC substrate

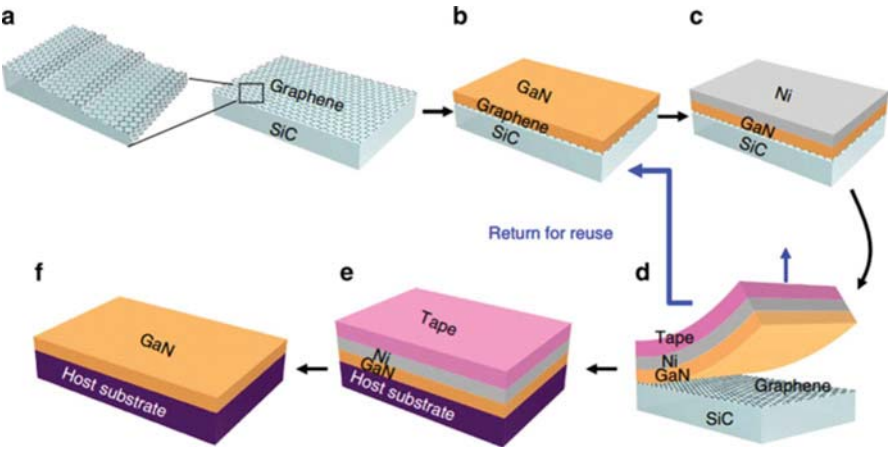

Fig. 6.5 Schematic method for growing/transferring single-crystalline thin films on/from epitaxial graphene

can be used again, as shown in Fig. 6.5. And also, there are many other groups who are focusing on the epitaxy release, like Qi et al. [32] in Soochow University, they grew crack-free gallium nitride microrods by HVPE and then achieved the release.

Thirdly we can use graphene as the heat dissipation layer.

Another advantage of graphene is the high thermal conductivity, so that we can use it as the dissipation layer. Han et al. [33] used the reduced graphene oxide (rGO) on sapphire substrate as such layer, and they found that the average temperature distribution on the chip surface is decreased from 51.4 °C to 47.06 °C, as shown in Fig. 6.5. Then, they adopted this method to grow GaN film on patterned sapphire substrate [34], and the averages of the surface temperature distribution decreased from 47.9 °C to 42.3 °C; the output power is 7% higher conventional counterpart.

It is obvious that we can improve the crystalline quality and even the device performance. However, there are still many questions we need to study, like the nucleation mechanism on graphene, the large-size graphene growth and transfer, and even the high-quality graphene grown on dielectric substrate to grow nitrides directly. There are much more work we need to do in the future.

Despite graphene, other 2D materials have also become a subject of great recent interest. Among these 2D materials, WS_2 and MoS_2 2D films whose lattice constants ($a = 3.15$ Å and 3.16 Å, respectively) [35] are remarkably close to those of AlN ($a = 3.11$ Å) and GaN ($a = 3.18$ Å) have lead to investigations to use relevant layered TMDCs as potential substrates for the epitaxy of AlN and further GaN films.

In 1997, Ohuchi and Chung [36] preliminary reported an attempt to grow AlN thin film on WS_2 films fabricated on Si(100) substrate. In the first part, they deposited highly oriented WS_2 films with WS_2 basal planes parallel to the substrate by MOCVD. Then, by a regular atomic layered growth (ALD) process, AlN films

were grown in the order of several hundred Å and with the FWHM of approximately 0.25°. Two years later, Yamada et al. [37] had an investigation comparing the structural and optical properties of GaN films grown on MoS_2 substrate and with those on Al_2O_3 substrate. The MoS_2 substrate used in the study was cut from native mineral rock, and 0.8 μm GaN films were grown by radio-frequency MBE with a two-step process: low temperature in 200 °C and high temperature in 800 °C. Through a detailed characterization, they verified the fact that flatter surfaces, lower stress, and dislocations in GaN on MoS_2 compared to those on Al_2O_3. While lacing deepen investigations about the nucleation mechanism, both the two groups were all proved the feasibility of high crystalline quality III-V nitride thin films on alterative near-lattice-match substrates—MoS_2 and WS_2.

Given the slow development of III-V nitrides at that time and the limited advance of 2D materials, the near-lattice-match epitaxy investment is in a longtime state of stagnation. However, in the past few years, with the frenzy of activity in research in III-V nitrides and 2D materials and motivated by the advantages in overcoming the existing large lattice mismatch problems among III-V nitrides, this epitaxy gradually comes back into our sight again. In 2016, Gupta et al. [37] reported the MOCVD growth strain-free, single-crystal islands of GaN on the mechanically exfoliated flakes of several layered WS_2 and MoS_2, as shown in Fig. 6.6. In the same year, Ooi et al. [38, 39] had a further investigation about an alignment parameters of GaN/single-layer MoS_2 and WSe_2 heterostructure and opened up a way to integrate III-nitrides with 2D TMDCs for designing and modeling their heterojunction-based electronic and photonic devices.

Our research center also draw a wide attention about this field and have achieved a rudimental result of GaN films grown on large-area quartz substrates by inserting MoS_2 and WS_2 interlayers. Even though, we still face many new challenges, such as the difficulty in grown high-oriented crystal surface of these 2D materials.

6.1.3 Design and Growth of High-Efficiency Blue LEDs

Light-emitting diodes (LEDs) are used in a very broad range of applications, from displaying information, sensing, communications, to lighting and illumination. Generally, developing the high-efficiency blue LEDs should be conducted from two aspects: internal quantum efficiency and light extraction efficiency (LEE). The light extraction efficiency has seen remarkable progress in the past decade, increasing for nitride-based LEDs from roughly 20% to 85%. However, there is one of the most significant and enduring challenges facing high-power GaN-based LEDs, called efficiency droop, or the decrease in external quantum efficiency (EQE) of an LED with increasing drive current. The efficiency droop in GaN-based light-emitting diodes has been extensively studied, and many physical origins of the droop effect have been proposed, including poor hole-injection efficiency, polarization charges,

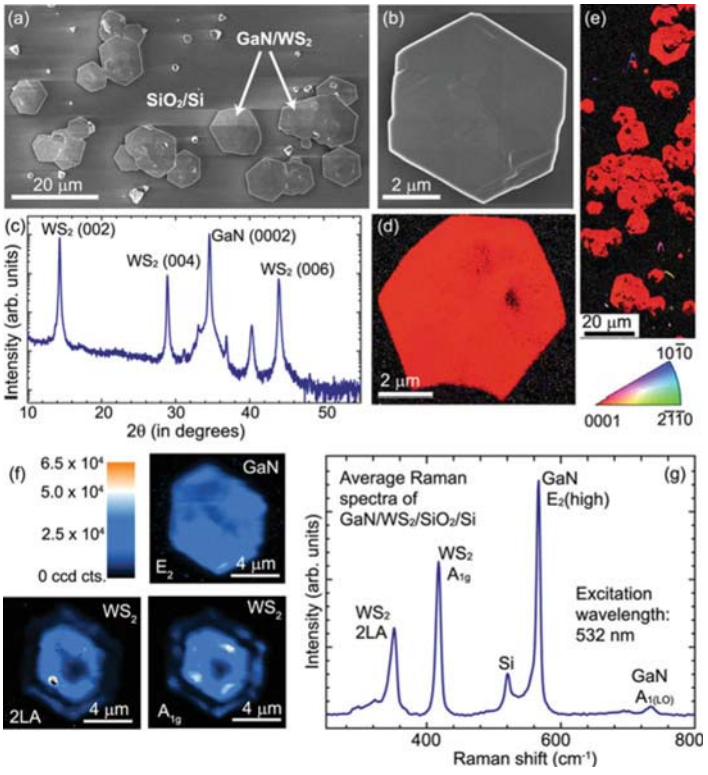

Fig. 6.6 Growth of GaN on exfoliated WS2 flakes. (**a**) Scanning electron microscopy confirms near-hexagonal crystals of GaN growing only in the region covered by the WS2 flakes. (**b**) Micrograph showing single hexagonal crystal of GaN grown on WS2. (**c**) X-ray diffraction profile of GaN on WS2 shows preferential (0002) orientation. (**d**) EBSD maps of GaN grown on exfoliated WS2 clearly show that the grown GaN layer is single crystal and (0002) oriented

Auger recombination, and carrier leakage, around which various design strategies and growth methods of high-efficiency blue LEDs are performed.

To improve the internal quantum efficiency of blue LEDs, several schemes have been put forward from different points of view, including improving hole injection, reducing polarization charge, and eliminating the carrier leakage.

Apart from the effect of electron-blocking layer (EBL) on the transport of holes, hole injection is further hindered as compared to electron injection due to the fact that there is a large disparity between electron and hole mobility. Some researchers aimed to enhance the hole injection by improving the hole concentration of p-GaN, but obtaining the high-quality and carrier concentration p-GaN is still a huge challenge.

Hwang et al. [40] introduced a new device named light-emitting triodes which have two anodes for promoting the injection of holes into the active region shown

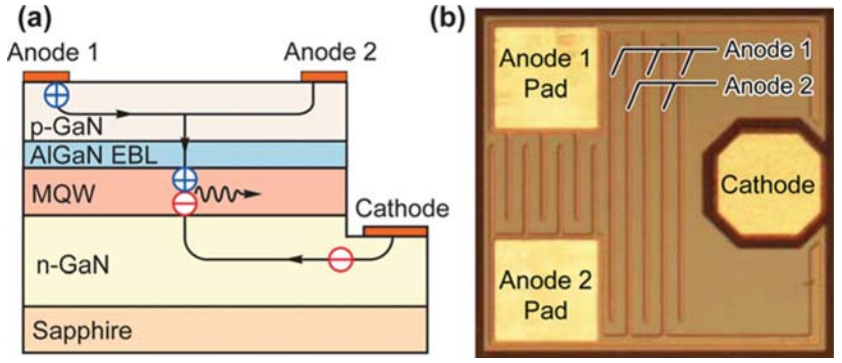

Fig. 6.7 (Color online). (**a**) Schematic drawing of the operation of an LET showing enhanced hole injection into active region by an anode-to-anode bias. (**b**) Photo of an LET with interdigitated anode fingers

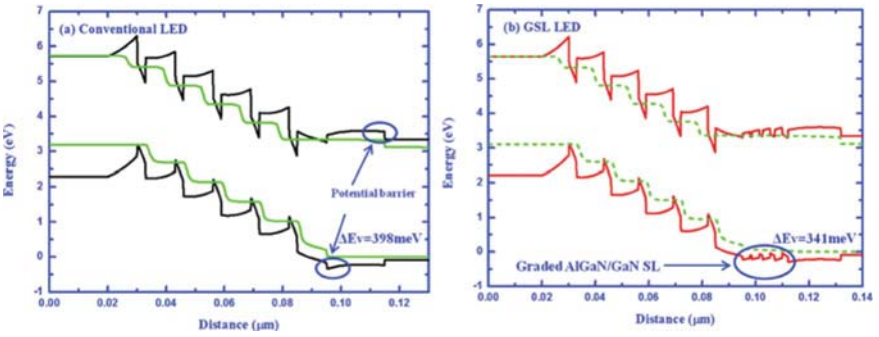

Fig. 6.8 Calculated energy-band diagrams of the conventional (**a**) and GSL (**b**) LEDs at current density of 100 A/cm^2

in Fig. 6.7. As the anode-to-anode bias increases, the efficiency at the same current density increases, whereas the efficiency droop decreases substantially.

Kang et al. [41] introduced a graded superlattice (GSL) AlGaN/GaN inserting layer to decrease the effective barrier height of holes, as presented in Fig. 6.8. The piezoelectric polarization field near the last barrier is suppressed effectively by introducing the GSL inserting layer. As a result, the efficiency droop radio is improved from 35.8% to 19.4% at current density of 100 A/cm^2.

Current commercially available InGaN-based LEDs grown on the "polar" c-plane of the crystal suffer from internal polarization-related electric fields that separate the electron and hole wave functions in the quantum wells and limit the radiative recombination rate. On the other hand, devices grown on nonpolar or semipolar orientations have been demonstrated with eliminated or reduced polarization fields and are theoretically predicted to have higher radiative recombination rates than c-plane devices.

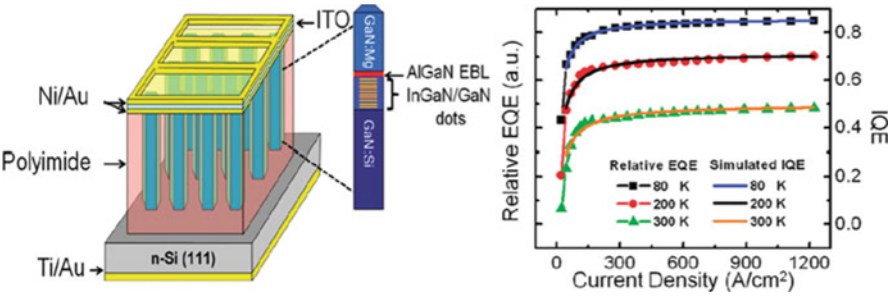

Fig. 6.9 Left: InGaN/GaN dot-in-a-wire LEDs with an AlGaN electron-blocking layer between the quantum dot active region and the p-GaN section. Right: Variations of the measured relative external quantum efficiencies with injection current at 80 K, 200 K, and 300 K. Variations of the simulated IQE with current using the ABF model show a good agreement with experimental results

Zhao et al. [42] report a high-power blue light-emitting diode (LED) with a high external quantum efficiency and low droop on a free-standing (20-2-1) GaN substrate; in higher current density regions, the LED showed outstanding performance.

Chung et al. [43] have introduced multilayer QBs (MLBs) as an alternative approach to reduce polarization effects, and time-resolved photoluminescence measurement showed that polarization field was reduced by 19% in the multilayer barrier light-emitting diodes structures. Besides, optical power measurements on packaged devices showed overall increase of external quantum efficiency for all currents up to the current density of 150 A/cm^2. The flow of energetic electrons flying over the active region (without being captured) to recombine with holes in p-type GaN or at the p-type contact electrode, i.e., electron leakage, is known as a common problem in GaN-based LEDs, and it is the reason why an AlGaN electron-blocking layer (EBL) is implemented on the p-side of the active region. However, the EBL in GaN-based LEDs is often unable to completely block election leakage.

Recently, Nguyen et al. [44] have investigated for the first time the impact of electron overflow on the performance of nanowire light-emitting diodes (LEDs), as showed in Fig. 6.9, and further demonstrated that electron overflow in nanowire LEDs can be effectively prevented with the incorporation of a p-doped AlGaN electron-blocking layer, leading to the achievement of phosphor-free white light-emitting diodes that can exhibit for the first time virtually zero efficiency droop for injection currents up to ~2200 A/cm^2.

Ni et al. [45] introduced an InGaN staircase electron injector with step-like increased In composition, an "*electron cooler*," proposed for an enhanced thermalization of the injected hot electrons to reduce the overflow and mitigate the efficiency droop, which is illustrated in Fig. 6.10.

To improve the light extraction efficiency, various texturing techniques have been used [46]. The two main ones have been surface roughening and substrate patterning, while side shaping can lead to sizeable low loss side extraction when

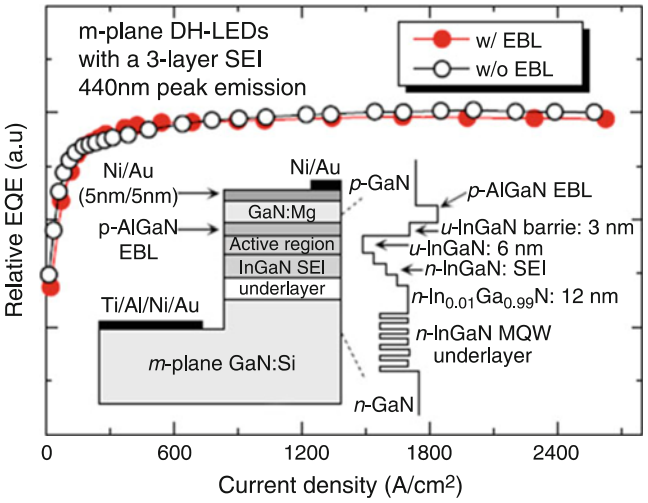

Fig. 6.10 (Color online). Relative EQE of two m-plane LEDs grown on freestanding m-plane (1-100) GaN substrates with a three-layer SEI: one with and one without the EBL. The inset shows the schematic for the LED with a 10 nm EBL (p-$Al_{0.15}Ga_{0.85}N$)

using transparent index-matched substrates. Photonic crystals also lead to remarkable LEEs, but their main advantage is emission directionality, which does not seem yet a large enough advantage to offset the demanding fabrication technology.

6.1.4 Device of High-Efficiency InGaN/GaN LEDs

There are three basic chip structures for InGaN/GaN LEDs: lateral LED, flip-chip LED, and vertical LED. The main light escaping surface of lateral LED and flip-chip LED are top surface and back sapphire surface, respectively. The p and n electrodes of the lateral LED and flip-chip LED are on the same side. However, the p electrode of the lateral LED is transparent or translucence, while that of the flip-chip LED has large reflectivity. The vertical LED has p and n electrodes on top and backside, respectively, so the substrate of the vertical LED is conductively.

6.1.4.1 InGaN/GaN Lateral LED

The chip structure of the lateral LED is the most easily implemented LED chip structure for InGaN/GaN LED on sapphire epitaxial wafers which are the most common used InGaN/GaN LED wafers and is a common form of structure. There are other kinds of lateral LEDs which have different substrates, for example, LEDs

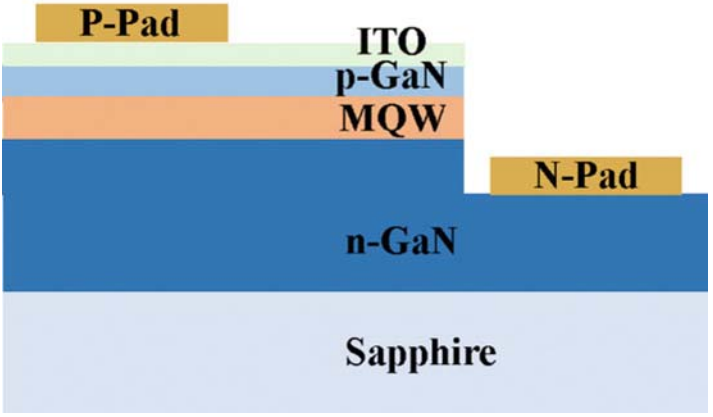

Fig. 6.11 The structure diagram of the InGaN/GaN lateral LEDs on sapphire substrate

with silicon substrate or silicon carbide substrate. Silicon absorbs blue light severely, and high-quality silicon carbide for GaN epitaxy is too expensive, so those LEDs are not common.

Figure 6.11 shows the LED for this structure. Since sapphire substrate is elecinsulating, the n-type GaN materials need to be exposed, which can be achieved by etching process. Because p-GaN is very thin, the current expansion capability is poor, and the p-GaN surface should be used as the light escaping surface, so it needs to deposit a layer of transparent conductive material on its surface, such as ITO, NiAu, ZnO, etc.

In early lateral LED chip, the p transparent electrode is made of NiAu thin film which has several nanometers thick. However, the light absorption of the NiAu thin film is severe, and the transmittance of it is about 70% for 460 nm blue light. The ITO application on InGaN/GaN LED is a big improvement which is used to replace NiAu thin film as p transparent electrode. ITO is indium tin oxide film which has a relative low absorption for blue light compared to NiAu thin film, and the light extraction efficacy of the LED is much improved when ITO is used to replaced NiAu thin film. Another big improvement for lateral LED is the application of PSS. PSS is patterned sapphire substrate, and it has aligned micrometer scale circular cone structures covered densely up its top surface which InGaN/GaN LED was grown on. The light extraction of the lateral LED with PSS is much better than lateral LED with flat sapphire substrate. Nichia is first to combine ITO and PSS technologies to improve the efficacy the InGaN/GaN blue LED. Figure 6.12 shows the structure of this kinds of high efficacy blue LED. The back surface of the sapphire is designed to reflect light, and the DBR (distributed Bragg reflector), metal reflector, or DBR metal combined ODR (omnidirectional reflector) reflector is deposited on the back sapphire surface to improve light extraction efficacy.

Because of the sapphire substrate, thermal conductivity is only 40 w/(m °C), only one over ten of copper, so a major defect of the lateral LED is a poor heat

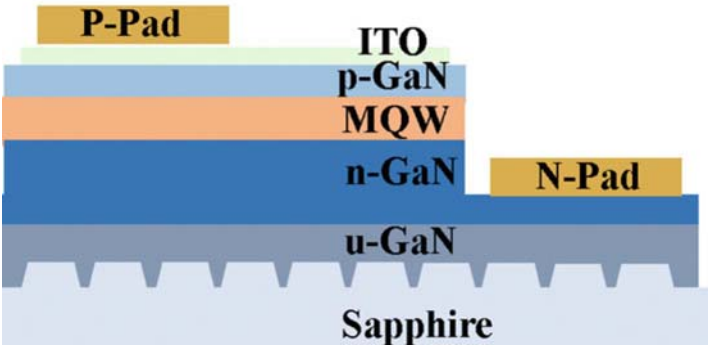

Fig. 6.12 The structure diagram of Nichia high efficacy InGaN/GaN lateral LED with ITO and PSS

dissipation performance. In addition, if the arrangement of electrode wire and the chip size do not match appropriately, it easily led to cause the edge-crowding effect of the current, leading to the local overheating of the chip. These problems will degrade the performance of the LED chip and shorten its lifetime.

Although it has some disadvantages, the lateral LED is easily fabricated and is cheaper compared to other LED chip form. The lateral LED has been widely used in indoor illumination, backlighting, decoration, display, and other lighting fields.

6.1.4.2 InGaN/GaN Flip-Chip LED

The light escape direction of the LED flip chip is the opposite of the lateral LED, so the flip-chip LED is inverted, and the p and n electrode are both down and have the ability to reflect light. Early flip-chip LED commonly has a silicon or ceramic substrate which has good thermal conductivity. The advantage for silicon substrate is that the electrostatic protection circuit is integrated in silicon substrates to protect LED chip. The p and the n electrodes of LED chip are connected to p and n electrodes on silicon substrate with little golden ball through flip-chip bonding technology. Its structure is shown in Fig. 6.13. The heat generated by such high-power LEDs does not need to pass through a chip's sapphire substrate but rather directly to a silicon or ceramic substrate with a higher thermal conductivity and then to the metal base.

The abovementioned flip-chip LED technology provides a solution to improving LED performance in thermal dissipation and light extraction when the lateral LED chips with NiAu thin and flat sapphire substrate are still mainstream chips. However, this kind of flip-chip LED has little advantages in thermal dissipation in practical application because the total cross area of the gold ball which is part of the heat dissipation channel is much smaller than the whole chip area though it has better thermal conductivity than sapphire. When the high efficacy lateral LED with ITO

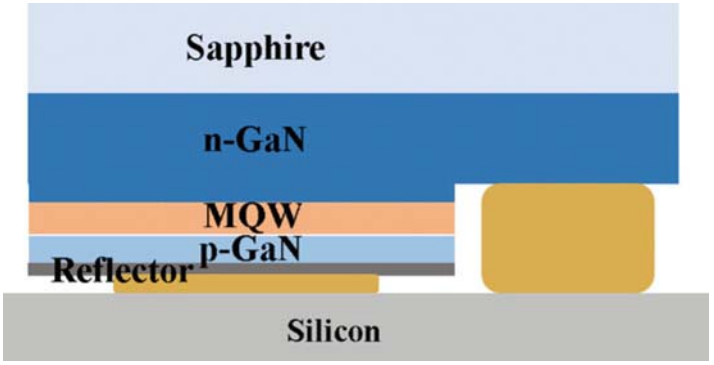

Fig. 6.13 The structure diagram of the InGaN/GaN flip-chip LED

and PSS became widely used and show better performance, this early type flip-chip LEDs were abandoned gradually due to its higher manufacture cost.

The flip-chip LED did not disappear. A new type flip-chip technology combined CSP (chip-scale packaging) was introduced to reduce the LED package cost in the 2010s. Chip-scale packaging without using gold line, based on the flip-chip bonded technology, on the basis of the traditional LED chip packaging, reduced the gold thread encapsulation process and save wire rack, Au wire bonding, leaving only the chip tie-in phosphors, and encapsulation adhesive is used. Figure 6.14 shows the structure of this new type flip-chip LED. There is no need for silicon or ceramic substrate. n pad is enlarged, and its area is as large as p pad. So the n large pad is overlapping with p electrode, and they were separated by passive layer such as dioxide silicon and nitride silicon thin film. The distance between p and n large pad is about 200 μm to insure soldering easily and successfully. After CSP, the top and four sides of the flip chip were covered by solidified encapsulated silica gel which is mixed with YAG phosphors. The CSP packaged LED is compact with relatively small size and can be directly used on PCB (printed circuit board) by SMD (surface mounting technology). The thermal resistance of the chip is much lower than that of the lateral LED, and the operation current is improved.

As a new packaging technology product, the non-gold-line chip level light source (CSP flip-chip LED) is completely free of the problems such as the lack of light, blinking, and light attenuation caused by the welding or contact of the gold thread. Compared with the traditional packaging process, the packaging density of the chip level light source has increased 16 times; the packaging volume has shrunk by 80%, and the design space of the lamp is larger. CSP flip chips with more stable performance, better heat dissipation, and more uniform light distribution, smaller volume, have favored by more and more LED lighting enterprises and end-product application enterprises.

Another type flip-chip LED is called thin-film flip-chip LED (TFFC LED). The top sapphire substrate was moved by laser lift off in TFFC LED. The InGaN/GaN LED thin film was transfer to a new substrate commonly on silicon substrate, and

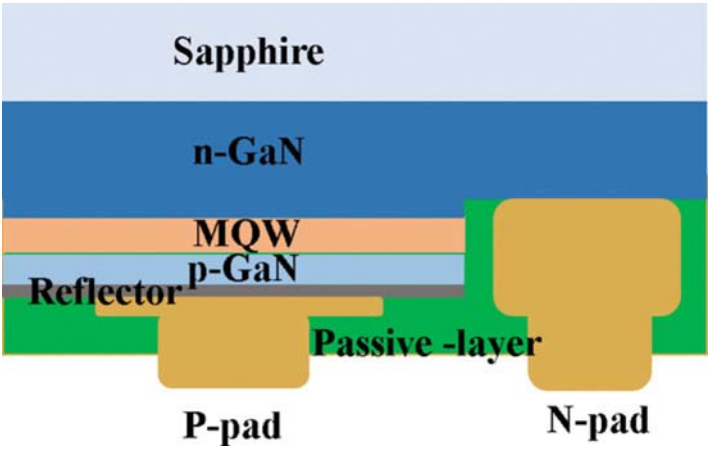

Fig. 6.14 The structure diagram of CSP flip-chip LED

the p and n electrodes of the InGaN/GaN LED are connected to p and n electrodes on silicon substrate. The total InGaN/GaN LED thin-film bottom surface with electrodes is cohered firmly to silicon substrate to avoid film cracking, while the top surface is roughened to improving light extraction. It is reported that the heat dissipation ability and light extraction efficacy of TFFC LED are excellent. The most severe problems of the TFFC LED are its low yield and high cost during manufacture process.

6.1.4.3 InGaN/GaN Vertical Structure LED

The p electrode and the n electrode of the vertical structure LED (VLED) are, respectively, on the top and bottom of the chip or on the contrary. The supporting substrate usually acts as heat dissipation path, while the substrate also acts as an electrode. Therefore, the LED of this structure overcomes the problem of current set edge effect and poor heat dissipation ability. Figure 6.15 is a typical structure diagram of the InGaN/GaN vertical structure LED. The vertical structure LED has many advantages, but it is difficult for GaN to grow directly on this new substrate. Sapphire and silicon are most commonly used substrates in nitride material growth by metal organic chemical vapor deposition (MOCVD). The sapphire substrate is insulating and has low heat conductivity, while the silicon severe absorb blue light, so these two kinds of material are not suitable to act as the vertical structure LEDs. So the vertical structure LED needs to remove the old substrate and attach the new substrate. This greatly increases the complexity and difficulty of the process. Still, vertical structural LEDs are favored by research institutions both at home and abroad. In particular, the news of the excellent high-power vertical structure LEDs, which has kept the most efficacy LED record for a long time, reported by Cree

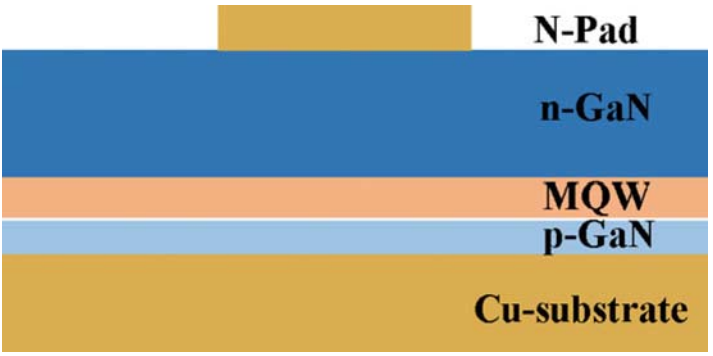

Fig. 6.15 The structure diagram of InGaN/GaN vertical structure LED

has enhanced the attention and confidence of the VLED. With the development of technology, the vertical structure LED may be the best solution to realize the general lighting of the semiconductor.

There are several schemes for implementing InGaN/GaN vertical structure LED chip technology. For the InGaN/GaN LED epitaxy material grown on sapphire substrate, to realize this structure, there are two key processes, one is to attach the InGaN/GaN LED epitaxy material to the new thermally conductive substrate, and the second is to remove the old substrate. As for the remaining chip technology, it is compatible with the chip technology of the lateral LED. These two key technologies are not only important but also difficult to achieve. The new conductive thermal substrate attachments include wafer bonding and electroplating. The methods of removing the old substrate include laser lift off, substrate grinding, and wet drilling [47–49]. The most commonly used method is laser lift off. The two steps combine to achieve the vertical structure LED with n-type GaN on the top and p-type GaN at the bottom. There are also twice substrate transfer method, which can realize the vertical structure LED with the p-type GaN on the top and the n-type GaN at the bottom. Electroplated copper alloy is used as the substrate in the vertical structured LED chip produced by SemiLEDs, ISCAS, which is shown in Fig. 6.16. During this kind of vertical structure LED manufacture process, the sapphire substrate is removed by the laser lift off and recycled.

For InGaN/GaN LED epitaxial wafer grown on a silicon substrate, in the production of vertical structure LED, the different process is substrate removal method. It is easier to find quick corrosion methods compared to the sapphire wafers. So, wet etching method is often used to remove the silicon substrate. If the epitaxy substrate is conductive silicon, the substrate is retained to act as the negative electrode, and it can also form a vertical structure LED. However, the visible light reflectivity of the silicon substrate is very low, and the absorption of the light is severe. The growth of the GaN base LED on silicon carbide is similar to that in silicon.

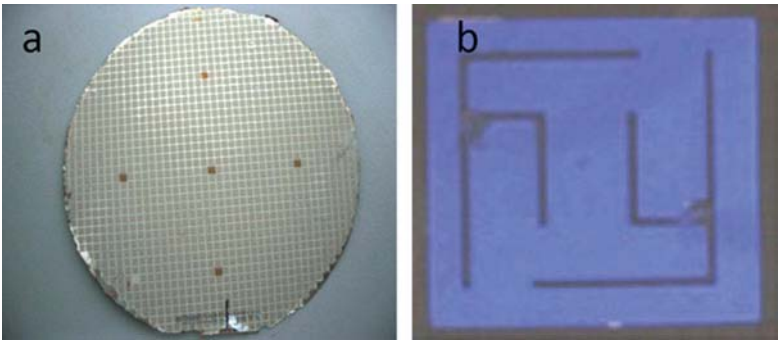

Fig. 6.16 VLED wafer and VLED chip photos with metal substrate produced by ISCAS

6.1.5 Tendency of Novel LEDs Structure and Application

Recently, the nanowire LED (Fig. 6.17) [50–54], mainly core/shell LED, has attracted large attention because of their potential advantages. In comparison to the conventional thin-film LEDs, core/shell nanorod structure LEDs have higher aspect ratio and larger active regions. Besides, the InGaN/GaN multi-quantum wells (MQWs) grown on nonpolar or semipolar GaN facets are suggested to be able to effectively increase the light extraction efficiency and reduce the quantum-confined stark effect (QCSE), which increases the internal quantum efficiency of LEDs through enhancing the radiative recombination rate in MQWs [55–57]. What's more, nanowires could improve the material quality with respect to thin films, a better handling of the strain induced by thermal expansion mismatch. Thus, the high-quality axial NW LEDs also have been reported a lot and proved to have some special performance [58, 59].

6.1.5.1 Synthesis

For the structure of nanowire LED, the growth of high-density ordered GaN nanowires is necessary for the follow-up metal contacting. The top-down etching, bottom-up selective vapor-liquid-solid (VLS) growth, and area MOCVD growth are three prevailing GaN nanowire growth methods. GaN dry plasma etching is widely used in the III-nitrides industry. However, reactive-ion etching (RIE) suffers from relatively low etch rates and plasma damage in devices. Compared with RIE, wet etching has the advantages of reducing surface damage and low cost and providing a simple method for device fabrication. Figure 6.18a shows the nanostructure mainly developed by wet etching. In our work [60–62], we found the suppression of the etch rate in the vertical direction could help to form the uniform nanowire. A thin AlGaN which was stable in the KOH solution was used to suppress the vertical direction. The wetting nanowires were surrounded by six $\{1\bar{1}00\}$ m plane. On the

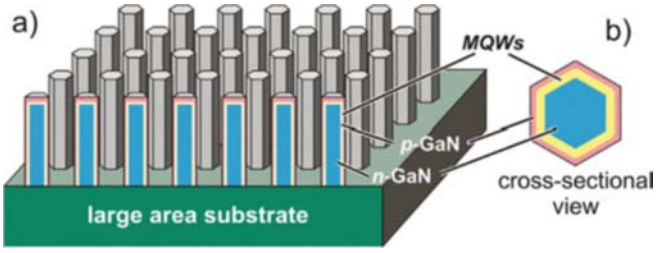

Fig. 6.17 Core-shell strategy for the fabrication of GaN-based nanoLEDs. Sketches of (**a**) core-shell nanoLED ensemble. (**b**) Cross-sectional view of a core-shell nanoLED. The active LED area can be increased approximately by a factor of four times the aspect ratio in comparison to a planar LED [57]

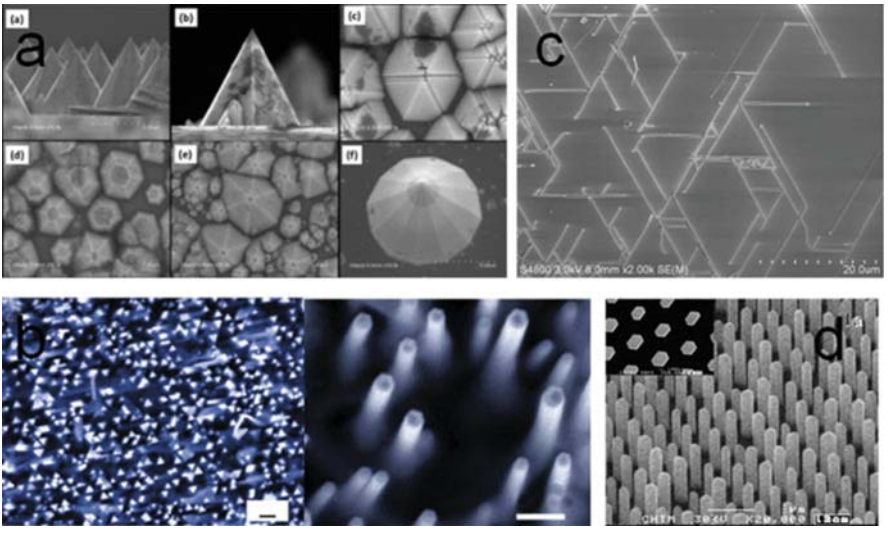

Fig. 6.18 Synthesis of GaN NWs by (**a**) top-down etching [61], (**b**, **c**) bottom-up selective vapor-liquid-solid (VLS) growth, and (**d**) area MOCVD growth [64, 68]

other hand, the existed large vertical etching could develop the pyramid structure with six $\{11\bar{2}1\}$ facets.

The top down may be an effective method to obtain the array nanowires. However, the nanowire crystal quality was poor because of the film growth and wetting. Since the discovery of the VLS process in 1964 by Wagner and Ellis [63], there have been many seminal works advancing NW synthesis and applications. To achieve GaN NWs with controlled orientation (or say, to obtain GaN NWs array), the most effective ways to control the growth direction of GaN nanowires is the epitaxial growth. Kuykendall et al. [64] have shown that hexagonal cross section, c-axis NWs grew perpendicular to (111) MgO, and m-axis NWs with a triangular cross section grow on (100) γ-LiAlO2 in MOVPE (Fig. 6.18b). Due to the epitaxial

relationship, horizontal GaN NWs with various growth directions and cross sections have been obtained on sapphire substrate with various facet orientations from our group (Fig. 6.25c). Recently, our group proposed the fast and controlled growth of high-quality GaN nanowires by VLS-HVPE [65–67]. We also achieved the first growing of horizontal GaN nanowires by HVPE with the growth rate more than 400 μm/h (Fig. 6.18c) [67].

The selective area growth (SAG) is the most practical GaN nanowire growth methods because the high crystal quality has no introduction of foreign metals. Hersee et al. [68] reported for the first time the successful MOCVD growth of GaN nanorods on patterned SiO_2/GaN using the pulsed growth mode (Fig. 6.18d). During the vertical growth phase, the Ga and NH3 flows were alternatively pulsed starting after the GaN nanorods extrude out the holes. This is claimed to be very critical since if the growth conditions for "filling the holes" were maintained, then as soon as the nanorods emerged from the growth mask, lateral growth occurred, and the nanorod geometry was lost. With the pulsed growth mode, GaN nanorods with good homogeneity in size and morphology were obtained. Our team also systematically studied the growth technology [69, 70]. We found the hydrogen content has a large impact on the morphology of the nanostructure. Interestingly, the results were similar to the wet etching. The high hydrogen content benefited to the development of long one-dimensional nanorods, while lack of or no hydrogen carrier gas leads to form the pyramid structure.

6.1.5.2 Nanowire LED

Nanowire-based LEDs were first reported in the early 2000s by Harvard University from liaber's group. However, in the early work, GaN core-shell NW LEDs were already fabricated in a single NW scale and are not ideal for mass production. The meticulous processes are needed to define the location of the nanomaterial and attach electrical contacts with nanoscale precision. The problems inherent to single nanowire LEDs can be resolved using the aligned nanowires (as shown in the front part), which is highly desirable for scalable LED fabrication. Corresponding to the synthesis methods of GaN NWs, there are also three types of NWs LEDs: top-down nanoLED, bottom-up axial nanoLEDs, and core-shell nanoLED.

A straightforward method to fabricate GaN nanoLEDs is to etch planar GaN LEDs with nanomasks. The GaN nanorods were defined by various methods like conventional photolithography, e-beam lithography, and nanoimprint lithography, or other low-cost methods, for example, nanoscale self-organized nickel islands as etching mask or SiO_2 nanosphere lithography. However, using a top-down method, a large portion of GaN material is etched away and does not contribute to light emission any more. This will add additional cost during device fabrication compared to the bottom-up (growth) method. Besides, other advantages of GaN nanorods, for example, defect reduction and tuning the indium concentration by the nanorod size will not be applicable. On the other hand, plasma-assisted MBE was also employed to fabricate LEDs based on arrays of GaN nanocolumns in an axial configuration,

which contain n-GaN/MQWs (InGaN/GaN)/p-GaN, on a Si substrate [57, 58]. By tuning the indium content in the MQWs, the emission color of the nanocolumn LED could be varied from violet to red [59, 71]. Moreover, white-light emission was achieved in these LEDs by gradually varying the indium composition within the InGaN segment [72]. However, for commercial application, these novel axial nanowires LED may face the challenge of high cost and inefficient.

Radial nanowire LED heterostructures generally consist of a nanowire core region, surrounding by an active region and coaxial shell layers [73]. Such radial nanowire LED structures are often grown by selective area growth using MOCVD, and the active region typically contains nonpolar (m-plane) and/or semipolar multi-quantum wells. Several fabrication methods have been developed to realize large area radial nanowire LEDs [50, 73, 74]. For example, the p-GaN shell can be overgrown to form a coalesced layer to effectively connect all the p-type segments of individual nanowires [73]. A relatively low turn-on voltage of ~2.65 V was measured, which is better than that of a reference planar LED device. It was also measured that the peak emission wavelength stayed nearly constant with increasing injection current, due to the absence of quantum-confined stark effect in the nonpolar m-plane InGaN quantum well active region. Other approaches for realizing large area core-shell nanowire LEDs are to fill the gap between individual nanowires and directly cover a graphene layer as the p-electrode contact [50, 74]. The core-shell nanowire LED has been considered the most likely to replace conventional thin-film LEDs. However, though several companies and numbers of research institutes have studied it a lot, the effectiveness of the NW LED is still low.

6.2 Green LEDs

This chapter describes a number of factors that affect the efficiency of green LED and analyzes the effects of polarization, carrier transport, carrier localization, current expansion, epitaxial structure design, Auger recombination and light extraction, and luminous efficiency. Aiming at the different influence mechanism, the droop effect of reducing the green LED is discussed, and the method of improving the quantum efficiency is discussed.

6.2.1 Polarization Fields in the InGaN-Based LEDs

The nitride materials have a wurtzite structure, which has the point group of C6V (6 mm). The C6V point group is a hexagonal structure with a single axis of symmetry or a polar axis. The centers of the positive and negative charge

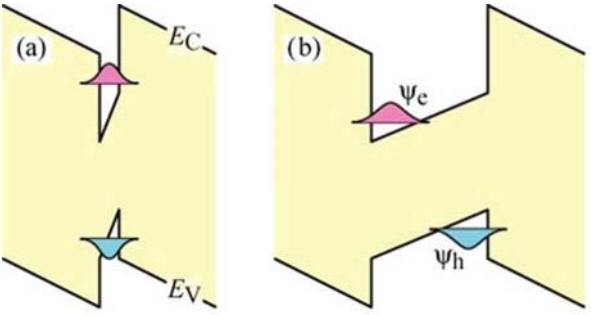

Fig. 6.19 The separation of the electrons and holes wave functions due to the band bending caused by the polarization electric field for the InGaN green LED

within the unit cells do not coincide, forming the torque and then resulting in spontaneous polarization effect. Spontaneous polarization field is determined by the nature of the material itself, regardless of whether it is subjected to the external stress. Piezoelectric polarization field is related to the stress applied on the nitride materials, which changed the position of the positive and negative charge centers in the unit cell, then resulting in a polarized electric field inside the material [75–77]. Unlike the III-arsenide compounds, an important property of the group III-nitride semiconductor material is its strong polarization effect, including spontaneous polarization and piezoelectric polarization. The total polarization in the nitride material is the sum of the piezoelectric polarization electrical field and the spontaneous polarization electric field [78].

This result shows that the lattice-mismatching between the InGaN layer and the GaN layer in the InGaN-based green LED produces a piezoelectric electric field on the order of MV/cm and bound sheet charges with a density of up to 10^{13} cm^{-2} at the interface of the heterostructure [75]. The polarization electric field will have a great influence on the band twist, the carrier distribution, and the photoelectric properties of the green LED [79].

As is shown in Fig. 6.19, the band bending caused by the polarization electric field in the quantum well leads to the separation of the electrons and holes wave functions. Thus, the effective band gap of the quantum wells and the recombination probability of the carriers will be reduced, which results in the decreasing of the luminous efficiency of the green LEDs. As the In composition in the multi-quantum well increases, that problem becomes more and more serious in the InGaN/GaN heterostructures [80]. The piezoelectric polarization along the [0001] crystal axis direction is at least one order of magnitude larger than spontaneous polarization [76]. For the In-rich green LEDs, the higher polarization filed in the InGaN/GaN multiple quantum wells has a great effect on the radiative recombination and efficiency droop. Various methods have been adopted to control the polarization fields and related QCSE in the green LED to weaken its negative effects and improve the luminous efficiency.

6.2.2 *Internal Quantum Efficiency Promotion in the Green LEDs*

The presence of the polarization electric field in the Ga-face InGaN quantum wells for the green LEDs will shift the emission wavelength [81]. Due to the screening of the polarization electric field by the carriers injected into the quantum wells, the emission peak wavelength will show a blueshift with the increasing of the injected carrier density under the forward bias. Furthermore, the peak wavelength will also shift with the increasing of the reverse bias voltage due to the reverse electric field which is opposite to the direction of the polarized electric field. The applied reverse fields flatten the energy band within the QW and then widen the band gap [82].

Controlling the stress in the epitaxial wafer can also effectively reduce the polarization electrical field in the active region of the green LED. It's reported that the stress alleviation in the high In composition quantum wells by pre-growing a low In composition of InGaN layer or InGaN/GaN superlattices layers between n-GaN and high In composition InGaN/GaN green light quantum wells (shown in Fig. 6.20) effectively reduced the polarization electric field within the green LED quantum well and then improved the wavelength stability and the luminous efficiency for green LED [83–87]. In order to reduce the wavelength blueshift in the green LEDs, Huang et al. inserted an InGaN layer between the n-GaN and the MQWs used as the pre-strained layer [83]. The growth temperature of the emitting QWs can be raised by 30 °C while keeping about the same emission wavelength in green region. The blueshift of the PL feature for the pre-strained sample grown under the same temperature with the compared sample indicated the reduction of the strength of the QCSE in the MQWs. The spectral blueshift in increasing injection current in the range of 45 mA was decreased by 46%. Similar results have been found by Park et al. [84]. They found that an employed graded superlattice (GSL) consisting of 12-stacked InGaN/GaN layers in the green LEDs showed a 4.7 nm blueshift and an enhanced output power under the photoexcitation. They attributed it to the increase of electron injection efficiency and the decrease of electron overflow to the p-GaN reduction in non-radiative defect sites due to the inserted GSL.

The transport of carriers in the Ga-face multiple quantum wells of the LEDs will be affected by the polarization fields [88–90]. Due to the strong polarization mismatch between the InGaN well and GaN barrier in the green LED, there is strongly polarization electrical fields with the direction from the p-GaN side toward the n-GaN side, resulting in band tilt. Then, a triangular barrier is formed in both the conduction band and valence band. As a result, the band bending of the quantum well reduces the confinement ability of carriers, making it easy for the electrons escaping from the quantum well and forming electrons leakage. Schubert argues that the presence of polarization fields reduces the carriers capturing probability in the quantum wells.

Effective dopant doping within the active regions can provide free electrons that shield the polarized sheet charges at the interfaces of the heterostructures in the active region and thus reduce the polarized electric field. The methods of providing

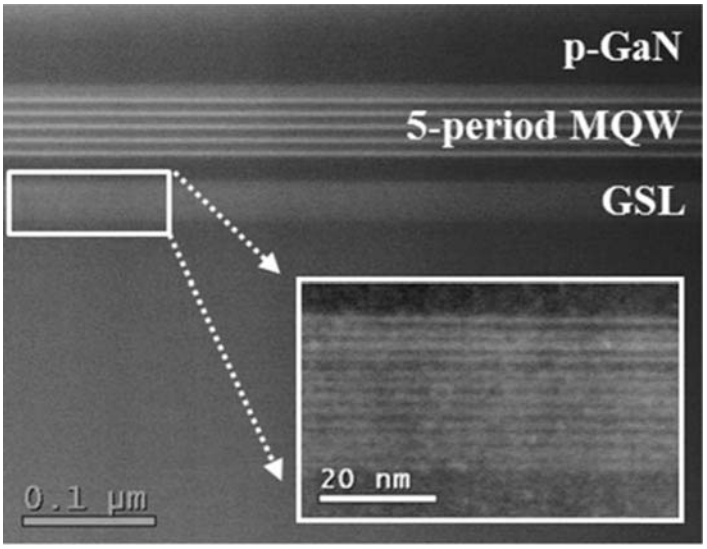

Fig. 6.20 TEM image with an inset of the inserted pre-strained structure for the LED sample. The inset shows the magnified image for the pre-strained superlattice structure

free carriers in MQWs by dopants doping mainly involve p-type or n-type impurity doping in the quantum wells or in the quantum barriers [91–95]. It has been reported that the donor impurity (Si) doping in the quantum barrier effectively shields the polarization electrical field and then improves the photoelectric performance [94]. Lin's group [94] reported that the Si doping in barrier layers with a dopants density of 3.4×10^{16} cm^{-3} for green LEDs not only screens the electrostatic field but also effectively reduces the roughness at the InGaN/GaN heterostructure interface. What's more, the current spreading could be enhanced by the Si doping in the barrier layers. The current crowding alleviation reduced the local heating and suppressing the efficiency degradation. But Ryou et al. [95] found that the Si doping concentration in the GaN barriers increases the barrier height for holes would block the holes transportation, thus decreasing the EL intensity. Zhang et al. employed the Mg doping in barriers in the InGaN-based green light-emitting diodes. The holes generated by the Mg impurity atoms in the barriers effectively screen the polarization fields and reduce the efficiency degradation of 12.4% at a high injection current. What's more, that research group also investigated the effect of the Mg back diffusion into the MQWs on the carrier recombination. The results show that the back-diffused Mg acceptors in the QWs closed to the p-layer could improve the hole injection efficiency and reduce the leakage current.

The nitride material with cubic structure has symmetry and no spontaneous polarization filed. However, that kind of nitride crystal for the green LEDs is difficult to be obtained by MOCVD. For the nitride materials with hexagonal phase, the intensity of the polarized electric field in the a-axis or m-axis directions

is smaller than that along the c-axis [96, 97]. A LED with a small polarization effect in the direction perpendicular to the multi-quantum well is obtained by growing a hexagonal phase nitride material on a semipolar or nonpolar substrate. For example, in the m-plane (1-100) and a-plane (11-20) InGaN quantum wells, since the polarized electric field is parallel to the InGaN/GaN interface, the energy band of the quantum well remain flat. However, due to the limitations of the epitaxial growth techniques, the nitride material having a nonpolar or semipolar surface has a large number of defects [98]. What's more, the surface roughness of the film is relatively high. Thus, there are many non-radiative recombination defects in the semipolar or nonpolar LED, which reduces the radiation recombination efficiency of the MQWs. Therefore, the increasing of the external quantum efficiency for the nonpolar or semipolar LED is difficult. In addition, nonpolar or semipolar substrates for the nitride materials are expensive, which are not suitable for the large-scale commercial production.

The energy-band engineering of the active region though reducing the lattice mismatch between the In-rich InGaN quantum well and the GaN quantum barrier can also improve the luminous efficiency of the green LEDs. Some ways, such as the AlInGaN or InGaN barrier, were adopted to reduce the lattice-mismatching-related polarization field in the active region, improving the carriers coincidence rate and finally improving higher carrier recombination efficiency [99–105]. For example, in order to suppress the efficiency droop in the green LEDs through energy-band engineering, Lee et al. [106] employed the gradual In-content InGaN QW to reduce the valence-band bending and enhance the hole injection. The IQE in the In-graded QW LED was increased by 45.5% and 55.7% under the injection current of 20 and 100 mA, respectively. Furthermore, the In-graded QWs also decreased the electron leakage, suppressing the efficiency droop.

The electrons could participate in the radiation recombination only after they were captured by the In-rich quantum wells in the green LEDs. Electrons leakage means that the electrons transported though the active region to the p-type GaN layer, participating in the non-radiative recombination [107]. In order to suppress the electrons leakage, an AlGaN electron barrier layer (EBL) is inserted between the p-type layer and the active region for the green LEDs [108]. However, due to the polarization effect, the barrier height of the EBL conduction band for the electrons is reduced. As a result, the ability of the EBL to block the electrons is limited, reducing the radiative recombination efficiency. Therefore, electrons leakages are also considered to be one of the causes of efficiency droops in the green LEDs.

Vampola et al. [109] demonstrated the electrons leakages experimentally by inserting a p-doped, low Indium InGaN quantum well in the p-type EBL. Under the lower injected current, the inserted quantum well shows no light emitting, which means that the electrons leakage could be ignored. As the current increases, electrons transport through the active region and inject into the inserted low In-content quantum well and then recombine with the hole. The emitting light shows a

shorter wavelength. The light with short wavelength, which is related to the electron leakage, appears when the external quantum efficiency is about to reach its peak. Then, the external quantum efficiency decreases when the intensity of the shortwave light increases.

The simulation results, shown in Fig. 6.21, by Chang et al. [110] show that the electrons leakage greatly reduces the peak EQE and moves the peak efficiency to a higher current density for the green LEDs with a 3.5-nm-thick undoped $In_{0.25}Ga_{0.75}N$ test well. In addition, some temperature-related EL testing results also show that electrons leakage may lead to efficiency droop. Nguyen et al. [44] reported that in the GaN-based nanowires LEDs, the most important factor limiting the quantum efficiency is the electron leakage, rather than the auger recombination. They demonstrated that droop was not present at a current density of 2200 A/cm^2 in a GaN-based nanowire LED with a p-doped AlGaN EBL layer.

The polarized sheet charges at the interface between the EBL and spacer layer are considered to be the fundamental factor in reducing the EBL limitation and the electrons leakage to the p-GaN layer [107, 111]. The Al composition in the AlGaN EBL is generally set from 5% to 30% in the green LEDs. However, with the increasing of Al composition in AlGaN, the polarization mismatch between AlGaN and adjacent GaN barrier layer also becomes more serious, and the effective barrier height of conduction band for the electrons in EBL is further reduced [107]. Thus, the electron-blocking effect of high Al component EBL is hard to achieve the desired target. Kim et al. showed that 60% of the electrons injected into the active region would overflow to the p-type layer [112]. In order to reduce the stress between the EBL and the barrier in the green LEDs, Lin et al. [113] adopted a quaternary InAlGaN/GaN superlattice electron-blocking layer (SL-EBL) (shown in Fig. 6.22) and improved the efficiency droop phenomena. With that new EBL structure, the optical output power of the green LED was enhanced by 57%, and the efficiency droop was reduced by 30%. Similar structure was also investigated by Tzou et al., and they found that the light output power for the green LEDs was enhanced by 53%.

The hole in the nitride LED has a large effective mass and a smaller mobility, which severely limits the transportation of holes in the active region, restricting the uniform distribution of holes in the multiple quantum wells. The inefficiency injection for the holes limits the external quantum efficiency of the green LED [114]. In addition, the existence of the EBL blocks the transport of holes into the In-rich MQWs. The high Al component also raises the valence-band barrier in EBL, then affecting the injection of holes into the active region. Hwang et al. introduced a new device called light-emitting triode (LET), which has two positive electrodes that can increase hole injection. With the LET, they demonstrated that low hole injection efficiency is an important cause of efficiency droop. To achieve a better hole injection, some methods were introduced. Lin et al. [115] coated Mg-modulation-doped InGaN/GaN superlattices on the In-rich MQWs. Due to the better conductivity, the light output power was enhanced by 100%, compared to that of the LEDs with a high-temperature grown p-GaN layer. It's known that Mg dopants react with the hydrogens in the GaN, resulting in the passivation of the Mg-related acceptor and lower activation efficiency of holes. Furthermore, the higher

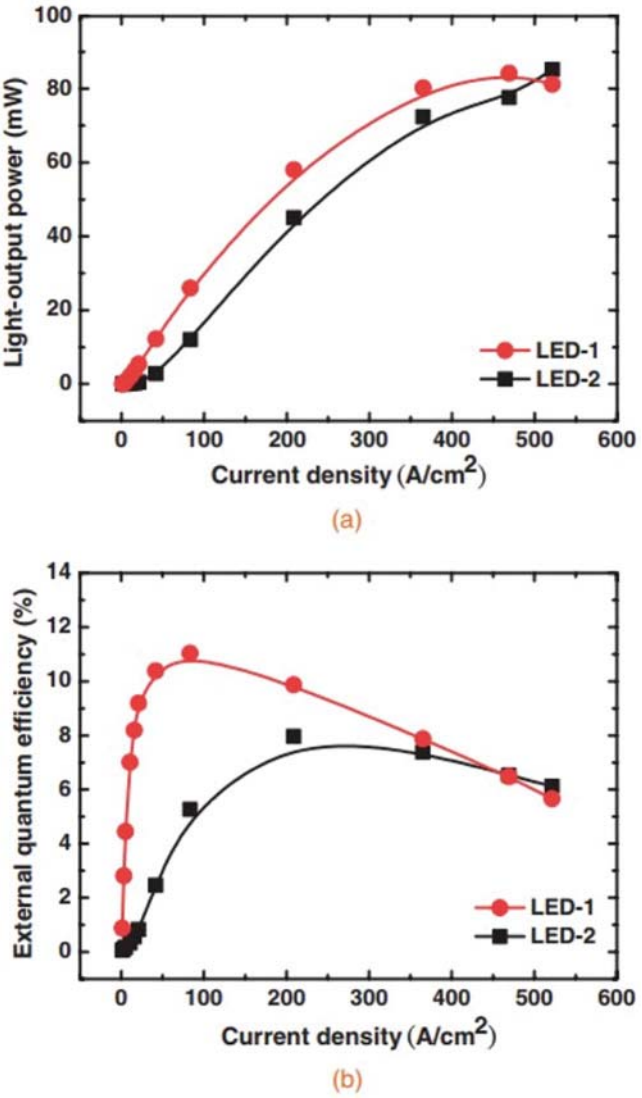

Fig. 6.21 (**a**) Light-output power of samples LED-1 (compared LED) and LED-2 (LED with a 3.5-nm-thick undoped $In_{0.25}Ga_{0.75}N$ test well) as a function of forward current density. (**b**) EQE of samples LED-1 and LED-2 as a function of forward current density

temperature to grow the p-GaN also causes some crystal damage to the InGaN layer, which is under the unstable state. To remove the hydrogen in p-GaN layer and suppress the thermal damage to In-rich MQWs pf the green LEDs, Kim et al. [116] proposed to anneal the p-GaN layer at a low activation temperature (600 °C) by coating a PdZn film on the top of the wafer and remove the hydrogen in the p-GaN

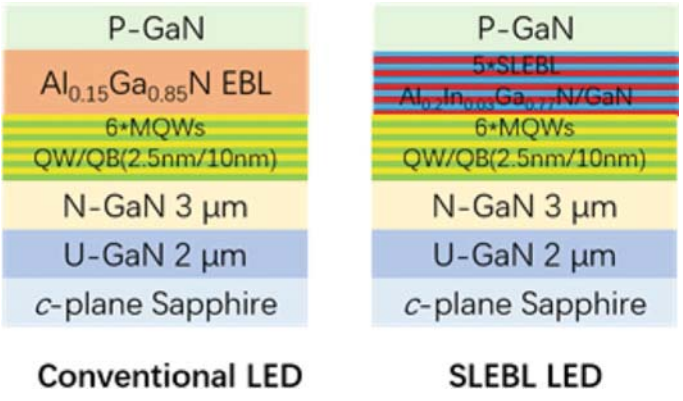

Fig. 6.22 Schematic diagrams of the conventional structure and SL-EBL LEDs

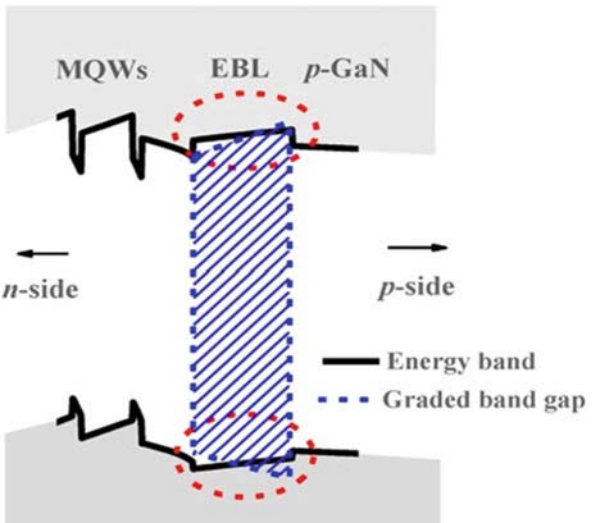

Fig. 6.23 Schematic diagram of the concept of band engineering at EBL

under the annealing temperature of 600 °C. This new annealing method helped to improve the EL intensity by 33% at 20 mA. Researchers also studied the effect of the graded-composition electron-blocking layer (GEBL) on the holes transportation in the green LEDs [117]. Results showed that the GEBL with aluminum composition increasing along the [0001] direction could level down the valence band (schematic diagram of the concept of band engineering at EBL is shown in Fig. 6.23) and then improve hole transportation across the EBL.

InGaN ternary alloy with high In composition is in the thermodynamically non-equilibrium state [77, 118, 119]. This problem is more serious for the green LEDs. In-rich InGaN in the metastable phase is prone to undergo phase separation, resulting in uneven composition distribution within the film. Furthermore, the change of the temperature, the rotating speed, inadequate atomic migration, and

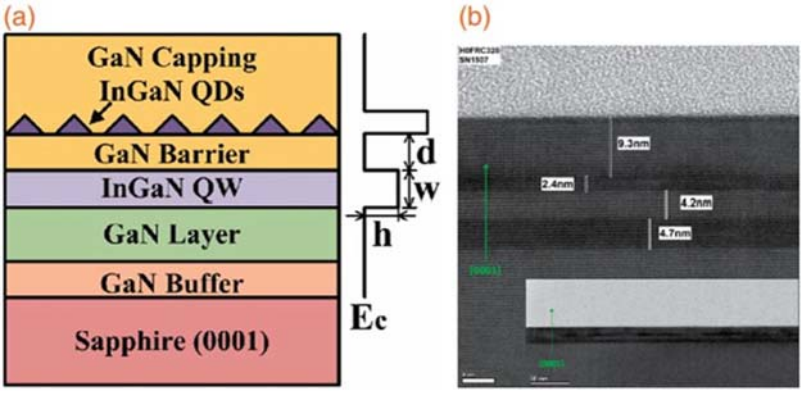

Fig. 6.24 (**a**) Schematic structure of the coupled QW-QD samples' epitaxial structure and conduction band. (**b**) High-resolution (HR) TEM image of sample A. The inset is bright-field (BF) TEM image of sample A. The images were taken along the GaN [11–20]

stress also will eventually lead to the phase separation of the InGaN. The fluctuation of the In composition in In-rich InGaN alloy will lead to the randomness of the potential energy distribution, resulting in the localization of the carriers [120, 121]. For the In-rich green quantum well, the shallow localization centers are related to the low In composition InGaN, in which the potential energy fluctuates around 150 meV. In comparison, the potential energy fluctuation of the deep localization center can reach 300 meV. With the increasing of injected carrier density, the carriers flow between the shallow local centers and the deep local centers. The localized center limits the carriers and reduces the transporting of electrons and holes to defects, thus suppressing the non-radiative recombination. Therefore, the localization of carriers is considered an effective way to increase the internal quantum efficiency [122–124]. Cheng studied the localization behaviors in green light quantum wells. The Si doping in the barriers will result in serious indium clusters, which is attributed to the strain.

Some groups tried to grow the self-organized quantum dots (QD) through phase separation of In-rich InGaN to realize the localization of the carriers for the green LEDs [122, 125–128]. With the $In_{0.25}Ga_{0.75}N$ QDs in the In-rich InGaN quantum wells, Zhang et al. [126] reduced the green LEDs efficiency droop by 32%. The recombination lifetime determined by the temperature-dependent photoluminescence measurements is 0.57 ns, which is due to the localization effect and the smaller piezoelectric field in the QDs. Yu et al. [128] employed the coupled InGaN/GaN QW and QDs structure (shown in the Fig. 6.24) in the green LEDs to enhance the internal quantum efficiency. The results showed that the carriers could tunnel from shallow QWs to deep QDs nearby. Compared with the conventional single QD layer, the IQE of the QDs was enhanced by more than two times, arriving at 45%.

It has been reported that internal non-radiative losses are associated with carrier delocalization in the InGaN-based LEDs [129]. Under low injection current densities, carriers are confined to the QD-like centers with the lowest potential in the quantum wells. As a result, in these localization regions, the defect-related non-radiative recombination efficiency is on the order of 10^7 s^{-1}. At high injection current densities, the carriers exhibit delocalization behavior and diffuse into other areas in the active region. The non-radiation recombination defects in these areas increase the SRH coefficient, making the droop more serious.

Auger recombination is the most widely debated issue in the study of the efficiency of nitride-based green LEDs [130–132]. Auger recombination means that electrons recombine with holes without emitting photons but rather passing energy to the third carrier. The Auger recombination efficiency is related to the Auger coefficient and is proportional to n^3, where n is the carrier concentration [133]. As the injected carrier density is enhanced, the Auger recombination increases, and the luminous efficiency is reduced. It is reported that only the Auger recombination coefficient greater than 10^{-31} cm^6 s^{-1} will significantly affect the green LED droop. In theory, for a single-crystal material, the Auger coefficient C is generally lower than 10^{-32} cm s^{-1}, while for the active region, C is 10^{-31} to 10^{-29} cm^6 s^{-1}. It is reported that when the Auger recombination coefficient is greater than 10^{-31} cm^6 s^{-1}, the effect of the Auger recombination on the droop is more obvious, which is in good agreement with the experimental results. Felix Nippert et al. found that the IQE losses are related to the temperature dependence of the radiative and Auger processes. While the radiative process increases only weakly with temperature, non-radiative Auger recombination increases steeply, becoming a significant contributor to the green gap [134].

6.2.3 Light Extraction

In the GaN-based green LED, the light extraction efficiency seriously restricts the improvement of external quantum efficiency. For the green LEDs, if the incident angle of the photon is less than the critical angle, the photon can escape from the materials; otherwise the photon is difficult to escape the semiconductor [135]. However, due to the high refractive index of the nitride semiconductor material and the absorption of photons in the material, the photon-extraction efficiency is very low.

To reduce the light absorption by the metal pads and enhance light extraction efficiency, the transparent highly conductive electrodes are employed in the LEDs. The transparent highly conductive electrode is used to increase the lateral current spread and reduce the photons absorption by the metal electrodes. Due to the low p-type carrier concentration in GaN, the lateral spread of current in p-type GaN is relatively poor. Therefore, indium tin oxide (ITO) [136] is widely used as a current spreading layer for the GaN-based LEDs. In addition, semiconductor materials such as ZnO [137], TiO2 [136], MgO [138], and graphene[139, 140], which are preferable in terms of lateral conductivity, are also used as the transparent electrodes.

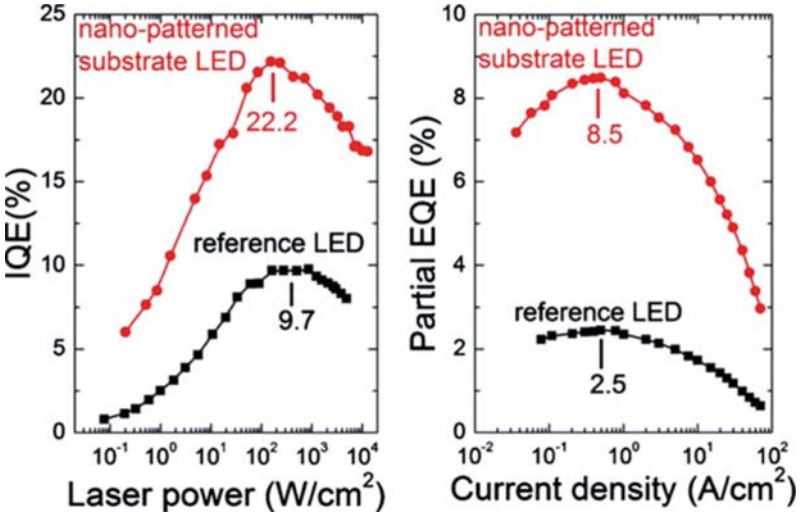

Fig. 6.25 (**a**) IQE as a function of excitation power density, (**b**) EQE as a function of current density for the nanopatterned substrate circles and the reference squares LED

The metal reflector is deposited on the back of the LED to improve the reflection of light, improving the efficiency of photons extraction [141, 142]. The most commonly used metal reflector for GaN-based LEDs is Ni/Al/Pt/Au. In addition, a distributed Bragg reflector (DBR) with multiple layers of different refractive index materials can also be used as the reflector [143, 144].

In order to improve the efficiency of photon extraction, new chip shapes are proposed [145–149]. Since the LED with a planar structure has a small critical angle, it is difficult for the photon to escape the semiconductor. Therefore, it is necessary to design a new chip shape structure to improve the probability of photon escape. For example, the hemispherical shape design can better improve the critical angle of the outgoing photon in the device. The small lens prepared by the etching method can greatly improve the light output power. Omron uses a combination of two lenses with different sizes and doubles the efficiency of LED light extraction. In addition, change in the shape of the LED chip, such as quadrilateral, triangular, round, pyramid, funnel, inverted trapezoid, etc., can increase the LED light area and finally improve the LED light extraction efficiency.

Patterned sapphire substrate (PSS) technology is also used to improve the efficiency of LED light extraction [150–153]. As is shown in Fig. 6.25, for the LED with sapphire substrate, the spectral interference and emission patterns reveal a 58% enhanced light extraction, while photoluminescence reveals a doubling of the internal quantum efficiency [152]. The nanoscale or microscale pattern on the substrate can effectively improve the photon reflection, change the emitting direction of the photons, and ultimately achieve the promotion of LED light extraction. Furthermore, PSS also can solve the problem of epitaxial growth quality.

Surface roughening technology can also improve the efficiency of LED light [154–156]. There are a variety of surface roughening techniques, such as laser bombardment of LED material surfaces, wet etching, secondary epitaxial growth of materials, or the combination of the above techniques. These surface roughening techniques are relatively simple and practical and can achieve better photon escape efficiency.

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Chapter 7
Al-Rich III-Nitride Materials and Ultraviolet Light-Emitting Diodes

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7.1 Heteroepitaxy of AlN Material by MOVPE

7.1.1 Al Precursor-Related Pre-reaction Issues in AlN MOVPE

High-quality AlN materials are the key element in obtaining efficient DUV LEDs. However, the chemical reactions between the Al related metal-organic precursors (trimethylaluminum, TMAl) and ammonia (NH_3) are very complicated in the MOCVD chamber and depend on the different growth atmosphere. The chemical equation for the AlN growth can be written as:

$$Al(CH_3)_3 + NH_3 = AlN\,(s) + 3CH_4 \tag{7.1}$$

Except for the formations of AlN, many parasitic products may form due to the parasitic gas reactions [1–5]. These products, such as Lewis acid-base adducts ($TMAl{:}NH_3$), polymers ($[DMAlNH_2]_n$, $[NH_3{:}DMAlNH_2]_n$, and so on),

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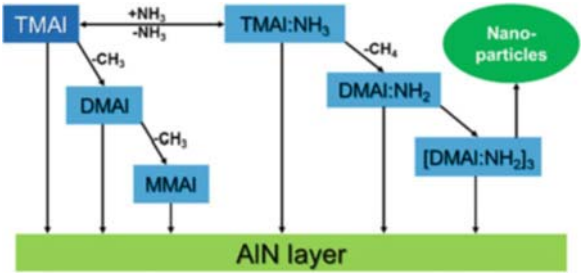

Fig. 7.1 Schematic of the main gas reaction paths in III-nitride MOVPE growth

and nano-sized particles, will interfere the growth process severely [6, 7]. The parasitic reactions will cause the contamination on the reactor walls and on the growing films. Furthermore, the surface morphology and the quality will be deteriorated [8, 9]. Besides, the growth efficiency will be decelerated owing to the waste of sources [8]. Thus, there are two essential aspects for improving the material quality and increasing the growth efficiency in AlN MOVPE growth. Firstly, the reaction mechanism including thermodynamic and kinetic theory should be studied. After that, the approaches to reduce the parasitic reactions should be found out.

7.1.1.1 Reaction Mechanism (Thermodynamics and Kinetics)

To date, many researches have been done to understand the gas reaction paths in AlN MOVPE growth. Generally, there are two competing paths in the gas reactions between TMAl and NH_3 which are called the adduct reaction path and the pyrolysis path [6, 9–11], as shown in Fig. 7.1. In the adduct reaction path, TMAl and NH_3 produce the donor-acceptor complex adduct, TMAl:NH_3, at room temperature upon mixing. When the temperature rose up, the adducts may decompose into amides, $DMAlNH_2$ (or $Al(CH_3)_2NH_2$), with the release of CH_4. The $DMAlNH_2$ adduct often can be observed near the nozzle [10]. After that, the amides can easily oligomerize into oligomers, $[DMAlNH_2]_x$ ($x = 2$ or 3), due to the high reactivity of amides. The oligomers are the main source of the nano-sized particles, which are the main contamination on the reactor walls and on the epilayers. Instead of contributing to the growing crystal, white powders are usually deposited on the reactor walls of the growth chamber. Additionally, it's possible that the second NH participates in the adduct reaction path to form the two-NH_3 adduct, NH_3:TMAl:NH_3, or the amide-adduct, NH_3:$DMAlNH_2$ for the large quantity of the NH_3 gas in the MOVPE chamber comparing with the quantity of the TMAl [7, 12–15]. In the pyrolysis path, TMAl directly pyrolyzes into DMAl, MMAl, and/or Al successively near the hot substrate region with the release of CH_3 [16].

The gas reaction paths as abovementioned have been proved by huge experimental results. At low temperature, the experimental mass spectrometry results confirmed the formation of cluster compounds in the gas phase upon laser irradiation of TMAl-NH_3 mixtures [16]. The TMAl:NH_3 adducts were structurally

characterized in the solid state by X-ray diffraction (XRD) [17]. Its pyrolysis in the condensed phase yields the amido- and imidoalanes and AlN [18]. Sauls and Interrante also studied the detailed formation and thermal decomposition of the $TMAlNH_3$ in solution phase [19, 20]. The dissociation enthalpy of the TMAl-NH_3 bond between donor and acceptor was evaluated by solution calorimetry in benzene (95 ± 5 kJ/mol) [20] and in hexane (115 ± 1 kJ/mol) [21]. The Fourier transform infrared spectroscopic studies revealed the activation energy of methane elimination considering the kinetics of the gas reaction paths between TMAl and NH_3 is 107.5 kJ/mol [6]. Amato proposed the existence of $DMAlNH_2$ in the gas phase at MOCVD conditions through the observation of the intermediate in the decomposition of $TMAlNH_3$ in solution [22]. Müller has found the monomeric $DMAlNH_2$ as a production of UV irradiation of matrix-isolated TMAl-NH_3 [23]. These experimental results can prove the reasonability of the gas adduct reaction paths. Also, there are many studies about the pyrolysis reaction paths [24–26]. For the reason that these reactions won't produce the parasitic productions, we don't talk more about the experimental results about that.

In order to understand the gas-phase chemistry, it's necessary to study the reaction mechanisms by the thermodynamics and kinetics theory. The density functional theory (DFT) method is often applied to study the theoretical mechanisms. All calculations are often done in Gaussian 03 software package, Gaussian 09 software package, the Vienna ab initio simulation package (VASP) code, and so on [18, 25, 27, 28]. The atomic structures should be optimized and the varied transition states should be induced to verify the connections between reactants and products. After the detailed calculation, the changes of enthalpies and Gibbs free energies of the reactions at different growth parameter can be used to postulate the detailed mechanisms and further useful for the achievement of the high-quality AlN films. Here, we mainly paid our attention on the formation of the parasitic productions which are usually formed by the adduct reactions. Thus, among the gas reactions, we'll introduce them in four aspects: the initial process of the adduct reactions, the adduct reactions as the functions of temperature, the adsorption of the adducts on the surface, and the decomposition processes of the TMAl precursor.

7.1.1.2 The Initial Process of Adduct Reactions

Lisovenko et al. have explored the mechanisms of initial stages of gas-phase reactions between TMAl and NH_3 by DFT studies [18]. They considered the subsequent substitution of CH_3 groups in TMAl by NH_3 groups and substitution of hydrogen atoms in ammonia by TMAl groups. So the intermediates include $TMAlNH_3$, $Al(CH_3)_x(NH_2)_{3-x}$, $NH_x(Al(CH_3)_2)_{3-x}$ ($x = 0$–3), and the transition states. There are 13 kinds of transition states that have been induced and calculated. Here they just considered the $[DMAlNH_2]_2$ dimer production which is formed by the subsequent reactions. According to these results, the initial corresponding reaction paths have been obtained, as shown in Fig. 7.2. According to the thermodynamic characteristics of the reactions, the first methane elimination from $TMAlNH_3$ is the highest point

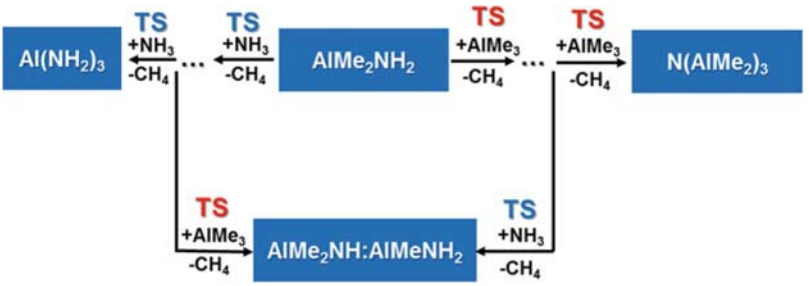

Fig. 7.2 The initial reaction pathways and corresponding compounds

on the reaction paths and the only one lying above the isolated TMAl and NH_3. It's an exothermic process for the subsequent substitution of methyl groups in TMAl by amido groups, but the intermediate steps make the activation energies of the reaction larger, even though the overall reaction profile is rather downhill. These results support that the first methane elimination is a rate-limiting step for the whole reactions. In addition, the reaction leading to $[DMAlNH_2]_2$ dimer and the reactions of subsequent substitution are competitive. Also, these processes may operate at the same time. Besides, they found higher vapor pressure is helpful for the dimerization reactions, while lower vapor pressures and excess of one of the reagents will favor the substitution pathways. According these results, the lower vapor pressure and excess of one of the reagents may suppress the formation of dimerization productions.

7.1.1.3 The Adduct Reactions as the Functions of Temperature

Ran Zuo calculated the changes of enthalpy ΔH and Gibbs free energy ΔG as the functions of temperature to predict the most probable reaction paths [27]. Their results and some literature values at room temperature are shown in Table 7.1, which indicates the accuracy of Zuo's quantum chemistry calculation. As shown in Fig. 7.3, there exists a critical temperature, T_{eq} ($T_{eq} \approx 480$ K), for the formation of TMAl:NH_3. When the $T < T_{eq}$, $\Delta G < 0$, and there is no energy barrier and the reaction will occur spontaneously; when $T > T_{eq}$, $\Delta G > 0$, and the adduct may dissociate back into TMAl and NH_3 with a small energy barrier equivalent to the heat release in the adduct formation; and when $T = T_{eq}$, $\Delta G = 0$, and the adduct formation and dissociation are in equilibrium. After the formation of TMAl:NH_3, there are two paths and corresponding two translate states: the traditional formation of $DMAlNH_2$ and the second participates of NH_3, which is the formation of the two-NH_3 adduct, NH_3:TMAl:NH_3. The changes of ΔH and ΔG at different temperatures in one-NH_3 involved adduct reaction path were shown in Fig. 7.4a, b. The changes of ΔH and ΔG at different temperatures in two-NH_3 involved adduct reaction path were shown in Fig. 7.4c, d. The two-NH_3 involved adduct reactions

Table 7.1 Comparisons of calculated results of ΔH and ΔG with literature values in the adduct reactions of TMX + NH3 (X = Ga and Al) at room temperature (ΔG* denotes values calculated from ΔG = ΔH − TΔS) [27]

Reactions	Calculated value (kcal/mol)	Literature value (kcal/mol)	Methods	Reference
$TMAl + NH_3 \rightarrow TMAl{:}NH_3$	ΔH: −21.56	ΔH: −19.06	B3LYP/def2-TZVPP	Lisovenko et al. [18]
		ΔH: −20.4	B3LYP/6-311++G(d,p)	Wang and Creighton [14]
		ΔH: −23.17	B3LYP/LanL2DZ*	Nakamura et al. [15]
		ΔH: −27.2	B3LYP/6-31G(d,p)	Simka et al. [12]
	ΔG: −8.27	ΔG: −7.21	B3LYP/def2-TZVPP	Lisovenko et al. [18]
		ΔG: −16.0	B3LYP/6-31G(d,p)	Simka et al. [12]

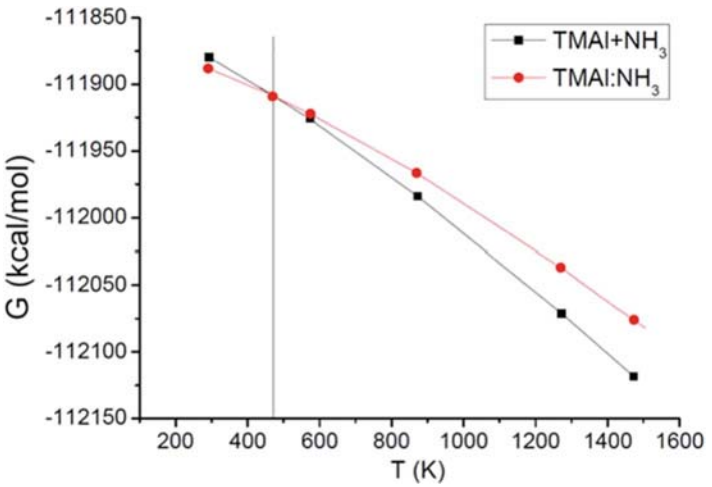

Fig. 7.3 Changes of Gibbs free energies with temperature for TMAl adduct reactions [27]

compared to the one-NH_3 involved adduct reactions are disfavored and the most probable adduct reaction path should be the one-NH_3 involved process. Their study indicated the importance of the temperature for the different reaction paths. The proper temperature should be chosen to obtain the high-quality AlN films.

7.1.1.4 The Surface Reaction of the Adducts

Yumi Inagaki studied the adsorption of the adducts on the surface of the epilayers [28]. They found $DMAlNH_2$ is one of the major reactive involved in the AlN

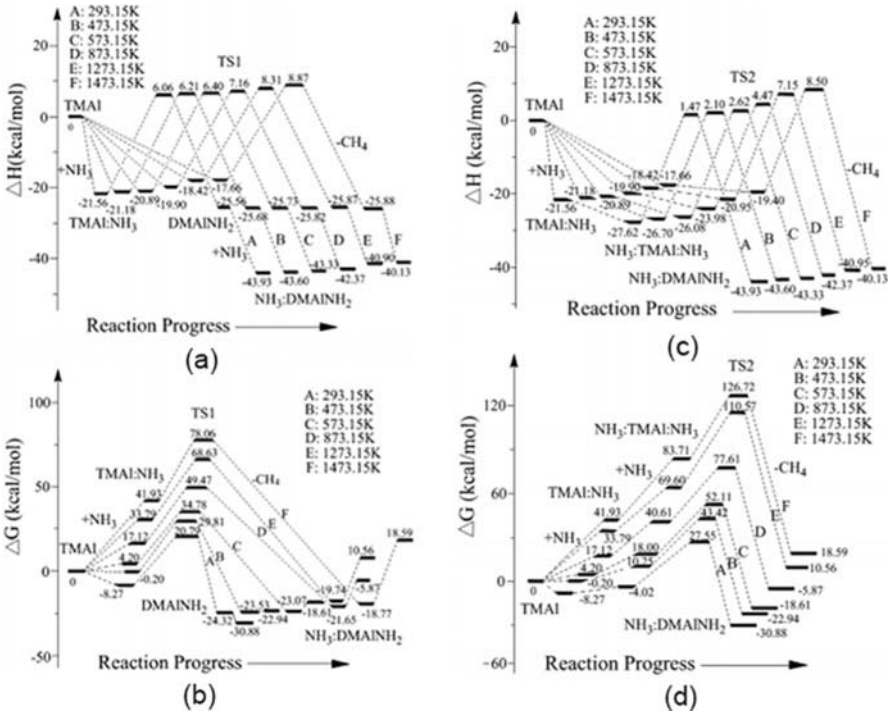

Fig. 7.4 Changes of ΔH (**a**) and ΔG (**b**) in one NH_3 involved adduct reaction path at different temperatures and changes of ΔH (**c**) and ΔG (**d**) in two NH_3 involved adduct reaction path at different temperatures [27]

growth according to the surface reactions between $DMAlNH_2$ and AlN, as shown in Fig. 7.5. The $DMAlNH_2$ can be adsorbed on the surface owing to their simulation results. Then the methane can eliminate from the surface, and finally the Al atoms of $DMAlNH_2$ have been incorporated into the lattice of the AlN epilayers with no energy barrier. So $DMAlNH_2$ is also one of the primary reactive species for AlN growth. This result shows the adduct reaction paths are also very important for the growth of AlN.

7.1.1.5 The Decomposition Processes of the TMAl

Obviously, the adduct reaction paths are the key element for the study of the parasitic reactions and parasitic products. However, the decomposition of the metal-organic precursor TMAl sometimes is also important for the design of the MOVPE. Kazuki Sekiguchi studied the decomposition processes of the TMAl at finite temperature [25]. The detailed chemical reaction formulas as shown follow and the calculated ΔG result is shown in Fig. 7.6.

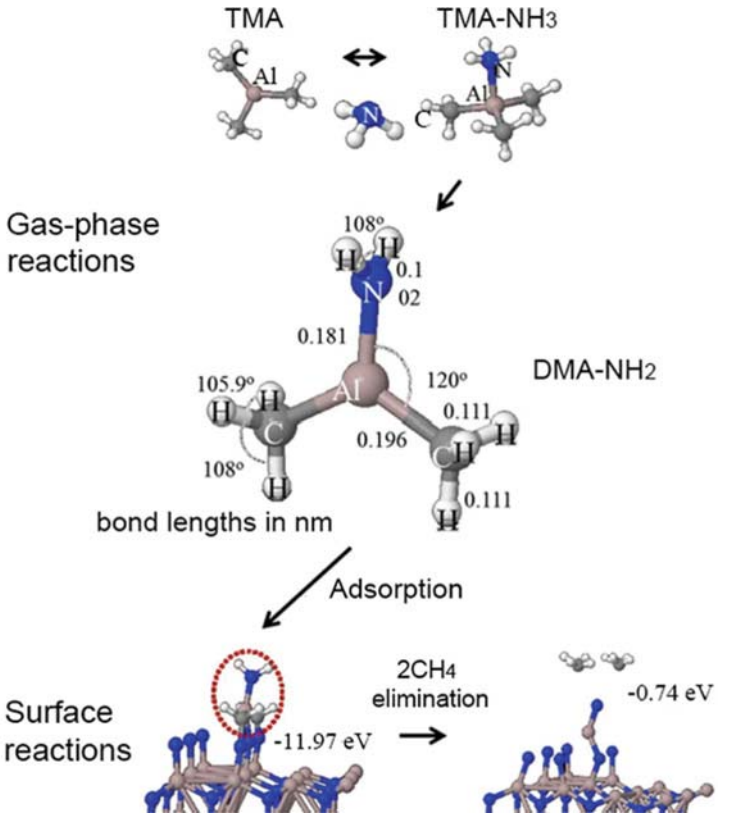

Fig. 7.5 Growth process, including gas-phase and surface reaction of AlN through DMAl-NH_2 (including the molecular structure of DMA-NH2 and adsorption and elimination energies at the surface) [28]

$$2Al(CH_3)_3\,(g) + H_2\,(g) = 2Al(CH_3)_2\,(g) + 2CH_4\,(g) \tag{7.2}$$

$$Al(CH_3)_3\,(g) + H_2\,(g) = Al\,(CH_3)\,(g) + 2CH_4\,(g) \tag{7.3}$$

$$2Al(CH_3)_3\,(g) + 3H_2\,(g) = 2Al\,(g) + 6CH_4\,(g) \tag{7.4}$$

$$Al(CH_3)_3\,(g) + NH_3\,(g) = (CH_3)_2\,AlNH_2\,(g) + CH_4\,(g) \tag{7.5}$$

The adduct reaction is the easiest to occur below 1500 K. TMAl almost completely reacts with not H_2 but NH_3, leading to the formation of the $(CH_3)_2AlNH_2$ adduct at 700 K. This is consistent with the AlN materials observed near the nozzle. Thus, it's important to design the nozzle to inhibit the reaction between precursors.

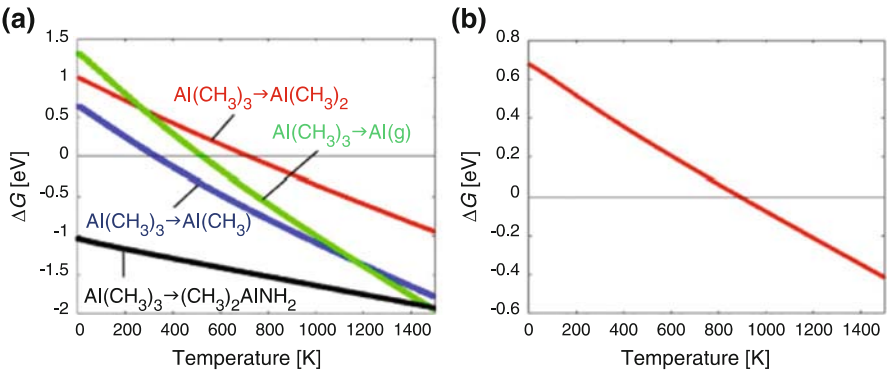

Fig. 7.6 (**a**) Calculated Gibbs free energy difference ΔG. The red, blue, green, and black lines show ΔG values for the reactions in which TMA becomes DMA, MMA, Al, and the $(CH_3)_2AlNH_2$ adduct, respectively. (**b**) Calculated Gibbs free energy difference ΔG. The red line shows ΔG for the reaction in which MMA decomposes into gas-phase Al Atoms [25]. Copyright (2017) The Japan Society of Applied Physics

TMAl was found to decompose into monomethylaluminum ($Al(CH_3)$) between 330 K and 1200 K and into gas-phase Al atoms above 1200 K. It's crucial for the design of the thermal field in the MOVPE chamber.

7.1.1.6 Approaches to Reduce the Parasitic Reactions

So far, many approaches have been used to reduce the parasitic reactions and further improve the AlN quality and growth efficiency. It does reduce the parasitic reactions to lower the chamber pressure or increase the growth temperature due to the study of the reaction mechanism mentioned above [4, 29–31]. However, the raising of the temperature is limited by the uniformity and stability of the chamber's thermal field. Moreover, the descending of the chamber pressure and the ascending of the growth temperature will impede the p-type doping as nitrogen vacancies acting as shallow donors in III-nitride materials are increasingly generated.

In recent years, the pulsed deposition method has been developed to inhibit the parasitic issue [32–34]. Through a pulsed and independent supply of the metal-organic gas precursors from NH_3, the pre-mixture of the gas reactant can be controlled and at last the AlN quality can be improved. What's more, the migration of Al atoms on the surface of the epilayers can be enhanced. Nevertheless, this method will waste huge time for waiting as the ordinary valve is difficult to switch at high frequency. So the growth rate has been decreased by a factor of two or three times owing to the limitation of the pulsed time. These inferiors make the pulsed method less attractive for production.

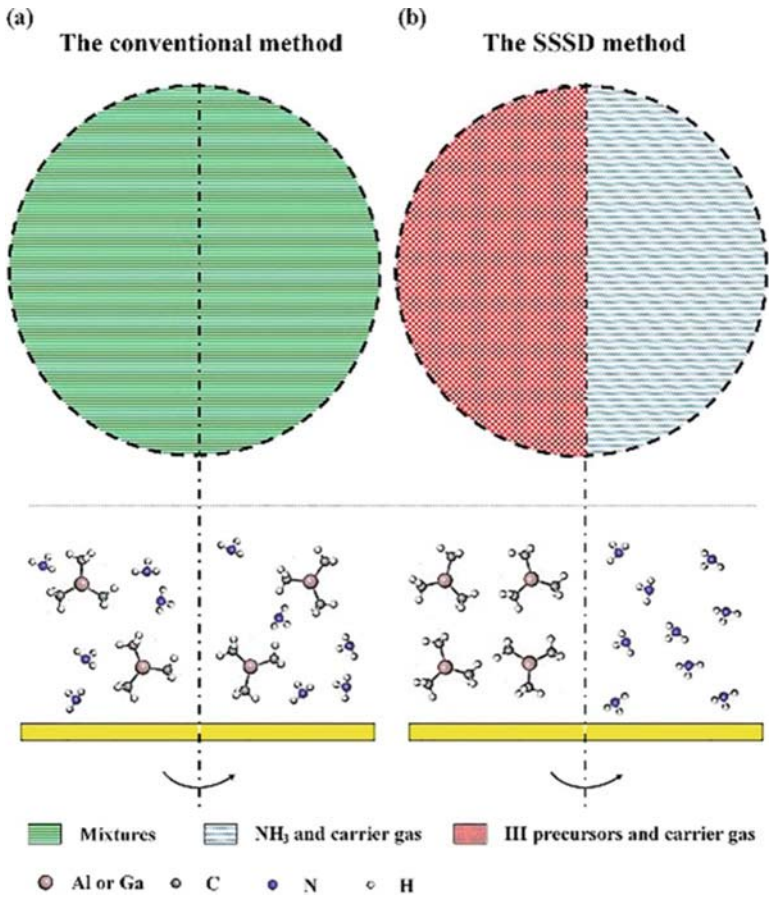

Fig. 7.7 (**a**) The conventional and (**b**) the spatial separated source delivery (SSSD) method of the MOCVD system [8]

Except for these conventional methods, some special approaches have been adopted [8, 35–37]. Lai et al. deposited an AlN epilayer with suppressed parasitic reactions by raising the hydrogen flow rate (20 slm) under a higher chamber pressure (100 torr) [37]. Yang et al. proposed a spatial separated source delivery (SSSD) method to alleviate the parasitic reactions between group III precursor and NH_3 [8]. The gas injection method of the MOCVD system has been modified, as shown in Fig. 7.7a. This design of the gas injection system can spatially separate group III precursor from NH_3 in gas phase. The separation of precursors near the injection system makes the combination reactions occur only on the surface of the substrates. This physical separation method directly prevents any reactions in the gas phase. Additionally, the growth rate has been promoted and the sources consumption has been reduced apparently. The uniformity of the epilayers has been improved. So the

SSSD method is a promising high-efficiency method to solve the parasitic reaction issue. Similarly, Chung et al. used the N_2 purge line to spatially separate the AlN precursors [36]. They separated TMAl and NH_3 by N_2 purge flow. It's similar as the SSSD method for spatially separating the precursors in the gas phase. So the parasitic reactions also can be inhibited efficiently.

It's crucial to inhibit the parasitic reactions between TMAl and NH_3 for improving the quality and the growth efficiency. The main gas reaction paths of AlN materials have been induced according the theoretical works and experimental works by researchers. The reaction mechanism has been induced, including the initial process of the adduct reactions, the adduct reactions as the functions of temperature, the adsorption of the adducts on the surface, and the decomposition processes of the TMAl. The conventional methods have been applied to induce the parasitic reactions: decreasing the chamber pressure and increasing the growth temperature, the pulsed method, and so on. In recent years, many new approaches have been employed: increasing the H_2 flow, the SSSD method through optimizing the gas injection system, and so on. These methods are promising to solve the parasitic reaction issue and do not decrease the growth efficiency. However, there are also many works need to be done about the parasitic reaction issues. The detailed chemical mechanism of the gas reaction pathways between TMAl and NH_3 gas should be unified and proved by more experimental results: translate states, intermediates, detailed gas reaction, and so on. Additionally, the relations between enthalpy ΔH, Gibbs free energy, ΔG and other growth parameters (such as the chamber pressure, the V/III ratio, the gas flow the rotation rate of the substrate, and so on) should be studied. The approaches to reduce the parasitic include the optimization of the growth parameter, the design of the MOVPE system, and so on.

7.1.2 Defects and Stress Control of AlN Epitaxy on Sapphire

The defects caused by parasitic reactions can be released by some methods as mentioned above. Additionally, the lattice mismatch and thermal mismatch between AlN and hetero-substrate owing to lack of native substrate bring the severe defects and stress issues [38]. Sapphire materials are usually chosen as the substrates caring about the crystal lattice and price factor [2]. There are still 13.3% mismatch existence between AlN and sapphire even after the two lattices rotate by a 30° angle [39, 40]. Moreover, the Al atomic surface mobility is very low comparing with Ga atom. It's difficult to form the 2D growth model for AlN resulting in the low-quality materials. The generation of threading dislocations along the island boundaries may decrease the internal quantum efficiency (IQE) of DUV LEDs due to the non-radiative recombination of excited carriers at these dislocations. The threading dislocation density (TDD) should be controlled in the range of 10^7 cm^{-2} to keep IQE close to unity according to Martin Guttmann's report [41]. Except for the defect issues, stress in AlN films also affects the property of DUV LEDs. Huge stress may result in cracks, wafer bowling, and high defect densities [42–44]. Cracks

in epitaxial layer may cause electric leakage. Wafer bowling results in the difficult control of the wafer uniformity. Thus, the defects and stress control of AlN grown by MOCVD on sapphire really matters. The convenient techniques will be introduced as follows.

The quality of GaN has been improved prominently due to the development of two-step method. The two-step method also has been used in the growth of AlN [38]: after the H_2 flowing the sapphire substrate at high temperature for a short time to clean the surface, the low-temperature AlN (LT-AlN) layers are usually grown as the buffer layer at low to medium temperatures of about 600–1000 °C with high V/III ratio (>1000), then the high-temperature AlN layers are deposited on the LT-AlN buffer. The growth atmosphere usually set at low power. However, the quality of AlN grown by two-step methods still needs to be improved. From now on, many methods have been developed to improve the AlN quality. Thanks to those methods, the external quantum efficiency (EQE) of DUV LEDs has been improved. Comparing with the EQEs of visible-wavelength LEDs, it's no doubt the efficiencies and output powers of DUV LEDs will continue to develop. Here, we divide the conventional methods of the AlN heteroepitaxy into four kinds of techniques: epitaxial lateral overgrowth (ELOG), buffer-assisted technique, different interlayers, and special growth process control.

7.1.2.1 Epitaxial Lateral Overgrowth

ELOG on masked AlN template or patterned sapphire substrate has been proved to be an effective way to further reduce the TDDs in GaN epitaxy [45, 46]. Researches about AlN ELOG also have been studied in recent years [47, 48]. Researchers have found many threading dislocations would generate from the AlN/sapphire interface and then spread upward in the support mesa regions. After that, some dislocations over the mesa region and near the air gap would be looped, bend, or get annihilated. Thus, the TDDs in AlN films deceased apparently. Khan et al. reported 290 nm emission AlGaN-based DUV LEDs exhibiting stable cw-powers in excess of 2 mW over pulsed laterally overgrown (PLOG) AlN [47]. AlN with 15–10-μm-thick was grown using a pulsed growth mode on the micro-sized air-bridge AlN template. The achieved AlN films had significantly reduced number of threading dislocations ($\sim 10^7$ cm^{-2}) and showed a smooth surface in the lateral overgrowth area. The schematic diagram of the LED structure and the cross-sectional SEM image of PLOG AlN were shown in Fig. 7.8. Comparing with the two-step method, the TDD of AlN grown by PLOG decreased 10^2–10^3 cm^{-2}. Except for the air-bridge AlN template, there are many other methods to be used for the ELOG method, such as self-assembled patterned AlN nanorods [49], nano-sized trench-patterned AlN [50], and so on.

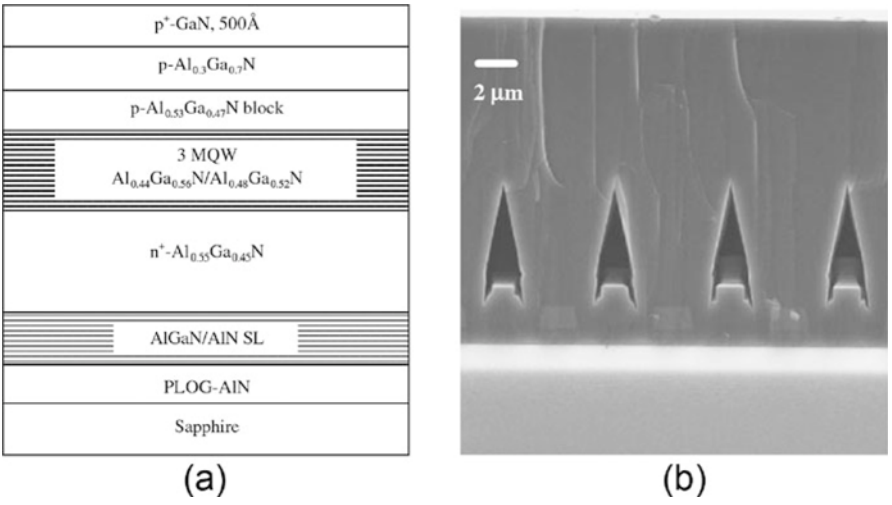

Fig. 7.8 (**a**) The schematic diagram of the LED structure and (**b**) the cross-sectional SEM image of PLOG AlN [47]. Copyright (2007) The Japan Society of Applied Physics

7.1.2.2 Buffer-Assisted Technique

Buffer plays a crucial role on the quality of epilayers [51]. There are mainly three effects for the growth of AlN. Firstly, buffer provides nucleation sites whose crystal orientation is similar with substrate for AlN epilayers. Secondly, the buffer layer can release some stress that comes from the lattice mismatch and thermal mismatch between the epilayer and foreign substrate. Thirdly, the buffer with the smooth and flat surface can help the nucleation of AlN for the reason of decreasing the growth contact angle of AlN crystal grains at high temperature. Thus, the AlN islands can coalesce in the range of smaller thickness and the growth model can easily transfer from 3D mode to quasi-2D mode.

The typical buffer of AlN films is AlN layer grown at low temperature (600–1000 °C). Recently, there are some advanced buffer layers that have been developed. Here we mainly introduce four kinds of advanced methods based on buffer-assisted technique: annealing of an AlN buffer at high temperature, sputtering AlN buffer, buffer with Mg-Si codoping pair, and dual buffer.

Miyake, Hideto et al. reported the annealing of an AlN buffer in a carbon-saturated N_2-CO gas AT 1650–1700 °C for 1 h [52]. The 2-μm-thick AlN on the annealed AlN buffer showed high quality by MOCVD. The FWHM values of the (002)- and (102)-plane XRCs were 16 and 154 arcsec, respectively, and the corresponding threading dislocation density was only 4.7×10^8 cm^{-2}. This annealing AlN buffer method is very significant to improve the quality of AlN films. Recently, researchers found the sputtering present a promising candidate as a buffer for AlN films owing to its low price and time-saving. Ohtsuka et al. improved the crystal quality of AlN by increasing the mobility of the Al sputtered atoms on the

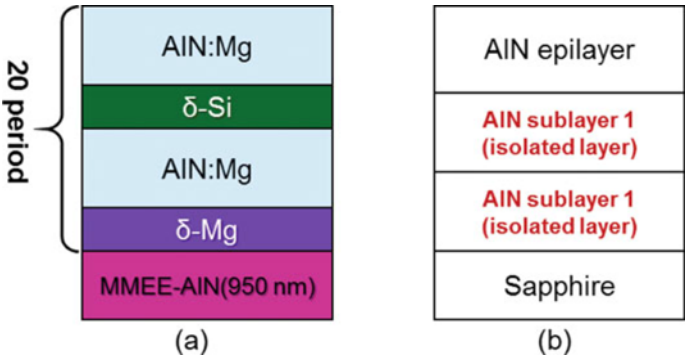

Fig. 7.9 (**a**) Schematic diagram of the Mg-Si codoping pair structure and (**b**) the schematic diagram of the dual buffer layer structure

surface through lowering sputtering pressure [53]. They investigated the effect of sputtering pressure on the morphology, crystal quality, and stress of AlN films by pulsed DC reactive sputtering. It was found that increasing pressure could cause the surface damage of the AlN sputtered films because of arcing. Meanwhile, the sputtering pressure would affect the crystal quality and residual stress of AlN films due to a change in the number and energy of Ar^+ ions and Al sputtered atoms. Soomro et al. reported a Mg-Si codoping pair for the quality improvement and misfit strain release of AlN films grown by MOCVD [54]. The schematic diagram of the Mg-Si codoping pair structure is shown in Fig. 7.9a. The achieved as-grown AlN:Mg-Si shows the release of misfit strain, whose stress was close to the stress-free statue. Zhao reported a dual buffer layer structure, which is shown in Fig. 7.9b [55]. This approach can weaken the negative nitridation effect and improve lateral growth condition in the initial growth stage. Their experiment results suggest the thicker the dual AlN buffer, the rougher the AlN surface and the higher the AlN quality. These advanced buffer-assisted techniques mentioned above were proved to improve the AlN quality through changing the growth process of structure of buffer layers.

7.1.2.3 Interlayers

In order to block the extend of the edge dislocations in the AlN epilayers, a few kinds of interlayers have been developed. Moreover, the interlayers can release residual stress in AlN films. The Mg-Si codoping pair structure mentioned above also can be regarded as an interlayer.

Four kinds of interlayers were introduced as follows: intermediate-temperature interlayers, in situ SiN_x masks, superlattice structure, and Si-doping AlN interlayers. Chen et al. reduced the TDD in AlN layers through adopting AlN intermediate-temperature interlayers [56]. They found the growth temperature and the thickness

of the AlN interlayer affected the growth mode. Their results showed the growth mode would change from three-dimensional (3D) growth to two-dimensional (2D) growth mode with the temperature of the interlayer increasing from 470 to 670 °C. Then the growth mode would change into 3D growth mode again when the temperature rose to 870 °C. They provided a promising way to improve the surface morphology and crystal quality of AlN films. Chen and Yan also proved the intermediate-temperature interlayer could reduce the density of defect in the reference [56, 57], respectively. Vennegues et al. reported an in situ SiN_x mask originating from the decomposition of silane and ammonia can reduce the TDD in GaN films [58]. This SiN_x mask can block the vertical propagation of some dislocations by lateral epitaxial overgrowth [59]. This method can be used in the UV range with AlGaN compositions [60]. The superlattice has been developed as another usual interlayer of reducing TDD and release stress in AlN films. It has been proved the effectiveness of the short-period superlattice of alternating Al(Ga)N/(Al)GaN as strain-releasing and dislocation-annihilation layers [61, 62]. Streubel et al. reported Si-doped (10^{19} cm^{-3}) AlN interlayer was another approach of reducing TDD [63].

7.1.2.4 Special Growth Process Control

Growth process plays an important role in the growth mode of AlN epilayers. Some methods based on the control of special growth process have been developed recently, such as changing V/III ratios [64–66], NH_3 pulsed flow [32, 67], migration enhanced epitaxy (MEE) [68, 69], and mixture carrier gases [70].

V/III ratio is an important parameter for the growth of AlN films. It affects the growth mode, lateral growth rate, and crystal quality. Usually, V/III ratio is constant during the whole growth. Imura et al. controlled V/III ratio into changeable during the growth of AlN films [64, 65]. The multiple modulation of the V/III ratio resulted in higher-quality AlN layers than growth with an unchangeable V/III ratio. The dislocation density of the AlN films was $<3 \times 10^8$ cm^{-2}. They found different V/III ratio led to different growth rate for each facet. Thus, the macroscopic form of grain would change at the transition V/III ratio. The threading dislocations were annihilated with the formation of dislocation loops at the changing of the macroscopic grain [65]. Wang et al. reported the annihilation of defects with alternating high and low V/III ratios [66]. They found this structure was suitable to fabricate the stacking structure and superlattice layers. This method could help achieve an AlN films with optimal quality at a low temperature.

Oshika and Shatalov et al. developed the NH_3 pulsed-flow multilayer growth method and reduced the TDD by a factor of 100 [32]. Hu et al. investigated the effect of $H_2 + N_2$ mixture carrier gases on the AlN films [70]. They found the size of the initial AlN islands and the stress statue in AlN films could be controlled by the different carrier gases. Especially, the in-plain stress is only 0.1 GPa with the 0.5 slm N_2 + 2.5 slm H_2 mixture gas. Moreover, the AlN films had good crystal quality under this condition.

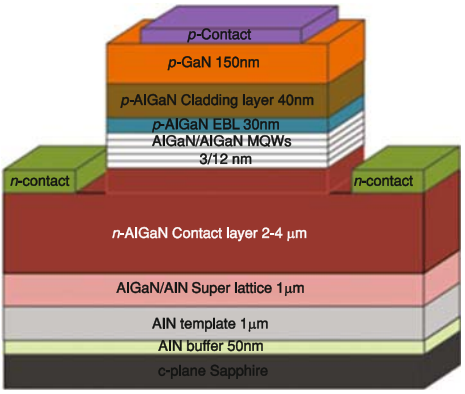

Fig. 7.10 Schematic diagram of a typical AlGaN-based DUV LED epitaxial structure

In conclusion, many methods have been developed to reduce the density of defects and release the stress in AlN films. These significant works paved the way on the commercial application of AlGaN-based DUV LEDs.

7.2 Structural Design for Efficient DUV LEDs

The typical epitaxial structure of a 280-nm AlGaN-based DUV LED is shown in Fig. 7.10, including high-temperature AlN template layer grown on planar sapphire substrate, AlGaN/AlN superlattice stress release layer, Si-doped n-AlGaN contact layer, $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ MQWs active region, Mg doped p-AlGaN electron blocking layer, p-AlGaN/p+-GaN hole injection layer.

The n, p, and active regions of the UV LED are all AlGaN materials; the quality of AlGaN material is closely related to the efficiency of DUV LED. The relationship between the internal quantum efficiency (IQE) and dislocation density of the 280 nm UV LED was simulated by Kneissl et al. [71]. Ban et al. [72] also reported the relationship between the IQE and dislocation density under weak excitation and 1×10^{18} carrier concentration. According to the researches, when the dislocation density is $>10^{10}$ cm^{-2}, the IQE is only a few percent. When the dislocation density is reduced to 10^9 cm^{-2} level, the IQE of the 280 nm UV LED will be increased to 10–40%. If the IQE is increased to more than 40%, the dislocation density is required to reduce to 10^8 cm^{-2} lower level. Therefore, obtaining high-quality AlGaN epitaxial material is the basis of preparation of high-efficiency DUV LED.

The quality of AlGaN based on sapphire substrate depends on the quality of AlN template. Therefore, it is the key to improve the quality of AlN template. In our research group, a crack-free AlGaN epitaxial layer was successfully obtained by using high-temperature AlN intercalation [73]. Compared to the low-temperature AlN and AlGaN intercalation techniques, respectively, reported by Kamiyama et al. [74] and Amano et al. [75], the high-temperature AlN intercalation layer is more favorable to the quality of the subsequent epitaxial AlGaN material.

7.2.1 AlN and High Al Component AlGaN Epitaxy Technology

In 1992, high-quality AlN was grown on sapphire substrates by Khan et al. [76–78] using a switched atomic layer epitaxy (SALE) technology. In 2005, migration-enhanced MOCVD technology (MEMOCVD) was developed by SETi and Khan et al. [79]; the MEMOCVD technology can grow high-quality AlN templates and AlN/AlGaN superlattices and improve the quality of AlGaN material [80].

In 2009, a 270 nm UVC LED with a maximum output of 2.7 mW light output was achieved by Hirayama et al. [81] using the NH_3 pulse access method on the micron grade grooved AlN/sapphire template. Moreover, the threading dislocation density was reduced to 10^8 cm^{-2}.

In 2013, our research group realized epitaxy AlN templates on a flat sapphire substrate (FSS) [82] and further improved the crystal quality of the AlN template by the nano-patterned sapphire substrate (NPSS) [83]. The results show that the NPSS can effectively alleviate the stress in the AlN epitaxial layer.

7.2.2 Study on N-Type Doping of AlGaN Materials

For n-type-doped AlGaN, great progress has been made at present. Several study groups showed that n-type doping efficiency of AlGaN can be improved significantly by restraining the formation of self-compensating defects, and even n-type conductive Si-doped AlN was obtained [84–89]. In 2002, Hwang et al. [90] prepared Si-doped high Al (50%) component AlGaN by molecular beam epitaxy (MBE). The AlGaN has an electron concentration up to 1.25×10^{20} cm^{-3}. But the electron mobility is low. In 2011, AlGaN material with an Al component of 85% and the resistivity of 0.1 Ω cm was achieved based on AlN single crystal substrate by Collazo et al. [91]. Moreover, the doping concentration, carrier concentration, and carrier mobility of $Al_{0.8}Ga_{0.2}N$ material are 6×10^{18} cm^{-3}, 1×10^{18} cm^{-3}, and 40 cm^2 V^{-1} s^{-1}, respectively. Therefore, n-type conductance can be provided for DUV LED with wavelengths as short as 250–260 nm.

7.2.3 Study on P-Type Doping of AlGaN Materials

The problem of doping efficiency of p-type AlGaN materials is more prominent. The activation energy of Mg acceptors in p-type GaN is 160–200 meV [92]. In AlGaN materials, the activation energy of Mg can be as high as 510–600 meV. Therefore, the activation efficiency of Mg is very low, causing low hole concentration of p-type AlGaN (far below n type AlGaN) and low conductivity. Research on p-doped of AlGaN has been studied, such as the common Mg doping, Mg-δ doping, superlattice doping, codoping, and polarization-induced doping.

Jeon et al. [93] studied the influence of Mg concentration on the resistivity of 0.5-μm-thick $Al_xGa_{1-x}N$. In 2003, Nakarmi et al. [94] reported Mg-δ doping. Compared with the homogeneous p-doped AlGaN material, the Mg-δ doping leads to an increase in hole concentration. The horizontal and vertical conductivities are increased by two times and five times, respectively. In 2009, Simon et al. [95] proposed a new type of p-doping method, polarization-induced doping. They grew the Mg-doping AlGaN monolayer on the nitrogen surface GaN, and the Al component was graded from 0 linearly to 0.3. The hole concentration is up to 1×10^{18} cm^{-3}.

7.2.4 Quantum Efficiency Study of UV LED Structure

The metal polarity of AlGaN material has a strong spontaneous polar effect. Its spontaneous polarization is [000-1]. The spontaneous polarization increases with the increase of Al component. Thus, a strongly polarized electric field is generated along the c axis of the heterojunction interface or AlGaN MQWs region, leading to band bending and the spatial separation of the electron and hole wave functions (quantum-confined Stark effect, QCSE). The QCSE leads to an increase in carrier lifetime, a decrease in radiative recombination efficiency, and red shift of luminous wavelength. The electric field induced by spontaneous polarization and piezoelectric polarization is as high as MV/cm, which reduces the internal quantum efficiency of UV LEDs.

Marcinkevicius et al. [96] studied the internal polarization field of $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ MQW with different components. The x value is 0.05–0.35, and the y value is 0.23–0.50. The result shows that, for low Al components, the measured polarization field values agree well with those calculated by the first principles; when the Al component is higher, the experimental values are contrary to the theoretical predictions. With the increase of applied bias, the electric field strength of the quantum well is decreased.

Fujioka [97] and Sumiya [98] et al. inserted a 1-nm AlN between AlGaN-MQWs and p-AlGaN electron barrier layers to suppress carrier overflow and the resulting parasitic luminescence and to block the spread of Mg to MQWs. Hirayama et al. [99] increased the effective barrier height by using multi-quantum barrier electron barriers to suppress the electronic leakage. As a result, current injection efficiency and external quantum efficiency were increased. The external quantum efficiency of 250 nm DUV LED was increased by 2.7 times. In order to improve the hole injection efficiency of UV LEDs, a gradual structure of p-AlGaN component was adopted in our research group [100], showing that the quantum efficiency of 297–299 nm UV LEDs was increased by 50%. A $AlN/Al_{0.7}Ga_{0.3}N$ electron barrier heterojunction was used in the 234–263 nm UVC LEDs by Mehnke et al. [101]. By optimizing the thickness of the AlN layer, the parasitic light was suppressed effectively, and the luminous efficiency of QW is improved.

7.3 Homoepitaxy of DUV LEDs on AlN Substrate

Rapid progress has been made recently in the development of AlGaN-based DUV-LEDs. The highest external quantum efficiency (EQE) of DUV-LEDs is higher than 20% at an emission wavelength of 275 nm [102]. However, DUV LEDs continue to have much lower output power from single chips than the more widely used blue LEDs, which is caused by high dislocation density in the AlGaN-based active layers and the extremely low light extraction efficiency of these devices. Traditionally, AlGaN-based DUV LEDs are grown on sapphire, SiC, or Si substrates. The large lattice and thermal expansion coefficient mismatches between these substrates and the epitaxial layers cause large numbers of dislocations and poor device reliability. The density of threading dislocations in nitride films grown on foreign substrates is high, typically $>10^8$ cm^{-2} even when special growth techniques are employed. In order to overcome the dislocation problem, AlN substrates with significantly lower dislocation density ($<10^4$ cm^{-2}) have been developed as a promising candidate due to similar thermal expansion coefficients and relatively small lattice mismatches.

7.3.1 Homoepitaxy on AlN Substrates

An aluminum hydroxide layer with the thickness of 5–10 nm forms on the surface when the AlN substrate is exposed to moist air or water, which consists of aluminum oxide hydroxide (AlOOH) or a mixture of AlOOH and aluminum trihydroxide [$Al(OH)_3$] [103, 104]. Nikishin et al. demonstrated that the aluminum hydroxide layer can result in increased dislocation density in homoepilayers [105]. In addition, surface scratches are incompletely removed after mechanically polishing (MP), which also may lead to strained AlN and the increased surface roughness due to re-nucleation and grain coalescence on these surfaces [106]. Therefore, the surface treatments of AlN substrates prior to epitaxy are critical to achieve high-quality homoepitaxy. The surface treatment schemes, including both ex situ and in situ processes, are reported to achieve suitably terminated surfaces. Ex situ surface treatments involve the removal of surface contamination with solvents and acids. A process of chemo-mechanical polishing (CMP) can obtain scratch-free substrates with the reduction of roughness, which is typically subjected to polishing in the alkaline slurry of submicron sized abrasives following the MP procedure. Figure 7.11 shows 2×2 μm^2 AFM images of MP and CMP AlN substrate surfaces. MP substrates had numerous polishing scratches, while CMP substrates were featureless, and root-mean-square (RMS) roughness is found to be 0.5 nm and 0.1 nm, respectively. These results suggest that work damage introduced during mechanical polishing is reduced by chemo-mechanical polishing. Then, wet etching with sulfuric and phosphoric acid mixtures is conducted to reduce the amount of surface hydroxide. In situ surface treatments include AlN substrates nitridation by

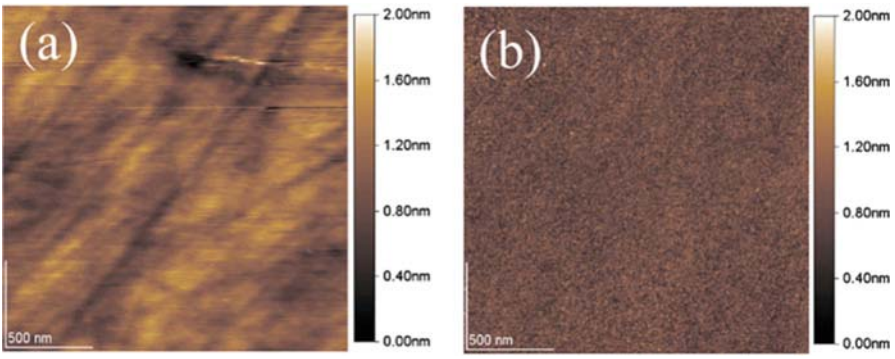

Fig. 7.11 $2 \times 2\ \mu m^2$ AFM images of (**a**) MP and (**b**) CMP AlN substrate surfaces [106]

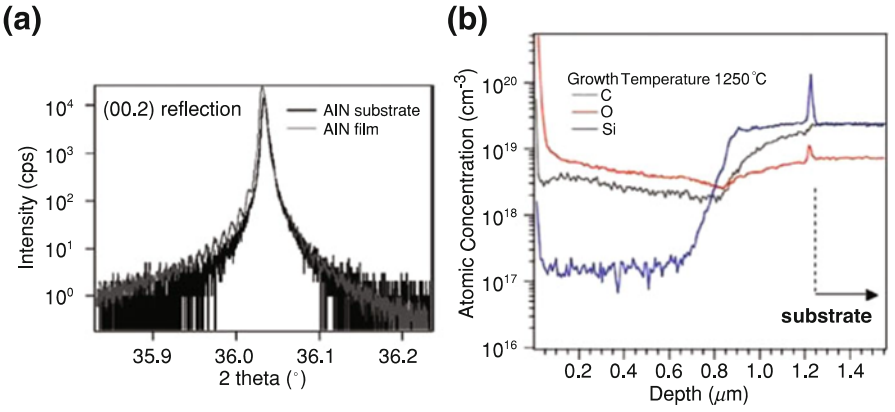

Fig. 7.12 HRXRD triple axis 2θ-ω scans of AlN substrates after CMP and after deposition of AlN homoepitaxial films grown at 1250 °C. (**b**) Calibrated SIMS depth profiles for C, O, and Si impurities in homoepitaxial AlN films grown at 1250 °C [107]

exposure to ammonia at high temperature. Generally, ammonia annealing at 1250 °C may convert the substrate hydroxide layer to AlN.

Once the AlN substrates surface is suitably prepared, high-quality homoepitaxial AlN may be achieved. Figure 7.12a shows HRXRD triple axis 2θ-ω scans of AlN substrates after CMP and after deposition of AlN homoepitaxial films grown at 1250 °C [107]. The lack of any peak shifts or shoulders in the films scan indicated that the film is epitaxial and strain-free. Kim et al. demonstrate modulated precursor flow epitaxial growth (MPEG) is an effective method to achieve high-quality homoepitaxial AlN with narrow X-ray rocking curve peak linewidths of 36 and 61 arcsec for the (002) and (102) diffraction conditions, respectively [108]. Note that homoepitaxial AlN films have low concentrations of background impurities, as shown in Fig. 7.12b.

7.3.2 Pseudomorphic AlGaN on AlN Substrates

Furthermore, the studies of strain relaxation in AlGaN alloys grown on AlN substrate are necessary to guide device design and ensure the low defect density is preserved in heterostructure active layers. Due to a low density of preexisting dislocations in the AlN substrate, the compressive strain during AlGaN heteroepitaxy cannot be relieved effectively. The built-up of strain energy eventually induces either an elastic surface roughening or plastic deformation via generation and inclination of dislocations, depending on the stressor interlayers and growth parameters used. Pseudomorphic AlGaN can be achieved by introducing graded alloy layer to the desired composition or properly superlattices (SLs) [109, 110].

The pseudomorphic growth has many advantages. At first, there are no misfit dislocations and new threading dislocations in the pseudomorphic AlN layer. For the pseudomorphic sample, the (0002) rocking curve width increases from 64 s for the AlN to 81 s for the $Al_xGa_{1-x}N$ layer, while the (10–12) rocking curve width increases from 89 to 104 s. This is in sharp contrast to the relaxed sample in which the (0002) rocking curve width increases from 49 s for the AlN to 239 s for the $Al_xGa_{1-x}N$ layer, while for the (10–12), rocking curve width increases from 30 to 302 s [109]. Secondly, it is possible to grow thick layers with a threading dislocation density (TDD) comparable to the starting substrate. The critical thickness for an n-type AlGaN contact layer with $x = 0.6$ on AlN is only about 40 nm as predicted by the Matthews and Blakeslee model [111]. This thickness is much less than the practical contact layer in an LED structure. Beyond this thickness, it is expected that misfit dislocations will form and lead to threading dislocations throughout the AlGaN layer based on energy equilibrium. However, layers of ~60% Al can be grown fully pseudomorphic up to a thickness of 0.5 μm, while layers of 70% Al can be grown nearly pseudomorphic up to a thickness of 1 μm, as shown in Fig. 7.13a. Thirdly, pseudomorphic AlGaN films exhibit smooth surfaces. It is found that layers begin relaxing by a surface roughening mechanism. Initially the surface appears to buckle to reduce the compressive strain in the layers. Upon continued growth, very rough surfaces were obtained for the $Al_xGa_{1-x}N$ layers with 60% Al at 0.5 mm thick. This is similar to what was seen previously in the growth of lower composition $Al_xGa_{1-x}N$ on low dislocation density bulk AlN substrates in which plateaus develop on the surface [110]. However the pseudomorphic $Al_xGa_{1-x}N$ layers with 70% Al can be grown with very smooth surfaces as seen in Fig. 7.13b. This step-flow growth pattern with atomically smooth surfaces is typical, and the RMS roughness is 0.1 nm in $2 \times 2\ \mu m^2$ scan range.

Si-doping of pseudomorphic AlGaN films grown on AlN substrates is necessary to achieve DUV LEDs. Electrical resistivity below 0.1 Ω·cm with Al content below 85% is demonstrated [91]. The electrical resistivity of AlGaN films increases with the Al mole fraction, which results from the reduction of n-type carrier concentration due to the increased donor activation energy or compensating point defects. On the one hand, a significant increase in the activation energy is demonstrated for

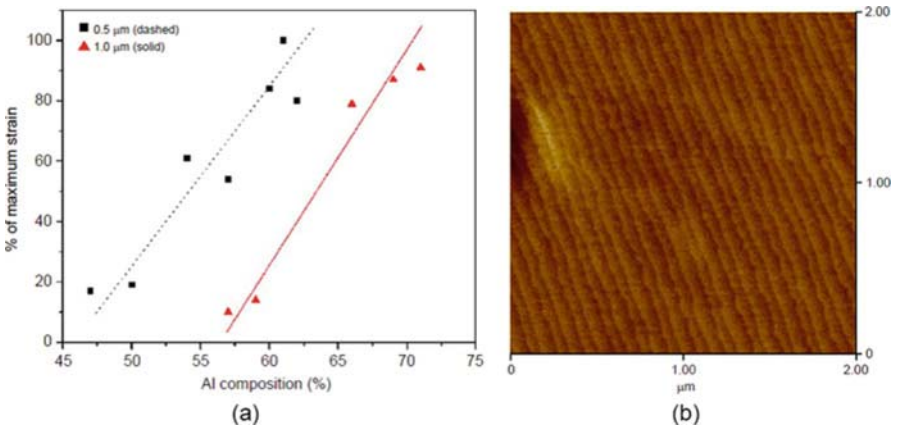

Fig. 7.13 (**a**) Percent of maximum (pseudomorphic) strain versus Al composition for different thickness layers (dashed line is 0.5 μm and solid line is 1.0 μm); (**b**) 2 × 2 μm^2 AFM scans showing the step-flow growth of the pseudomorphic n-type $Al_xGa_{1-x}N$ layer with a composition of 70% Al [109]

films with Al content greater than 80%. On the other hand, electrical compensation is another factor identified as causing a reduction in the carrier concentration.

7.3.3 Pseudomorphic DUV LEDs on AlN Substrates

The next step in obtaining a full LED structure is the growth of the multi-quantum wells (MQWs). The step-flow growth mode and atomically smooth surface continue during growth of the MQWs. Finally, pseudomorphic DUV LEDs on AlN substrates are fabricated, typically consisting of an Al-rich electron blocking layer, a p-type $Al_xGa_{1-x}N$ hole injection layer, and a p-type GaN contact following the MQWs growth. Figure 7.14 shows cross-sectional transmission electron microscopy (TEM) image in the active region and corresponding schematic of the device structure. No dislocations are generated in the whole LED structure except for p-GaN layer [112]. The dislocation density in the MQWs estimated is less than 10^6 cm^{-2}. In contrast, misfit and threading dislocations are observed at the interface between the p-GaN and p-AlGaN, which propagates through the p-GaN layer due to the large lattice mismatch (∼2%).

Pseudomorphic DUV LEDs on AlN substrates exhibit noticeable improvement over those on sapphire in device efficiency due to the reduction of dislocation defects in the active region. An output power of over 60 mW has been demonstrated for pseudomorphic LEDs emitting at a peak wavelength of about 270 nm [33]. Especially, Bryan et al. report a record high IQE of ∼80% by using $Al_{0.55}Ga_{0.45}N/Al_{0.85}Ga_{0.15}N$ MQW structures emitting at ∼258 nm [113]. Another

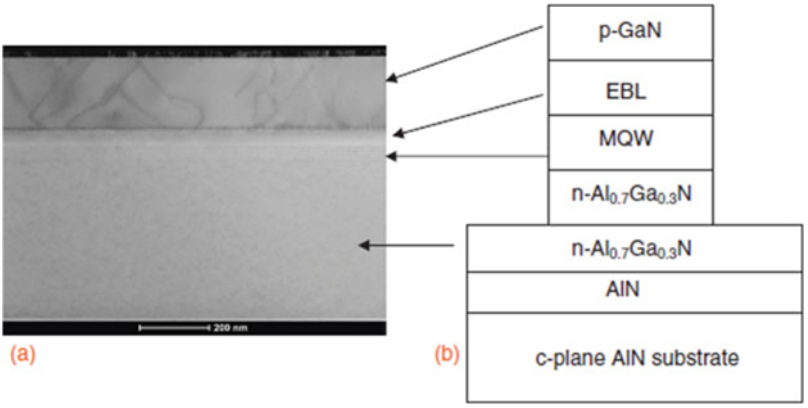

Fig. 7.14 (**a**) Cross-sectional TEM image showing low dislocation density in the active region and (**b**) corresponding schematic of the device structure [112]

important feature of the pseudomorphic DUV LEDs is the improved reliability and lifetime due to the high-quality pseudomorphic growth and high thermal conductivity of the AlN substrate. Along with advanced chip package technology, L50 lifetimes of LEDs are well in excess of 1000 h [114].

7.3.4 Light Extraction Efficiency for Pseudomorphic DUV LEDs on AlN Substrates

The pseudomorphic DUV LEDs are successful in reducing the dislocation density of devices. However, these devices are still challenged by the extremely low light extraction efficiency, which is mainly caused by total internal reflection and the absorption resulting from p-GaN contact layer and AlN substrates. While p-GaN layer strongly absorbs DUV light, a p-GaN contact layer is required to provide a good ohmic contact and to reduce the series resistance for reliable high-power LED operation. Therefore, flip-chip designs are generally used for DUV LEDs, and the light emission is thus extracted through the AlN substrate. The AlN substrate is generally prepared by physical vapor transport (PVT) with significant decrease of optical transparency at photon energies below the band gap, which is thought to be caused by the presence of Al vacancies, substitution impurities, and their complexes. Typically, PVT-AlN substrates with an absorption coefficient of 35 cm^{-1} may absorb approximately 50% of the light. Kinoshita et al. demonstrate that thick AlN grown by hydride vapor phase epitaxy (HVPE) on PVT-AlN substrates have both low dislocation density and high DUV optical transparency [115]. Figure 7.15 shows that external optical transmission spectra of PVT- and HVPE-AlN substrates measured at room temperature in air. The external optical

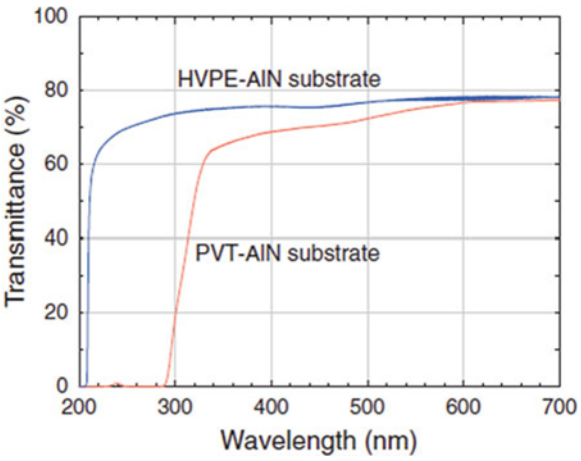

Fig. 7.15 External optical transmission spectra of PVT-AlN and HVPE-AlN substrates measured at room temperature at air [115]

transmittance of HVPE-AlN substrates in the deep-UV range of 220–300 nm was above 63%. DUV-LEDs fabricated on these substrates exhibit a single emission peak at 268 nm with the output power (LOP) and EQE of 28 mW and 2.4%, respectively [116]. Note that thinning AlN substrate may relieve the absorption of AlN substrate. For typical values of absorption coefficients in the AlN substrate (35 cm^{-1}), this reduces the light absorption in the substrate by an order of magnitude from the starting thickness of 425–200 μm [33].

Total internal reflection between AlN substrate and the ambient medium also results in low light extraction efficiency for the pseudomorphic DUV LEDs. The light extraction efficiency from a flat bottom side surface of the transparent AlN substrate of a DUV-LED at 265 nm is estimated to be <4% by three-dimensional (3D) finite difference time-domain (FDTD) calculations. Therefore, it is important to find ways to enlarge the light escape from AlN substrate surface. Many approaches, such as surface roughening and photonic crystal, have been proposed to increase the photon extraction efficiency. Shin-ichiro Inoue et al. reported the highest output power to date for DUV-LEDs with emission wavelengths shorter than 280 nm during CW operation by roughed AlN surfaces. Output power of more than 150 mW is observed at an injection current of 850 mA at a peak emission wavelength of 265 nm [117]. Figure 7.16 shows the schematic of DUV-LEDs on transparent AlN substrates with nanophotonic light extraction structures. The AlN bottom side surface configuration, which is composed of a hybrid structure of photonic crystals and sub-wavelength nanostructures, has been designed using FDTD calculations to enhance light extraction [118]. The LED with the nanophotonic light extraction structure shows considerably wider and stronger light emission in its both near-field and far-field patterns, very low efficiency droop, and an approximately 20-fold increase in the output power over that of a conventional flat surface LED.

With the large-size and high-quality AlN substrates available, the high-power and high-efficiency pseudomorphic DUV LEDs on these substrates will be achieved and thus allow replacement of traditional high-power mercury lamps.

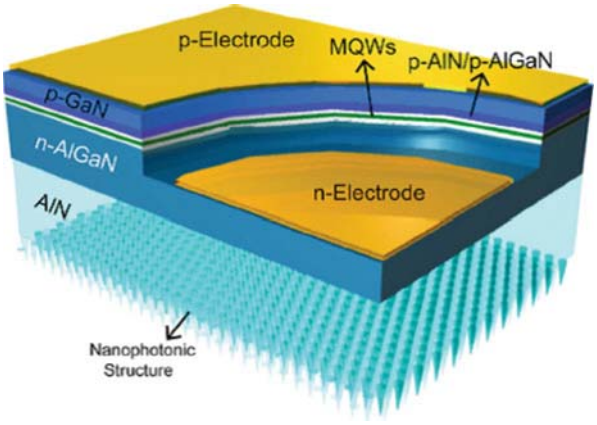

Fig. 7.16 Schematic of DUV-LEDs on transparent AlN substrates with nanophotonic light extraction structures [118]

7.4 Light Exaction Issues of DUV LEDs

Another challenge in obtaining highly efficient AlGaN-based DUV LEDs is the poor light extraction efficiency (LEE). DUV LEDs usually adopt flip-chip configuration for the light-absorbing p-GaN layer on the top of the LED structure. Serious total internal reflection (TIR) occurs at the semiconductor layer/substrate interface and the sapphire substrate/ambient interface due to the large refractive index difference (n_{AlN}~2.3, n_{sapphire}~1.8, $n_{\mathrm{air}} = 1$). According to the Snell's law, the critical angle of TIR on the interface of sapphire substrate to air is only about 33° at a wavelength of 275 nm. Furthermore, the intrinsic anisotropic optical polarization properties of Al-rich AlGaN materials also affect the LEE significantly [119]. Light can be emitted from c-plane AlGaN-MQWs as either transverse electric (TE) mode with electrical field vector **E** perpendicular to **c**-axis or transverse magnetic (TM) mode with **E** parallel to **c**-axis. And the TM mode light comes to predominate over the TE mode light when the emission wavelength gets shorter than 300 nm [120]. The TE mode light mainly propagates in the vertical direction, while the TM mode mainly transmits in the horizontal direction, which is difficult to extract due to large incident angle on the surface. Ryu et al.'s simulation showed that the TM mode LEE is much lower than the TE mode LEE, which is partly responsible for the decrease of LEE in DUV LEDs with shorter wavelength [121].

7.4.1 Al-Rich-Induced Optical Polarization Effect in DUV LEDs

As shown in Fig. 7.17, the wurtzite GaN or AlN alloy has three valence subbands, including the heavy hole (HH) band, the light hole (LH) band, and the crystal field split-off hole (CH) band. The topmost valence subband depends on the crystal

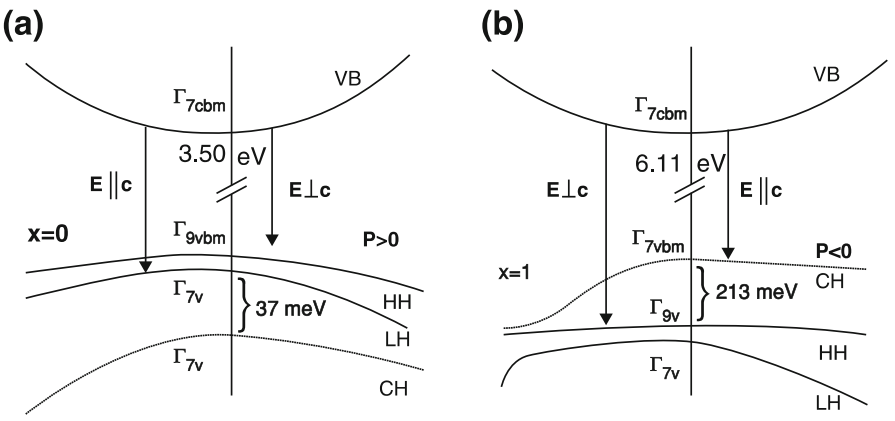

Fig. 7.17 The band structure near the Γ point of (**a**) GaN and (**b**) AlN. E is the electric field vector of the emission light and P is the degree of polarization [123]

field split-off energy (Δ_{CF}). GaN has a positive Δ_{CF} of 38 meV [122], making the HH band as the topmost subband. In contrast, AlN has a large negative Δ_{CF} of −219 meV, leading to the CH band as the topmost subband. Therefore, light emission due to the recombination between the conduction band and the topmost hole subband near the Γ point is mainly polarized with **E** perpendicular to c-axis (TE polarization) in GaN and with **E** parallel to **c**-axis (TM polarization) in AlN.

The $Al_xGa_{1-x}N$ alloy has an intermediate property, depending on the Al composition x. Nam et al. reported at $x = 0.25$, the three valence subbands near the Γ point become degenerated, and the degree of polarization is zero [123]. Thus $Al_xGa_{1-x}N$ generates predominant TM-polarized light when $x > 0.25$.

For the AlGaN multiple quantum well (MQW) DUV LEDs, the switch occurs at higher x due to other parameters, such as the strain in the QWs [124–126], the QW thickness [127–129], and the temperature and carrier density [127, 130, 131] within the QWs. Kolbe et al. [120] showed that the intensity of the TE-polarized light relative to the TM-polarized light decreases with decreasing emission wavelength from the AlGaN active layers. The degree of polarization is ~0 for LEDs with a wavelength of around 300 nm. They also found that the TM-polarized light becomes more dominant relative to the TE-polarized light for AlGaN MQWs with decreasing tensile in-plane strain [132]. Banal et al. [129] reported polarization switching up to x~0.80 in AlGaN/AlN (1.5 nm/13.5 nm) MQWs on sapphire substrates due to the in-plane compressive strain and the quantum confinement due to narrow quantum wells at 8.5 K. Bryan et al. [126] reported the polarization of the emitted light transitioned from TE mode to TM mode at 245 nm in pseudomorphically strained AlGaN grown on AlN template. Reich et al. [133] demonstrated strongly TE-polarized light emission as short as 239 nm from AlGaN MQW DUV LEDs on pseudomorphically strained epitaxial lateral overgrowth AlN/sapphire based on k·p perturbation theory.

The polarization property of the emitted light from the AlGaN MQWs influences the light extraction efficiency of DUV LEDs significantly. Since the TM-polarized light mainly propagates along the c-plane, it suffers more serious TIR issue at the back surface of the sapphire substrate and lower light extraction efficiency than the TE-polarized light. Therefore, to obtain high-efficiency DUV LEDs, it's necessary to either enhance the intensity of the TE-polarized light relative to the TM-polarized light emitted at a certain wavelength using narrow compressive QWs or to develop new strategies to efficiently extract TM-polarized light.

7.4.2 Surface Patterning and High Reflective Techniques for DUV LEDs

7.4.2.1 Surface Patterning

Surface pattering is one promising approach to reduce the internal reflections of light. Khizar et al. [134] reported a 55% enhancement of the light output power in 280-nm AlGaN based DUV LEDs with an integrated microlens array on the sapphire substrate. Pernot et al. [135] reported the average light output power of 270-nm DUV LED with moth-eyes structure on the sapphire substrate is improved by a factor of 1.5. Inoue et al. [117] showed high-power 265-nm DUV LEDs with large-area nanophotonic light extraction structure on the HVPE-AlN substrate, exhibiting a ∼20-fold increase in the output power compared with a flat surface DUV LED. Dong et al. [83] reported higher internal quantum efficiency and also higher light extraction efficiency 282-nm AlGaN-based DUV LEDs on nano-patterned sapphire substrate (NPSS). The light scattering at the AlN/NPSS interface and AlN/air voids interface can decrease the internal reflection and thus increase the photon's escape opportunity from the LED structure [136].

Since the TM-polarized light mainly propagates within the c-plane and is extracted from the device sidewalls, disrupting the internal reflection on the substrate sidewalls would be beneficial to improve the extraction efficiency of TE-polarized light. Substrate sidewall roughening can be implemented by ultra-short pulse laser machining during the chip separation process and has been proven to be advantageous for enhanced light extraction efficiency in visible or UV LEDs [137–139]. Lee et al. [139] reported the roughened sidewalls of thick sapphire substrate using stealth laser dicing can promote the extraction probability of photons outside the DUV LED chip in the lateral directions.

We investigated the influence of the roughening position at the sapphire substrate sidewall on the light extraction of AlGaN-based 275-nm UV LEDs and found that effective regions for roughening exist on the substrate sidewalls for light extraction enhancement. Roughening outside the effective roughening region will decrease the sidewall light extraction efficiency due to the undesirable inward photon scattering at the substrate sidewall.

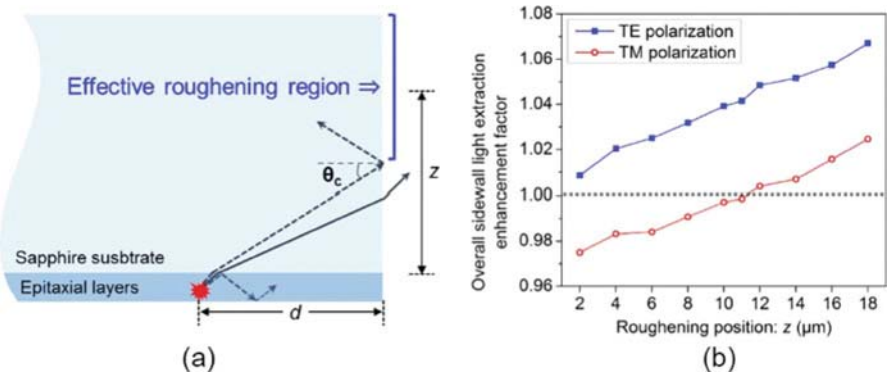

Fig. 7.18 (**a**) Schematic of the effective roughening region on the reference substrate sidewall; (**b**) the dependence of overall sidewall light extraction enhancement factor on the roughening position z simulated by the finite-difference time-domain (FDTD) method [140]

As shown in Fig. 7.18, for a TE- or TM-polarized dipole in LED's active layer, the effective roughening region is from $d \times \tan(\theta_c)$ away from the epitaxial layers to the substrate backside surface, where d is the distance from the dipole to the roughened sidewall and θ_c is the critical angle. Considering multiple TM-polarized dipoles in a real deep-UV LED, the effective roughening region is found equal to that of the point dipole in the central portion of the active layer. Therefore, in one LED with a side length of *L*, the effective roughening region of TM polarization is deduced to be the area from the sapphire substrate's backside to $L/2 \times \tan(\theta_c)$. On the other hand, the overall sidewall light extraction enhancement factor of TE polarization remains higher than one wherever the roughening position is, revealing that the whole sapphire substrate's sidewall is suitable for roughening for TE-polarized light extraction in DUV LEDs. The experimental results show that compared to the counterpart with two roughening layers, the TM polarization-dominant DUV LED with three roughening layers has 13.2% higher average light output power (LOP) at 20 mA thanks to the larger roughening area in the effective roughening region. However, when further applied additional roughening layers beyond the effective roughening region, the LOP decreases, which is inconsistent with the simulation.

Modifying the geometry of the LED chip can also help outcouple the light trapping in the structure. Krames et al. [141] reported 40% EQE enhancement of truncated-inverted-pyramid AlGaInP-based LEDs sawn by a beveled blade. Lee et al. [142] reported 55% light output enhancement in flip-chip GaN-based LEDs with oblique sapphire substrate sidewalls using a wet etching technique. Laser micromachining has been developed to shape the sapphire substrate, such as nanosecond (ns) laser dicing either with a laser-beam turning mirror [143] or with an oblique sample stage [144] to fabricate oblique substrate sidewalls, and shifted picosecond (ps) laser stealth dicing to form wavy substrate sidewalls [145]. We report a convenient ps laser multiple scribing method to shape the

sapphire substrates of AlGaN-based flip-chip 276-nm LEDs into an oblique sidewall geometry for enhanced LEE [146]. The applied multiple scribing lines in the sapphire substrate are intentionally aligned to guide the wafer diced along oblique sidewalls with designed angles. Compared to a convention LED chip with vertical sidewalls, the LED with two opposite sidewalls partially shaped with 60° inclination shows 13.8% higher LOP at 50 mA. The FDTD simulation results also reveal that the oblique substrate sidewall geometry is effective for TM-polarized light extraction.

7.4.2.2 High Reflective Techniques

By introducing reflective structures in the DUV LEDs, part of the emitted light can be reflected back and the probability of light escaping through the substrate is improved. A transparent p-type contact layer, such as p-AlGaN layer [67, 147] or AlGaN/AlGaN short-period superlattice [148], and a high reflectivity p-metallization stack in the DUV spectrum can reduce the light absorption loss and improve the LEE. Shatalov et al. [67] reported a twofold increase of output power from the LED chip. Maeda and Hirayama [147] reported the external quantum efficiency of 287-nm DUV LED increasing from 2% to 5.5% by suing transparent p-AlGaN contact layer and highly reflective Ni(1 nm)/Al layers as the p-type electrode.

On the other hand, reflective structure at the slant mesa sidewalls can efficiently deflect the photons guided laterally along the c-plane and into the vertical direction and thus enhance the LEE. Lee et al. reported sidewall-emission-enhanced DUV LED with active mesa stripes [149] or arrays of truncated cone-shaped active mesas [150] to effectively extract TM-polarized photons down through the sapphire substrate. We reported a sidewall reflection method consisting of microarray mesas with a hexagonal shape and on-chip high reflective metal pads for DUV light [151]. The LOP of 278-nm LEDs was improved by 30.1% compared with that of LEDs without high reflective metal pads. The LOP can be further increased when reducing the side length of the hexagonal mesa thanks to the larger sidewall area for DUV reflection. Wierer et al. [119] demonstrated the enhancement is greater when there is a larger faction of in-plane light.

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