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Multi-Step Resistance Memory Behavior in $Ge_2Sb_2Te_5$/GeTe Stacked Chalcogenide Films

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The multi-step resistance behavior was observed in the $Ge_2Sb_2Te_5$/GeTe bistratal stacked films investigated by utilizing in situ temperature-dependent film resistance measurements. The [$Ge_2Sb_2Te_5$ (30 nm)/GeTe (70 nm)] stacked films had a larger resistance difference among different resistance states. The data retention temperatures for 10 years of amorphous and intermediate states of [$Ge_2Sb_2Te_5$ (30 nm)/GeTe (70 nm)] films were estimated to be 126°C and 166°C, respectively. X-Ray Diffractomer revealed the changes of phase structure in $Ge_2Sb_2Te_5$/GeTe bistratal stacked films with different annealing temperature. Theoretical simulation of the temperature distribution of the PCM cell with bistratal films was used to examine the multi-step switching mechanism.

Keywords Stacked films; multi-step resistance memory; data retention; phase-change random access memory; theoretical simulation

1. Introduction

In recent years, phase change memory (PCM) has widely recognized as a leading contender among emerging non-volatile memory technologies due to its advantages of fast operation speed, high capacity, good reliability, low power consumption, and so on [1–3]. Data storage is realized by electrical pulse induced reversible phase transition between high resistivity state (amorphous state) and low resistivity state (crystalline state). The dramatic difference of resistivity between the two states makes it possible to use phase change random access memory devices as practical high performance memory elements.

To achieve higher storage density, considerable efforts have been made in optimizing the properties of phase-change materials and reducing the recording cell size [4–6]. Large-scale, long-range-ordered phase-change material nanoparticle arrays were fabricated and the density of the arrays could reach as high as 10^9 cm^{-2} [7–9]. Based on the N-doped $Ge_2Sb_2Te_5$(GST) phase change storage material, a two-bipolar-two-PCRs (2B2R) cell

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structure was devised to reduce the cell size and achieved high density [10]. Besides, a lot of other measures including doping, optimizing the heat electrode shape et al had been used to obtain PCM with high storage capability [11, 12].

However, miniaturizing the cell size to some extent will greatly increase the crosstalk between adjacent cells, resulting in unavoidable reading errors[10]. Another effective method to increase the storage density is multi-level phase change memory by stacking several different phase-change materials [13]. In multilevel PCRAM scheme, one phase change resistor (PCR) can be programmed into intermediate resistance value between the highest and the lowest values, thus can store more than one bit data in a cell. Gyanathan et al. [14] investigated multi-level phase change random access memory (PCRAM) devices comprising two GST layers sandwiching a thermal insulating Ta_2O_5 barrier layer. The stability and reproducibility of the multi-level states were improved greatly, which made it suitable for high density storage.

In this work, the stacked chalcogenide films with GST and GeTe were prepared to realize multi-step resistance storage. The amorphous-to-crystalline transition of the stacked films with various thickness ratios of GST to GeTe was investigated by utilizing in situ temperature-dependent film resistance measurements. The data retention temperatures for 10 years of the amorphous and intermediate states were estimated. X-Ray Diffractomers were applied to confirm the processes of phase change. Thermal analysis was performed to investigate the reasons for the multi-step resistance storage of the bistratal films.

2. Experiments

GST/GeTe bistratal stacked films with various layer thicknesses ratios were deposited on 0.5 mm thick oxidized Si (100) wafers using a radio-frequency (RF) magnetron sputtering system at room temperature. The total thickness of the stacked films was set to about 100 nm. The stacked films were obtained by rotating the substrate holder and letting samples face GST (2 in., 99.999% purity) and GeTe (2 in., 99.999% purity) alloy targets, respectively. The thickness of each individual layer was controlled by the deposition time. Various layer thicknesses ratios were obtained in order to optimize the electric property. All deposition processes were carried out in an argon atmosphere at pressure of 0.2 Pa, with a flow of 30 SCCM (SCCM denotes standard cubic centimeter per minute at standard temperature and pressure), and an RF power of 20 W for both targets. The substrate was rotated at an autorotation speed of 20 rpm to increase the deposition uniformity. Prior to the growth of the bistratal films, GST and GeTe deposition rates were estimated by depositing a single layer of the corresponding alloy targets and measuring their thicknesses with a DEKTAK surface Profiler.

In situ temperature-dependent sheet resistance (R-T) measurements of the specimen were performed in Ar atmosphere using a custom-made two-point-probe setup. Thermal stability of amorphous films was evaluated by isothermal time-dependent resistance measurements. The crystalline structures of the films were analyzed by X-ray diffraction (XRD, Rigaku D/MAX 2550 V) with Cu K_α radiation in the 2θ range from 20° to 60°, with a scanning step of 0.01°.

3. Results and Discussion

Figure 1 shows the sheet resistance as a function of annealing temperature for GST/GeTe bistratal stacked films and monolayer films at a constant heating rate of 10°C/min. The

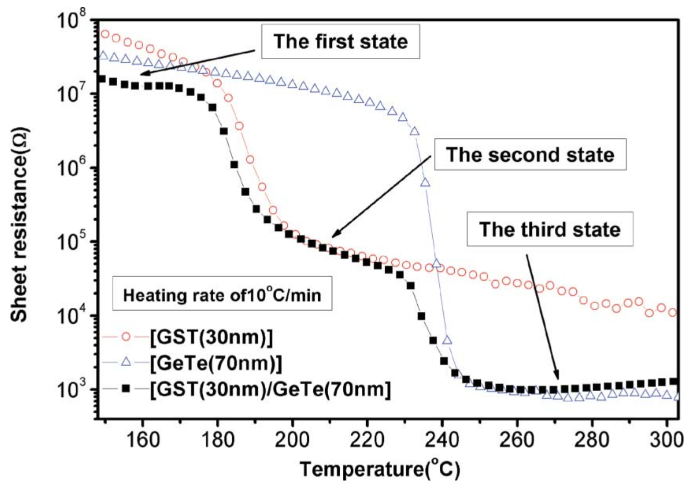

Figure 1. The change in sheet resistance as a function of temperature for GST/GeTe films and monolayer films at a constant rate of 10°C/min. (Figure available in color online)

thicknesses of GST and GeTe films are 30 nm and 70 nm, respectively. It can be observed that for monolayer films of GST and GeTe, there are only two resistance steps in the *R–T* curves from 150°C to 300°C, which indicates the two-state storage capability of monolayer films. However, for GST/GeTe bistratal film, there are three steps with three relatively stable resistance values in the *R-T* curve. The temperature at which the sheet resistance starts to decline rapidly is defined as crystallization temperature T_c. The T_c of the first and second crystallization is measured to be 180°C and 230°C, respectively. When the temperature is lower than 180°C, the sheet resistance keeps in the original value ($\sim 10^7$ Ω). With increasing of measuring temperature from 180°C to 230°C, the sheet resistance rapidly decreases and keeps in the relatively stable intermediate resistance value ($\sim 10^5$ Ω). Further heating to more than 230°C, the sheet resistance drastically decreases once again to the lowest resistance value with about 10^3 Ω. In the practical applications, the highest resistance with 10^7 Ω can be stored as "0" state, the resistance values of 10^5 Ω and 10^3 Ω can be seen as "1" and "2" states, respectively. The resistance ratios between the adjacent states are 2 orders of magnitude, which is sufficient for PCM operation. In addition, the two crystallization temperatures T_c of 180°C and 230°C are in agree with that of the monolayer films of GST and GeTe, respectively, which indicates that the stacked film can maintain the character of monolayer film. Therefore, three resistance values can be realized as multi-step resistance storage in the stacked film structure.

The XRD patterns of GST (30 nm)/GeTe (70 nm) bistratal films annealed in Ar atmosphere for 10 min at different temperature were analyzed to confirm the multi-step phase change. As we can see from Fig. 2(a)–2(c), the diffraction peaks are not observed in the as-deposited GST/GeTe film, which demonstrates that it is in amorphous state. After annealing at 210°C, face-centered cubic (FCC) (200) and (220) peaks of GST film emerge, proving that GST has been crystallized at this temperature. More diffraction peaks corresponding to GST and GeTe are observed at 260°C, which gives obvious evidence that both GST and GeTe have been crystallized. Moreover, the intensity of diffraction peaks increases at 260°C compared with the one at 210°C, implying more crystalline phase. These results are in agreement with the analysis of previous resistance change in phase-change.

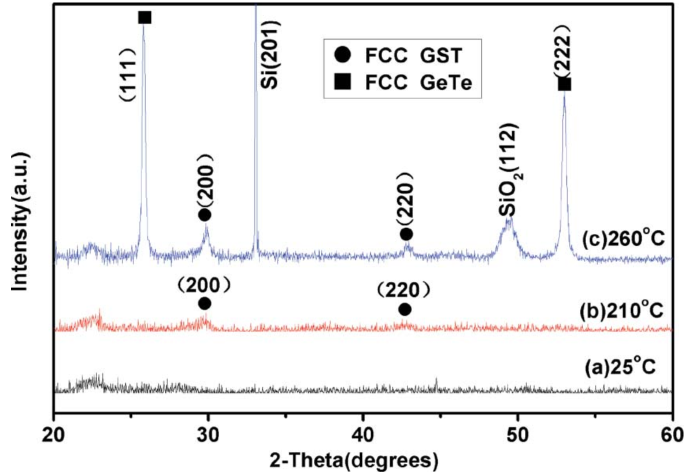

Figure 2. XRD patterns of $Ge_2Sb_2Te_5$ (30nm)/GeTe(70nm) film annealed at several temperatures.(a)25°C, (b)210°C, (c)260°C.

The film thickness influences intensively the crystallization temperatures T_c [15, 16]. The greater the jump from one resistance value to another, the better the performance of the device [14]. Hence, this relatively large difference in resistivities is essential in establishing good resistance windows between consecutive states. Take the above factors into account, GST/GeTe bistratal films with various thickness ratios were fabricated for optimization. In Fig. 3, we can see that the film thickness really has some influence on crystallization temperature and resistance gap. However, all GST/GeTe bistratal stacked films show multi-step phase change behavior. Thereinto, the GST (30 nm)/GeTe (70 nm) bistratal film has a relatively larger resistance difference between adjacent resistance states and a broader temperature range of the intermediate resistance state. Therefore, we regard

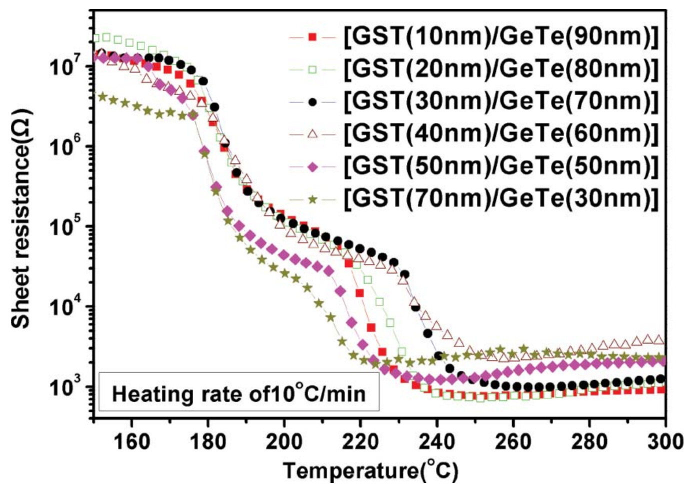

Figure 3. The change in sheet resistance as a function of temperature for GST/GeTe films with different thickness ratio at a constant rate of 10°C /min.

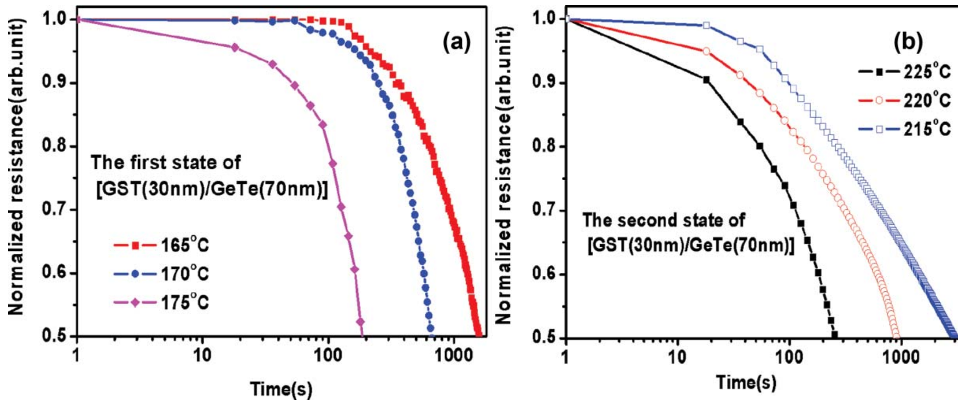

Figure 4. Normalized resistance of GST(30nm)/GeTe(70nm) bistratal films as a function of annealing time at various temperatures: (a) The first resistance state, (b) The second resistance state. (Figure available in color online)

the GST (30 nm)/GeTe (70 nm) bistratal films as more promising multi-step resistance memory materials, which is also an important reason why it is specifically selected to be investigated previous.

The data retention is an important index for a nonvolatile memory[17]. The data retention of the two states of GST (30 nm)/GeTe (70 nm) bistratal films and GST film was determined by evaluating the failure time upon annealing temperature. In this work, the failure time at a specific isothermal temperature is defined as the time when the decreasing resistance drops to 50% of its initial value. Normalized resistance as a function of annealing time at different temperature is shown in Fig. 4. The film resistance exhibits a sudden drop after an incubation time which strongly depends on annealing temperature.

The plot of logarithm failure time vs. 1/kT, shown in Fig. 4, fits a linear Arrhenius relationship due to its thermal activation nature[18]. In our case, the fitted straight line can be described as:

$$t = \tau_0 \exp(E_c/k_b \cdot T) \tag{1}$$

where k_{b}, τ_0, t and T are Boltzmann's constant, the pre-exponential factor depending on the material's properties, failure time and absolute temperature of concern, respectively.

According to the Arrhenius equation, basing on the failure time gotten from Fig. 4(a) and (b), extrapolated temperatures of all resistance states for 10-years data retention were included in Fig. 5. The first and second resistance states of GST (30 nm)/GeTe (70 nm) film have $T_{10\mathrm{Y}}$ values of 126°C and 166°C, respectively. As a comparison, the $T_{10\mathrm{Y}}$ reported for an undoped GST film is only 85°C. Consumer appliances and automotive systems require 10 year retention at temperatures higher than 125°C [19]. From this perspective, GST(30 nm)/GeTe(70 nm) bistratal stacked film possesses better reliability of the resistance state than GST film, resulting in much more promising use for high density PCRAM applications.

Figure 6(a) schematically shows cross-section diagram of the cell structure, in which about 100 nm-thick PCLs with the diameter of 1.0 μm was prepared as storage medium. The temperature contour plots of the GST (30 nm)/GeTe (70 nm) bistratal structure during the set process were simulated as shown in Figs. 6(c) and 6(d). The successively applied

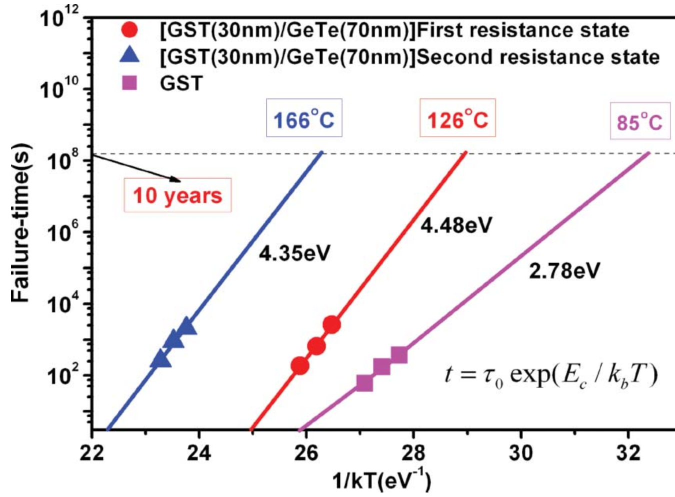

Figure 5. The relationship between logarithm failure time and reciprocal temperature of the GST(30nm)/GeTe(70nm) first resistance state, the GST(30nm)/GeTe(70nm) second resistance state, and GST films.

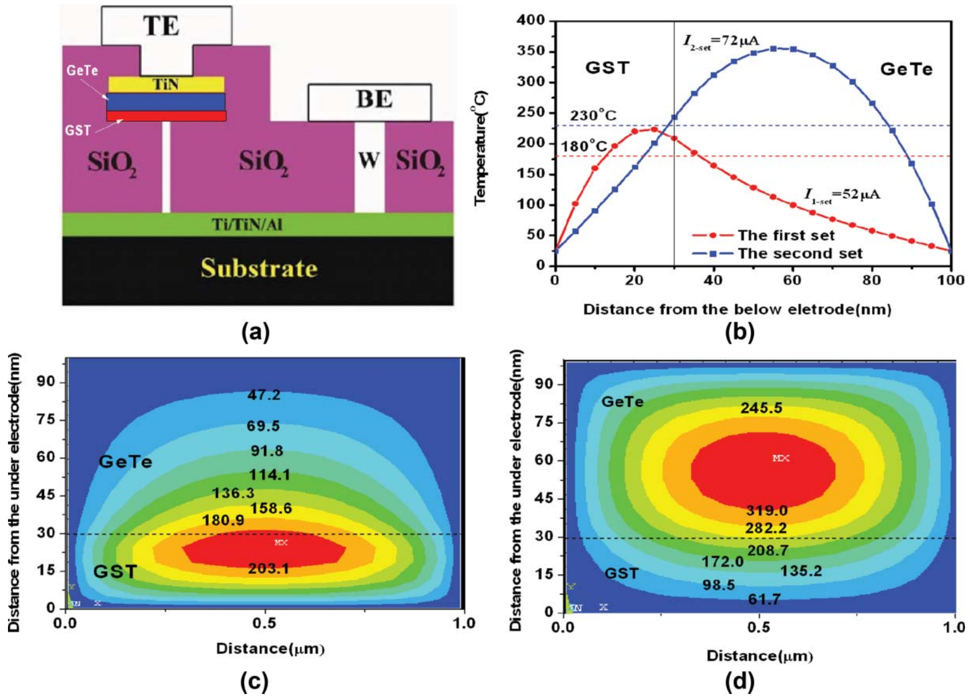

Figure 6. (a) Schematically diagram of the PCM cell structure. (b) The temperature profiles vs. the distance from the below electrode. (c) Temperature contour plot of a simulated device undergoing the first set process, and (d) the second set process.

currents of were 52 μA and 72 μA, respectively. From the comparisons between Figs. 6(c) and 6(d), we can see that the hottest region are in GST and GeTe layers in succession, which exactly contributes to the first and second set processes. The simulated temperature profiles vs. the distance from the below electrode were shown in Fig. 6(b) in detail. It can be seen from Fig. 6(b) that when the applied current is 52 μA, the temperature in GST layer is higher than 200°C which is enough to make the GST transform from amorphous to crystalline. Meanwhile, the highest temperature is 206°C in GeTe layer due to its lower resistivity, which can make the GeTe in stable amorphous state. When 72 μA current is applied, the highest temperature in GeTe layer almost reaches 358°C. Therefore, the GeTe is crystallized while the GST also keeps in crystallization state with its temperature lower than the melting point 620°C far away. Thus an intermediate resistance state is obtained between fully amorphous and fully crystalline states.

4. Conclusions

GST/GeTe bistratal stacked films were prepared by alternatively sputtering GST and GeTe targets. Multi-level phase change was observed by utilizing in situ temperature-dependent resistance measurements. Among bistratal films with various thickness ratio of $Ge_2Sb_2Te_5$ to GeTe, the resistance difference of adjacent states in GST (30 nm)/GeTe (70 nm) reached 2 orders of magnitude, which meant better distinguishing performance of the device. The XRD of GST (30 nm)/GeTe (70 nm) films confirmed their multi-level phase change. The temperatures for 10-years data retention of the first and second resistance states were 126°C and 166°C, respectively, meeting the consumer appliances and automotive systems requirement 125°C. Theoretical simulation of the temperature distribution in two set processes of the PCM cell showed a successive crystallization process that GST layer was crystallized firstly and then GeTe layer was transformed to crystallization state. This study manifested that GST (30 nm)/GeTe (70 nm) films possess good stability and data retention, which results that it can be a promising multi-step resistance memory material to increase the storage density.

Acknowledgments

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