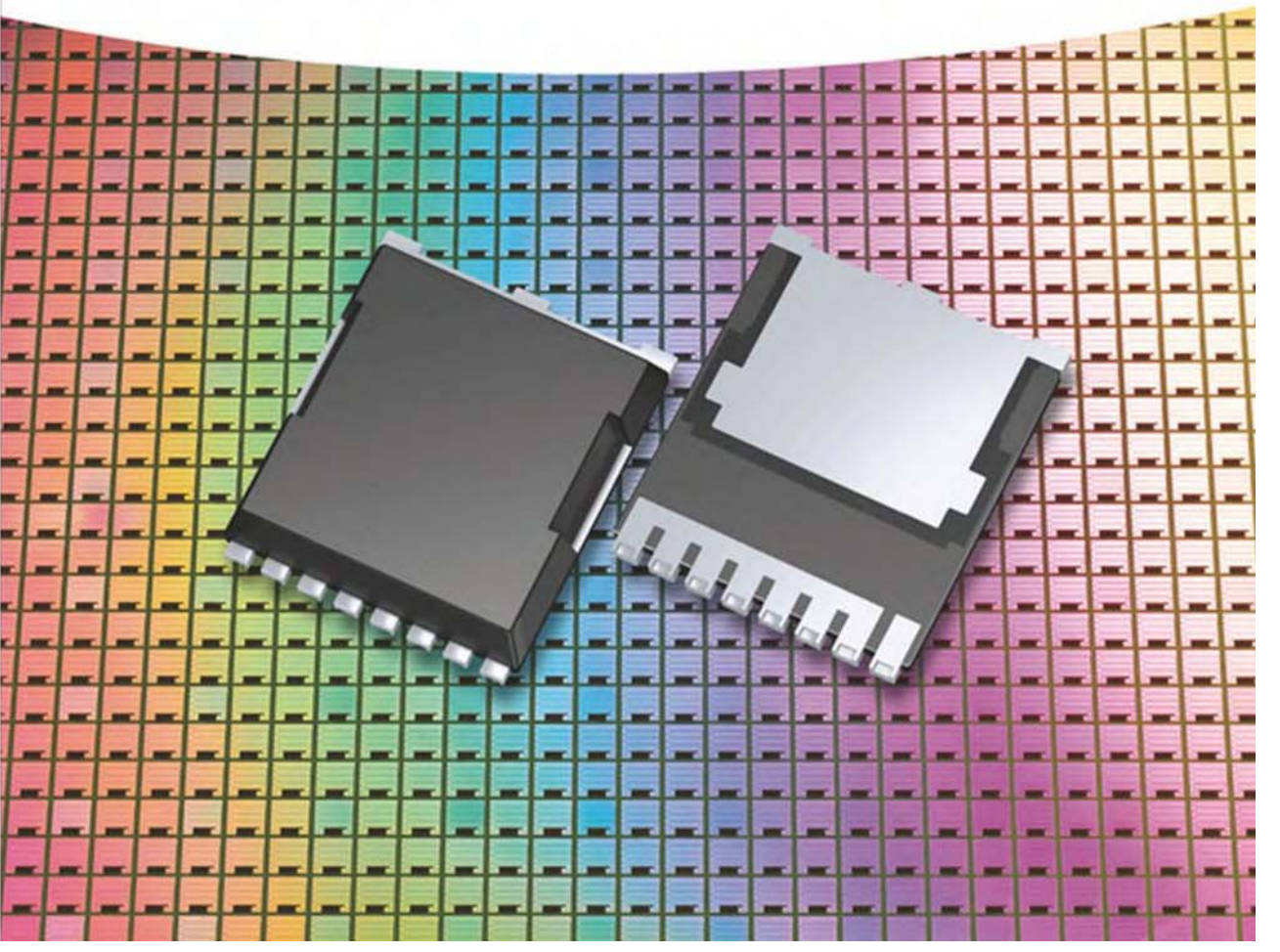
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Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp

Wide Bandgap Semiconductors for Power Electronics

Materials, Devices, Applications



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Volume 2

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Cover Design: Wiley
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Library of Congress Card No.:
applied for

British Library Cataloguing-in-Publication Data
A catalogue record for this book is available from the British Library.

Bibliographic information published by the Deutsche Nationalbibliothek
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available on the Internet at <http://dnb.d-nb.de>.

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Boschstr. 12, 69469 Weinheim,
Germany

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Print ISBN: 978-3-527-34671-4
ePDF ISBN: 978-3-527-82470-0
ePub ISBN: 978-3-527-82471-7
oBook ISBN: 978-3-527-82472-4

Typesetting Straive, Chennai, India
Printing and Binding

Printed on acid-free paper

10 9 8 7 6 5 4 3 2 1

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Preface

Introduction

The scope of this edited book is to provide a state of the art of the technology and application of SiC and related wide bandgap materials. The focus lies on the material SiC with 16 review articles from internationally well-known experts covering major aspects of fundamental physics, applied science, as well as industrial development and manufacturing. In addition, five experts are reporting on the technological status of further wide bandgap materials GaN, diamond, and Ga_2O_3, which have the potential to even outperform SiC with respect to certain physical properties relevant for power electronics.

The semiconductor Si has dominated the fabrication of electronic devices for switching of electrical currents or for the application in microelectronics almost since the beginning of semiconductor technology in the early 1950s. For the application in power electronic devices, however, two major material properties limit the performance of Si: the medium breakdown field limits the achievable conductivity at a certain desired breakdown voltage as well as the medium heat conductivity hinders the release of excess power during device operation (e.g. overcurrent, short circuit, avalanche) and, hence, may cause thermal failure. From a physical point of view, wide bandgap materials like SiC, Diamond, GaN, AlN, and Ga_2O_3 exhibit a much higher breakdown field that outperform their medium bandgap counterparts like Si and GaAs by a factor of 10 and more (see Table 1). Due to their strong covalent chemical bonding, the wide bandgap semiconductors diamond and SiC show a significant higher heat conductivity than the standard semiconductor Si. Hence, SiC- and diamond-based power electronic devices can handle much higher power densities than Si devices would do.

A key parameter for the choice of the proper semiconductor in power electronics is the so-called on-resistance of a power semiconductor device (Figure 1). Related to this, the Baliga's figure of merit (BFOM) defined as $\varepsilon \mu E_C^3$ (ε = dielectric strength, μ = charge carrier mobility, E_C = breakdown field) provides a selection rule for the proper choice of a semiconductor material for power electronic transistors. In literature, BFOM values are often calculated from idealized material properties that do not reflect the conditions under real device operation. Nevertheless, the BFOM value allows to rate the ultimate potential of each semiconductor related

Table 1 Physical properties (room temperature values) of wide bandgap semiconductors for power electronic applications in comparison to classic semiconductor materials (data from [1–3]).

	4H-SiC	GaN	AlN	β-Ga_2O_3	C	Si
Lattice parameter (Å)	$a = 3.08$	$a = 3.19$	$a = 3.11$	$a = 12.23$	3.57	5.43
	Hexagonal	Hexagonal	Hexagonal	$b = 3.04$	Cubic	Cubic
				$c = 5.80$		
				$\beta = 103.7°$		
				Monoclinic		
E_G (eV)	3.2	3.44	6.2	4.8	5.5	1.1
E_B (10^5 V/cm)	40	50	150	80	100	3
ε	9.7	10.4	9.1	10	5.7	11.9
λ (W /cm/K)	3–5	1.3	2.9	0.23	20	1.5
v_S (10^7 cm/s)	2.5	2.5	2.5[approx.]	2	2.7	1
μ_n (cm^2/V/s)	<900	<1000	300	250	<2200	1400
E_D (meV)	60 (N)	22 (Si)	90–250 (Si)	20–30 (Sn)		45 (P)
E_A (meV)	250 (Al)	160 (Mg)	500 (Mg))		400 (B)	44 (B)
T_S (°C)	2830	2500	3000	1740	3900	1420
Doping capability	n-type[med]	n-type[med]	n-type[high]	n-type[med]	n-type difficult	n-type
	p-type[high]	p-type[high]	p-type difficult	No p-type	p-type[high]	p-type
Baliga FOM $\varepsilon\mu E_B^3$ with relation to Si	500	1100	8100	1350	11,000	1
Johnson FOM $v_S E_B/2\pi$ with relation to Si	25	31	75	40	68	1
Native wafer material size	150 mm	50 mm[lowav]	50 mm[dem]	150 mm[dem]	c. 100 mm[dem,lim]	200 mm
	200 mm[dem]	100 mm[lowav]				300 mm
						450 mm[dev]
Matureness of technology	c)	Power[b)]	a)	a), b)	a)	d)
		High frequency[c)]				
		Optoelectronics[d)]				

approx., approximated value; med, medium excitation energy; high, high excitation energy; dev, developed; dem, demonstrated; lim, limited crystal quality; lowav, low availability

The calculated Baliga FOM is based on idealized charge carrier transport properties that are usually not realized in a real electronic device. The usage of the materials breakdown field E_B as critical breakdown field E_C is an overestimation. Also, in the case of the Johnson FOM, the critical electrical field E_C was approximated by the breakdown field E_B, which is the upper limit.

a) R&D.
b) Demonstrators.
c) Well developed.
d) Mature.

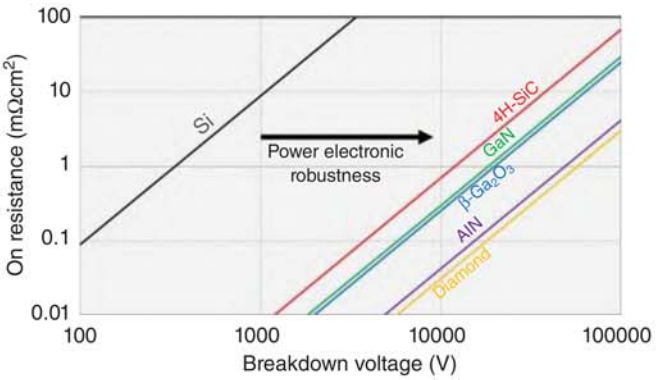


Figure 1 Relation of the on-resistance and the breakdown voltage of a power semiconductor device. The underlying material properties have been listed in Table 1. In general, a larger bandgap causes a significant reduction of the on-resistance at a given device operation voltage.

to power electronics. In addition to the BFOM value, a large heat conductivity of the semiconductor material is quite favorable in power electronics. Among the wide bandgap semiconductors listed in Figure 1 and Table 1, SiC outperforms its counterpart by simultaneously exhibiting a large BFOM value (compared to Si), a great heat conductivity (compared to GaN and Ga_2O_3), and a quite mature device-processing technology that makes use of major parts of Si processing lines. In addition, high-quality SiC wafer substrates are available with a diameter of 150 mm, and even the 200 mm size has been demonstrated. Further, a quite significant cost down for the SiC substrate costs (US$/mm^2) in the range of 10%/a–12%/a has been observed in the last two decades since the introduction of the very first SiC diode to the market in year 2001.

Another important issue for the application of a wide bandgap material in an electronic device is the capability to carry out intentional doping by donor and acceptor atoms to tailor electron and hole transport and to establish bipolar device operation. From the application point of view, at least one kind of doping, i.e. by donor or acceptor atoms, is necessary to establish unipolar device operation. In this context, SiC exhibits reasonable n-type and p-type doping options using the donor nitrogen and the acceptors boron and aluminum, respectively.

Wide bandgap semiconductors also exhibit superior physical properties for the application in high-frequency switching devices. In this context, the Johnson figure of merit $v_S E_C/2\pi$ (v_S = charge carrier saturation velocity, E_C = critical electrical field in the device structure) may be applied for materials selection (Table 1). From the application point of view, GaN epitaxial layers grown on semi-insulating SiC substrates are widely used for the fabrication of high-frequency and medium-power switches, as they are needed in mobile communication networks. This kind of application of SiC profits from the progress in bulk growth of conductive n-type conducting 4H-SiC substrates.

To link the high potential of the wide bandgap semiconductor SiC with the technologic implementation capabilities, all chapters on defects, bulk growth, epitaxial growth, and device processing stemming from fundamental physics and/or materials science and engineering are combined with chapters that comprise the status of the industrial-driven technology development. Following this structure in Part I of the book, the reader gains a comprehensive insight into today's SiC technology. The strong focus on the semiconductor SiC is related to the fact that the well-developed technology is ready to replace the standard semiconductor Si in power electronics. To point out that the materials focus on SiC is not dogmatic, also related wide bandgap materials featuring extraordinary power electronic-related properties, i.e. GaN, diamond, and Ga_2O_3, are surveyed in the shorter Part II of the book.

September 2021

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Noboru Ohtani, Sanda
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Part I

Silicon Carbide (SiC)

1

Dislocation Formation During Physical Vapor Transport Growth of 4H-SiC Crystals

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1.1 Introduction

Silicon carbide (SiC) is the leading candidate among wide-bandgap semiconductor materials for next-generation power semiconductor devices. Over recent decades, the quality of SiC single crystals has improved considerably, thereby making it feasible to fabricate high-performance SiC power devices. 4H-SiC epitaxial wafers of 100 and 150 mm in diameter, with low dislocation density are already available in the market and have been used to fabricate high-performance SiC power devices [1]. However, the widespread commercialization of such devices remains hindered by technological issues related to SiC crystal growth. It is abundantly clear that further successful development of SiC semiconductor technology relies on understanding the process of SiC crystal growth and thus improving the technology for manufacturing large high-quality SiC crystals.

In this chapter, I describe recent progress in understanding the formation of defects during physical vapor transport (PVT) growth of SiC, focusing particularly on the formation of dislocations in 4H-SiC. Currently, commercially available SiC bulk crystals are almost always grown by PVT, namely, by the modified Lely method [2]. However, dislocation formation during the PVT growth of bulk SiC crystals remains a major obstacle to realizing high-performance SiC power devices. Certain types of dislocation are detrimental to the yield and reliability of SiC power devices. Dislocations in PVT-grown SiC crystals are classified broadly into two types, namely, (i) threading dislocations extending along the *c*-axis and (ii) basal plane dislocations (BPDs) lying in the basal plane. Threading dislocations, particularly threading screw dislocations (TSDs), degrade the blocking capabilities of SiC diodes [3–5], whereas BPDs have a serious impact on the reliability of unipolar devices such as SiC metal oxide semiconductor field-effect transistors (MOSFETs) and junction gate field-effect transistors (JFETs) [6, 7] as well as SiC bipolar devices [8, 9]. Therefore, over the decades, considerable effort has gone into reducing the TSD and BPD densities in SiC crystals.

TSDs and BPDs differ markedly in how they form during the PVT growth of SiC crystals. Most TSDs are inherited from the seed crystal and often form in the initial

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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stage of crystal growth [10–12]. BPDs can also be inherited from the seed crystal and form during the initial seeding process, but they do not propagate throughout the entire crystal because their propagation or extension directions are restricted to the basal plane, almost normal to the growth direction. Therefore, the high density of BPDs in the top and middle portions of SiC crystals cannot be explained by the aforementioned mechanisms, and the causes of the BPDs observed in these portions remain poorly understood.

A plausible explanation is that BPDs are nucleated at the growth front (growing crystal surface) and then incorporated into the growing crystal. In general, defect formation at the growth front is closely related to the shape and morphology of the growing crystal surface; the crystal shape determines the magnitude and distribution of the thermoelastic stresses imposed on the grown crystals [13–16], and the surface morphology at the growth front largely affects the defect formation kinetics. Therefore, control of these growth parameters is crucial to obtain high-quality SiC single crystals.

In Section 1.2, I discuss the BPD formation during the PVT growth of 4H-SiC crystals. SiC single crystals of the 4H polytype are the ones studied and implemented most intensively by the industry. The present author's group investigated the BPD formation by characterizing the BPD distributions at the growth front as well as inside 4H-SiC single-crystal boules grown by PVT. The investigation was focused to identify where and how BPDs are nucleated and multiplied in PVT-grown 4H-SiC crystals. As described earlier, the growth front of 4H-SiC crystals is the most plausible location where BPDs are nucleated. The growth front comprises the $(000\bar{1})$ facet and its outer (non-facet [NF]) regions; they exhibit characteristic surface morphologies in terms of the step-terrace structure. The morphologies of these two regions are quite different [17, 18], and thus different defect formation kinetics would govern the defect formation on the two surface regions. Furthermore, these two regions grow into different crystal shapes; the facet is fairly flat and has a temperature distribution across the surface during PVT growth [18], whereas the non-facet regions are convex-shaped toward the growth direction and are assumed to be roughly isothermal during growth [19]. The degree of the convexity of the growth front is also a crucial parameter for defect formation during the PVT growth of SiC. As such, investigating the crystalline properties of the facet and non-facet regions at the growth front provides valuable information about the formation of defects during the PVT growth of SiC crystals.

As described earlier in this section, another relevant issue for dislocation formation during the PVT growth of 4H-SiC crystals is the seeding process. In general, the seeding process, namely, how crystal growth is initiated on the seed crystal, is a key issue for reproducible growth of high-quality single crystals. This is also true for the PVT growth of 4H-SiC single crystals, and thus, establishing a well-controlled seeding process for the PVT growth of SiC is necessary for obtaining high-quality 4H-SiC bulk single crystals. Several authors have tried to reveal the growth mode and the defect formation process during the initial stage of PVT growth [10–12, 20–25]. However, detailed knowledge about the seeding process of SiC PVT growth remains lacking, and further intensive study is required to explore

this important technological issue in SiC PVT growth. An obstacle to investigating the seeding process of SiC PVT growth is that defect formation occurs within a very narrow range near the interface between the seed and grown crystal, and this greatly hinders detailed observations and analyses of the defect formation at the interface.

Another reason why it is difficult to study the defect formation at and near the grown-crystal/seed interface is the complexity of causes of defect formation during the initial stage of SiC PVT growth, such as thermoelastic stress [10, 12], growth kinetics [10, 11, 21], surface conditions of the seed crystal [20], and nitrogen doping enrichment near the grown-crystal/seed interface [12, 22–25]. Section 1.3 is dedicated to this issue, and recent studies of the dislocation formation at the grown-crystal/seed interface during PVT growth of 4H-SiC crystals are described. Slightly off-oriented $(000\bar{1})$ wafers containing the beveled interface between the grown crystal and seed crystal were prepared, which revealed a characteristic dislocation structure formed at the interface and indicated the important role of vacancy injection during the initial stage of the PVT growth of 4H-SiC crystals.

In Section 1.4, I summarize this chapter and draw some conclusions.

1.2 Formation of Basal Plane Dislocations During PVT Growth of 4H-SiC Crystals

1.2.1 Plan-View X-ray Topography Observations of Growth Front

Figure 1.1 shows schematically (a) the PVT growth reactor of 4H-SiC crystals and (b) the scheme for preparing the top portion of the grown crystal with the $(000\bar{1})$ facet and a 4H-SiC $(1\bar{1}00)$ or $(11\bar{2}0)$ wafer sliced vertically along the growth direction from a 4H-SiC single crystal. The crystal was grown on an on-axis or off-oriented 4H-SiC $(000\bar{1})$C seed crystal. The vertically sliced $(1\bar{1}00)$ or $(11\bar{2}0)$ wafer consisted of two

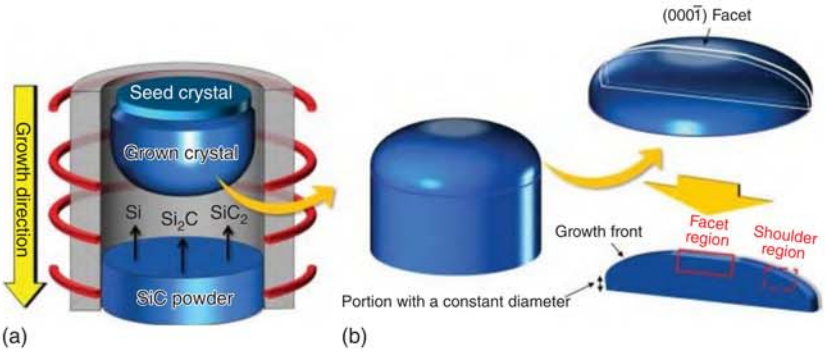


Figure 1.1 Schematics of (a) physical vapor transport (PVT) growth reactor and (b) preparation scheme of top portion of grown crystal with $(000\bar{1})$ facet and a 4H-SiC $(1\bar{1}00)$ or $(11\bar{2}0)$ wafer sliced vertically in the growth direction from a 4H-SiC single-crystal boule grown on a 4H-SiC $(000\bar{1})$C seed crystal. The areas in the wafer examined by transmission X-ray topography are indicated by red open rectangles. Source: Nakano et al. [26]. © 2019, Elsevier.

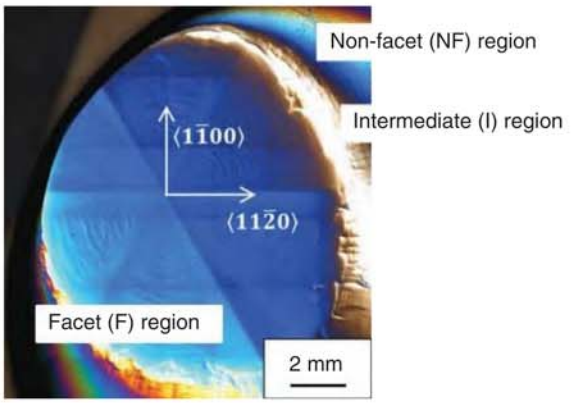


Figure 1.2 Differential interference contrast (DIC) optical microscopy image of growth front of nitrogen-doped (mid-10^{18} cm^{-3}) 4H-SiC single-crystal boule examined in this study. The growth front consists of three distinct morphological regions, namely, the (000$\bar{1}$)C facet (F) and non-facet (NF) regions and the intermediate (I) region between them (after [27]). Source: Sonoda et al.

portions that are classified from the perspective of crystal growth. One was accompanied by the growth front that showed a domed shape (convex toward the growth direction). In this portion, crystal growth occurred during PVT growth. The other portion contained the side surfaces of the crystal, on which there was nominally no crystal growth, and thus it had a constant diameter.

Figure 1.2 shows a differential interference contrast (DIC) optical microscopy image of the growth front of a nitrogen-doped (mid-10^{18} cm^{-3}) 4H-SiC boule examined by Sonoda et al. [27]. The figure reveals that the growth front of the nitrogen-doped 4H-SiC single-crystal boule comprised three distinct morphological regions, namely, (i) the (000$\bar{1}$)C facet region (denoted as F in the figure), (ii) the non-facet (NF) region, and (iii) the intermediate (I) region between F and NF. The facet region exhibited hexagonal symmetry comprising six vicinal (000$\bar{1}$)C surfaces tilted toward the <1$\bar{1}$00> direction. The vicinal surfaces were separated by six crystallographically equivalent ridges extending along the <11$\bar{2}$0> direction. The non-facet region exhibited macroscopically smooth morphology, and the convexity of the region varied depending on the growth conditions, particularly, the temperature distribution in the growth cell. The intermediate region was arranged on the perimeter of the facet region, was narrow, and exhibited a macroscopically slightly rough morphology.

Figure 1.3 shows reflection X-ray topographs of the growth front of a nitrogen-doped 4H-SiC boule in the diffraction conditions (a) $\boldsymbol{g} = 11\bar{2}\bar{8}$ and (b) $1\bar{1}0\bar{7}$, obtained by Sonoda et al. [27]. In the topographs, the boundaries of the facet, intermediate, and non-facet regions are marked by dashed lines. Both topographs contain relatively intense linear contrasts extending roughly along the <1$\bar{1}$00> direction; some of them are marked with open triangles in the topographs. They correspond to low-angle grain boundaries consisting of threading edge dislocations (TEDs) penetrating the crystal along the *c*-axis. Small dot-like contrasts were also observed in both topographs. They had two possible origins, namely, TSDs and TEDs, but were ascribed to TSDs based on their estimated density (~10^3 cm^{-2}). As shown in Figure 1.3, no marked difference in the defect structure was found among the three regions of the as-grown surface, namely, the facet, intermediate,

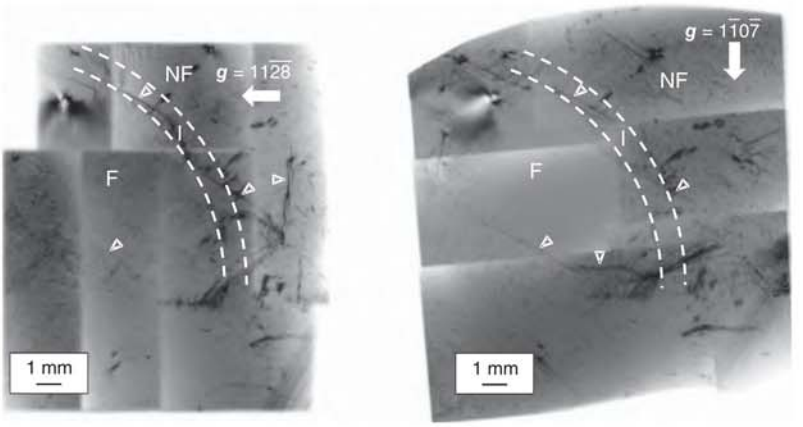


Figure 1.3 Reflection X-ray topographs from the three regions at the growth front of a PVT-grown 4H-SiC crystal. The diffraction vector was (a) $11\bar{2}\bar{8}$ and (b) $1\bar{1}0\bar{7}$. In the topographs, the facet, non-facet, and intermediate regions are denoted as F, NF, and I, respectively, and their boundaries are marked by dashed lines. Source: Sonoda et al. [27].

and non-facet regions, implying that the faceted growth front hardly affects the formation of extended defects during PVT growth of 4H-SiC boules.

The topographs with diffraction vectors $\boldsymbol{g} = 11\bar{2}\bar{8}$ and $1\bar{1}0\bar{7}$ shown in Figure 1.3a,b exhibit slightly different image textures. This is thought to be due to BPDs existing in the crystal portion just beneath the as-grown surface of the boule. BPDs, which have Burger vectors within the basal plane, are out of contrast when the diffraction vector is perpendicular to their Burgers vector, and thus, the two topographs taken with different diffraction vectors exhibit slightly different contrast patterns (image textures).

Figure 1.4 shows enlarged X-ray topographs for more detailed investigation of the dislocation structure underneath the facet and near-facet regions [27]. In the figure, wider-area topographs (Figure 1.4a,c) are also presented, in which the $(000\bar{1})$ facet region is marked by a white circle, and the positions at which the enlarged X-ray topographs (Figure 1.4b,d) were taken are indicated by open squares. The topographs shown in Figure 1.4a,b were taken with the diffraction vector $\boldsymbol{g} = 11\bar{2}\bar{8}$, whereas those in Figure 1.4c,d were taken in the diffraction vector $\boldsymbol{g} = 1\bar{1}0\bar{7}$. Figure 1.4b,d was acquired from the same area in the as-grown crystal surface of a 4H-SiC single-crystal boule (indicated by open squares in Figure 1.4a,c). In Figure 1.4b, both TSDs and BPDs were observed; they are indicated by closed and open triangles, respectively. By contrast, only TSDs were detected in Figure 1.4d in which BPDs exhibited no distinct contrast because the diffraction vector was set perpendicular to their Burgers vectors. These observations indicate that at this particular region of the grown crystal, most BPDs had the same Burgers vector, which implies that they arose from the same cause during the PVT growth process.

In Figure 1.4b, note that many of the observed BPDs seem to emanate from TSDs. Sonoda et al. examined other areas on the as-grown surface and found similar cases of BPDs emanating from TSDs [27]. These results suggest that the existence of

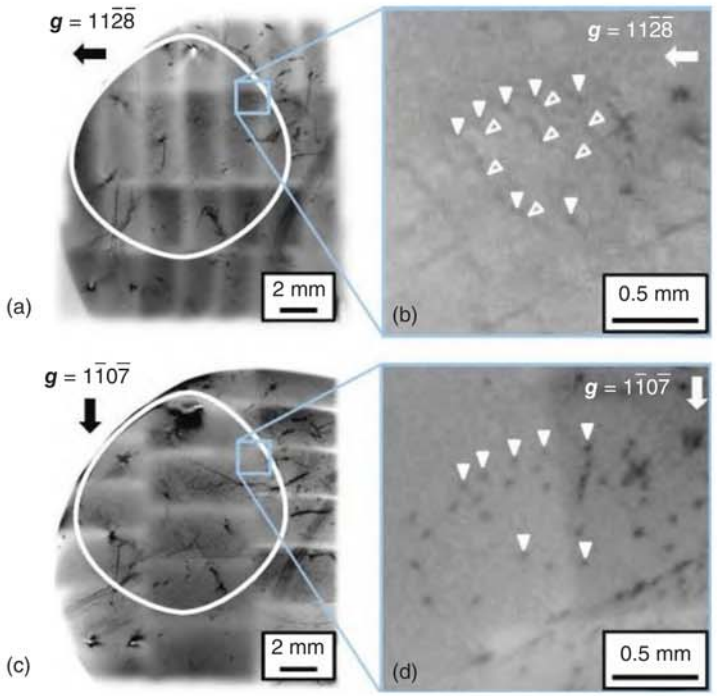


Figure 1.4 Reflection X-ray topographs of the growth front in the diffraction conditions (a) $\boldsymbol{g} = 11\bar{2}\bar{8}$ and (c) $1\bar{1}0\bar{7}$. (b, d) Enlarged X-ray topographs of the areas indicated by open squares in (a, c), respectively. In (b, d), some of the dot-like and line contrasts due to threading screw dislocations (TSDs) and basal plane dislocations (BPDs) are marked by closed and open triangles, respectively. Source: Sonoda et al. [27].

TSDs is related to the BPD formation at the growth front, and TSDs intersecting the growing crystal surface would induce the nucleation of BPDs at the surface during PVT growth of 4H-SiC boules. The mechanism is yet to be clarified, but the elastic interaction between TSDs and the growing crystal surface would play a crucial role in this phenomenon. In this respect, Wang et al. reported an important result that is helpful when considering the origin of this phenomenon [28]. They found that BPDs existing in commercially available 6H-SiC substrates connect or emanate from micropipes (super screw dislocations), comprising dislocation networks in the substrates. Similar BPD structures have also been reported in 4H-SiC epitaxial layers [29]. Micropipes and TSDs extending along the *c*-axis in an infinite crystal do not have a shear stress component parallel to the basal plane, and hence, they could not be the cause of BPDs in an infinite crystal. However, in a finite crystal, they interact elastically with the free surface, and the resultant surface relaxation due to the image force effect of dislocations [30] can provide a shear stress parallel to the basal plane. Compared to micropipes, TSDs provide lower shear stress because of their relatively smaller Burgers vector. However, the Burgers vector of TSDs would be still large enough for them to provide a shear stress exceeding the critical resolved shear stress for BPD formation at the PVT growth temperature (2300–2400 °C) and

nucleate BPD loops and/or half loops at the growing crystal surface during PVT growth of 4H-SiC crystals.

Another important finding made in the X-ray topographs shown in Figures 1.3 and 1.4 is that the density of BPDs in the facet and near-facet regions of the as-grown crystal is significantly lower than the typical BPD densities in commercially available 4H-SiC substrates. The densities of BPDs in 4H-SiC substrates are typically 10^4–$10^5\,cm^{-2}$ [31, 32] and of the order of $10^3\,cm^{-2}$ for state-of-the-art 4H-SiC substrates [33]. By contrast, the estimated BPD density in the facet and near-facet regions of the crystal was less than $10^3\,cm^{-2}$. Sonoda et al. also examined two other 4H-SiC boules and found similar BPD densities in the crystal portion just beneath the facet and near-facet regions of the boules, although 4H-SiC substrates sliced out from the portions of the boules far from the growth front had typical BPD densities (10^4–$10^5\,cm^{-2}$) [27]. These results indicate that although BPDs could nucleate at the growing crystal surface, they hardly multiply in the facet and near-facet regions of PVT-grown 4H-SiC boules.

1.2.2 Cross-Sectional X-ray Topography Observations of Growth Front

To examine in more detail the BPD formation at the growth front, cross-sectional X-ray topography observations of PVT-grown 4H-SiC boules were performed [27]. The two portions in a vertically sliced wafer examined by transmission X-ray topography are illustrated schematically by open rectangles in Figure 1.1b. The solid-line rectangle corresponds to a portion right beneath the facet, whereas the dashed-line rectangle corresponds to a crystal portion near the shoulder region of the grown front.

Figure 1.5a shows a cross-sectional transmission X-ray topograph for the diffraction condition $\boldsymbol{g} = 11\bar{2}0$ of the portion right beneath the $(000\bar{1})$ facet, obtained by Sonoda et al. [27]. The topograph shows several dark vertical band and line contrasts, which correspond to low-angle boundaries and threading dislocations, respectively, penetrating the boule along the growth direction (c-axis). In addition to these vertical band and line contrasts, a number of horizontal line contrasts are also observed in the topograph. Figure 1.5b shows an enlarged topograph of the portion indicated by an open rectangle in Figure 1.5a. In Figure 1.5b, some of the horizontal line contrasts are marked by open triangles. The $\boldsymbol{g} \cdot \boldsymbol{b}$ contrast analysis revealed that these contrasts were caused by BPDs in the boule. Note here that a portion very close to the as-grown surface (facet), marked by a double-headed arrow in Figure 1.5b, is almost free of BPDs. This implies that BPDs hardly multiply in the facet and near-facet regions of the grown boule during PVT growth of 4H-SiC, which agrees well with the results of the plan-view X-ray topography observations shown in Figures 1.3 and 1.4.

Figure 1.5a also reveals that a number of BPDs exist in crystal portions distant from the growth front. This is consistent with the fact that 4H-SiC substrates prepared from these portions contain a high density of BPDs (10^4–$10^5\,cm^{-2}$). An important question here is where they came from. To clarify this point, a series of X-ray topographs (not shown) was taken from the center to the edge of the boule, and it was found that many BPDs extended continuously toward the edge of the

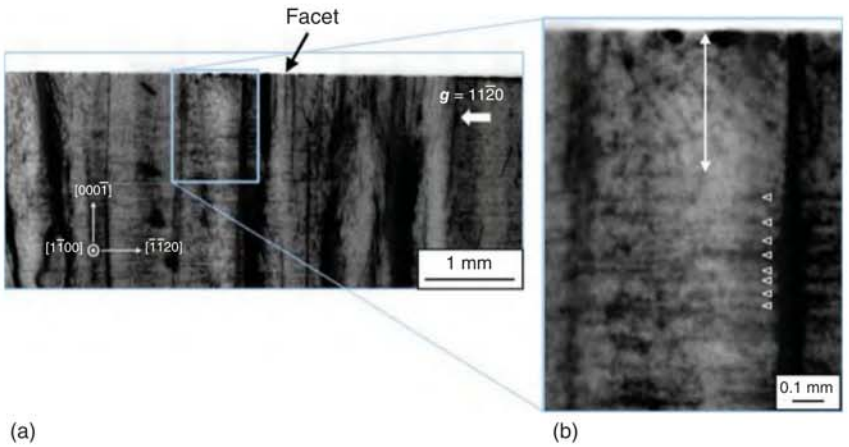


Figure 1.5 Cross-sectional X-ray topographs for diffraction condition $\boldsymbol{g} = 11\bar{2}0$ of a crystal portion right beneath the $(000\bar{1})$ facet of a PVT-grown 4H-SiC boule. (b) An enlarged topography image of the portion indicated by an open rectangle in (a). In (b), some of the horizontal line contrasts caused by BPDs are marked by open triangles. Source: Sonoda et al. [27].

boule and terminated at the shoulder region of the growth front. Figure 1.6 shows X-ray topographs of a crystal portion underneath the shoulder region of a 4H-SiC single-crystal boule [27]. The location of the crystal portion in the boule is indicated by a dashed-line rectangle in Figure 1.1b. Figure 1.6a,b shows X-ray topographs of the portion for the diffraction conditions $\boldsymbol{g} = 11\bar{2}0$ and $000\bar{8}$, respectively. As shown in Figure 1.6a ($11\bar{2}0$ topograph), a number of horizontal line contrasts extend along the basal plane; some of them are marked by open triangles in the figure. As shown in the figure, the horizontal line contrasts terminate at the as-grown surface of the boule. By contrast, they are lost in Figure 1.6b ($000\bar{8}$ topograph), and thus, they were ascribed to BPDs. To elaborate the BPD formation process, Sonoda et al. examined the other ends of these horizontal line contrasts and found that many of them terminated within the crystal at positions roughly below the facet. They observed a similar distribution of BPDs in the other half of the wafer and thus inferred that BPDs were nucleated at the shoulder region of the growth front and extended toward the inside of the grown boule via dislocation glide and multiplication processes during PVT growth. By contrast, such BPD glide and multiplication processes hardly occur in the facet and near-facet regions, resulting in a very low BPD density in the crystal portion right beneath these regions.

These BPD behaviors are illustrated more clearly in a wider-area transmission X-ray topograph shown in Figure 1.7, where the BPD-free crystal portion right beneath the facet and near-facet regions is bounded by a dashed line. In the figure, some of the BPDs extending along the basal plane in the grown crystal are indicated by open triangles. As shown in the figure, the boundary between the BPD-free portion and the other portions has a characteristic "round neck" shape that indicates that the BPD distribution in PVT-grown 4H-SiC crystals is controlled

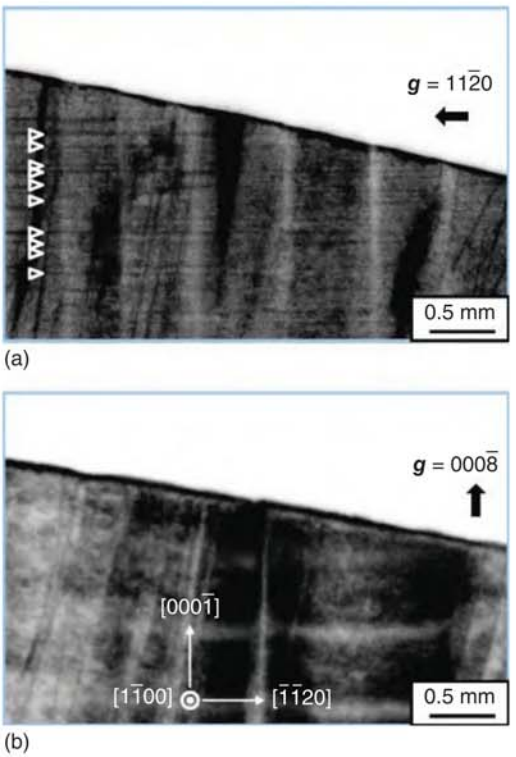


Figure 1.6 Cross-sectional X-ray topographs for diffraction conditions (a) $\boldsymbol{g} = 11\bar{2}0$ and (b) $000\bar{8}$ of a crystal portion underneath the shoulder region of the growth front of a PVT-grown 4H-SiC crystal, whose location in the crystal is indicated by a dashed line rectangle in Figure 1.1b. In (a), a number of horizontal line contrasts due to BPDs are observed; some of them are marked by open triangles. Source: Sonoda et al. [27].

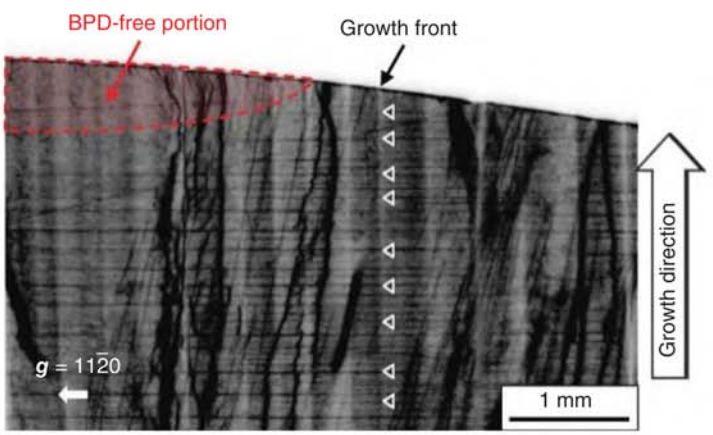


Figure 1.7 Wider-area transmission X-ray topograph for diffraction condition $\boldsymbol{g} = 11\bar{2}0$, which shows the existence of an almost BPD-free crystal portion right beneath the facet and near-facet regions at the growth front. Some of the BPDs extending along the basal plane are indicated by open triangles. The "round-neck" boundary between the BPD-free portion and the other portions is indicated by a dashed line.

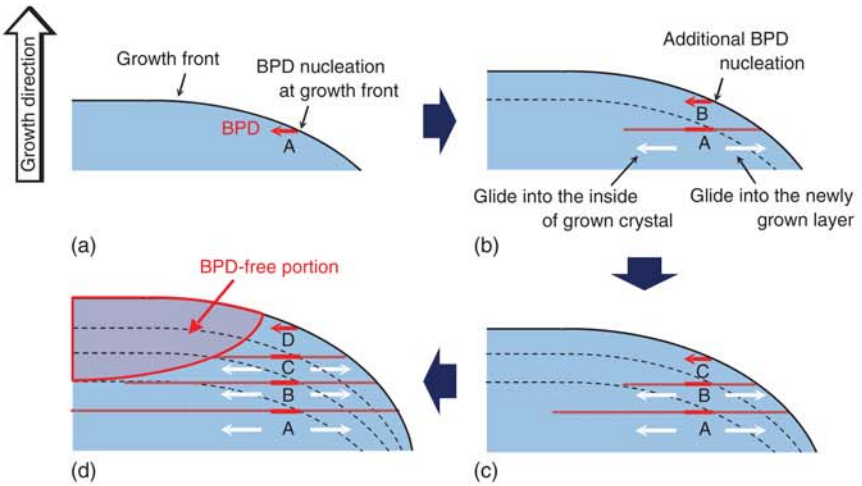


Figure 1.8 Schematics of temporal change of BPD distribution in a 4H-SiC crystal during PVT growth. (a) Nucleation of BPDs at the shoulder region of the grown crystal, and (b) glides of BPDs into the crystal and also toward the growth front of the crystal through the newly grown layer, together with the nucleation of additional BPDs at the growth front. (c) Repetition of processes (a, b) at the growth front of the newly grown layer during PVT growth, and (d) resulting round-neck distribution of BPDs due to the different glide distances of BPDs nucleated at different times in the PVT growth process.

by the BPD nucleation at the shoulder region of the grown crystal. This important conclusion was drawn by considering the glide and multiplication of BPDs after they nucleate at the shoulder region. These processes are illustrated in Figure 1.8, which shows schematically how the BPD distribution in a 4H-SiC crystal changes with time during PVT growth. Figure 1.8a shows the nucleation of BPDs at the shoulder region of a PVT-grown 4H-SiC crystal, and as the PVT growth proceeds, the nucleated BPDs glide into the grown crystal and also extend toward the growth front through the newly grown layer (Figure 1.8b). At this stage, additional BPDs nucleate at the growth front of the newly grown layer, and the aforementioned processes are repeated during PVT growth (Figure 1.8c), resulting in the round-neck distribution of BPDs (Figure 1.8d) because of the different glide distances of BPDs nucleated at different stages of the PVT growth process.

The BPD formation at the shoulder region of the PVT-grown SiC crystals coincides well with numerical results by Gao and Kakimoto [16]. They conducted three-dimensional numerical modeling of BPD multiplication in 4H-SiC bulk crystals. They calculated the resolved thermoelastic shear stresses on the basal plane during PVT growth of 4H-SiC and then substituted them into the Alexander–Hassen model to obtain the BPD distribution in PVT-grown 4H-SiC crystals. Their results showed that the shape of the growth front is key for BPD multiplication, with a largely convex growth front giving rise to a high resolved shear stress on the basal plane at the shoulder region of 4H-SiC boules during PVT growth, thus introducing many BPDs from the region. Their results also suggested that BPD multiplication occurs mainly in the crystal growth stage of the PVT growth process rather than in

the cooling stage. I believe that some irregularities at the growing crystal surface, such as TSD outcrops, become the nucleation sites of BPDs and lead to dislocation multiplication if a sufficiently high thermoelastic shear stress is imposed at these sites during PVT growth. The observed characteristic distribution of BPDs in the growth-front portion of 4H-SiC single-crystal boules corroborates this assumption.

1.2.3 Characteristic BPD Distribution in PVT-Grown 4H-SiC Crystals

In Section 1.2.2, it was revealed that many BPDs are introduced from the shoulder region of 4H-SiC crystals grown in the $[000\bar{1}]$ direction. However, it remains unclear how these BPDs behave in the crystals after their introduction. To clarify their behaviors, X-ray topography and Raman microscopy were conducted on a vertically sliced 4H-SiC $(11\bar{2}0)$ wafer, which is shown schematically in Figure 1.1b. Figure 1.9a,b shows transmission X-ray topographs of a 4H-SiC $(11\bar{2}0)$ wafer for the diffraction conditions $\boldsymbol{g} = 000\bar{8}$ and $1\bar{1}00$, respectively, obtained by Nakano et al. [26]. The area where the topographs were taken is indicated schematically by a red open square in Figure 1.9c. As shown in the topographs, strong horizontal line contrasts are observed in Figure 1.9b (diffraction vector: $1\bar{1}00$), which almost diminish in Figure 1.9a (diffraction vector: $000\bar{8}$). By contrast, in Figure 1.9a, line contrasts extending along the *c*-axis (growth direction) are observed, which correspond to TSDs. In Figure 1.9a, broad band contrasts are also observed at the positions where the strong horizontal line contrasts are observed in Figure 1.9b. The strong horizontal line contrasts observed in Figure 1.9b were caused by either BPDs or basal plane stacking faults in the crystal. To clarify the origin of the strong horizontal line contrasts observed in Figure 1.9b, Nakano et al. performed defect-selective etching

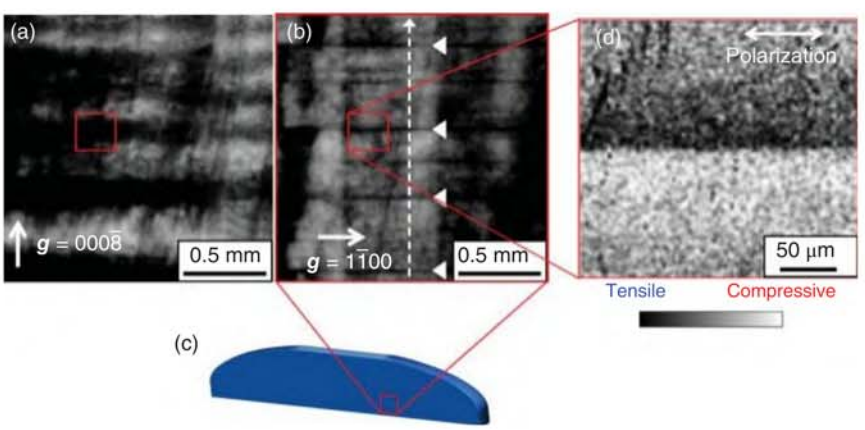


Figure 1.9 Transmission X-ray topographs for diffraction conditions (a) $\boldsymbol{g} = 000\bar{8}$ and (b) $1\bar{1}00$ of a vertically sliced 4H-SiC $(11\bar{2}0)$ wafer. In (c), the area in the wafer examined by transmission X-ray topography is shown as an open rectangle. (d) Raman microscopy image of a layer with a high density of BPDs (bunched BPDs). The white dashed arrow in (b) indicates the points and direction where the variations of the E_2 mode peak position and the *a*-lattice constant (Figure 1.10) were measured. Source: Nakano et al. [26]. © 2019, Elsevier.

(molten KOH etching) and found that they were caused by a high density of BPDs; Nakano et al. referred to this type of BPDs as "bunched BPDs" [26]. Note here that such bunched BPDs are arranged almost periodically along the growth direction in the grown crystal, as revealed in Figure 1.9b, where some of the bunched BPDs are indicated by closed white triangles.

To examine the structure of bunched BPDs in more detail, Raman microscopy imaging of bunched BPDs was conducted. The imaged area is indicated by a red open square in Figure 1.9a,b, and the peak position of the E_2 mode at ~776 cm^{-1} was plotted across this area with the polarization vectors of the incident and scattered light parallel to the basal plane. The obtained image is shown in Figure 1.9d, in which the light polarization is indicated by a double-headed arrow. As shown in the figure, there is a clear difference in the peak position between the upper and lower sides of bunched BPDs. In the upper side, the peak of the E_2 mode shifts to a lower position, while the peak is positioned at higher wavenumbers in the lower side, implying the existence of tensile (compressive) strain in the upper (lower) side of bunched BPDs.

Figure 1.10 shows how (i) the E_2 peak position and (ii) the a-lattice constant (lattice constant within the basal plane) vary in the growth direction as measured by high-resolution X-ray diffraction (HRXRD). These variations were measured along the line indicated by a white dashed arrow in Figure 1.9b. As shown in Figure 1.10a, the peak position shifted abruptly where bunched BPDs existed. The

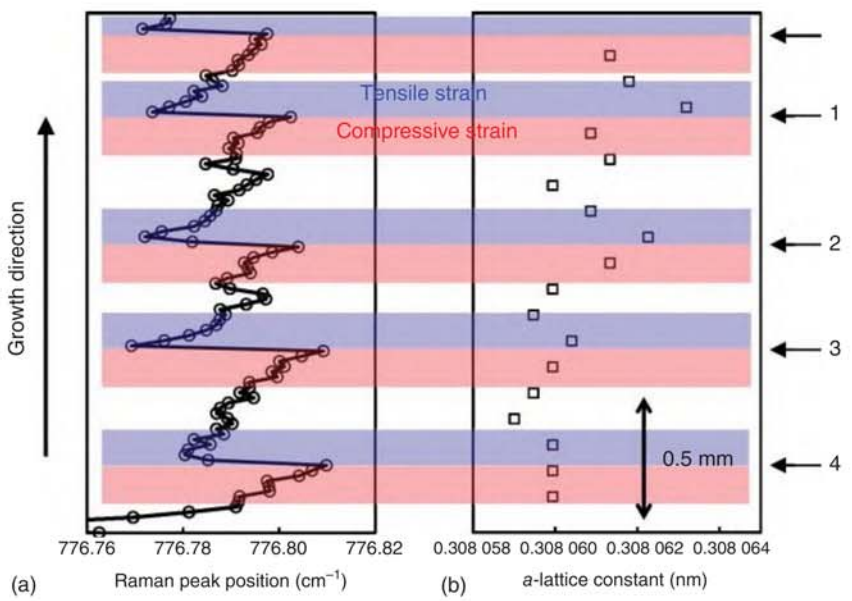


Figure 1.10 Variations of (a) peak position of Raman-active E_2 mode around 776 cm^{-1} and (b) the a-lattice constant measured using HRXRD in the growth direction on a vertically sliced 4H-SiC $(11\bar{2}0)$ wafer. The measured points and direction are indicated by a white dashed arrow in Figure 1.9b. (a) shows clearly that abrupt shifts of the E_2 peak position occurred at bunched BPDs; the positions of some of the bunched BPDs are indicated by arrows in the right-hand side of the figure (after [26]).

positions of some of the bunched BPDs are indicated by arrows in the right-hand side of Figure 1.10; those indicated by the arrows numbered from 1 to 4 correspond to the bunched BPDs indicated by closed white triangles in Figure 1.9b. The shift at bunched BPDs always occurred toward lower wavenumbers when the light beam was scanned from the bottom to the top of the grown crystal, implying that tensile strain within the basal plane always exists in the upper side of bunched BPDs [34–36]. The *a*-lattice constant also varied in the growth direction and increased in the upper side of bunched BPDs. This is consistent with the variation of the E_2 mode peak position, and it can be concluded that the tensile strain within the basal plane existing in the upper side of bunched BPDs resulted in a larger *a*-lattice constant.

The aforementioned results indicate that bunched BPDs are accompanied by extra half-planes pointing toward the seed crystal. This is reasonable if bunched BPDs are introduced by the thermoelastic stress imposed on the growing crystal during the PVT growth of SiC. The SiC PVT growth process is driven primarily by the temperature gradient along the *c*-axis (growth direction), and thus, a high σ_{rz} shear stress is imposed on the growing crystal during PVT growth, where *r* and *z* denote the radial and axial directions, respectively, of the grown crystal (*z* is parallel to the *c*-axis). At typical PVT growth temperatures (>2300 °C), SiC crystals deform plastically and the σ_{rz} shear stress is relieved considerably by the introduction of BPDs into the crystal. During the PVT growth process, a positive temperature gradient is maintained in the growth direction, and thus when the thermoelastic stress is relieved, BPDs are introduced that have extra half-planes pointing toward the seed crystal.

1.2.4 BPD Multiplication During PVT Growth

To investigate in more detail how BPDs behave during the PVT growth of 4H-SiC crystals, further extended Raman microscopy imaging of bunched BPDs in the lateral direction (parallel to the basal plane) was performed. The result of the Raman microscopy imaging is shown in Figure 1.11a. The image is a two-dimensional mapping of the peak position of the E_2 mode around 776 cm^{-1} on a vertically sliced 4H-SiC $(11\bar{2}0)$ wafer. Similarly to Figure 1.9d, the peak position differs clearly between the upper and lower sides of bunched BPDs. Note in this figure that the contrast difference between the upper and lower sides of bunched BPDs varies along the basal plane. In Figure 1.11a, portions with larger and smaller contrast differences are indicated by closed and open triangles, respectively. Nakano et al. found that the observed variation of the contrast difference (magnitude of the abrupt shift of the E_2 mode peak position at bunched BPDs) along the basal plane was correlated with the TSD density in the crystal [26]. Figure 1.11b shows the relationship between the contrast difference and the TSD density; the latter was estimated from the density of the line contrasts extending along the *c*-axis in X-ray topographs with the diffraction vector $\boldsymbol{g} = 000\bar{8}$ (e.g. Figure 1.9a) at the position where the contrast difference was measured by Raman microscopy. As shown in the figure, the magnitude of the abrupt peak shift at bunched BPDs is correlated well with TSD density: as the TSD density increases, the abrupt peak shift at bunched

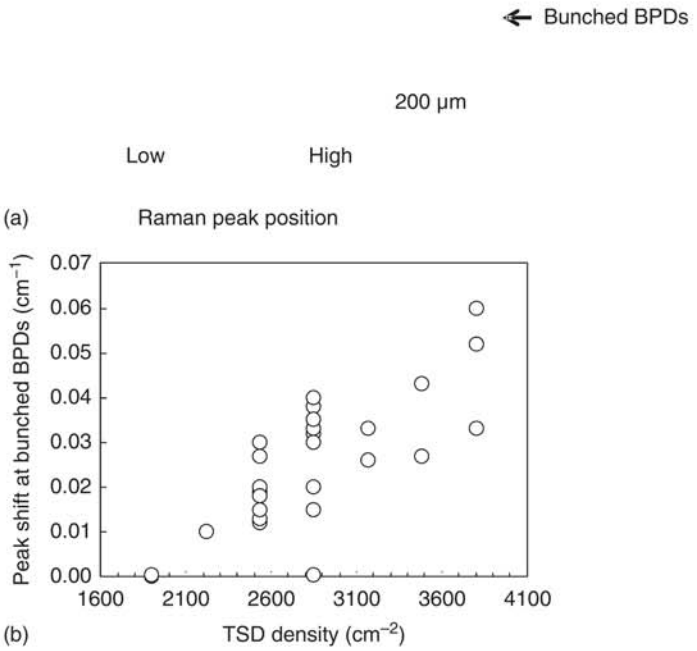


Figure 1.11 (a) Extended Raman microscopy image of bunched BPDs along the basal plane. The image shows variation of the E_2 mode peak position around bunched BPDs. The open and closed triangles in the image indicate portions that exhibited smaller and larger abrupt peak shifts, respectively, at the bunched BPDs. (b) A positive correlation between the magnitude of the abrupt peak shift at the bunched BPDs and the TSD density. Source: Nakano et al. [26]. © 2019, Elsevier.

BPDs becomes larger, which implies that the TSD and BPD densities in PVT-grown 4H-SiC crystals are correlated positively.

Ohtani et al. [37] reported a similar positive correlation between the TSD and BPD densities in PVT-grown 4H-SiC crystals. They conducted defect-selective etching using molten KOH to estimate the TSD and BPD densities in PVT-grown 4H-SiC crystals and found that the BPD density increased with the TSD density in the crystals. They ascribed this positive correlation to BPD multiplication around TSDs. Temperature gradients in 4H-SiC crystals during PVT growth cause BPDs to glide on the basal plane and cut through a forest of TSDs extending along the *c*-axis in the crystals. After crossing TSDs, BPDs have super jogs parallel to the *c*-axis, which are immobile and anchored in the crystal. When the BPDs glide further under thermoelastic stress during PVT growth and/or post-growth cooling, the well-known Frank–Read-type BPD multiplication occurs, and consequently the BPD density increases significantly around TSDs [32, 38]. This is why the BPD and TSD densities are correlated positively in 4H-SiC crystals.

As described in Section 1.2.3, BPDs have a characteristic distribution in the growth direction in PVT-grown 4H-SiC crystals; layers exist with a high density of BPDs (bunched BPDs) arranged almost periodically in the growth direction. As for the BPD formation in PVT-grown 4H-SiC crystals, it was also revealed in Section 1.2.2 that a number of BPDs are introduced from the shoulder region of the grown crystal during PVT growth. In this respect, it is noteworthy that bunched BPDs were observed relatively far from the shoulder region of the grown crystal. Given these results, an important question arises as to where and when bunched BPDs are introduced in crystals. A possible mechanism is that bunched BPDs are introduced from the side surfaces of grown crystals. The constant-diameter portion of a grown crystal has side surfaces that are located very close to the crucible inner walls, and under certain growth conditions, they can come into contact with the walls during PVT growth or cooling because of the different coefficients of thermal expansion of SiC and graphite. Therefore, the side surfaces of the grown crystal could be subject to high stress during PVT growth, thereby introducing a number of BPDs from the side surfaces. However, X-ray topography observations of a crystal portion near the side surfaces of 4H-SiC grown crystals revealed no bunched BPDs near the side surfaces [26].

To examine further the origin of bunched BPDs, further extended Raman microscopy analysis was performed in the growth direction. Figure 1.12 shows how the E_2 peak position varies in the growth direction [26]. The variations were measured along two lines, one that started from the bottom of a vertically sliced wafer and ended near the $(000\bar{1})$ facet region at the growth front (denoted by line A) and one that was close to the side surface (edge) of a grown crystal (denoted by line B). The locations of these two lines (lines A and B) in a vertically sliced $(11\bar{2}0)$ wafer are indicated schematically by dashed arrows in the inset of Figure 1.12. As shown in Figure 1.12, the E_2 peak position often shifted abruptly along line A;

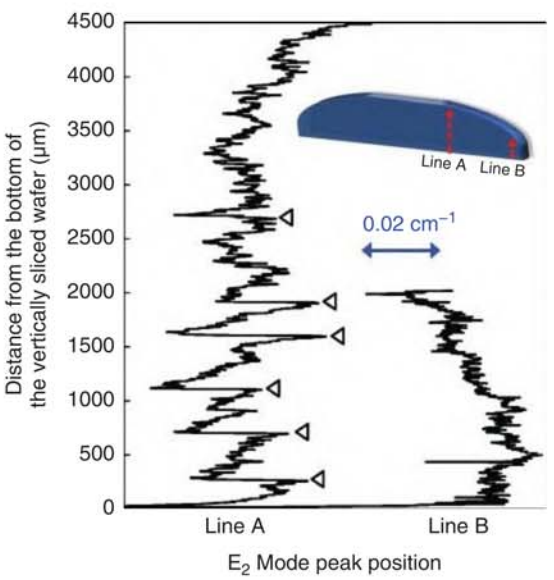


Figure 1.12 Variations of E_2 mode peak position in growth direction measured in the near-facet (line A) and edge (line B) portions of a vertically sliced 4H-SiC $(11\bar{2}0)$ wafer. The locations of the two measured portions (lines A and B) in the wafer are indicated by dashed arrows in the inset figure. Source: Nakano et al. [26]. © 2019, Elsevier.

some of the shifts are indicated by open triangles in the figure. By contrast, no such abrupt shifts were seen along line B. Note here that the abrupt shift intensified as the measured point approached the bottom of the vertically sliced wafer, implying that the BPD density in bunched BPDs increases gradually toward the seed crystal. Such an increase in BPD density toward the seed crystal is reasonable if bunched BPDs are introduced from the growth front (top surface of the growing crystal) during PVT growth. Once bunched BPDs are introduced from the growth front, their BPD density increases gradually as the growth proceeds, this being because the total duration of thermoelastic stress imposed on the growing crystal increases with the growth time.

The abovementioned discussions combine to give the important conclusion that bunched BPDs or their nuclei would be introduced at the growth front (domed surface) but hardly so from the side surfaces of grown crystals. The most plausible location where bunched BPDs are introduced would be the shoulder region of the growing crystal. Gao and Kakimoto [16] showed theoretically that the domed shape of the growth front gives rise to a high resolved shear stress on the basal plane in the shoulder region of the grown crystal during PVT growth of 4H-SiC, thus causing many BPDs to be introduced from that region. This theoretical prediction was subsequently confirmed experimentally by Sonoda et al. using X-ray topography [27]. The aforementioned results of Nakano et al. [26] indicate that the shoulder region of the growing crystal is a major source of BPDs, including bunched BPDs or their nuclei, and the BPDs introduced from that region would determine the distribution of BPDs throughout PVT-grown 4H-SiC crystals.

1.3 Dislocation Formation During Initial Stage of PVT Growth of 4H-SiC Crystals

1.3.1 Preparation of 4H-SiC Wafers with Beveled Interface Between Grown Crystal and Seed Crystal

In this section, I describe the formation of dislocations at the grown-crystal/seed interface of PVT-grown 4H-SiC crystals. As described in Section 1.1, most threading dislocations in PVT-grown 4H-SiC crystals form during the initial stage of PVT growth, and thus, it is essential to control the growth initiation to obtain high-quality 4H-SiC crystals. To reveal the processes for dislocation formation in the initial stage of 4H-SiC PVT growth, Shioura et al. [39] prepared 4H-SiC wafers containing a beveled interface between the grown crystal and the seed crystal and used them to examine the detailed distribution of crystallographic defects at and near the interface. Figure 1.13 shows schematics of the slicing geometry of a 4H-SiC crystal grown on a 4° off-oriented $(000\bar{1})$ seed crystal, providing a 1.5° off-oriented $(000\bar{1})$ wafer, which has a beveled interface between the grown crystal and seed crystal [39]. Figure 1.13a is a schematic side view of a nitrogen-doped 4H-SiC crystal grown on a 4° off-oriented $(000\bar{1})$ seed crystal and a slightly off-oriented (1.5° off-oriented approximately toward $[11\bar{2}0]$) $(000\bar{1})$ wafer sliced out from the grown crystal, while

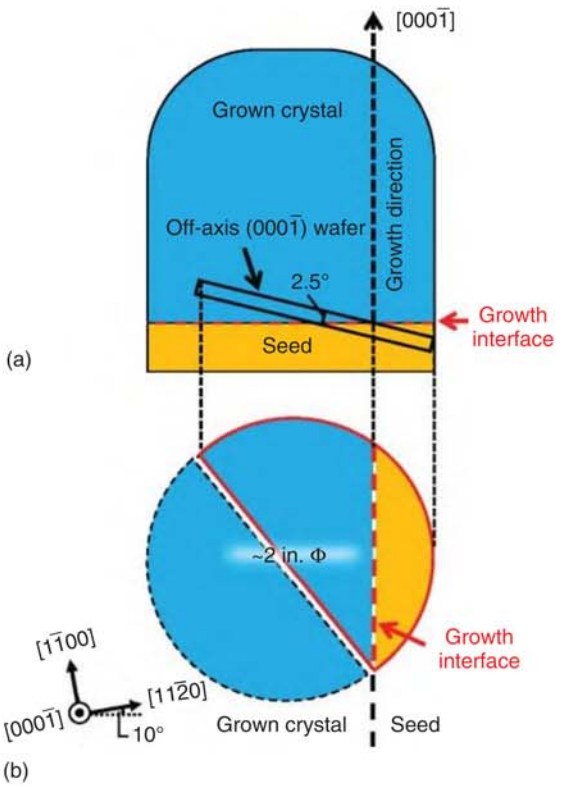


Figure 1.13 Schematics of slicing geometry of a nitrogen-doped 4H-SiC crystal grown on a 4° off-oriented (000$\bar{1}$) seed crystal, providing a 1.5° off-oriented (000$\bar{1}$) wafer, which has a beveled interface between the grown crystal and the seed crystal. (a) Side view of grown crystal and 1.5° off-oriented (000$\bar{1}$) wafer sliced out from the crystal. (b) Top view of sliced wafer. Source: Shioura et al. [39]. © 2019, Elsevier.

Figure 1.13b shows a top view of the sliced wafer. The angle between the wafer surface and the grown-crystal/seed interface was relatively shallow (2.5°), and thus, the defective near-interface region was substantially enlarged to facilitate detailed observations and analyses of defects at and near the interface. Shioura et al. examined this substantially enlarged interfacial region between the grown crystal and seed crystal using Raman microscopy and X-ray topography, and on the basis of the obtained results elucidated the formation mechanisms of crystallographic defects during the initial stage of PVT growth of 4H-SiC crystals [39].

1.3.2 Determination of Grown-Crystal/Seed Interface by Raman Microscopy

Figure 1.14 shows (a) an intensity mapping image of the whole 1.5° off-oriented 4H-SiC (000$\bar{1}$) wafer containing the grown-crystal/seed interface, acquired using the intensity of the longitudinal optical phonon–plasmon-coupled (LOPC) mode around 983 cm^{-1}, and (b) a reflection X-ray topograph of the wafer for the diffraction condition $\boldsymbol{g} = 11\bar{2}8$ [39]. The intensity of the LOPC mode is known to be very sensitive to the carrier (electron) concentration in 4H-SiC crystals: as the electron concentration increases, the intensity decreases rapidly [40, 41]. As shown in Figure 1.14a, the LOPC mode scattering intensity differs markedly between the seed

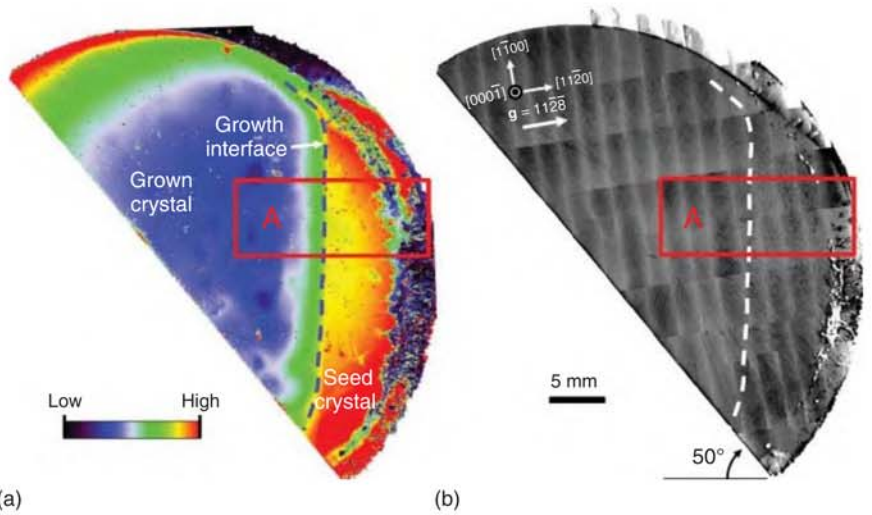


Figure 1.14 (a) Raman mapping image using longitudinal optical phonon–plasmon-coupled (LOPC) mode intensity of a 1.5° off-oriented 4H-SiC (000$\bar{1}$) wafer with a beveled interface between the grown crystal and the seed crystal, which corresponds to the upper right part of the wafer illustrated schematically in Figure 1.13b. (b) Reflection X-ray topograph of the 1.5° off-oriented 4H-SiC (000$\bar{1}$) wafer in the diffraction condition $\boldsymbol{g} = 11\bar{2}\bar{8}$. The position of the interface between the grown crystal and seed crystal is indicated by a dashed line, and the region used for subsequent Raman microscopy and X-ray topography analyses is indicated by a red open rectangle (region A) in both (a, b). Source: Shioura et al. [39]. © 2019, Elsevier.

and grown crystal regions, and thus, their interface can be determined by Raman microscopy. Figure 1.15 shows enlarged Raman microscopy images across region A in the wafer, whose location is indicated by a red open rectangle in Figure 1.14a,b. In Figure 1.15, mapping images of (a) Raman scattering intensity, (b) peak position, and (c) width of the LOPC asymmetric peak are shown, together with their line profiles across the grown-crystal/seed interface, namely, (d) intensity, (e) peak position, and (f) peak width. As shown in Figure 1.15d, the Raman scattering intensity decreases rapidly from the point indicated by a red triangle in the figure toward the left-hand side of the figure (in the growth direction). Ohshige et al. reported that the electron concentration in PVT-grown 4H-SiC crystals increases abruptly at the grown-crystal/seed interface because of the enrichment of nitrogen donors in the crystal in its initial growth stage [23]. The rapid decrease in the scattering intensity shown in Figure 1.15d is thought to be due to the nitrogen enrichment at the grown-crystal/seed interface, and thus, using the LOPC intensity profile, the location of the interface between the grown crystal and the seed crystal can be determined reasonably as the point indicated by a red triangle in Figure 1.15d.

According to the scheme described earlier, the grown-crystal/seed interface was determined and indicated as a dashed line in Figures 1.14 and 1.15a–c [39]. In all the figures, the left-hand side of the dashed line is the grown crystal, while the right-hand side corresponds to the seed crystal.

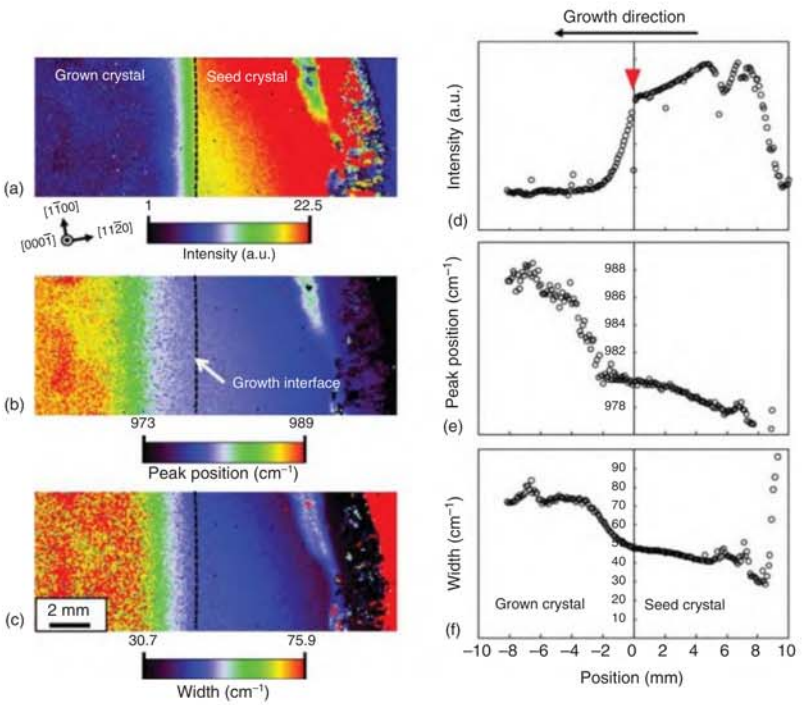


Figure 1.15 Raman microscopy images of region A, which is indicated by a red open rectangle in Figure 1.14: (a) scattering intensity, (b) peak position, and (c) width of the asymmetric LOPC peak around 983 cm^{-1}, where the position of the grown-crystal/seed interface is indicated by a dashed line in each image. The variations of the intensity, peak position, and width of the LOPC peak across the interface are shown in (d–f), respectively, where the data were averaged in the direction parallel to the grown-crystal/seed interface (after [39]). Source: Shioura et al.

1.3.3 X-ray Topography Observations of Dislocation Structure at Grown-Crystal/Seed Interface

To examine more clearly the defect structure near the grown-crystal/seed interface, an enlarged X-ray topograph from the interface region was taken and is shown in Figure 1.16 [39], which is a reflection X-ray topography image for the diffraction condition $\boldsymbol{g} = 11\bar{2}\bar{8}$ acquired from region A indicated by a red open rectangle in Figure 1.14. The grown-crystal/seed interface determined by Raman microscopy imaging is indicated by a dashed line in Figure 1.16. The image shows the existence of widespread networks of BPDs near the grown-crystal/seed interface; some of them are marked by white triangles in Figure 1.16. Similar BPD networks have been reported by Tani et al. [24]. They conducted high-voltage transmission electron microscopy (HVTEM) observations and found that BPDs in the networks connected to each other to form cell-like structures and decomposed into stacking faults at the triple nodes of the networks. In Figure 1.16, a cell-like feature of the BPD networks formed at the grown-crystal/seed interface is also observed, and more interestingly, it was found that the networks extended considerably into the seed crystal.

Shioura et al. conducted $\boldsymbol{g} \cdot \boldsymbol{b}$ contrast analyses of the BPD networks observed at the grown-crystal/seed interface to determine the nature of the networks [39]. The results are shown in Figure 1.17, where reflection X-ray topographs of region B, which is indicated by an open square in Figure 1.16, are shown; they were taken for the diffraction conditions (a) $\boldsymbol{g} = 11\bar{2}\bar{8}$, (b) $\bar{1}01\bar{7}$, (c) $\bar{1}10\bar{7}$, and (d) $01\bar{1}\bar{7}$. Figure 1.17 reveals that under each diffraction condition, some parts of the BPD networks become out of contrast; the parts that are out of contrast under each diffraction condition are indicated by white lines in each topograph. The extinction of the diffraction contrast means that the Burgers vectors associated with these parts of the BPD networks are perpendicular to the diffraction vector, and thus, the results of the $\boldsymbol{g} \cdot \boldsymbol{b}$ contrast analyses shown in Figure 1.17 demonstrate that the BPD networks

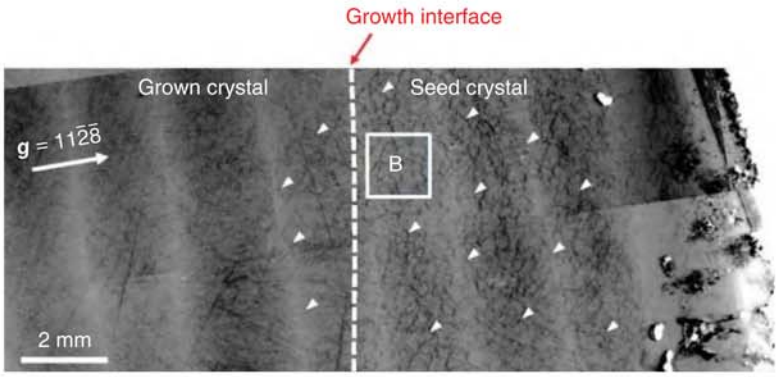


Figure 1.16 Reflection X-ray topograph for diffraction condition $\boldsymbol{g} = 11\bar{2}\bar{8}$ of region A in 1.5° off-oriented 4H-SiC (000$\bar{1}$) wafer, where the position of the grown-crystal/seed interface is indicated by a white dashed line. In this figure, the region used for subsequent $\boldsymbol{g} \cdot \boldsymbol{b}$ analyses (see Figure 1.17) is indicated by a white open square (region B). Source: Shioura et al. [39].

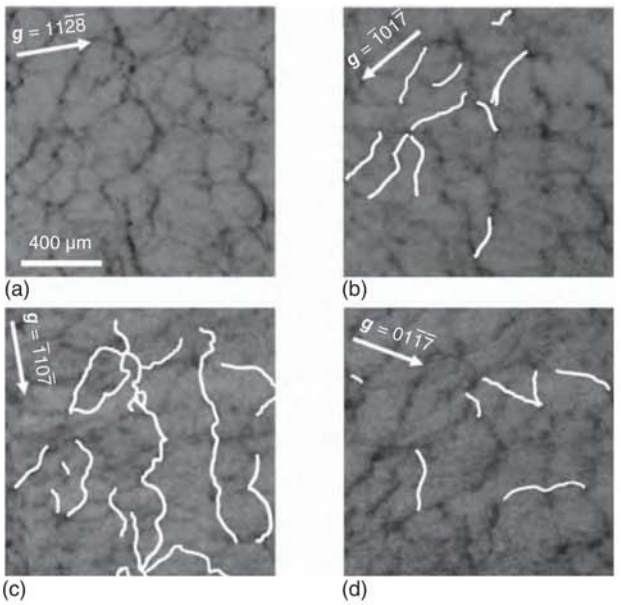


Figure 1.17 Reflection X-ray topographs of BPD networks observed in region B of 1.5° off-oriented 4H-SiC (0001) wafer for diffraction conditions (a) $\boldsymbol{g} = 11\bar{2}\bar{8}$, (b) $\bar{1}01\bar{7}$, (c) $\bar{1}10\bar{7}$, and (d) $01\bar{1}\bar{7}$. The diminished parts of the BPD networks under each diffraction condition are indicated by white solid lines in each topograph. Source: Shioura et al. [39].

consist mainly of edge-type BPDs that have a Burgers vector perpendicular to the dislocation line. This result suggests that a high density of BPDs observed at the grown-crystal/seed interface would have been caused by some form of misfit stress within the basal plane imposed at the interface during the initial stage of PVT growth.

To investigate further the nature of the BPD networks, the bending of the (0001) basal plane was examined by means of measurements of the peak position shift of the ω-scan 0008 HRXRD rocking curve across the grown-crystal/seed interface [39]. The results indicated that the (0001) basal plane in the slightly off-oriented $(000\bar{1})$ wafer contained the beveled interface between the grown crystal and seed crystal bent in a concave manner in the $[000\bar{1}]$ growth direction, which implies that the crystal near the grown-crystal/seed interface contained extra half-planes pointing in the [0001] direction (the backside of the seed crystal).

1.3.4 Formation Mechanism of BPD Networks and Their Migration into Seed Crystal

It was revealed by HRXRD measurements that there were extra half-planes pointing in the [0001] direction in the crystal near the grown-crystal/seed interface [39]. These extra half-planes are thought to be associated with the BPD networks existing near the grown-crystal/seed interface. It was also revealed that most parts of BPDs comprising the networks have an edge component, and thus, they are likely to have

been caused by misfit strain accommodated at the interface during the initial stage of SiC PVT growth.

The misfit strain within the basal plane at the grown-crystal/seed interface has two possible origins, namely, (i) nitrogen enrichment at the interface and (ii) the temperature gradient in the growth direction imposed on the growing crystal in the initial stage of PVT growth. The nitrogen enrichment at the grown-crystal/seed interface has been reported by several authors [12, 22–25]. The grown crystal was doped intentionally with nitrogen in the same concentration as the seed crystal; however, residual nitrogen impurities in the growth atmosphere and/or those adsorbed on the source powder surface could give rise to a relative enrichment of nitrogen in the crystal grown during the early stage of PVT growth. Nitrogen doping has been reported to give rise to a smaller lattice spacing [42] and also a smaller coefficient of thermal expansion [43] within the basal plane for 4H-SiC crystals; thus, a higher nitrogen concentration in the grown crystal than that of the underlying seed crystal would give rise to misfit strain between the grown crystal and the seed. However, in this case, the sign of the misfit strain is opposite to that having caused the BPD networks; the nitrogen enrichment in the grown crystal results in a smaller lattice constant within the basal plane at the PVT growth temperature (~2300 °C), yielding BPDs with extra half-planes pointing in the growth direction when the misfit strain is relieved. This is contradictory to the result of the HRXRD measurements.

Another possible origin of the misfit strain at the grown-crystal/seed interface is the temperature gradient at the interface. Usually, during SiC PVT growth, a positive temperature gradient in the growth direction is set in the growth zone by placing the growth crucible asymmetrically in the radio-frequency (RF) induction coil or the heating furnace (see Figures 1.1a and 1.18a). In addition to this intentionally imposed temperature gradient, the latent heat dissipation associated with the condensation of Si- and C-bearing species sublimed from the source powder would result in an enhanced positive temperature gradient during PVT growth. In this respect, note that SiC has an extremely large latent heat of phase transition from the vapor to the solid (heat of condensation/sublimation), which is estimated to be 580 kJ/mol [44] and more than 10 times larger than that of Si solidification from the melt (50.6 kJ/mol) [45].

With respect to the heating due to the latent heat, another important factor that should be considered is the thickness of the grown crystal in the initial stage of growth. Figure 1.18 explains schematically how the thickness of the grown crystal affects the dissipation of latent heat. Upon condensation of the Si- and C-bearing species, the latent heat is released on the growing crystal surface. The seed crystal is usually placed on a graphite holder, which has a much lower thermal conductivity than that of 4H-SiC at the PVT growth temperature. In the initial stage of PVT growth, the SiC crystal (seed crystal plus grown crystal) is very thin, and thus, all the heat generated by the condensation of Si- and C-bearing species must be dissipated through the backside of the seed crystal (Figure 1.18d). However, the low thermal conductivity of the graphite seed holder means that the generated heat is not dissipated efficiently, and thus, an even larger positive temperature gradient is established at the growing crystal surface during the initial stage of PVT

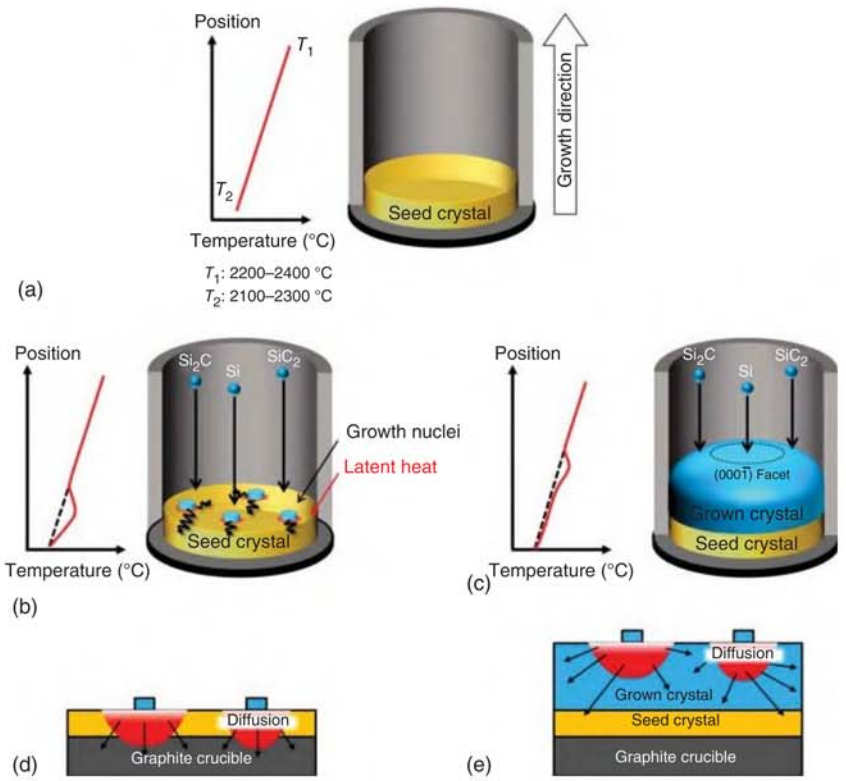


Figure 1.18 Schematics of latent heat dissipation during PVT growth of 4H-SiC crystals. (a) Positive temperature gradient in the growth direction imposed intentionally in the growth crucible by placing it asymmetrically in the RF induction coil or the heating furnace. (b) Enhancement of temperature gradient at growth front of the grown crystal caused by the poor latent heat dissipation in the initial stage of PVT growth because of the low thermal conductivity of the graphite seed holder; this effect is shown schematically in (d). (c) Case of a thick grown crystal after sufficient time of crystal growth; the enhanced temperature gradient at the growth front is lessened considerably because the generated latent heat can be dissipated efficiently through the thickly grown SiC crystal, as shown schematically in (e).

growth (Figure 1.18b). This large positive temperature gradient causes a large misfit strain within the basal plane at and near the grown-crystal/seed interface, which is relieved by the introduction of BPDs during growth. By contrast, as the grown crystal becomes thicker as it grows, the latent heat is dissipated more efficiently through the body of the thick grown crystal (Figure 1.18e). This lessens considerably the enhanced temperature gradient at the growth front due to the condensation of the Si- and C-bearing species (Figure 1.18c).

The aforementioned strain generation and relaxation processes due to the latent heat are illustrated schematically in Figure 1.19. The figure depicts sequentially (a) the seed crystal prior to PVT growth, (b) the basal plane bending associated with the large temperature gradient in the initial stage of growth, which occurs in a convex manner in the growth direction, (c) the introduction of BPDs to relieve the

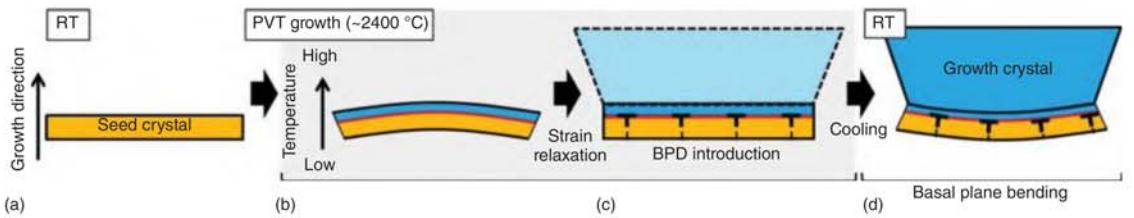


Figure 1.19 Schematic of introduction of BPDs at grown-crystal/seed interface during PVT growth process, and the resulting basal plane bending after the growth process. Source: Shioura et al. [39]. © 2019, Elsevier; (a) seed crystal prior to PVT growth, (b) basal plane bending associated the large temperature gradient at the initial stage of growth, which occurs in a convex manner toward the growth direction, (c) introduction of BPDs to relax the misfit strain within the basal plane at the grown-crystal/seed interface, and (d) concave-shape basal plane bending toward the growth direction after cooling to room temperature.

misfit strain within the basal plane at the grown-crystal/seed interface, and (d) the resultant concave-shaped basal plane bending in the growth direction after PVT growth. The large basal plane bending due to the poor heat dissipation in the initial stage of PVT growth of SiC was observed experimentally by Hock et al. using in situ X-ray diffraction [46]. They found that the degree of basal plane bending increased with the growth rate, implying that the latent heating due to the condensation of source gas species plays an important role in the basal plane bending in the initial stage of PVT growth.

The final concave shape of the basal plane in the growth direction shown in Figure 1.19d is consistent with the lattice bending observed by HRXRD, and thus, the large positive temperature gradient established at the growing crystal surface during the initial stage of PVT growth would be the most plausible cause of the observed BPD networks. The relationship between the observed BPD networks and the formation of threading dislocations in the initial stage of PVT growth [10–12] is yet to be clarified. However, in Figure 1.17, in addition to the BPD networks, dot-like features are also observed at the nodes of the BPD networks. They are likely to correspond to threading dislocations and suggest that the BPD networks are related closely to them and would be an important source of threading dislocations in PVT-grown 4H-SiC crystals.

As revealed in Figure 1.16, the BPD networks extended fairly deeply in the seed crystal. The maximum depth of the networks in the seed crystal can be estimated from their positions on the surface of the 1.5° off-oriented $(000\bar{1})$ wafer; the networks extended up to 7 mm on the wafer surface from the grown-crystal/seed interface toward the backside of the seed crystal. The distance of 7 mm on the wafer surface corresponds to a depth of 300 μm from the grown-crystal/seed interface toward the backside of the seed crystal. In the initial stage of PVT growth, growth islands are likely to nucleate on the seed crystal surface and then coalesce as the crystal growth proceeds (see Figure 1.18b). Under a large positive temperature gradient, the growth islands tend to incorporate BPDs to relieve the misfit strain due to the temperature gradient, and when the islands coalesce, the BPDs are rearranged and form networks at the grown-crystal/seed interface. The results obtained by Shioura et al. indicated that these BPD networks at the interface were accompanied by extra half-planes pointing toward the backside of the seed crystal and caused the (0001) basal plane to bend in a concave manner in the growth direction after the PVT growth process [39]. An important question here is how and why these BPD networks migrated into the seed crystal during PVT growth.

There are two possible mechanisms for the migration of the BPD networks into the seed crystal, namely, (i) the glide motion of BPDs on the basal plane and (ii) the climb motion of BPDs across the basal plane. To clarify the mechanism for BPD migration into the seed crystal during PVT growth, Shioura et al. conducted a masked PVT growth experiment on a 4° off-oriented $(000\bar{1})$ seed crystal [39]. The result is shown in Figure 1.20, where a reflection X-ray topograph for the diffraction condition $\boldsymbol{g} = 11\bar{2}\bar{8}$ acquired from the boundary area between the masked and unmasked regions of the seed crystal is shown. The masked region (right-hand side of the figure) was covered with a graphite plate during PVT growth to prevent

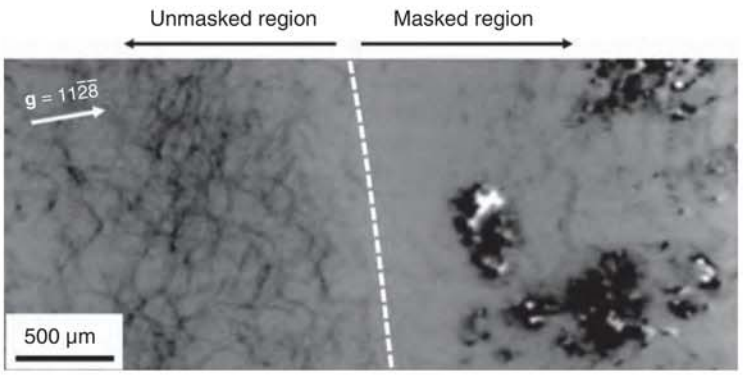


Figure 1.20 Enlarged reflection X-ray topograph for diffraction condition $\boldsymbol{g} = 11\bar{2}\bar{8}$ acquired from the boundary area between the masked and unmasked regions of the seed crystal; the 4H-SiC crystal was grown on the unmasked region (left-hand side of the dashed line in the topograph), whereas no crystal growth occurred on the masked region (right-hand side of the dashed line). The topograph shows clearly that the BPD networks in the seed crystal existed only in the unmasked region of the seed crystal. Source: Shioura et al. [39].

crystal growth. As shown in the figure, BPD networks exist only in the unmasked region and do not extend into the masked region. This result shows clearly that the observed BPD networks migrated into the seed crystal through the climb motion of dislocations, as schematically illustrated in Figure 1.21, rather than the glide motion. This is because, had the glide motion been the dominant mechanism for BPD migration, then the BPD networks formed during the initial stage of PVT growth should have glided on the basal plane into the masked region beyond the boundary between the unmasked and masked regions and then been observed in the masked region of the seed crystal after the crystal growth.

The climb motion of dislocations is driven by the injection, diffusion, and incorporation of intrinsic point defects, such as vacancies and interstitials, to the dislocations [47]. As described in Section 1.3.3, the observed BPD networks were accompanied by extra half-planes pointing toward the backside of the seed crystal, and thus, their migration toward the backside of the seed crystal requires vacancies to be incorporated in the dislocations as illustrated schematically in Figure 1.20. Given the migration depth of the BPD networks, it is clear that a large number of vacancies were injected during the initial stage of PVT growth. The mechanism for this remains unclear, but the poor dissipation of the latent heat in the initial stage of PVT growth (see Figure 1.18b,d) would cause local heating of the growing crystal surface, which may induce the injection of a large number of vacancies into the growing crystal.

1.4 Conclusions

SiC is a promising material for the next generation of power semiconductor devices, and the adoption of SiC power devices is critical for enabling faster, smaller, lighter,

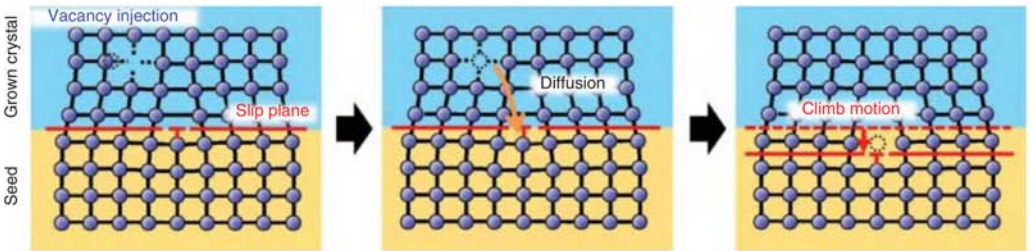


Figure 1.21 Schematic of the climb motion of a BPD toward the backside of the seed crystal due to the vacancy injection into the growing crystal during PVT growth. Source: Shioura et al. [39]. © 2019, Elsevier.

and more powerful power electronic systems. However, it is amply clear that such a successful adoption of SiC power devices for a wide range of power electronics systems relies considerably on establishing the manufacturing technology for large-diameter high-quality SiC single crystals. This chapter described recent progress in understanding the dislocation formation processes in PVT-grown SiC crystals, which is essential for obtaining high-quality SiC crystals.

After a brief introduction (Section 1.1), Section 1.2 was dedicated to understanding the BPD nucleation and multiplication processes during the PVT growth of 4H-SiC crystals. A large number of BPDs are introduced from the shoulder region of the growth front of 4H-SiC crystals, where a large thermoelastic shear stress is thought to be imposed during PVT growth. Detailed investigations of the BPD distribution in grown crystals suggest that BPDs nucleated at the shoulder region of a growing crystal largely determine the BPD distribution across the entire crystal.

In Section 1.3, the defect structure at the grown-crystal/seed interface of PVT-grown 4H-SiC crystals was investigated using 4H-SiC wafers with a beveled interface between the grown crystal and seed crystal. The existence of BPD networks at the grown-crystal/seed interface was revealed, and they extended considerably into the seed crystal. Such networks were likely to be caused by a large positive temperature gradient imposed on the growing crystal surface because of the local heating by the latent heat dissipation associated with the condensation of Si- and C-bearing species from the vapor during the initial stage of PVT growth. It was also revealed by masked-growth experiments that the migration of the BPD networks deep into the seed crystal was caused by the injection of a large number of vacancies during the initial stage of PVT growth of 4H-SiC crystals.

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Industrial Perspectives of SiC Bulk Growth

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2.1 Introduction

In this chapter, we discuss the inherent differences between growing SiC wafers for specialized high-end niche markets and the production of SiC wafers substrates for large-volume manufacturing. Both are critical in developing a robust commercial market. In the case of SiC, many academic and industrial players have contributed to the impressive ramp in quality and diameter that SiC wafers have experienced over the last 30 years. Figure 2.1 shows how the maximum diameter of SiC wafers has increased since the first commercial release in 1991 along with some of the critical milestones [1–4].

Currently, there are three primary markets for SiC wafers: (i) low-doped substrates for GaN light-emitting diode (LED) structures, (ii) high-doped substrates for high-power SiC device structures, and (iii) semi-insulating substrates for high-frequency GaN devices. In the following sections, we will discuss the commercial needs of each of these in turn. For each, we will address the key question of price vs. quality. For commercialization, it is important to remember that the perfect substrate is the one that meets all the customer needs at the lowest cost to produce. It is this balance between providing substrates that meet all customer requirements and are priced as low as possible that distinguishes industrial development from academic research.

2.2 SiC Substrates for GaN LEDs

The first high-volume usage of SiC substrates was driven by the release of high-brightness blue and green LEDs in the early 2000s by both Cree and Osram. This was the product that took the production of SiC substrates into true commercialization. GaN LEDs are fabricated on SiC substrates through heteroepitaxy. The unit cells and thermal expansion of SiC and GaN are not perfectly matched;

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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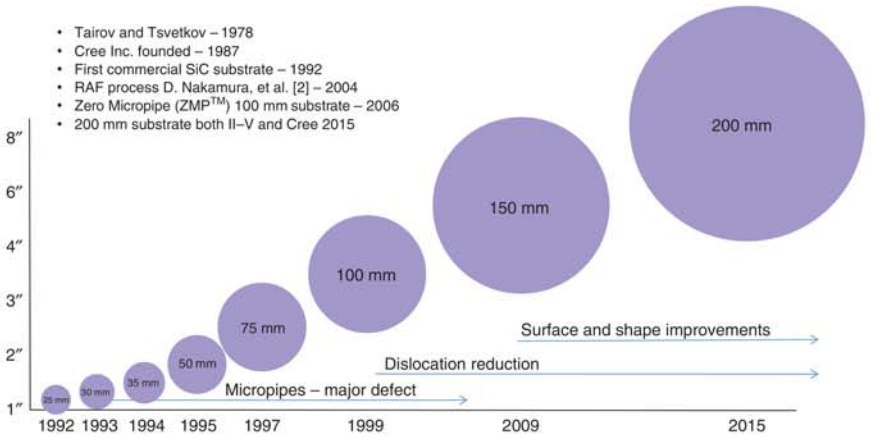


Figure 2.1 Progression of demonstrated single-crystal wafer diameter.

however, the match is superior to other available substrates (Si or Sapphire), and the nucleation of high-quality GaN layers can be achieved.

The primary factor that controls this nucleation is the offcut angle of the substrate. Thus, tight tolerances to <0.25° are required here, and any curvature of the lattice planes within the substrate must be avoided. However, even with optimal nucleation conditions, the interface between SiC and GaN introduces many, typically greater than $10^5\,cm^{-2}$ dislocations [5, 6], which are subsequently controlled by complex buffer structures in the GaN epitaxial growth. The consequence of this for the SiC substrate manufacturer is that dislocation densities in the substrates become non-critical at substrate values below $10^5\,cm^{-2}$. The final critical parameter for LED substrates is their optical characteristics. Many of the LED chip structures rely upon the generated light traveling through the substrate and therefore a transparent substrate is desired, this in turn defines a purity level required. In the case of SiC, the most problematic impurities are nitrogen, boron, and aluminum. Since all three of these are electrically active and cause absorption of the light emitted by the LED, in general the level of impurities in the substrates must be kept below $10^{17}\,cm^{-3}$. In the most recent decade, the ability to produce these LED diode structures on Sapphire substrates has improved, and so it is anticipated that further market growth of this segment will be static due to the lower price point of Sapphire substrates.

2.3 SiC Substrates for Power SiC Devices

LEDs allowed the first commercialization of SiC substrates; however, as we enter the next decade, it is expected that the volume of the power product will expand. In 2019, over 1 billion dollars of expansion was announced by various SiC substrate manufacturers mostly directed toward power device structures. SiC power devices include Schottky and MOSFET diodes. These devices are fabricated in SiC epitaxy grown directly on SiC substrates. For SiC epitaxy, the growth is carried out on

4° offcut surfaces, and this in turn reduces the requirement for very low lattice plane curvature. However, the quality requirements of the epitaxial SiC on SiC substrates are extremely high, and therefore, any defects in the substrate that thread into the epitaxy are a great concern. This leads to stringent limits on defect densities in the substrate with micropipes typically below 1 cm^{-2} and dislocations $<10^3$ cm^{-2}. Unlike LEDs, these device structures electrically connect through the substrate requiring highly doped, low resistivity material. Generally, nitrogen is the active dopant, and resistivity values are desired to be as low as possible (0.015–0.028 Ω-cm) so as to minimize device on resistance. It is known that a higher doping concentration leads to the occurrence of stacking fault defects in the active devices [7] and so this sets the minimum wafer resistivity.

2.4 SiC Substrates for High-Frequency Devices

High-frequency power devices are made from GaN on SiC; consequentially, the demands are similar to those of LED structures with the additional requirement that the substrate must not electrically couple to the active device. Thus, a very high resistivity substrate is desired. This can be achieved either through the addition of a deep level impurity such as vanadium [8] or by reducing the level of all impurities to a level less than 2×10^{-16} cm^{-3} [9]. Table 2.1 shows the key aspects of substrate quality that must be present to allow high-yielding stable device structures to be manufactured for all three product types.

2.5 Cost Considerations for Commercial Production of SiC

The basic wafer supplier question is "how to provide high quality wafers, at a minimal cost." For SiC, that means that the manufacturer must consider where the

Table 2.1 Indicating substrate characteristics beyond which significant final device yield hits might be expected[a].

Characteristic	LED (GaN on SiC)	Power (SiC on SiC)	High frequency (GaN on SiC)
Surface orientation	0.0 ± 0.25	4.0 ± 0.5	0.0 ± 0.25
Micropipe density	<5 cm^{-2}	<1 cm^{-2}	<1 cm^{-2}
Basal plane	$<10^5$ cm^{-2}	$<10^3$ cm^{-2}	$<10^5$ cm^{-2}
Threading screw	$<10^5$ cm^{-2}	$<10^3$ cm^{-2}	$<10^5$ cm^{-2}
Threading edge	$<10^5$ cm^{-2}	$<10^5$ cm^{-2}	$<10^5$ cm^{-2}
Resistivity	>0.2 Ω-cm	$0.015 < x < 0.03$ Ω-cm	$>10^5$ Ω-cm

a) Commercial specs are often set well inside these limits.

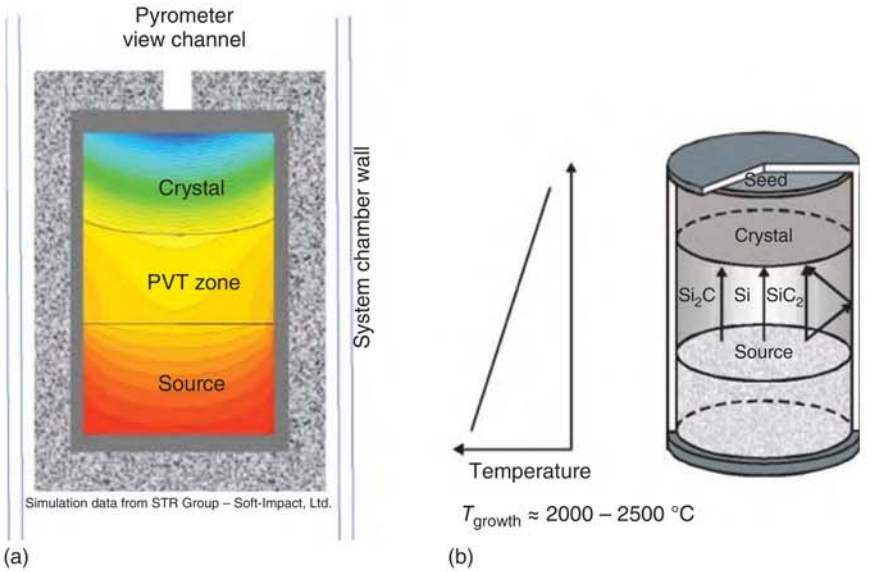


Figure 2.2 (a) Schematic of a SiC growth system, (b) schematic of gases present during growth. Source: Tairov and Tsvetkov [1].

main cost drivers are in the process and reduce them. Currently, in 2020, virtually all commercial SiC production utilizes the modified Lely technique, shown in Figure 2.2. Here, a seed wafer of SiC is placed at the top of the crucible and SiC source material placed at the base. The crucible is then heated to temperatures in excess of 2000 °C. The overall temperature is controlled by pyrometer feedback to the power supply, and the thermal field shape is controlled both by the positioning of the thermal insulation and by where the heat energy is coupled into the crucible. In a typical growth, both the absolute temperature and the axial thermal gradient are adjusted to maintain optimal thermal fields. As the seed/crystal region is kept cooler than the source region, the SiC sublimation gases sublime from the source and condense on the growing crystal.

From a cost point of view, we have several items to consider and these are outlined in Table 2.2.

2.6 Raw Materials

For modified Lely growth, one requires a seed of similar diameter to the final grown crystal. This of course has a cost similar to that of a completed SiC wafer. In this style of growth (unlike Si growth), there is no necking down of the crystal diameter, and therefore, any threading defects or misoriented regions in the seed wafer will be propagated into the growing crystal. This difficulty in producing crystals with significantly larger diameter than the seed used is one of the factors that has slowed the increase in SiC wafer diameter available to the commercial market. Two main approaches have been used for seed diameter expansion; the

Table 2.2 Cost considerations for SiC bulk growth.

Requirement	Subsystem	Cost is a function of
Raw materials	Seed, SiC source material	Part purity and efficiency of conversion to final crystal
Reactor hot zone	Graphite crucible, insulation	Part purity, part size, part lifetime
Equipment	Crystal growth system	Time required for growth process (turns per year)
Wafer manufacture	Wafering and polish	Equipment cost and throughput, slurry cost
Yield	Fraction of high-quality product per start	Bulk crystallographic defects, boule and processing machining errors, kerf loss, and wafer thickness

first is a gradual increase in crystal diameter, here the region of high-quality crystal is expanded, growth after growth, where the general orientation of the growth direction is in the "*c*" axis direction, an example of a 2″ to 2.75″ diameter expansion was shown by II-VI Inc. [10] (Figure 2.3a), and the second approach was pioneered by Denso Inc. [2] and termed "Repeated A Face" growth (Figure 2.3b). In this second approach, a crystal is first grown on the "*c*" axis direction; however, instead of slicing perpendicularly to the "*c*" axis, an orthogonal slice is taken perpendicular to the $(1\bar{1}00)$ plane, this slice is used as a seed to grow a second crystal in the $\langle 1\bar{1}00\rangle$ direction, from which an orthogonal slice is also taken, this time allowing growth in the $\langle 11\bar{2}0\rangle$ direction, again this slice is then used to grow a crystal and an orthogonal slice taken, this time the slice is perpendicular to the $\langle 000\bar{1}\rangle$ direction and it is suitable to be a seed for a conventional growth, and thus a high-quality *c*-axis seed boule can be produced. It should be noted that due to the challenges involved in creating high-quality seeds, many manufacturers place restrictions on their wafer sales, preventing the use of a commercially sold wafer as a seed substitute.

The other primary input is the source material; in the modified Lely process, this is SiC powder, and the key cost parameter here is what fraction of powder is transported to grow the crystal, rather than to create parasitic deposits elsewhere in the crucible, gas leakage out of the crucible, or simply residual source not consumed during growth.

2.7 Reactor Hot Zone

The modified Lely approach for SiC is unusual compared to other commercial crystal growth processes in that it operates at very high temperatures 2200–2400 °C [11, 12]. At these temperatures, there is a limited pallet of materials available that (i) withstand the temperature without decomposing and (ii) can be fabricated at high purity levels. The most commonly used material for both crucible and insulation is graphite. Figure 2.2a shows a typical reactor configuration for the hot zone showing

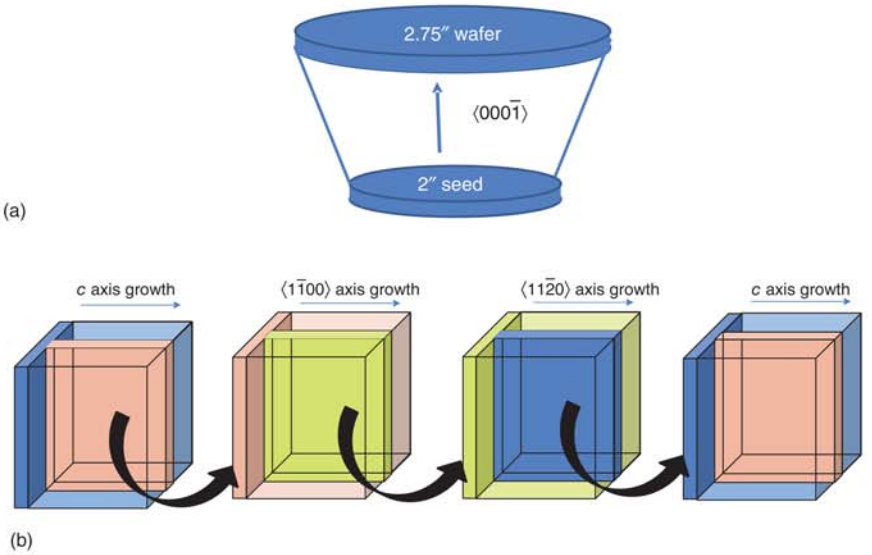


Figure 2.3 Two differing methods for expanding SiC seed: (a) schematic of gradual expansion and (b) schematic of repeated A-face growth (RAF) technique.

(i) crystal location, (ii) source location, (iii) crucible walls, (iv) insulation materials, and (v) reactor walls.

The challenge with graphite for the crucible build at these high growth temperatures, and in the presence of typical gases Si, Si_2C, and SiC_2, is that serious etching can occur on the inside walls of the crucible. It is key that the crucible remains whole for the entirety of the growth process. This etching behavior is enhanced at higher temperatures, again leading to a compromise choice between costs in terms of crucible parts lifetime vs. the savings achieved through increasing the growth rate by increasing growth temperatures.

Next out from the crucible is the insulation package that serves two major functions. The first of these is to keep the heat in the hot zone, to avoid high power consumption levels, without any insulation; the simple crucible shown in Figure 2.2a would need about 700 kW to maintain its temperature, this would not be financially viable. The second function is to allow control of the thermal profile within the growth crucible, by variation of the thickness and thermal properties of the insulating material surrounding that crucible. For example, it can be seen in Figure 2.2a that the gap in the insulation at the top of the crucible provides both a clear path for temperature control via a pyrometer and an exit route for energy in the crucible. This in turn locally cools the crystal directly below the "pyrometer view channel," thus providing a concave thermal field in the crystal region. Since SiC will deposit preferentially at the coolest location, this configuration would be expected to grow a convex SiC crystal as suggested by the schematic.

As one moves away from the hot zone, other more standard insulation materials become more viable, and the system design tends toward more standard low-pressure grower designs.

2.8 System Equipment

Many SiC wafer vendors keep their reactor geometry proprietary, though some early images are available [13]; in addition, there are currently several commercial vendors of SiC furnaces. However, whatever the source of the reactor, the cost of ownership is high and the factory floor space requirement is substantial. As an example, consider a published growth rate of 0.1 mm/h [14]. Assuming very effective reactor turn around, one might then grow 800 mm of crystal in a year from this grower. If one then assumes a US$ 1 million grower cost, a five-year depreciation, and excellent yields, a typical wafer slice would have a contributory cost of over US$ 200 from the grower equipment alone. This high cost drives the desire to increase the SiC growth rate. However, as the growth rate is pushed up, there is a tradeoff between high growth rates and induced crystalline defects. This will be discussed in the following section.

2.9 Yield

Left till last, but as in all processes, the yield is of immense importance. The cost of growing a defective crystal is the same as that of growing a high-quality crystal, so we must ensure that our growth process creates few defective crystals. Unfortunately, the need to produce a high-growth-rate, long-length crystal from a low-cost starting set of raw materials is often in direct competition to growing low defectivity crystals. The science of production is to create the optimal balance between these competing factors. Figure 2.4 shows many of the defects associated with the growth of SiC boules. Some of these have been well characterized by the scientific community and the mechanisms of their formation well understood. However, the nucleation mechanisms of others are still not fully explained, and much exciting work remains in the field to identify root causes and optimal ways to prevent the defect formation in standard growths.

The creation of a new product or process requires several stages – each with a unique focus. Originating in research phase, where researchers champion the few excellent crystals to highlight where the process can go, the process typically moves through to early production where the focus changes to how to increase the total number of passing wafers, i.e. yield enhancement. From there, the process typically moves on to full production, where reducing process cost is of primary concern. For SiC, this yield and cost improvement is generally split into three categories: (i) Reduction of total failures: typical causes of these are equipment failure and nucleation of differing polytypes and orientations near the start of growth (Figure 2.4a,d,f). (ii) Reduction of mid boule fails: typical causes are incorporation of particles and local switching of polytype (Figure 2.4c,e). (iii) Finally, overall tightening of slicing and surface finish processes help to boost the yield to acceptable levels.

As the understanding of how the input materials, and process variables, effect the different fail modes, the overall process yield can be continually increased whilst simultaneously allowing some loosening of non-key input specifications to allow for lower cost inputs.

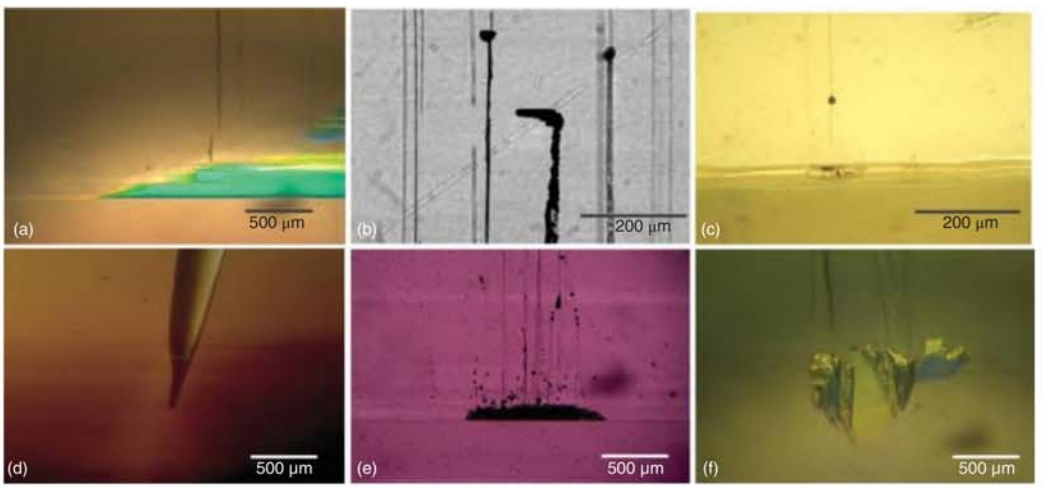


Figure 2.4 Images of six defect modes that are commonly observed in SiC growth, in all cases the growth direction is upward. (a) Polytype switch from 4H, to 6H, 15R, and back, (b) large voids migrating through the crystal, (c) defect inclusion generating a small tear-shaped void, (d) initiation point of an inclusion of different orientation of SiC, (e) large growth disruption introducing many pipes and dislocations, (f) 3C inclusion, here some of the side facets of the 3C inclusion are clearly visible with the center region showing a characteristic yellow color.

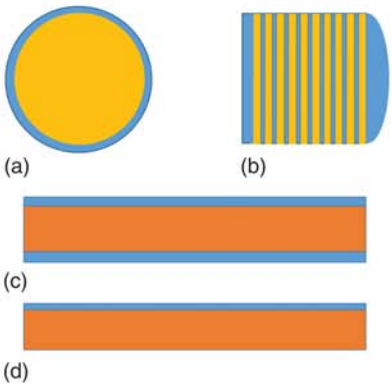


Figure 2.5 Schematic illustrating overall kerf loss for wafer manufacture processes, (a) OD grind loss from outer perimeter, (b) saw loss, (c) loss in double side polish, and (d) loss in final single side CMP.

2.10 Turning Boules into Wafers

Once a SiC boule has been grown, it must then be converted into high-quality wafers. For SiC, there are challenges here due to its high hardness value of 9.4 Mohs and general chemical inertness. The general process is as follows:

(a) Grind the crystal down to the desired diameter
(b) Slice this boule into wafers
(c) Mark the wafers with identification, orientation flats, and appropriate edge shape
(d) Rough polish the wafers
(e) Final chemical mechanical polish (CMP) step
(f) Characterize and supply to customer

From a cost point of view, it is worth considering that each processing step removes SiC crystal and thus represents a kerf loss. Typical kerf loss mechanisms and values are shown in Figure 2.5: Outer diameter (OD) grind 3–10%, seed and dome removal 1–5%, wafer slicing 30–40%, rough double side polish 10–20%, and final CMP <1%. Together, these can easily represent more than half of the grown crystal mass. Kerf loss has a critical role to play in the final cost of SiC wafer product and is particularly hurtful to crystal growers, as it represents the loss of high-quality material to the shaping operations. Much development work has gone into improving processing techniques to reduce overall kerf losses and increase the yield of these processes.

2.11 Crystal Grind

This is a fairly typical process for bulk crystal processing, where the SiC crystal is rotated and brought into proximity with a high-speed diamond grind wheel. The diamond cutting teeth on the wheel will then locally scrape away the SiC crystal material; however, SiC is unusual in that for most crystal materials, the local heating caused by the cutting diamond tooth causes the crystal to exceed the ductile to brittle transition temperature. Thus, the material removal is conducted in the

ductile domain where cracking is eliminated. For SiC, since the ductile to brittle transformation is high [15], the grind operation is generally in the brittle domain, and consequently, cracks are initiated at the outer grind surface. Care must be taken to ensure that these cracks do not propagate deeply into the crystal. In practice, to minimize this crack depth, a low grind rate is used, and the final outer edge of the crystal is effectively cleaned up later in the wafer edge grind and polish steps.

2.12 Wafer Slicing

Wafer slicing is where the thickness, orientation, and much of the final wafer shape are determined. Over the past two decades, multi-wire slicing has become the dominant process for slicing boules (http://www.takatori-g.co.jp/english). In multi-wire slicing, a thin steel wire is coated with a diamond slurry, and this wire is pulled backward and forward across the SiC surface at a speed up to 10 m/s. The process is essentially a lapping process directly between the wire and the SiC surface, with the diamond slurry providing the abrasive material and the wire acting to provide both the downforce and the lateral velocity to the diamond particles. This process creates a trench at each wire location that gradually becomes deeper as the operation continues. This operation is inherently slow since the removal rate for the lapping process is roughly 5 mm/h. Thus, many hours are needed to cut through a 150-mm-diameter boule. To effectively speed up this process, the wire is wrapped around rollers such that a wire web is created with several hundred parallel wires; consequentially, although the slicing process itself is slow, the ability to cut several hundred slices concurrently alleviates this (Figure 2.6).

While this slicing process is simple in concept, many parameters such as wire tension, wire speed, diamond slurry composition, downforce applied to the wire, and wire diameter must be tightly controlled to cut the crystal successfully without imparting excessive shape into the sliced wafers. One further consideration is the need to maintain a stable cutting zone. Effects such as differential temperatures or nonoptimal thermal expansion loops will tend to cause the wires to move sideways during the cut which will often cause displacement of wires w.r.t. the crystal and poor wafer shape particularly at the start and end of a cut where the rapidly changing cut length makes it more difficult to hold slicing conditions stable.

In addition to wafer shape induced by the saw, there is additional shape induced due to both residual stress in the grown crystal and due to differential damage depths on the Si face vs. the C face of the wafers. This tends to impart a radially symmetric shape into the wafer. Figure 2.7 shows how the shape of 150 mm wafers have been improved through the optimization of growth and slicing processes.

There is interest in other slicing techniques predominantly due to the potential of lower kerf loss. These include laser splitting [16], electrical discharge machining (EDM) [17] slicing, and diamond impregnated wire slicing.

Laser splitting utilizes a high-power laser to locally heat a region of the crystal beneath the surface, and this thermal expansion in turn creates microcracks that are predominantly in the basal plane direction. Through careful control, this heating

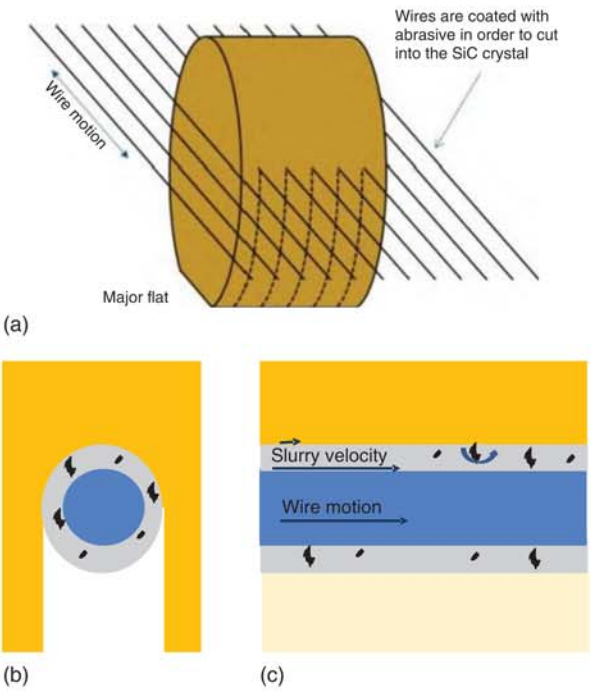


Figure 2.6 Schematic showing modern wire saw configuration: (a) configuration of boule with respect to wire web, (b) cross section of wire coated in slurry cutting crystal, (c) lateral cross section showing slurry velocity causing a rolling motion in the diamond particles. Note for many commercial saws, the wire cuts upward into the crystal as shown in the figure.

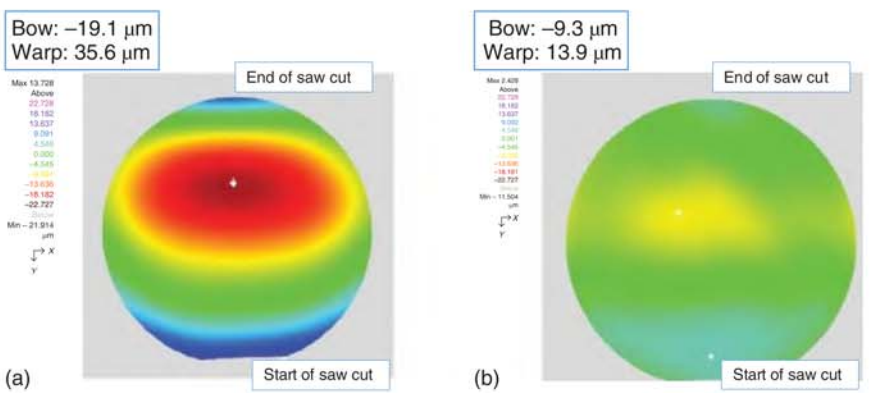


Figure 2.7 (a) A 150 mm wafer shape obtained from an unoptimized cut, (b) 150 mm wafer shape obtained once slicing parameters are optimized.

can be maintained within a very tight depth window from the surface of the boule, and thereby, as this laser is scanned across the wafer, a "sheet of cracks" can be produced. It then becomes possible to peel or pull this top wafer from the boule. This technique could in principle reduce kerf loss to below 50 μm and is only limited by the accuracy of the optical system controlling the depth of penetration and the degree of localization of the cracking behavior.

EDM slicing is similar to wire slicing except that in this case a high voltage in the wire is used to strike a plasma between the wire and the crystal. This plasma in turn

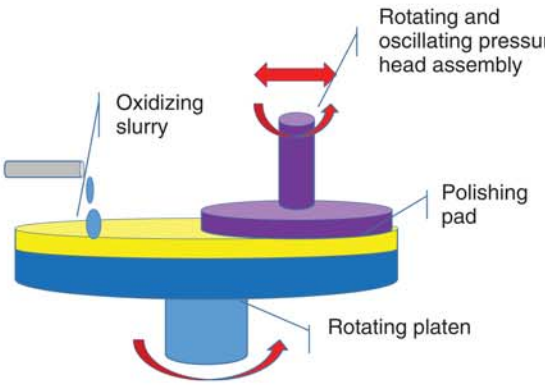


Figure 2.8 Schematic of a CMP process.

etches the crystal to create the slicing operation. Since the wire is not being required to both carry slurry and provide the downforce, it may be possible to reduce wire diameter significantly and therefore reduce material kerf loss.

Diamond impregnated wire slicing, as oppose to diamond slurry wire slicing, is gaining in popularity due to the potential of reduced wire tension, and thus the reduced diameter wire required, thereby producing reduced kerf loss. As the name implies, this technique is very similar to typical wire slicing, except that the abrasive (diamond) is actually bonded to the wire before the cutting operation.

2.13 Wafer Polish

Once the crystals have been sliced into wafers, the processing becomes similar to that of other semiconductors in that a series of surface finishing steps are used that typically consist of polishing with successive steps of abrasive material reducing the abrasive diameter with each step (diamond for SiC wafers). This type of removal will always leave a damaged sublayer in the wafer whose depth is proportional to the abrasive size. Consequentially, the final finish is provided by a CMP step, Figure 2.8, where an oxidizer is combined with a soft abrasive. The oxidizer converts the surface layer of SiC to SiO_2, and this oxide layer is then removed by the soft abrasive. Fortunately, the soft abrasive is not aggressive enough to scratch SiC, and so a high-quality surface can be achieved.

2.14 Summary

Over the last 30 years, SiC materials growth has developed into a mature industry with multiple manufacturers of high-quality wafers who have supplied millions of wafers to the market. This industry has also increased the diameter of these wafers from 25 mm up to as large as 200 mm representing an almost two-order-of-magnitude increase in surface area available for device manufacture on each wafer. Simultaneously, these manufactures have increased the wafer quality

to enable the creation of large power devices of 1 cm^2 area and above. It is expected that over the next decade the SiC will blossom into a very significant industry, with many commercial players and significant impact on future technology.

Acknowledgments

One of the key aspects to consider when transitioning from a research environment to a development and production process is that the entire effort relies upon the skills and expertise of a large group of individuals. For this work, I am immensely grateful to the entire Cree/Wolfspeed materials team and feel that the role I played here should be considered as a scribe outlining aspects of the process that takes an R&D development and creates a commercial product out of it.

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3

Homoepitaxial Growth of 4H-SiC on Vicinal Substrates

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3.1 Introduction

Many review papers [1–3] and text books, e.g. [4, 5]), have been published over the decades on SiC epitaxial growth and defect characterization. These publications are mirroring the great advance that has been made with regard to structural quality of substrate and epitaxial layer, epitaxial growth process, and scientific insights. This technological progress brought the focusing on *4H-SiC polytype* by *step-flow growth mode* on vicinal substrates with a specified off-cut using a *CVD process* for *SiC power electronic applications*. Still, there are ongoing activities worldwide for epitaxial growth of 3C-SiC on the silicon substrate for other applications than power electronics and solution growth of 4H-SiC, which promises an even better structural quality of the epilayer and deeper scientific insights into SiC growth in general. However, this paper is dealing with 4H-SiC homoepitaxial growth for power applications only.

This chapter about epigrowth and carrier lifetime is written for new comers in the SiC technology, draws a bow across the basic relations, and explains basic knowledge and the current state of the art. For the very details of epigrowth, readers are referred to the very comprehensive review on the SiC epitaxial process in the textbook edited by Kimoto and Cooper [5].

It summarizes briefly the fundamentals of 4H-SiC homoepitaxial growth and then focuses on the very important topics of extended defects (mainly dislocations and stacking faults) and point defects in epilayers – their origin, properties, and strategies for avoidance.

3.2 Fundamentals of 4H-SiC Homoepitaxy for Power Electronic Devices

The production of today's power electronic devices demands for an 4H-SiC epilayer (stack) with specified doping concentrations and thicknesses, excellent doping and

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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thickness homogeneities, and (ideally) freedom of any defects grown on the Si-face of a low-resistive/highly doped 4H-SiC substrate. These aspects will be explained in the following, except the doping and thickness homogeneity, which is described in the book chapter "Industrial Perspective of SiC Epitaxy" from Al Burk.

3.2.1 4H-SiC Polytype Replication for Homoepitaxial Growth on Vicinal Substrates

Silicon carbide is famous for existing in various crystallographic structures with the same stoichiometry of 50 at % Si and 50 at % C, called polytypes. Under typical epitaxial growth conditions (see later in the chapter for more details), polycrystalline epilayers of 3C-SiC polytype are forming on on-axis, c-plane 4H-SiC substrates, which is an undesired heteroepitaxial growth and useless for power electronic devices. In the 1990s, Kimoto and Matsunami transferred the concept of step-flow growth mode by using vicinal (off-cut) substrates [1, 6] from other semiconductors to SiC epitaxial growth – and succeeded in a proper polytype replication from the 4H-SiC substrate to the 4H-SiC epilayer and a much more robust epitaxial growth process at lower temperatures. Initially, they used 8° off-cut substrates and got very smooth epilayers consisting mainly of micro steps with $c/4$ step height (c: unit cell height of 4H-SiC, $c = 1.008$ nm). As the substrates became larger in diameter and reached 3 inch diameter in 2005, the off-cut angle was reduced from 8° to 4° because of severe cost aspects in cutting out "large" tilted substrates from short on-axis grown crystals. This technological change brought drawbacks such as higher defect densities (especially stacking faults, carrots, and comets) and higher epilayer surface roughness (especially on the Si-face) due to intensified step bunching. Today, rough epilayers can be smoothened by post-epi chemo-mechanical polishing (CMP) processes, but the defect densities are still an important issue. On the other hand, the density of so-called basal-plane dislocations (BPDs) in the epilayer has been reduced dramatically by reducing the off-cut angle from 8° to 4° due to image force effects [7, 8], which is of much greater technological importance than the increased surface roughness and higher densities of other defects. The attention in epigrowth process development shifted to BPDs at that time as they were identified being the root cause of the so-called bipolar degradation, which was feared as showstopper of any bipolar SiC power electronic device including the body diode of SiC metal oxide semiconductor field-effect transistors (MOSFETs) and therefore SiC power electronic devices with blocking voltages larger than 3 kV. BPDs in the epilayer can be eliminated by using substrates with even smaller off-cut angle (such as 2° or less [7, 9]). Vicinal SiC substrates are usually off-oriented towards $[11\bar{2}0]$ direction (see Figure 3.1), other off-cut directions, e.g. the $[1\bar{1}00]$ direction, influence the step morphology and surface roughness [1, 10–12], but are not of technological relevance today.

Proper polytype reproduction from the 4H-SiC substrate to the growing epilayer is achieved by maintaining step-flow growth mode. This in turns means that the supersaturation on the growth terraces is kept in a reasonable range to avoid 2D seeding. The basic processes for stable step-flow growth have been described in a

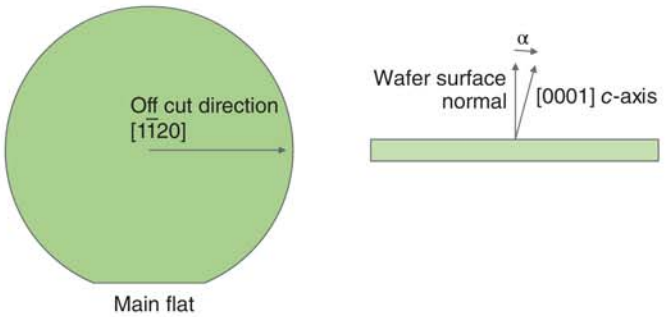


Figure 3.1 Schematic drawing of off-cut angle α and off-cut direction on a vicinal 4H-SiC wafer relative to main flat. The off-cut direction coincides with the resulting step-flow direction during step-controlled epigrowth.

general perspective by Burton, Cabrera, and Frank (BCF model, [13]), and this BCF model has been applied to SiC epitaxy by Matsunami and Kimoto [1].

During epitaxial growth, several reactions and processes are taking place simultaneously as briefly summarized in Figure 3.2: the precursor molecules (e.g. silane SiH_4 and propane C_3H_8) are transported in the reactor to the growth zone by carrier gas (typically hydrogen [H_2]) and start cracking to reactive species (Si and C atoms) as they reach the hot zone of the reactor. Side reactions can take place such as the condensation of Si atoms to dimers or small clusters, which is undesired as it reduces both the growth rate and the layer quality. Then, reactive Si and C atoms are adsorbed on the growth surface, diffuse on the terraces for a certain while or distance λ, and then incorporate at the step edge, nucleate 3C-SiC growth islands, or desorb from the growth surface. To find a suitable incorporation site, it is typically assumed that the actual diffusion length λ needs to be at least half of the terrace width ($w/2$). The terrace width w is a simple function of the off-cut angle α of the substrate and the step height h:

$$\tan \alpha = \frac{w}{h} \tag{3.1}$$

The diffusion length λ has a more complex dependence, e.g. on growth temperature, concentration of species on the terrace, chemical reactions, and ambient. If the concentrations of reactive species (either only Si atoms or both Si and C atoms) exceed a critical limit, Si droplets or SiC islands nucleate on the terraces; both are destroying the proper step-flow growth mode and degrade the epilayer quality dramatically. To avoid such nucleation on the growth terrace, either the supply with reactive species can be reduced (e.g. precursor and/or carrier gas flows, process pressure) or the growth temperature can be increased as higher temperature forces desorption of adatoms from the surface. All these basic reactions and processes have their specific temperature dependence; hence, the growth temperature is a key parameter in the growth process.

Based on the growth temperature, three different growth regimes can be determined: at low growth temperatures <1500 °C for 4H-SiC growth, the growth rate is kinetically limited. That means the precursor molecules provided in the process cannot be thermally decomposed completely as the temperature is too low and the

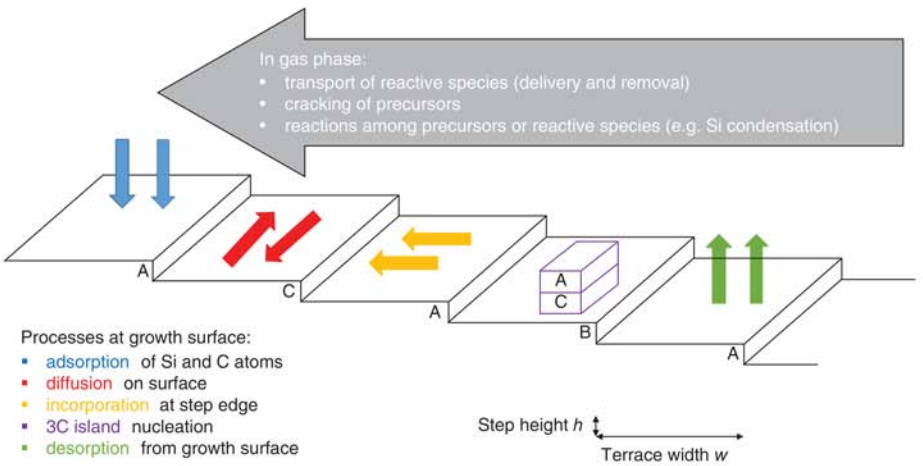


Figure 3.2 Sketch of the BCF theory for 4H-SiC homoepitaxy on the vicinal surface.

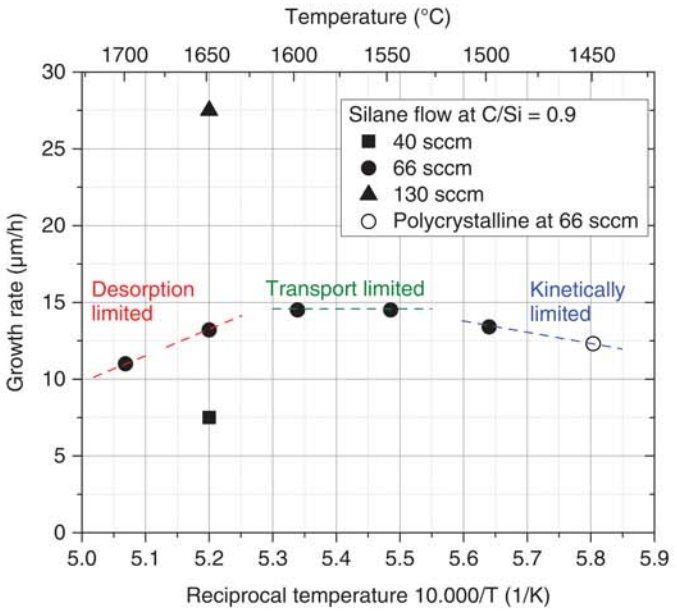


Figure 3.3 Epitaxial growth rate vs. reciprocal growth temperature showing different growth regimes. Polycrystalline growth occurs at very low growth temperatures below 1500 °C. Higher precursor gas flows lead to higher growth rates.

precursors are not used efficiently. As the precursor cracking becomes more efficient with increasing growth temperature, the growth rate is increasing accordingly in the kinetically limited growth regime. In a temperature window from 1500 to 1650 °C, the growth rate is transport limited. That means all precursor molecules can be cracked and contribute to the epilayer growth. Therefore, the growth rate increases proportionally to the supply of precursors (up to a certain limit at which step-flow growth turns into polycrystalline growth, see above), but is constant (for a certain precursor supply) within this temperature range. This is the desired growth regime for exact control of the growth rate and hence, the epilayer thickness. At even higher temperatures, adatoms leave the growth surface faster than they can be incorporated – or in other words: thermal back-etching competes with epilayer deposition. Therefore, the growth rate drops with increasing growth temperature within the desorption-limited growth regime (Figure 3.3).

These basics have several implications and consequences for the design of the growth step:

- Growth steps need to be present at the Si-face of the polished wafer from the very beginning of the growth phase: suitable back-etching of the off-cut substrate is required already during heat up/before growth starts.
- Growth on substrates with small off-cut angles (e.g. 4° instead of 8°): As can be seen from Eq. (3.1), the terrace width increases with decreasing off-cut angle; hence, the diffusion length of adatoms needs to become larger for smaller off-cut angles such as 4° or even 2°. That means, in turn, for growth on 4° off-cut

substrates, either the growth temperature needs to be set higher and/or the concentration of reactive species (and hence, the growth rate) has to be reduced in comparison to growth on 8° off-cut substrates.

- For step-flow growth in the transport-limited growth regime, the maximum growth rate depends on the onset of Si droplet and/or SiC island nucleation on the growth terraces, which in turn depends on the critical Si concentration. To push the maximum growth rate and hence, the maximum Si concentration to larger values, either the process pressure can be reduced and/or chloride species can be added, e.g. in terms of hydrogen chloride (HCl) or trichlorosilane (TCS, $SiHCl_3$) [14]. Chloride atoms can bond even stronger to Si atoms than other Si atoms and release the Si atoms at the surface again; therefore, higher Si concentrations become tolerable without Si condensation.

The use of vicinal substrates in epitaxial growth has several implications on the epitaxial growth process:

- step-flow growth mode needs reasonable supersaturation on terraces, realized by balancing growth temperature and precursor supply for a given terrace width or off-cut angle;
- basal planes are intersecting the growth surface, and hence, defects on the basal plane are "transferrable" from substrate to epilayer.

3.2.2 Homoepitaxial Growth by Chemical Vapor Deposition (CVD) Process

Based on the scientific understanding as briefly summarized in the previous section (3.2.1), a typical SiC epitaxial growth process should follow this general setup:

1. Wafer loading and conditioning of the reactor: the wafer is loaded (either manually or automated) into the reactor, and the reactor is evacuated to remove oxygen, nitrogen, and moisture residuals for low doping background and safety reasons. The wafers need to be handled carefully to avoid any scratches/damage/contamination on the wafer surface and to avoid particle generation from the sidewalls of the reactor.
2. The reactor is purged with carrier gas, typically high-purity (> 6N) hydrogen (H_2), and starts heating up toward growth temperature.
3. During heating up in hydrogen-containing atmosphere, back-etching is taking place, which transforms the polished and smooth surface to a stepped surface and removes surface contaminations and native oxide. Back-etching can be tuned by adding C-containing precursors with regard to surface morphology (occurrence of pits and defects) and the back-etching rate [15, 16]. Depending on the reactor type, the growth process, and the substrates used, a dedicated process step for back-etching is used at growth temperature or slightly lower temperature with a specific growth atmosphere.
4. Growth step: Si- and C-precursors (e.g. silane (SiH_4), propane (C_3H_8), trichlorosilane ($SiHCl_3$)) are introduced as well as dopants (N_2 for n-type doping with nitrogen, trimethylaluminum (TMA) for p-type doping with aluminium) and

any additional species such as chlorine (HCl, Cl_2, and TCS), under large carrier gas flow (typically > 99% of total gas flow). Epilayer stacks are grown by adapting the dopant gas flow and/or the mixture of Si- and C-precursors.

5. Cooling down: typically in H_2-containing atmosphere. Back-etching and condensation/crystallization of excess Si species may occur and can degrade the surface quality (e.g. pit formation and Si droplets) of the grown epilayer. Therefore, rapid cooling until $T < 1400\,°C$ and fast removal of reactive species from the growth front are favored.
6. Wafer unload and reactor maintenance (if needed after a certain accumulated growth thickness due to parasitic Si–C compound growth on reactor components).

Growth processes are usually characterized by growth temperature and important gas-mixing ratios, such as Si concentration in carrier gas (SiH_4/H_2) and the precursor-mixing ratio ("C/Si", i.e. 1/3 C_3H_8/SiH_4), relevant for supersaturation/growth mode, growth rate, and defects, and incorporation of dopants (see below). These gas-mixing ratios are calculated for cold gases at the reactor inlet/in gas-mixing cabinet. The true gas-mixing ratios, or better concentration profiles for reactive species (elements), can only be accessed by numerical simulation of each reactor and process (needs temperature distribution, gas flows, process pressure, chemical reactions, and growth model) [14]. The process pressure is also of great importance as it distinguishes between turbulent and laminar gas flow, determines the decomposition of gaseous precursors according to the mass action law, and enters directly in the calculations of the species' partial pressures.

3.2.3 Doping in Homoepitaxial Growth

Today, 4H-SiC is doped with nitrogen (N) and aluminum (Al) atoms for n-type and p-type doping, respectively. These elements have acceptable ionization energies and are technologically well controllable. As can be easily seen from the covalent radii given in Table 3.1 for the elements, N has a similar size as C and is incorporated on the C site, analogously Al on the Si site. Therefore, N competes with C about the lattice site and Al with Si. This so-called site-competition effect [18] can be used in epitaxial growth to either suppress or promote the incorporation of dopant atoms to

Table 3.1 Properties of silicon (Si) and carbon (C) host atoms and nitrogen (N) and aluminum (Al) doping atoms.

Element	Function	Covalent radius [17] (pm)	(preferred) Incorporation site	Ionization energy
C	Host atom	77		n.a.
N	Donor	70	On C site	35–100 meV
Al	Acceptor	125	On Si site	190–240 meV
Si	Host atom	117	—	n.a.

the growing layer – simply by providing more or less C- or Si-precursor in the growth step. Suppressing the incorporation of a dopant means that the doping background can be kept very low and promoting can help to grow highly doped epilayers.

Moreover, Al has a so-called memory effect. Once a highly Al-doped epilayer was grown in the epi reactor, Al remains in the parasitic SiC deposition on the reactor parts and emits continuously Al atoms during the subsequent growth processes. Consequently, the Al doping concentration in the subsequent growth runs is higher than that expected from the relevant gas-mixing ratios (Al/Si, C/Si). This memory effect can be reduced or suppressed by mechanical cleaning of the reactor parts and deposition of undoped SiC – or by a chemical cleaning process with chloride-containing precursors at elevated temperatures, such as HCl etching. Some (older) reactor types provide dedicated chambers for n- and p-type doping, but – in combination with cleaning of reactor parts – it can be sufficient to use dedicated n- or p-type reactor kits for the growth chamber.

As mentioned at the beginning of the chapter, SiC homoepitaxial layers are grown on low-resistive, highly N-doped 4H-SiC substrates. Nitrogen doping leads – as the covalent radius of N is smaller than that of C [17, 19] – to a contraction of the SiC unit cell. High N dopant concentrations (as for substrates) lead to a stronger contraction of the unit cell than moderate or low N concentrations (as for epilayers). Therefore, highly N-doped SiC substrates have the smallest unit cell (volume), followed by moderate or low N-doped epilayers. Contrarily, Al incorporation leads to a dilation of the SiC unit cell as Al has the larger covalent radius than the substituted Si atom [17, 19]. Additional size effects might occur due to electronic effects [20], but they seem to be negligible compared to the atomic size effect for 4H-SiC. The unit cell volume V follows the general doping rule:

$$V_{\text{highly N-doped}} < V_{\text{moderate N-doped}} < V_{\text{undoped}} < V_{\text{moderate Al-doped}} < V_{\text{highly Al-doped}}$$

Several working groups worldwide have been already dealing with doping-induced crystal lattice misfit. It is challenging to measure and determine the small values of doping-induced misfit, and classical as well as innovative attempts have been made: reciprocal space maps obtained by high-resolution X-ray diffraction and high-precision lattice constant determination [20–22], wafer bow measurements on epilayers grown on thin substrates [19], and theoretical models [21, 23]. The reported misfit values are summarized in Figure 3.4.

Therefore, any combination of highly N-doped substrate and epilayer with different N or Al doping concentration has different lattice constants and hence, a doping-induced lattice misfit. Of course, the misfit is very small in the order of 10^{-5} to 10^{-6} (especially if compared to heteroepitaxy), but relatively thick epilayer (stacks) is grown in the SiC technology: 10 µm epilayer thickness on 350 µm substrate (thickness ratio 1 : 35 for 1200 V devices) up to 65 µm epilayer on 350 µm substrate (~1 : 5 for 6.5 kV devices). For simple comparison, in GaN-on-Si heteroepitaxy, a <5 µm thick GaN layer is grown on a stress management layer stack on a 750 µm thick Si substrate (1 : 150). Therefore, wafer bowing occurs in

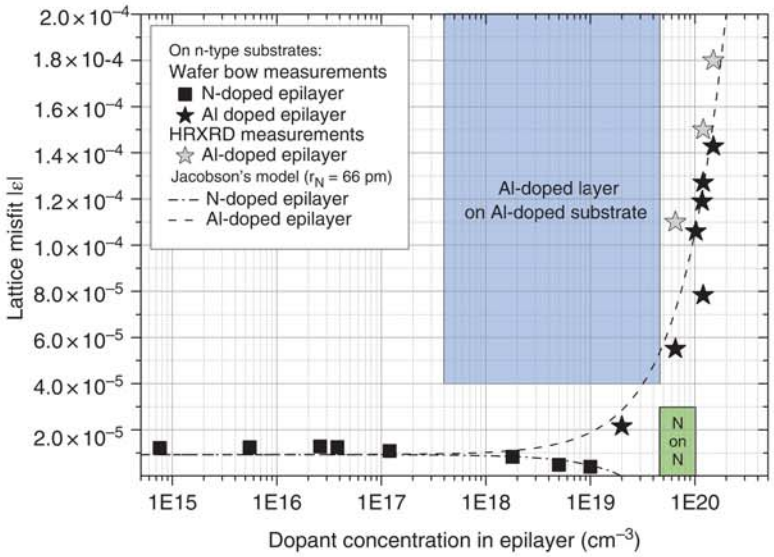


Figure 3.4 Summary of reported doping-induced misfit values as a function of epilayer doping concentration. Misfit data for N- and Al-doped epilayers grown on N-doped substrates taken from [19, 21] and for Al-doped epilayers grown on Al-doped substrates from [22].

4H-SiC homoepitaxial growth, but even misfit dislocation generation is possible for large misfits (abrupt doping gradients) in combination with thick layers. It can be shown that – in case of misfit dislocation generation – BPDs are generated as they have the appropriate configuration (line direction, Burgers vector direction) to reduce the strain energy at the substrate–epilayer interface (if critical shear stress at the respective epi growth temperature is exceeded). The classical models about the onset of misfit dislocation generation by Matthews–Blakeslee [24, 25] and People–Bean [26] predict different critical values for the epilayer thickness/doping difference and need to be adapted and reproven.

3.3 Extended Defects in Homoepitaxial Layers

This section deals with extended defects in the 4H-SiC substrate and homoepitaxially grown material, i.e. dislocations, stacking faults, and complexes thereof. These types of defects range from microscopic to macroscopic level and are relevant for device performance and device production yield. First, extended defects are classified, i.e. which defect types can occur in the hexagonal lattice of 4H-SiC, followed by an introduction which defect types do occur under real conditions. Their origins will be discussed as well as their behavior during homoepitaxial growth because these two factors often determine the actual morphology of the defects. Finally, common characterization techniques for extended defects in epilayers are briefly introduced.

3.3.1 Classification of Extended Defects According to Glide Systems in 4H-SiC

Dislocations have a specific Burgers ($\vec{b}$) and line ($\vec{l}$) vector, which represent the distance and direction of displacement ($\vec{b}$) and the orientation ($\vec{l}$) of the actual disturbance, respectively. Due to energetic reasons, the Burgers vector needs to be a closely packed direction and the glide plane (which contains the line vector) a closely packed plane. Hence, discrete glide systems occur in crystal structures, and dislocations cannot form with "random" configuration. From a theoretical perspective [27], six different glide systems are possible in a hexagonal lattice (with stacking sequence AB). These glide systems need to be adapted to the actual stacking sequence ABAC of 4H-SiC, resulting in the six independent glide systems as summarized in Table 3.2.

Table 3.2 Glide systems in hexagonal lattice (as given in textbook from Hull and Bacon [27] for stacking sequence AB) adapted to the 4H stacking sequence of 4H-SiC. BPD, basal-plane dislocation; TED, threading edge dislocation; TSD, threading screw dislocation; TMD, threading mixed dislocation.

Type	a	c	$\sqrt{c^2+a^2}$	$a/\sqrt{3}$	$c/4$	$\sqrt{\frac{a^2}{3}+\frac{c^2}{16}}$
$\vec{b}$	$\frac{1}{3}\langle 11\bar{2}0\rangle$	$\langle 0001\rangle$	$\frac{1}{3}\langle 11\bar{2}3\rangle$	$\frac{1}{3}\langle 1\bar{1}00\rangle$	$\frac{1}{4}\langle 0001\rangle$	$\frac{1}{6}\langle\bar{2}203\rangle$
$\|b\|$	0.308 nm	1.008 nm	1.054 nm	0.178 nm	0.252 nm	0.308 nm
Glide plane	(0001) $\{1\bar{1}00\}$ $\{1\bar{1}01\}$	$\{1\bar{1}00\}$	$\{1\bar{1}00\}$ $\{\bar{2}112\}$	(0001)	$\{1\bar{1}00\}$	$\{\bar{2}112\}$
Examples	BPD, TED	TSD, MP	TMD	Shockley partial	Frank partial	

There are two closely packed directions and hence, Burgers vectors, in the hexagonal lattice, called a and c, and their combination $\sqrt{c^2+a^2}$. Additionally, partial dislocations can occur with Burgers vectors of types $a/\sqrt{3}$ and $c/4$ and their combination $\sqrt{\frac{a^2}{3}+\frac{c^2}{16}}$. Partial dislocations always surround stacking faults, i.e. planar defects.

Dislocations with a-type Burgers vector have prominent representatives such as the before-mentioned BPDs and threading edge dislocations (TEDs). BPDs are lying on the basal plane (0001) and can occur in edge, screw, or mixed configuration. TEDs have a distinct line direction of [0001]; hence, they are in edge configuration, and their line vector is part of the prismatic m-plane $\{1\bar{1}00\}$. Dislocations with c-type Burgers vector mainly occur with the dislocation line along [0001] direction, i.e. they are in screw configuration and called threading screw dislocation (TSD). Threading mixed dislocations (TMDs), i.e. with line direction [0001] but mixed $(a+c)$-Burgers vector, have been reported recently [28, 29], but occur quite seldom.

Shockley partial dislocations with a Burgers vector of type $\vec{b}=a/\sqrt{3}$ always surround a stacking fault; the latter ones are often called Shockley stacking faults (SSF) in the SiC terminology. A certain subtype (those with Si core) of these partial dislocations is mobile and the leading actor of the so-called bipolar degradation [30]. Analogously, Frank partials with Burgers vectors of type $\vec{b}=c/4$ border Frank

stacking faults (FSF). Frank partials and hence, FSF, are sessile and cannot grow during device operation etc. The SiC-specific "carrot" defect is a certain combination of FSF and SSF [31, 32]. Representatives of the sixth glide system $\sqrt{\frac{a^2}{3}+\frac{c^2}{16}}$ have been reported by Mike Dudley's group [33]. This fault can be generated by macrostep overgrowth of a TSD.

3.3.2 Dislocation Reactions During Epitaxial Growth

Dislocations cannot simply end inside a crystal volume, as their distortion energy needs to be conserved. Hence, all dislocations present at the surface of the substrate need to proceed somehow during epitaxial growth. Today, commercially available 4H-SiC substrate contain BPDs, TEDs, TSDs, TMDs, but hardly any micropipes. As the dislocation density of substrates depends on multiple factors, such as the grade of the substrate quality and the substrate vendor, and has been continuously reduced over the years, it is very difficult to provide exact numbers, but the following data can be taken as a rough indication: TSDs occur usually with a density of 10^2 to low $10^3/cm^2$, TEDs with low $10^4/cm^2$ and BPDs with 10^2 to low $10^3/cm^2$. During epitaxial growth, beside the propagation of dislocations without any change to the dislocation line or Burgers vector, several dislocation reactions can take place at the growth surface. All these dislocation reactions can only take place if the total energy can be minimized by the dislocation reaction (driving force) and if a critical stress level is exceeded. The following dislocation reactions can occur:

- change of the dislocation line direction (while keeping the Burgers vector), e.g. the *conversion* of BPDs to TEDs,
- splitting of the Burgers vector from perfect to partial type (and vice versa), known as *stacking fault generation* (or annihilation),
- the *recombination* of two dislocations, such as the formation of superscrew dislocations or micropipes with *n***c* Burgers vectors or the recombination of a TED and TSD to a mixed type dislocation with Burgers vector $\sqrt{c^2+a^2}$,
- the *annihilation* of two dislocations with similar Burgers vectors, but different sign,
- the *generation of misfit dislocations* due to (local) lattice strain.
- Multiplication of existing dislocations due to high local strain (local dislocation source e.g. Frank–Read type).

In case of *dislocation propagation* during homoepitaxial growth, the dislocation goes on straightforward without any change to its line or Burgers vector. Typically, all kinds of threading dislocations (TEDs, TSDs, and TMDs) propagate as they cannot further minimize their dislocation line energy during growth. Some of the BPDs, usually < 5% of the substrate BPDs, propagate as well. It has been discussed that the line vector of the propagating BPDs is parallel to the step-flow direction [7, 8, 34]. Most of the BPDs, typically more than 95%, from the substrate *convert* to TEDs during epitaxial growth within the first grown micrometers. The propagation and conversion of dislocations can be described adequately by the model of Klapper [7, 8, 35], which is based on the idea of image forces acting on dislocations close to

the growth surface. This model was first invented for bulk crystal growth [35] and has been applied successfully to epitaxial growth of other semiconductors, such as GaN [36]. In case of propagation and conversion of dislocations, the dislocation density (in terms of intersection points on a certain surface area, given in cm^{-2}) remains unchanged.

Stacking faults can either propagate from the substrate to the epilayer – analogously to dislocations – or be generated by dislocations: an a-type Burgers vector, i.e. as for BPDs and TEDs, can split into Shockley partials, and a c-type Burgers vector, as for TSDs, can split into Frank partials. This stacking fault generation is energetically possible and favorable in SiC due to its low stacking fault energy [37]. Other semiconductor materials have a much higher stacking fault energy and thus a much weaker tendency to form any stacking faults.

Generation of misfit dislocations and multiplication of dislocations happen if a critical strain level is exceeded (locally), due to doping-induced lattice misfit or interactions of dislocations with growth steps, such as pinning. Dislocations generated by such mechanisms are of a distinct type and geometric arrangement: misfit dislocations in 4H-SiC epilayers are BPDs lying at the substrate–epilayer interface, or the so-called TED half loop arrays [38, 39] are generated by pinned BPDs, which are acting as Frank–Read sources. Such dislocation generation mechanisms do not necessarily lead to a higher dislocation density at the wafer surface (in terms of dislocation intersection points on a certain surface area), but increase the total length of dislocations inside a crystal volume (also given in $cm/cm^3 = cm^{-2}$!).

The *annihilation*, i.e. the recombination of 2 TSDs with c-type Burgers vectors of different sign, and/or the *combination of dislocations*, i.e. TED and TSD combine to a TMD, is possible in SiC, but very unlikely. The two involved dislocations need to be within an interaction distance, which can be estimated based on the Peierls barrier (as lattice resistance against dislocation movement) [40] and Peach–Köhler force (interaction force between two dislocations) [27, 41] and is in the order of single micrometers [42]. For comparison: for a typical dislocation density of 1×10^4 cm^{-2}, the average distance between two dislocations amounts to 100 µm, which is much too far for any interaction of dislocations.

The types of defects lying on the (0001) basal plane of SiC, such as BPDs, SSF, carrots, can "grow" very large due to the substrate's off-cut. There is a simple geometric relation between the depth (d), at which the defect starts growing, its projected length (L) and the wafer off-cut angle α:

$$d = L \cdot \tan \alpha \tag{3.2}$$

This relation implies that defects on the basal plane become larger, the thicker the epilayer grows and can be used to analyze the origin of defects within epilayers, i.e. if the defect was generated at the substrate–epilayer interface or during epitaxial growth (see Figure 3.5). Hence, the defect density can be minimized by tuning the back-etching and initial epigrowth conditions or by changing epitaxial growth conditions.

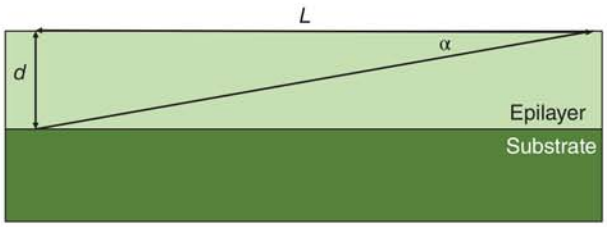


Figure 3.5 Schematic drawing for illustrating the relationship between depth (d) of defect nucleation on the basal plane and its projected length (L) for a certain off-cut angle α of the wafer. Source: Kallinger et al. [19].

3.3.3 Characterization Methods for Extended Defects in 4H-SiC Epilayers

Among a broad spectrum of characterization methods for extended defects in 4H-SiC, there are three methods of great importance and commonly used: defect-selective etching (DSE), X-ray topography (XRT), and UV-excited photoluminescence (UVPL) imaging. They are briefly introduced in this section.

DSE is a simple, robust, and well-established method for the determination of the dislocation density and distribution on a 4H-SiC wafer. It has been used since the beginning of 4H-SiC commercialization. The intersection points of dislocations on the (Si-face of the) wafer surface are more strongly attacked by a chemical etchant than the undisturbed wafer area between these intersection points. Hence, etch pits are forming at these intersection points of dislocations. It is commonly expected that the size and shape of the etch pits are characteristics for the dislocation type due to the size and form of the dislocation strain field, which again goes back to the Burgers vector and type of the dislocation [3]. Hence, oval-shaped etch pits are expected for BPDs and small and large hexagonally shaped etch pits for TEDs and TSDs, respectively. This expectation holds for 4H-SiC with moderate N doping, Al doping, and undoped materials [43]. For highly N-doped material like low-resistive substrates, this classification for TEDs and TSDs is not true if etched with the standard etchant, molten potassium hydroxide (KOH). It has been reported that the selectivity of the etching process can be improved by adding Na_2O_2 to KOH (KN etching) [44] instead of pure KOH melt. Nevertheless, the density and lateral distribution of BPDs and all threading dislocations (TEDs + TSDs + TMDs) as well as micropipes (if present) can be determined routinely. The etching process of wafers (substrates as well as epi-wafers), image recording of the etched surface, and image analysis with regard to etch pit densities can be automated and is a cost-effective, reliable method. But, it is a destructive method as it destroys the wafer surface and it can only reveal defects intersecting the wafer surface.

XRT is based on the diffraction imaging of X-rays at crystal (defects) and is able to identify the dislocations including their Burgers and line vectors. Moreover, it is a nondestructive method and needs no special sample preparation despite of good surface quality. However, for long time, XRT had to be done at synchrotron facilities to record images with good contrast in reasonable time. Generally, defect

identification, as well as Burgers vector analysis by XRT, needs images from different diffraction reflexes, which need to be compared and analyzed in detail. These conditions were time-consuming and expensive; hence, it was a method only for scientific studies of dislocation types, dislocation reactions, and stacking faults inside the wafer (or bulk crystal). Today, XRT studies can be done with lab tools with micro-focus X-ray tubes, high-resolution charge-coupled device (CCD) cameras, facilitating the access to XRT images and bringing down the time for image recording. For example, a 150 mm wafer can be scanned within two hours with an image resolution sufficient for dislocation analysis, like TSD counting based on the symmetric 0008 reflex. XRT can image and identify dislocations, stacking faults, and complexes thereof such as carrots, giving the possibility to generate expected yield maps for devices based on these killing defects. Still, the determination of the dislocation type and their densities by automated image analysis is very demanding.

In the last decade, UVPL imaging has been developed to a methodologically sound and fully automated method, which can provide data on density and distribution of stacking faults, defect complexes, and particles across the epiwafer without sample preparation or damage. Current systems like the Lasertec SICA or the Intego AQUILA can scan a 150 mm wafer and deduce the defect density and distribution within a few minutes. Hence, these systems can be used as inline monitoring systems for quality control and improvement of epilayers and epitaxial growth. However, UVPL imaging cannot provide reasonable data for threading dislocation (TEDs and TSDs) densities and distributions, only for BPDs, and can hardly image defects in highly N-doped substrates. In UVPL imaging, the 4H-SiC material is excited with a wavelength in the UV range (typically 305, 313, 340, or 365 nm) and the emitted photoluminescence (PL) signal is recorded by a CCD camera in imaging mode (not in spectral resolution). As 4H-SiC is a semiconductor with an indirect band gap, the defect-free material remains quite dark (it has a very small probability to emit near band edge radiation, and hence, the SiC background in the pictures is not completely black, but gray). On this dark background, some defects are actively emitting light and, hence, appear as bright features with a specific emission wavelength, size, and shape. Still, the defects have a large variance in appearance and that complicates the automated defect detection. Examples for typical defects in epiwafers are summarized in Figure 3.6, for the UVPL channel as well as for surface sensitive channels as dark field (DF) and differential interference contrast (DIC) imaging.

Moreover, there is no common, standardized classification of defects available yet for the different measurement systems and SiC suppliers worldwide. Defects are often named according to their appearance, e.g. dark or bright triangles, but this naming is purely phenomenological, since the appearance of defects is determined by the measurement conditions. Some attempts of standardization have been done, e.g. SEMI standards [45] or the Japanese standard from JEITA [46], but they are not yet commonly applied. Therefore, it remains difficult to translate defect densities from one system or wafer supplier to another. The basic UVPL imaging method is not spectrally resolved, but the systems offer the opportunity to insert optical filters to collect UVPL emission in a specific wavelength range, such as near-infrared (NIR, suitable for dislocations), visible spectrum (VIS, for stacking faults), or near band

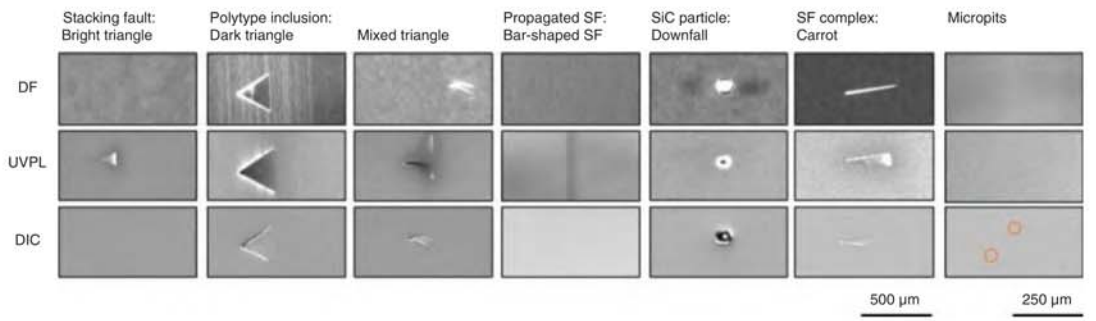


Figure 3.6 Examples for typical epilayer defects: appearance in dark field (DF), UVPL imaging, and differential interference contrast (DIC) mode. Pictures recorded with an Intego AQUILA at Fraunhofer IISB. DF, dark field; UVPL, UV-excited photoluminescence; DIC, differential interference contrast; SF, stacking fault.

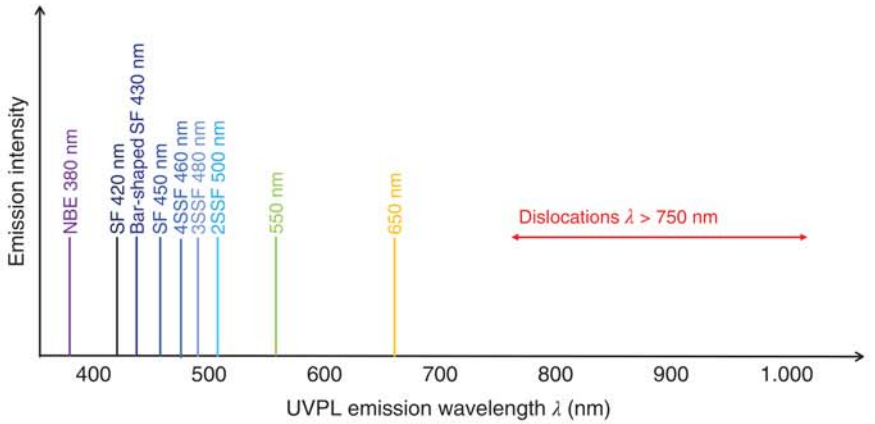


Figure 3.7 Summary of room-temperature luminescence data from stacking faults (SF) after UV excitation according to [9, 37, 47–50]: near band edge emission (NBE), double Shockley stacking fault (2SSF), triple Shockley stacking fault (3SSF), and quadrupole Shockley stacking fault (4SSF).

edge emission (NBE). A comprehensive overview to reported emission wavelengths of defects is given in Figure 3.7.

Besides these difficulties in defect classification and counting, UVPL imaging has become the standard characterization method for extended defects in epiwafers and it can be used for estimating the device production yield for a certain device type on a certain wafer and allows for inking out defective devices.

3.4 Point Defects and Carrier Lifetime in Epilayers

3.4.1 Classification and General Properties of Point Defects in 4H-SiC

Point defects are 0-dimensional defects in the crystal lattice and classified into intrinsic and extrinsic point defects. **Intrinsic defects** are "misaligned" host atoms, i.e. Si and C atoms, which are either missing on their regular lattice sites ("vacancies") or placed on an interstitial site ("interstitials"). There are four basic intrinsic point defects, such as Si and C vacancy (V_{Si} and V_C) as well as Si and C interstitials (Si_i and C_i). They can occur as single defects or as complexes, such as $V_{Si}C_i$. In a compound semiconductor like SiC, antisite defects like Si_CC_{Si} can occur. Intrinsic point defects have various origins: They have a thermodynamical probability of formation (at the high growth temperature and quenched during fast cool down), but they can also form during nonequilibrium processes like irradiation with ions, electrons, high-energetic photons, and particles. Point defect annihilation during thermal annealing can be considered as back reaction of the so-called Frenkel pair formation reaction:

$$C_C \Leftrightarrow V_C + C_i \tag{3.3}$$

A Frenkel pair is generated when a C (or Si) atom is leaving its regular lattice site (C_C) and therefore, generating a C (or Si) vacancy and a C (or Si) interstitial simultaneously and in close distance. The C vacancy is sessile, whereas the C interstitial is quite mobile. As the formation of a Frenkel pair is taking place at elevated temperatures, the C interstitial is diffusing away; therefore, the Frenkel pair is not stable and cannot easily recombine (i.e. annihilate). The mobile C interstitials might diffuse to other defects, e.g. other point or extended defects, and agglomerate there or vanish if they reach a crystal surface. Hence, the originally stoichiometric concentration of $V_C : C_i = 1 : 1$ is not necessarily conserved, but changes to an excess of C vacancies in the material volume. This is the challenge of point defect annealing: bringing the reaction partners back together, which will be discussed later in this section.

To make a complex process like the Frenkel pair generation more simple, Eq. (3.4) shows the Arrhenius-type equation for C vacancy formation – although we already know that a *pair* of C vacancy and interstitial is formed:

$$[V_C] = N_C \cdot \exp\left(\frac{S_F}{k}\right) \cdot \exp\left(\frac{-H_F}{kT}\right) \tag{3.4}$$

The concentration of C vacancies $[V_C]$ and regular C lattice sites N_C, the formation entropy S_F, the formation enthalpy H_F and the absolute temperature T enter Eq. (3.4). As the formation entropy of point defects is usually not known, a value of $5k_B$ is a reasonable assumption for further calculations [51, 52]. The formation enthalpy for a Si vacancy (8 eV) is much larger than that of a C vacancy (5 eV, [51]); hence, in any processes at elevated temperature such as epitaxial or bulk growth or thermal annealing, much more C vacancies are generated than Si vacancies.

Besides the intrinsic point defects, **extrinsic point defects** are present in SiC material such as dopant atoms, which are intentionally incorporated, or impurity atoms (unintentional incorporation). Extrinsic defects can either substitute host atoms (like for doping) or incorporate on interstitial sites, if the impurity's covalent radius does not fit to those of the host atoms. Extrinsic point defects have extremely low diffusion constants in 4H-SiC (as shown in Figure 3.8) and are, hence, quite sessile. Consequently, the growth conditions, especially the purity of the growth environment in bulk and epitaxial growth, are decisive for the concentration of extrinsic point defects in SiC substrates and epilayers.

Point defects can be charged with electrons and/or holes and, therefore, show (several) steps of charging. Some have acceptor-like character if they trap an additional electron and become negatively charged; others have a donor-like character. This charging and de-charging of defects under defined external conditions (temperature, voltage, …) can be used for defect characterization – either by electrical methods such as deep level transient spectroscopy (DLTS) or optical methods like (deep temperature) PL spectroscopy. Magnetic properties of point defects can be investigated by means of electronic spin resonance (ESR) and similar methods. As this chapter is dedicated to the relationship between point defects and carrier lifetime in epitaxially grown material, hence, it is focused on the electrical properties (i.e. energetic level and capture cross section) of point defects, which are usually determined by DLTS measurements.

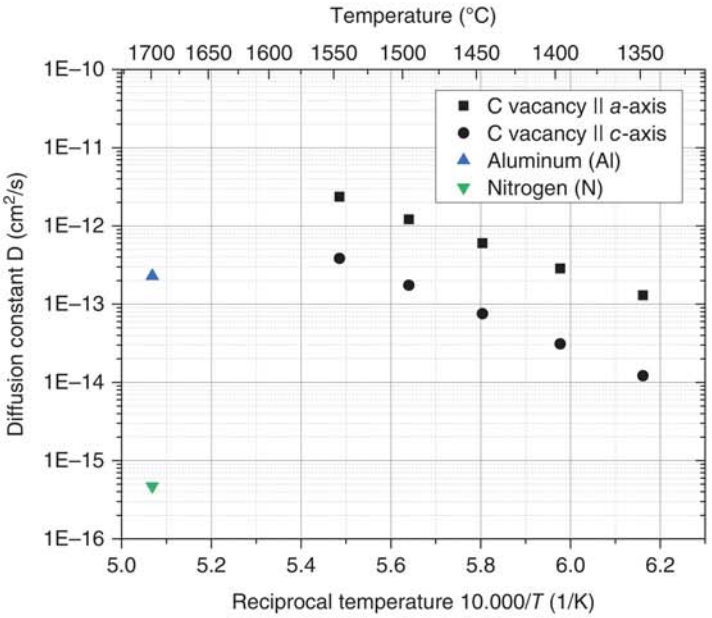


Figure 3.8 Diffusion constants for carbon vacancies (parallel to *a*- and *c*-axis) [53], N donor [54], and Al acceptor [55].

3.4.2 Basics on Recombination Carrier Lifetime in 4H-SiC

There are three recombination processes in semiconductors, called Auger, radiative, and Shockley–Read–Hall (SRH) recombination [56]. Auger recombination takes place under high injection conditions and at high doping concentrations, whereas radiative recombination is dominant at low doping and moderate injection conditions. SRH recombination is a model describing the recombination processes at point defects, and it includes both radiative and non-radiative recombination processes at the point defects. As all these basic recombination processes (and multiple point defects in SRH recombination) concur, the overall reciprocal recombination carrier lifetime is the sum of all reciprocal lifetimes:

$$\frac{1}{\tau_{SiC}} = \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{SRH}} \tag{3.5}$$

The physical nature of these recombination processes is explained in textbooks, e.g. Schroder [56] or review papers [57]. Figure 3.9 shows exemplarily the overall recombination carrier lifetime as well as Auger, radiative, and SRH lifetimes calculated for 4H-SiC substrates and epilayers.

For the calculation of the recombination lifetimes shown in Figure 3.9, basic equations given in the textbook from Schroder [56] have been used together with recombination coefficients for Auger [58] and radiative [59] recombination, as well as the capture cross sections and energetic levels of the carbon vacancy and its typical point defect concentrations of 10^{12}–10^{13} cm^{-3}. The C vacancy is represented by the $Z_{1/2}$ and $EH_{6/7}$ defects, which are the electronic signatures of

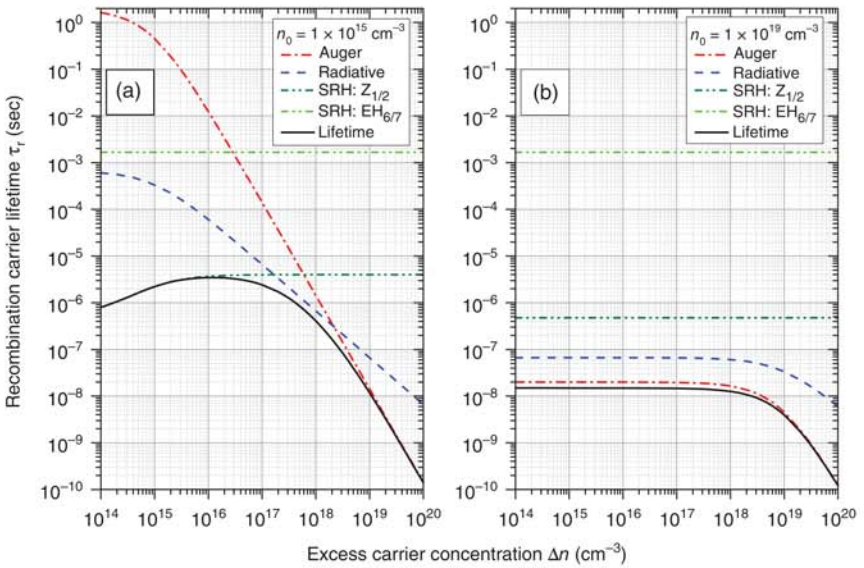


Figure 3.9 Calculated recombination carrier lifetime in a typical low N-doped epilayer (a, doping concentration $n_0 = 1 \times 10^{15}$ cm^{-3}) and a highly N-doped substrate (b, doping concentration $n_0 = 1 \times 10^{19}$ cm^{-3}) as a function of excess carrier concentration. A trap concentration $N_T = 5 \times 10^{12}$ cm^{-3} is assumed for $Z_{1/2}$ and $EH_{6/7}$.

V_C in DLTS measurements [60, 61]. In case of a low doped epilayer (Figure 3.9a), the SRH-lifetime obtained for the $Z_{1/2}$ defect is the shortest and therefore, limiting carrier lifetime for low to moderate carrier injection. As the carrier injection becomes larger than approximately 1×10^{17} cm^{-3}, radiative recombination comes into play, but Auger recombination becomes the dominant recombination process for injected carrier concentrations larger than 2×10^{18} cm^{-3}. As such high injection conditions are typically found in forward operation of bipolar devices, point defects are not the limiting factor for poor lifetimes in forward operation, but the intrinsic recombination processes, Auger and radiative recombination. N-type substrates have very short carrier lifetimes due to their high doping concentration as can be seen from Figure 3.9b and their overall lifetime value is dominated by Auger recombination for all magnitudes of carrier injection.

3.4.3 Carrier Lifetime-Affecting Point Defects

Auger and radiative recombination are intrinsic properties of the SiC material, which cannot be tuned or improved by material development, but point defects, which determine the SRH lifetime, can be controlled in epitaxial growth and post-epi processes. This section deals with the current state of the art and knowledge.

The impact of point defects on the SRH lifetime is characterized by their capture cross sections for electrons (σ_n) and holes (σ_p) as well as their trap energy (E_T) and naturally their defect concentration. Lifetime-affecting point defects have a large trap energy, i.e. are close to the mid of the band gap, and have both large capture

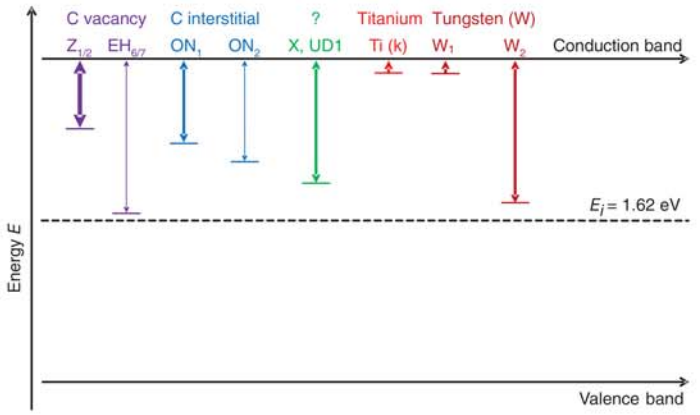


Figure 3.10 Trap energies and capture cross sections of intrinsic and extrinsic point defects in n-type 4H-SiC. Thicker arrows indicate larger capture cross sections; thinner arrows smaller capture cross sections.

cross sections for electrons and holes. For example, $Z_{1/2}$ has a smaller trap energy, but larger capture cross sections for electrons and holes than $EH_{6/7}$, and therefore, causes a much shorter SRH lifetime (for the same trap concentration) as can be seen from Figure 3.9. It has been shown by several work groups that both $Z_{1/2}$ and $EH_{6/7}$ are signatures of the C vacancy in 4H-SiC [60, 61].

Figure 3.10 summarizes the trap energies and capture cross sections of technologically relevant intrinsic and extrinsic point defects in n-type 4H-SiC, which have been discussed recently in relation to carrier lifetime. More detailed information about electronic properties of point defects can be found in the book chapter "Intrinsic and Extrinsic Electrically Active Point Defects in SiC" from Ulrike Grossner.

In highly N-doped 4H-SiC substrates, the Auger and radiative recombination are the dominant recombination processes, resulting in very short carrier lifetimes of nanoseconds or tens of nanoseconds. Besides the high doping concentration, considerable concentrations of intrinsic and extrinsic point defects might be present in the substrate material. Intrinsic defects, e.g. C and Si vacancies are generated due to high growth temperatures > 2000 °C in bulk crystal growth and their thermodynamical probability of formation. Extrinsic defects such as tungsten (W) [62, 63] and titanium (Ti) [64] can be incorporated at high growth temperatures from graphite parts and typically originate in the SiC seed powder. However, these point defects play a minor part in lifetime considerations of the substrates.

On these substrates, epilayers are deposited typically at epigrowth temperatures around 1600 °C from highly pure precursors. Therefore, extrinsic defects are quite unlikely being incorporated or at very low concentrations. Intrinsic defects can be formed, and the concentration of the C vacancy is expected to be larger than that of the Si vacancy due to their different formation enthalpies. It has been shown that the concentration of C vacancies (in terms of $Z_{1/2}$ defect measured by DLTS) follows the growth temperature, which fits to the general thermodynamic model [65, 66]. Additionally, if the epigrowth is performed in deficiency of C, e.g. at small C/Si ratios,

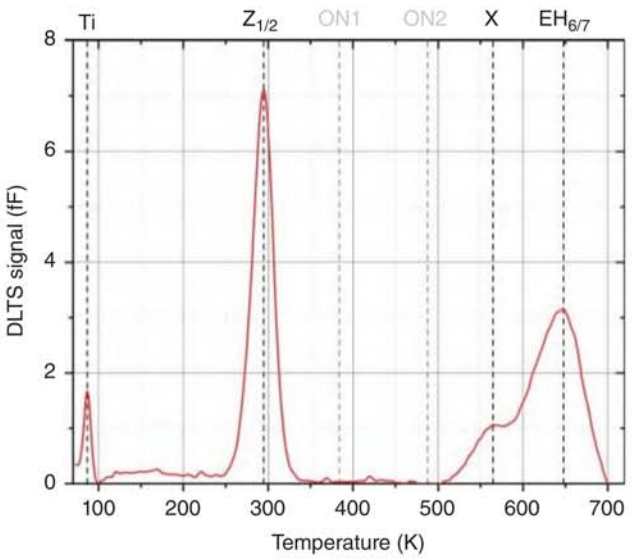


Figure 3.11 Typical DLTS spectrum for an as-grown n-type epilayer. Common point defect signatures are indicated by broken vertical lines in the spectrum, such as Titanium, $Z_{1/2}$, X, and $EH_{6/7}$. Commonly observed peaks like the ON1 and ON2, which are absent in this sample, are indicated by gray broken lines.

even more C vacancies are present. Conclusively, the concentration of C vacancies or, $Z_{1/2}$ in DLTS measurements can be controlled by the epitaxial growth parameters temperature and C/Si ratio. In epigrowth, the $Z_{1/2}$ concentrations can be reduced to 2×10^{12} cm^{-3} [65–67], corresponding to a SRH lifetime of 10 µs. For proper current modulation in bipolar devices, such a SRH lifetime is still too short and needs further optimization, e.g. by post-epi processes.

Besides the lifetime-limiting $Z_{1/2}$ defect and the $EH_{6/7}$ defect, titanium (Ti) and the so-called X defect are commonly observed in DLTS spectra of as-grown epilayers (as shown in Figure 3.11). Ti is a very common impurity in SiC epilayers, although its origin is not really clear. It has one peak in DLTS spectra at ~80 K. The UT1 [68] or X defect [69] occurs only in epilayers grown on n-type substrates from a few vendors, suggesting a relation to a substrate property. It is characterized by a single peak in DLTS spectra around 560 K and is a lifetime-affecting defect in n-type 4H-SiC. A recent study [70] indicates that it might be an extrinsic impurity in the substrate, which agglomerates on the growth surface during back-etching at the beginning of epitaxial growth and is incorporated into the growing epilayer with a specific segregation coefficient. Currently, this thesis needs more experimental and theoretical proofs and publication.

In post-epi lifetime engineering, the basic idea is to insert excess C atoms to annihilate the C vacancies. This can be realized by thermal oxidation of the epilayer [71, 72], annealing [51], and ion implantation [73]. Thermal oxidation consumes the Si atoms of SiC for the formation of the silicon oxide, whereas the C atoms leave the material as long as they can diffuse through the thin oxide layer. As the oxide is growing

thicker, the C atoms can hardly leave anymore, but enrich at the oxide–epilayer interface as C interstitials or C clusters [74]. In case of ion-implanted N atoms (as well as other C substituting elements) and subsequent annealing, N displaces C atoms from their regular lattices sites and hence, generates C interstitials. Both thermal oxidation and ion implantation insert excess C atoms, i.e. C interstitials, close to the epilayer surface and these C interstitials need to diffuse into the epilayer to recombine with C vacancies. Hence, the resulting $Z_{1/2}$ concentration profile is increasing with increasing depth in the epilayer. Annealing of the samples is another alternative for minimizing the C vacancy concentration and hence, the carrier lifetime, in as-grown epilayers. Due to the thermodynamics of Frenkel pairs, a post-epi annealing process can reduce C vacancy concentration, when it is performed at a temperature lower than the epigrowth temperature, i.e. less than 1600 °C. The lower the annealing temperature, the lower the resulting C vacancy concentration – but, the longer the annealing time as the C interstitials need to diffuse and diffusion velocity slows down at low temperatures. The advantage of annealing compared to thermal oxidation and ion implantation might be that it happens throughout the material volume simultaneously. Several annealing steps are performed at several stages of device production, also at late stages e.g. for contact formation etc. Here, annealing temperatures higher than the epigrowth temperature increase the C vacancy concentration again, and hence, degrade the carrier lifetime. Therefore, the annealing temperatures in the device processing need to be adapted to maintain high carrier lifetimes.

3.4.4 Carrier Lifetime Measurement in Epiwafers and Devices

There are many techniques established for measuring the recombination carrier lifetime in substrates, epiwafers, and devices. Today, recombination carrier lifetime of *epiwafers* is usually measured by optical methods such as time-resolved photoluminescence (TR-PL) or microwave-detected photoconductivity decay (μ-PCD) because these methods are fast, contactless, and do not need any sample preparation. They are called optical methods because they use optical excitation of the SiC material with UV light, i.e. a photon energy larger than the band gap, with a certain light intensity. The wavelength and the intensity of the UV light determine the excess carrier concentration profile in the sample during the measurement, which is a key factor for the recombination process taking place (see above). Only a small spot of the sample can be excited at one time; hence, the wafer needs to be scanned to get a full wafer lifetime distribution map. Real samples consist of both the low doped epilayer (stack), with certain doping concentration and thickness profiles, and the highly doped substrate as well as the epilayer surface and the back side of the wafer. Therefore, the lifetime values determined by optical measurement techniques are a kind of mean lifetime value and usually called *effective lifetimes*. Kimoto [67] has proven that the reciprocal effective lifetime is the sum of the reciprocal SRH lifetime and another reciprocal lifetime term (τ_{other}), which covers all other recombination mechanisms, e.g. surface recombination of the sample, and all other effects on the optical lifetime measurement. Moreover, the injected carrier concentration is not constant throughout the sample thickness and decreases during the measurement, which brings

many locally and timely shifting measurement conditions. The resulting transient curve has several regimes, representing different stages of the measurement and recombination processes, and their slopes yield the carrier lifetime value. Therefore, from a single measurement or transient, different lifetime values can be extracted. Hence, the measured lifetime values are not easy to understand or even to compare. Deeper insights into this complex situation can be gained from the simulation of the recombination carrier lifetime based on the physical equations, true doping and thickness data of the epilayer stack and substrate, as well as available recombination data [75]. The user is able to play around with surface recombination velocities, defect types, and their concentration profiles as well as intrinsic properties of the SiC material and epiwafer and check their impact on the resulting lifetime values.

Besides the optical measurements on epiwafers, the recombination carrier lifetime can be characterized at pn junctions, e.g. in bipolar power devices or the body diode in MOSFETs, by electrical methods such as the open-circuit voltage decay (OCVD). This is important as this measurement yields the actual carrier lifetime during device operation – however, the measurement takes place under high injection conditions at the pn junction. Such measurements often reveal recombination carrier lifetimes in the order of single nanoseconds or tens of nanoseconds, which are to be expected for the dominant radiative and Auger recombination processes under high injection conditions. Hence, it is probable that an epiwafer has been characterized several times during bipolar device processing with optical methods, yielding effective carrier lifetimes in the order of microseconds, and the final lifetime test in the operating device reveals much shorter carrier lifetimes during device operation.

Conclusively, recombination carrier lifetime depends on many factors, e.g. sample doping and thickness, surface recombination velocities, carrier injection, types, and their concentrations of point defects. Consequently, carrier lifetimes cannot be characterized adequately by a single lifetime value. This is the reason, why different measurement setups or measurement techniques provide different lifetime values for the same sample – the measured values are correct, but represent different measurement conditions.

3.5 Conclusion

This chapter summarizes and explains the main inventions in 4H-SiC homoepitaxial growth, such as step-flow growth on vicinal substrates by a CVD process, and its implications on the design of the growth process. Moreover, the most important extended defects such as dislocations and stacking faults are introduced as well as point defects, which are relevant for carrier lifetime. It has been shown that 4H-SiC homoepitaxy is a mature technology today, which reached a technological level that has been inconceivable some years ago with respect to doping control and epilayer quality. Many researchers around the world contributed to a deep understanding of phenomena and relations, e.g. the bipolar degradation mechanism and strategies for BPD avoidance and the relation between point defects and (minority) carrier lifetimes. Besides this, new characterization methods such as the UVPL imaging and

μ-PCD for extended defects and carrier lifetime have been established within the last years and useful measurement tools are commercially available – allowing for high wafer throughput and short feedback times. Hence, SiC has been established as *the* semiconductor material for power electronic applications – and will be a main part of future technologies such as electric mobility.

Acknowledgments

I would like to thank the editors Roland Rupp, Peter Wellmann and Noboru Ohtani for giving me the opportunity to contribute to this book. However, the chapter would be rather short without the work done by my co-workers Jürgen Erlekampf, Patrick Berwian, Jochen Friedrich, Mathias Rommel, Daniel Kaminzky, Katharina Roßhirt-Lilla, and many more student workers. Last but not least, I acknowledge our industrial partners for cooperation and many interesting topics to work on as well as the funding institutions.

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4

Industrial Perspective of SiC Epitaxy

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4.1 Introduction

In this chapter, the status of high-throughput production of large-area silicon carbide (SiC) epitaxial wafers for advanced SiC power devices is addressed. Because of the nature of this compound semiconductor, and high temperatures required, SiC epitaxial growth is very challenging. While maturing into a reliable manufacturing technology, it is still a highly competitive and rapidly developing field, making any review difficult. The authors of this paper apologize in advance for any inadvertent omission. A companion paper in this volume will focus more deeply on several of the important theoretical and scientific developments in the field of SiC epitaxy. However, as the performance, device parameter distributions, cost, and even reliability depend critically on the SiC epitaxial active layer properties, these topics will also be touched on here. More specifically, even after the layer metallurgical uniformity and quality, growth chamber capacity, layer growth rate, fixed growth cycle times, up time, and throughput are optimized, it is the throughput of the actual device quality epitaxy that meets the requisite device input specifications that matters. For example, one could relax epitaxial layer uniformity or defectivity for higher epi yield and lower epitaxial wafer cost, but there is so much value added in the subsequent device processing that these epi trade-offs are often overwhelmed by the final device yields to specification, pressing SiC epi to ever tightening requirements.

In large part, however, these technical challenges have been satisfied for the high-throughput supply of SiC epitaxial layers capable of producing 3.3 kV power devices (~0.1 kV/μm) even demonstrating 6.5 kV [1] with low background doping concentrations $<1 \times 10^{14}$ cm^{-3} and intentional n-type doping from $\sim 1 \times 10^{15}$ cm^{-3} to $>1 \times 10^{19}$ cm^{-3}. These most recent SiC epitaxial layer growth results, particularly those from the still highest reported throughput, 8 × 150-mm, warm-wall planetary vapor phase epitaxial (VPE) reactor, will be presented in detail. The epitaxial layers have intrawafer thickness and n-type doping uniformity (σ/mean) of 1.17% and 4.99%. While under active process control to counter small run-to-run systematic drifts, long-term run-to-run variations (σ/mean) are currently 1.01% for thickness and 5.13% for doping (*vide infra*) [2].

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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Multi-wafer SiC epitaxial layer throughput has been increased by almost 2 orders of magnitude over the past 20 years with continuously improving layer quality characteristics with further improvements underway. This and other reactor configurations will be discussed. These new SiC epitaxial growth capacities have greatly enabled the economical production of advanced SiC devices for the marketplace.

4.2 Background

SiC is now a preferred semiconductor material for high-power, high-temperature, and microwave devices because of its superior thermal and electrical properties [3]. SiC substrates with a diameter of 150 mm and epitaxy are commercially available, and larger 200 mm diameter SiC materials are in the early stage of development. SiC metal-semiconductor field-effect transistor (MESFETs) [4], static induction transistors (SITs) [5], BJTs [6], metal oxide semiconductor field-effect transistors (MOSFETs) [7], PiN diodes [8], insulated gate bipolar transistors (IGBTs) [9], and gate turn-off thyristers (GTOs) [10] fabricated on epitaxial grown layers have demonstrated performance far exceeding than that of Si- and GaAs-based devices, and SiC Schottky diodes and MOSFET power devices have reached widespread commercial acceptance [7], with even greater adoption projected with regard to electric vehicle applications. The development of these advanced wide-bandgap (WBG) devices has been greatly aided by the development of economical device-quality SiC epitaxial layers. These SiC epitaxial layers are the active layers of controlled thickness and doping that form the heart of all advanced WBG power semiconductor devices. The economical production of these layers has been made possible by the large area, high capacity VPE reactors with continuing and new developments described herein.

4.3 The Basics of SiC Epitaxy

Figure 4.1 contains a cartoon of the SiC epitaxial layer deposition process [11]. Chemical reagents such as silane and propane are delivered into the growth chamber by a carrier gas, typically hydrogen. The reagents flow over an inductively heated graphite susceptor (or directly over the SiC wafer, *vide infra*) at a temperature of ~1600 °C. In the ideal case, the reagents quickly heat and crack into intermediate chemical compounds that flow in a controlled laminar fashion over the SiC substrates to be deposited on. Tendencies for the gas to recirculate from convection or turbulence and silicon agglomeration in the gas phase (and on cold surfaces) due to supersaturation reduce epitaxial layer growth rates and increase layer defectivity. These undesirable characteristics are inhibited by increased growth temperature, reduced chamber pressure, and the addition of chlorine- containing compounds [12]. The natural depletion of the reagents in the gas stream must be compensated for by geometrical (including wafer rotation) or gas flow means to obtain uniform layer thickness across the substrates. Under the typical growth conditions employed

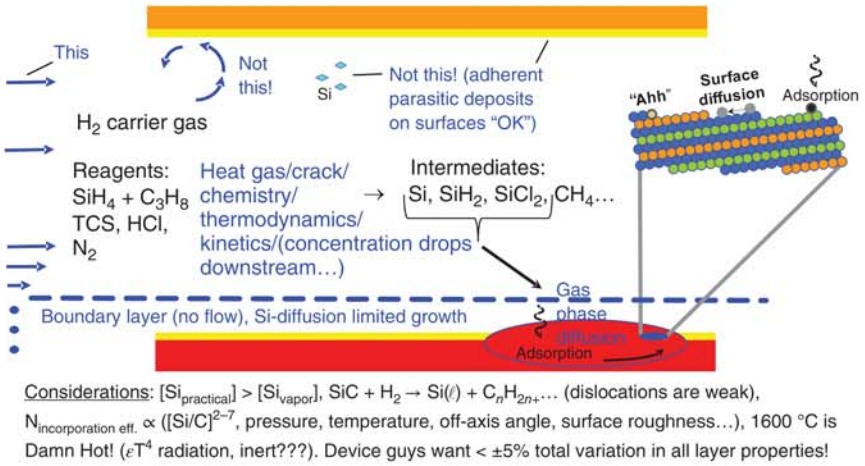


Figure 4.1 SiC epi growth mechanism cartoon.

(~100 mbar, 1600 °C, >20 μm/h), partially cracked chemical intermediaries such as $SiCl_2$ and SiCl [13] diffuse through a boundary layer of stagnant gas flow typically depleted of silicon (i.e. Si-diffusion growth rate limited conditions). Once adsorbed on the surface, the surface adatoms diffuse to an appropriate atomic step to correctly replicate the underlying SiC polytype or a polytype inclusion or other morphological defect will ensue.

Additional critical considerations are that the concentration of silicon-containing species for a practical growth rate will certainly at some location and temperature in the reactor exceed the allowed silicon vapor pressure as the gas heats (hence the tendency for silicon supersaturation). At the temperatures of SiC epitaxy, the hydrogen carrier gas etches the SiC substrate [14]. Despite significant improvement, unlike silicon, the SiC substrate and its surface still contain hundreds of crystallographic dislocations per square centimeter that are chemically weaker than the surrounding surface, so some pitting and other surface roughness typically result. Certain of these features can adversely impact devices [15]. Further, while the growth rate only depends linearly on the naturally reducing silicon concentration, dopant incorporation (nitrogen for n-type) is exponentially dependent upon the local Si/C ratio [16] at the growing surface and also depends on pressure, temperature, off-axis crystal angle, and atomic surface roughness. To further complicate matters, all of these diverse physical and chemical steps occur at temperatures where most supposed refractory materials and coatings are not truly physically stable to thermal gradients or shock nor chemically inert to hydrogen, chlorine, or certainly liquid silicon. Despite these challenging factors, device designers require very tight epitaxial thickness and doping distributions ~±5% total variation and low defectivity (≪0.5 defects/cm^2) to within 5 mm of the wafer edge, and in the case for bipolar devices, zero basal plane crystallographic dislocations (both of materials and processing origins [17]) to satisfy their equally demanding device performance, yield, and reliability specifications.

4.4 SiC Epi Historical Origins

While interest in SiC has its origins in the late 1950s, alongside the elemental semiconductors Si and Ge, its technological development has been delayed by the extreme temperatures (~1600 °C) required to grow good-quality SiC epitaxial layers, the late development of suitable substrates, and the various polytypes that can form in SiC. Several reactor geometries have been successfully employed for the growth of SiC epitaxial layers. They include basic "cylindrical"-horizontal and vertical (or chimney) reactors, barrel reactors, rapidly rotating disk reactors, and "planetary"-horizontal (hereafter referred to only as planetary) reactors. Figure 4.2 contains a schematic of the basic reactor geometries. A historic distinction between these reactor geometries is whether the input gas flows perpendicular or parallel to the surface as it approaches the wafer. While either flow condition can be realized regardless of the gross orientation of the reactor, conventionally gases flow roughly horizontally over the wafers in cylindrical-horizontal, barrel, and planetary reactors and perpendicularly in vertical reactors. An important distinction used here between "cylindrical" and planetary reactors for multi-wafer configurations is that the gas must flow longitudinally over two or more wafer diameters in the former whereas it need only flow over one in the latter (*vide infra*). Note also that this distinction still holds true even if planetary motion is used in a cylindrical-horizontal reactor (hereafter referred to as horizontal). While the rapidly rotating reactor has a vertical orientation, the rapid rotation drags the gas flow stream lines horizontally by viscous pumping [18]. These reactor configurations can also be further categorized with regard to the temperature of the surfaces opposite to the wafer. These are referred to as either cold or hot "walls" where the hot wall is actively heated or "warm-wall" where the surface is passively heated yet is still hotter than silicon's melting point, 1410 °C. Both greatly reduce

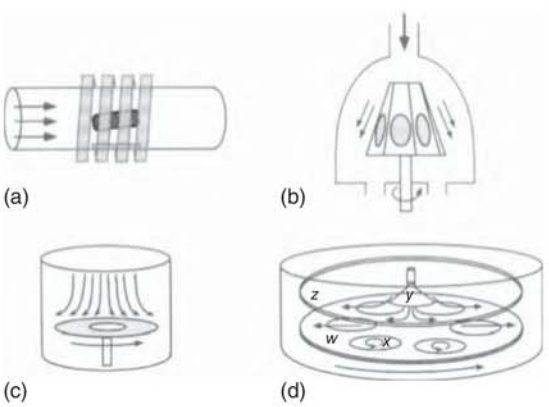


Figure 4.2 Schematic drawings of (a) cylindrical-horizontal (shown with inductive coil), (b) barrel, (c) rapidly rotating, and (d) planetary-horizontal-VPE SiC reactors. All employ inductively heated graphite susceptors to reach the extreme, ~1600 °C, epitaxial growth temperature. Critical components of the planetary reactor are the susceptor (*w*), wafer holders (*x*), reagent injection nozzle (*y*), and ceiling (*z*).

gas phase Si-supersaturation and surface Si-condensation which damage both reactor components and increase epitaxial layer defectivity. While in theory either condition can be realized for all of the reactor geometries, the extreme ~1600 °C temperatures required for SiC epitaxial growth have in practice limited barrel (and until recently, *vide infra*) rapidly rotating geometries to the cold-wall condition.

Prior to 1980, SiC epitaxial growths were still primarily performed in small, single μm/h growth rate, home-made horizontal and vertical quartz cold-wall reactors capable of growing only on very small, several millimeter on a side, SiC crystals. Given the high temperatures, all reactors were necessarily constructed with high-temperature-tolerant materials and coatings, such as quartz, graphite, SiC, Ta, and TaC and were normally inductively heated. Even with these refractory materials, judicious use of active water cooling and thermal insulation was required to enable growth temperature to be reached while still protecting the reactor and its components from degradation and even catastrophic mechanical failure. Moreover, in contrast to conventional semiconductors such as Si and GaAs, at growth temperatures required for SiC, none of the reactor components are truly inert; quartz devitrifies, graphite, and SiC coatings are susceptible to reaction with hydrogen, and refractory metals suffer hydrogen embrittlement and also react with hydrocarbons and silicon to form metal carbides and silicides depending upon the local environment. Unlike narrow bandgap semiconductors, the inherent chemical strength and attributes above of SiC make *in situ* cleaning of parasitic deposits highly problematic. Also, SiC readily sublimes from hotter to colder surfaces in contact or close proximity. Additionally, given the superlinear T^4 dependence of radiative heating, changes in component coating thickness, composition, and emissivity by parasitic deposition or reaction can significantly change both reactor component and wafer temperatures for a fixed reactor input power.

Early SiC epitaxial growths by Jennings et al. [19] and Campbell and Chu [20] used silicon and carbon tetrachloride for silicon and carbon sources, respectively, with hydrogen as the carrier gas. Rai-Choudhury and Formigoni [21] employed dimethyldichlorosilane with argon carrier gas. Minagawa and Gatos [22] used the now more typical silane and propane reagents with hydrogen carrier gas. Nitrogen and trimethyaluminum are conventionally used for n-type and p-type doping. However, arsine, phosphine, and diborane have also been employed [20]. Some reactors also incorporated HCl as a complementary means (in addition to hydrogen) to etch substrates prior to [14, 23], or more recently, during [24–26] growth. HCl also helps avoid Si-droplet formation on the wafer surface and in the gas phase by the formation of various gaseous chlorosilanes [14]. Initially, researchers had available only very small (several millimeter on a side) 6H on-axis (0001) Lely or Acheson crystals for their SiC epitaxial growths and required high growth temperatures (~1650 °C). Slightly lower temperatures yielded unwanted yellow cubic SiC deposits. Slightly higher temperatures resulted in net etching not growth. Both extremes were also a function of reagent concentrations. Even in the relatively narrow process window where epitaxial growth was observed, the layers had relatively poor quality, suffering various polytype inclusions, and double positioning grain boundaries [27]. Nonetheless, epitaxially grown pn junctions in

such layers still exhibited basic rectification and even low levels of light emission [20]. Foreshadowing the promise of SiC-based WBG devices, these early devices blocked 50 V at 500 °C [20].

Kuroda et al. [28], Matsunami et al. [29], and Kong et al. [30] obtained specular homoepitaxial growth at reduced temperature (e.g. <1600 °C) by using 6H-SiC substrates off-oriented from the *c*-axis by several degrees toward the $\langle 11\bar{2}0\rangle$ *a*-axis direction, thus facilitating atomic step flow. While the two-dimensional step-flow growth model of Frank and van der Merwe [31] is well known in crystal growth, in SiC epitaxial growth, the use of off-axis substrates has the critical added benefit of exposing the atomic stacking sequence of the substrate, thereby facilitating effective polytype replication [32]. In particular, the $\langle 11\bar{2}0\rangle$"*a*-axis" directions have been shown to yield improved epitaxial layer morphology [33] and to be the fast growth direction for SiC [34].

Itoh et al. successfully grew 4H-SiC epitaxial layers using 5–10° off-oriented 4H-SiC substrates [35]. Larkin et al. [36] first observed the large dependence of dopant incorporation efficiency on input Si/C ratio for both 6H, 4H, and 3C-SiC (analogous to the impact of III/V ratio in that semiconductor family [37]) helping to both reduce background doping density and extend the range of intentionally doped SiC layers.

Continued investigations of SiC epitaxial growth proceeded primarily using basic single wafer cold-wall horizontal reactors. Kong et al. [38], however, developed a cold-wall multi-wafer barrel reactor. This reactor, capable of growing epitaxial layers simultaneously on eight 10 mm diameter wafers, was the largest capacity reactor during the early 1990s. In 1993, Kordina et al. [39] developed a hot-wall reactor primarily for the purpose of reducing the perceived large (20–40 kW) power requirements of the other reactors by using a hollow, inductively heated susceptor in an otherwise basic horizontal reactor. Later, this hot-wall configuration would prove to have other beneficial attributes for the growth of thick epitaxial layers (*vide infra*). Investigating an alternate approach, Rupp et al. [40] developed the cold-wall, single-wafer, rapidly rotating vertical reactor.

4.5 Planetary Multi-wafer Epitaxial Reactor Design Considerations

With the exception of the barrel reactor, all of the above SiC reactors were initially designed for single wafer use. Historically, however, it has proven very difficult to achieve the <±5% total variation of epitaxial layer doping and thickness desired for high yield production of solid-state power or microwave devices in scaled-up horizontal reactors or barrel reactors when using large diameter wafers. In III/V epitaxial growth, two basic types of multiwafer metal–organic chemical vapor deposition (MOCVD) reactors produced the most uniform 3 and 4-in. diameter wafers, the rapidly rotating vertical reactor [41] commercialized by Emcore and the planetary reactor [42] commercialized by Aixtron. Two key benefits sometimes overlooked regarding planetary reactors are the high reagent efficiency, and more importantly,

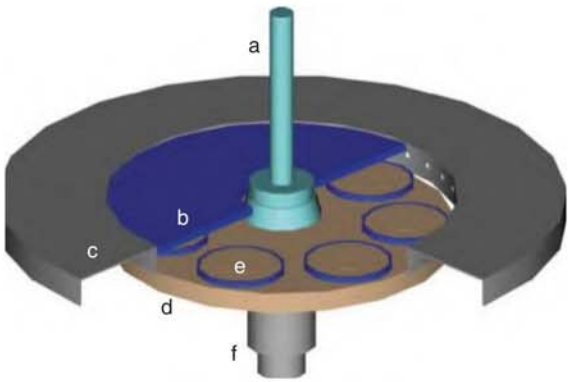


Figure 4.3 Detailed view of the 8–100 mm warm-wall planetary VPE reactor including, (a) water-cooled gas injector, (b) warm-wall (ceiling), (c) exhaust gas collector, (d) susceptor, (e) wafer holder, and (f) rotating susceptor support.

that ideal epitaxial growth conditions need only be maintained over a little more than one wafer diameter as opposed to two or more in horizontal cylindrical configurations. This is particularly challenging at the extreme temperatures of SiC growth.

First reports on the extension of the planetary design to the much higher temperatures of SiC epitaxial growth were reported by Burk in 1997 [43, 44] for a 7×35-mm and 7×2-in. warm-wall configuration. In the warm-wall configuration shown in Figure 4.3, a passively heated insulating ceiling is used. The temperature of the ceiling's bottom surface is determined by the thickness and thermal conductivity of the insulation, radiative and conductive heating from the susceptor, and conduction through a gas present in a thin gap between the back of the insulated ceiling and a water-cooled flange. The conductivity of this gap can be actively controlled by varying the relative concentrations of hydrogen and argon gas in the gap. To minimize susceptor mass, and thereby reduce thermal cycle times, mechanical rotation is used for the susceptor, and gas is used only to rotate the wafer holders. Initial growth rates for this warm-wall configuration were relatively low, between 2 and 5 μm/h [43, 44]; however, specular morphology, reasonable background doping ($\sim 1 \times 10^{15}$ cm^{-3}), and 2% σ/mean thickness and 8% σ/mean doping intrawafer uniformity were cited for 8×100-mm wafers [45]. The latest results for a significantly scaled up 8×150 mm warm-wall reactor are reported in [2, 11] and Section 4.6.

4.5.1 Rapidly Rotating Reactors

Rupp [46] successfully extended his single-wafer, rapidly rotating, cold-wall reactor to 6×2-in. configuration for Schottky layer production. Further scaling of this configuration, however, presents many challenges. In SiC epitaxial growth, cold-wall reactors in general have suffered limited growth rate (<5 μm/h) and poor layer uniformity due to significant silicon supersaturation in the gas phase [47]. This is caused by silicon's very low vapor pressure, at temperatures at which silane is readily decomposed ($\sim 10^{-9}$ Torr at ~900 °C). Supersaturation can also result in morphology degradation if the ensuing Si and SiC clusters come into contact with the wafer surface. Silicon supersaturation can be significantly reduced by using a "hot-wall" configuration; however, until recently, this was not implemented in the rapidly rotating reactor as the reactor is designed to have the gases enter uniformly through

the ceiling, making pre-reaction and clogging very problematic if heated. Another challenge for the rapidly rotating reactor is that planetary rotation is not likely to be achieved due to the enormous centripetal forces from the >500 RPM required to obtain stable and laminar flow patterns for consistent and uniform epitaxial growth and depending upon *in situ* wafer flatness, wafers can literally fly off of the susceptor.

4.5.2 Horizontal Hot-Wall Reactors

Horizontal hot-wall reactors evolved from small single wafer reactors but have been successfully scaled up to as large as 3 × 150 mm configuration including the addition of planetary rotation, using gas levitation for susceptor and wafer rotation [48, 49]. These reactors historically reported the best combination of purity (low background doping concentration <1E14 cm^{-3}), layer thickness uniformity, and defectivity (~<0.25 defects/cm^2), particularly for epitaxial layers with thickness greater than 100 µm [2].

Our latest in-house 3 × 150 mm hot-wall results are shown in Figure 4.4. While having challenges regarding edge doping uniformity (Table 4.1), they have demonstrated the ability to maintain good defect densities and 5 × 5 mm useable areas (killer defect [KD] free area for 5 × 5 mm device die) for epitaxial layers of greater than 100 µm thickness [2], enabling the pilot-line production of 10 kV SiC power devices with high yields. As shown in Figure 4.5, even the much higher throughput 8 × 150 mm warm-wall reactor have demonstrated 6.5 kV suitable layers with similar, 89% 5 × 5 mm useful areas showing a path to future production of higher power devices [1].

Externally, Hochbauer et al. reported on a 3 × 150 mm Tokyo Electron Ltd. (TEL) hot-wall reactor with 0.68% sigma/mean thickness and 4.92% doping uniformity with a 5-mm edge exclusion and fixed cycle times as low as 1.5 hours (excluding epitaxial growth time) [53]. Wada et al. [54] have also reported on a custom made 3 × 150 mm hot-wall horizontal hot-wall reactor with equally impressive 1.9% sigma/mean thickness and 2.2% doping uniformity trade-off but without independent wafer rotation, <0.1 defects/cm^2 and 99% 5 × 5 mm useful area for albeit thin, 10 µm-thick, epitaxial layers. While certainly possible, further scaling of the horizontal configuration to 3 × 200 mm capacity, where, as mentioned previously, the carrier gas has to flow longitudinally over two or more wafer diameters while still maintaining optimum epitaxial growth conditions, may result in higher than desired carrier gas flow and cycle time requirements.

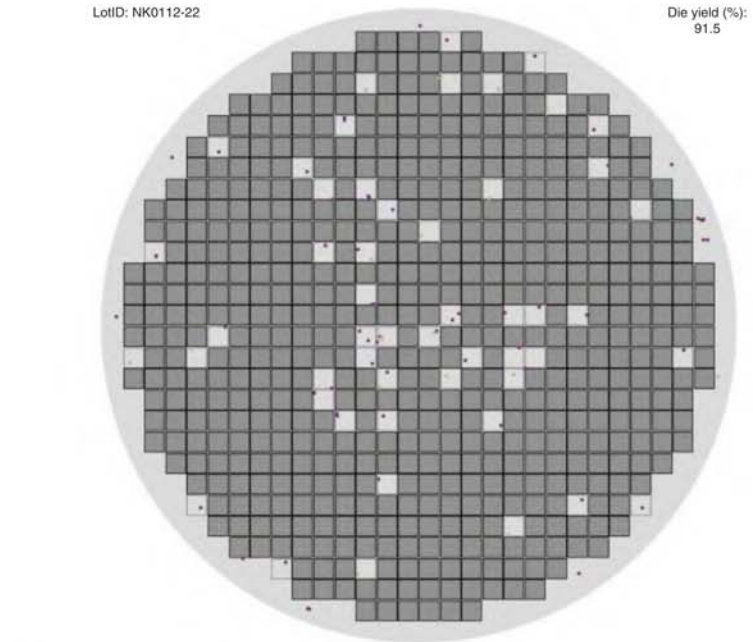
4.6 Latest High-Throughput Epitaxial Reactor Status

Of course, many of the above reactors were considered state-of-the-art, high-capacity, and even high-throughput reactors for their time. Table 4.1 includes a list of the salient properties for several of these production proven

Table 4.1 SiC epitaxial growth reactor comparisons.

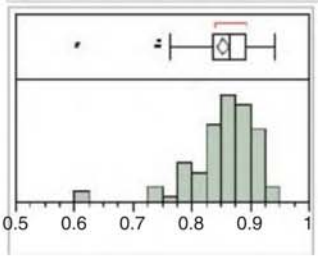
Reactor family	Wolfspeed planetary warm-wall reactors				Wolfspeed hot-wall		Rapidly rotating vertical	
Reactor	**7 × 35-mm**	**8 × 100-mm**	**8 × 150-mm (manual)**	**5 × 200-mm (automated) (projection!)**	**3 × 150-mm**	**3 × 150-mm (automated) (projection!)**	**1 × 150 (automated)**	**1 × 200-mm (automated) (projection!)**
Reference(s)	[45]	[45]	[2]	[50]	[2]	na	Current [51, 52]	na
Wafer count per run (capacity)	7	8	8	5	3	3	1	1
Wafer OD (mm)	35	100	150	200	150	150	150	200
Single wafer area (cm^2)	10	79	177	314	177	177	177	314
Single useful wafer area (cm^2[a])	4.9	63.6	153.9	283.5	153.9	153.9	153.9	283.5
Total useful wafer area (cm^2[a])	34	509	1232	1418	462	462	154	284
Growth rate (mm/h)	3	10.0	45	60	14	20	60	60
Approximate fixed heat/cool cycle time (h)	1.00	3.00	2.00	0.75	5.50	1.00	0.38	0.38
Unloading/loading time	0.50	0.50	0.50	0.19	0.50	0.25	0.08	0.08
Total time per 17-μm thick epi run, h (~1200 V blocking + buffer)	7.17	5.20	2.88	1.22	7.21	2.10	0.75	0.75
Yielded cm^2 of 17 mm-thick epi/day	84	1712	7487	20 317	1120	3848	3594	6620
Normalized 17 μm layer throughput	**1**	**20**	**89**	**242**	**13**	**46**	**43**	**79**
Thickness uniformity (% sigma/mean)	2.4	2	1.17		1.03		1.3	
Doping uniformity, 5 mm EE (% sigma/mean)	3.6	8	4.99		11.7		2.6	
Defectivity[b] ("killer" defects/cm^2) (Candela CS20 or equivalent)	~5	~2	0.29		0.47		<~0.1[d]	
% 5 × 5-mm useful area (Candela)	na	na	93.0		90.5		na	
% 5 × 5-mm useful area (SICA KD4[c])	na	na	95.3		93.4		>~98[d] [52]	
% 5 × 5-mm useful area (SICA KD1[e])	na	na	83.9		78.8		na	

a) 5 mm edge exclusion. Assuming 90% each for % Uptime, % Production, and % Yield to epi specification.
b) Calculated by Poisson equation.
c) Lasertec System 88 (Triangles + Falldown).
d) Lasertec SICA (Triangles + "Large" Pits + Diagonal).
e) Lasertec System 88 (Triangles + Carrots + Falldown + Particles).



Distributions Type=10kV MOS

5x5_ALL



Quantiles		
100.0%	maximum	0.942
99.5%		0.942
97.5%		0.93248
90.0%		0.913
75.0%	quartile	0.8915
50.0%	median	0.864
25.0%	quartile	0.835
10.0%		0.7827
2.5%		0.66353
0.5%		0.605
0.0%	minimum	0.605

Summary Statistics	
Mean	0.8538229
Std Dev	0.0569861
Std Err Mean	0.0058161
Upper 95% Mean	0.8653694
Lower 95% Mean	0.8422765
N	96

Figure 4.4 Candela optical surface analyzer (CS20) defect map and typical defect distribution for 100 μm thick epi wafers from a 3 × 150 hot-wall epi reactor averaging 85% useful area.

high-throughput reactor configurations along with more modern developments and as will be discussed later, projections for 200 mm diameter capability. The projections assume the same 90% uptime, percent product time, and yield to epi layer specification so are only approximations. We do include the latest reported uniformity, defectivity, and cycle times and attempt to project reasonable cycle times when scaling to 200 mm diameter wafers.

There are many different ways to achieve high epitaxial layer areal throughput. First and most desirable is increasing wafer diameter as that has the greatest direct benefit to device processing costs, which accrue on a per wafer basis almost regardless of the actual die count per wafer. Second would be the epitaxial reactor

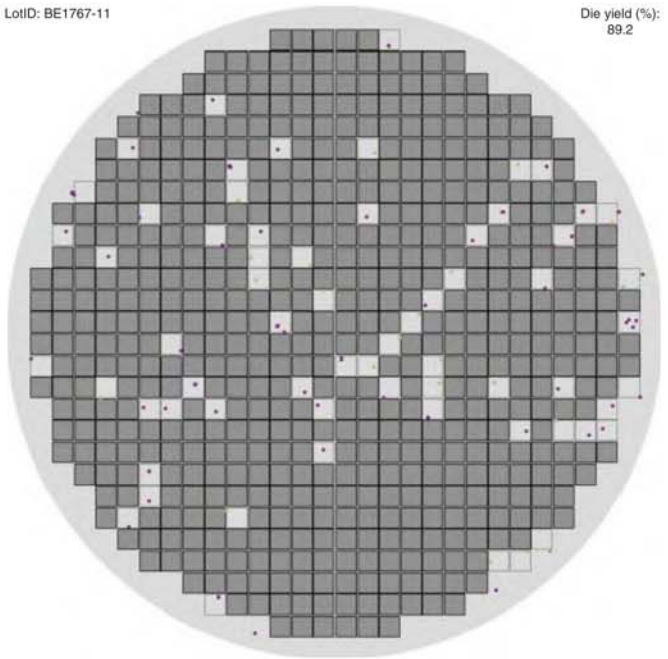


Figure 4.5 Candela optical surface analyzer (CS20) defect map for an example 65 µm thick epi wafer from a 8 × 150 warm-wall epi reactor with 89% useful area.

capacity (number of wafers of a certain size per run). The third typically addressed and included here is increased epitaxial layer growth rates. However, given the high 1600 °C temperatures, significant heat up and cool down times can dominate overall growth run cycle times particularly for thinner epitaxial layers. These "fixed" cycle times can be reduced somewhat by automation, but most importantly, can be cut in half by allowing 600 or even 900 °C temperature hot loading and unloading. Heat up times can of course be reduced to a point with increased heater power, however, at the risk of thermal shock to reactor components and larger capacity reactors already tend to have much more thermal mass. For all reactors, the passive cool-down driving force (ΔT) is naturally reduced in the final stages of cooling well before wafers can be manually manipulated. Automation has been emphasized first in single and lower capacity wafer reactors perhaps in an attempt to catch up to the inherent through-put advantage of higher capacity multi-wafer reactors); however, automation [50] is now being applied to these too.

In addition, any of the reactors described in this paper could be combined in a cluster of two or more growth chambers for certain hardware and cost efficiency, but for truly independent operation, it is assumed that any cost savings per chamber would be modest (and likely similar for competing reactor styles), so comparisons in Table 4.1 have been made for single reactor chambers only. Not included but very important for eventual real-world cost consideration is of course the footprint of a given reactor and capital cost.

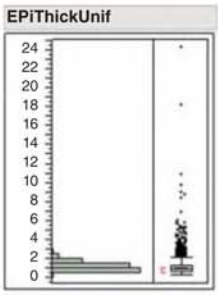
4.7 Benefits and Challenges for Increasing Growth Rate in all Reactors

Increasing growth rate obviously offers important throughput benefits for all wafer sizes and reactor configurations particularly for thicker layers where the fixed cycle times are less significant. Layer defectivity, however, can increase if supersaturation limits are exceeded and/or surface adatom diffusivity is inadequate for the rate, causing stacking faults and other defects to increase [55]. Increasing temperature to counter these undesirable trends can unfortunately cause dislocation etch pitting and subsequent defectivity [56–58]. Despite this, horizontal hot-wall reactors had already demonstrated increased growth rates [24] reportedly as high as 18 μm/h. [25]. Extreme growth rates as high as 250 μm/h by Ito [59] have been reported in horizontal hot-wall reactors and 380 μm/h by Ellison et al. for high temperature chemical vapor deposition (HTCVD) [60]. Despite these promising demonstrations, there have been no reports that these impressive growth rates have been extended to large diameter or multi-wafer production reactors. Most conventional epitaxial growths are still typically performed at 1600 °C at approximately a tenth of these rates, likely due to the remaining (and increasingly stringent) device layer defectivity requirements.

4.8 Increasing Wafer Diameters, Device Processing Considerations, and Projections

Given the current 150 mm diameter SiC wafer standard, increasing wafer diameter to 200 mm alone would nearly double the number of device die per wafer if the epitaxial layer uniformity and defectivity requirements can still be satisfied. Moreover, in true production quantities, even larger area SiC epitaxial wafers should eventually represent the same or less epi cost per unit area (and represent only a quarter of the final device cost).

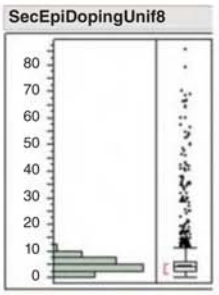
Table 4.1 includes some projections for automated growth on 200 mm wafers (to compare to the results from the current 150 mm state of the-art). All of the configurations included in the table show significant increases in areal throughput. On balance, the factors discussed in this paper still favor the throughput of high-capacity, multi-wafer, larger diameter epitaxial growth reactors in SiC epitaxy, particularly the 8 × 150 mm (and projected 5 × 200 mm configuration) Planetary reactor [2]. Figure 4.6, shows the thickness, doping, and defectivity distributions for a subset of over 10 000 150 mm wafers we have grown in our 8 × 150 mm reactors. Good thickness 1.17% and doping 4.99% uniformity (5-mm edge exclusion) were achieved. While not shown, long-term run-to-run reproducibility is 1.01% and 5.13% for thickness and doping, respectively. About 93% 5 × 5 mm useful Candela (CS20) KD areas, 83.9% Lasertec System 88 KD1 (the sum of Triangles, Carrots, Fall-down and Particles), and 95.3% KD4 (Triangles + Falldown) were also observed. Not surprisingly, the newer Lasertec optical surface analyzer is able to detect more defects (even down to nm-scale dimension [not shown here]), but by our experience



Quantiles		
100.0%	maximum	24.3261
99.5%		3.21567
97.5%		2.26916
90.0%		1.74216
75.0%	quartile	1.38851
50.0%	median	1.06369
25.0%	quartile	0.82942
10.0%		0.67625
2.5%		0.56001
0.5%		0.4868
0.0%	minimum	0.40124

Summary Statistics	
Mean	1.166179
Std Dev	0.5674098
Std Err Mean	0.0050397
Upper 95% Mean	1.1760576
Lower 95% Mean	1.1563004
N	12676

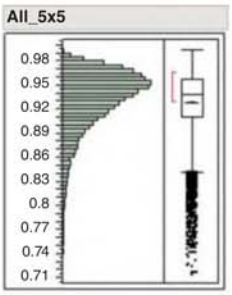
(a)



Quantiles		
100.0%	maximum	86.2173
99.5%		28.6643
97.5%		9.96893
90.0%		8.13336
75.0%	quartile	6.48186
50.0%	median	4.41972
25.0%	quartile	2.90201
10.0%		1.87066
2.5%		1.13586
0.5%		0.77486
0.0%	minimum	0.46592

Summary Statistics	
Mean	4.9906104
Std Dev	3.9028877
Std Err Mean	0.0348472
Upper 95% Mean	5.0589162
Lower 95% Mean	4.9223045
N	12544

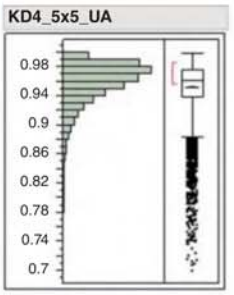
(b)



Quantiles		
100.0%	maximum	0.995
99.5%		0.987
97.5%		0.98
90.0%		0.97
75.0%	quartile	0.958
50.0%	median	0.94
25.0%	quartile	0.912
10.0%		0.877
2.5%		0.823
0.5%		0.767
0.0%	minimum	0.715

Summary Statistics	
Mean	0.9297025
Std Dev	0.0399522
Std Err Mean	0.0003549
Upper 95% Mean	0.9303981
Lower 95% Mean	0.9290069
N	12676

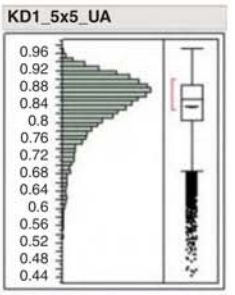
(c)



Quantiles		
100.0%	maximum	1
99.5%		0.99604
97.5%		0.99167
90.0%		0.985
75.0%	quartile	0.97667
50.0%	median	0.96333
25.0%	quartile	0.94
10.0%		0.91
2.5%		0.85333
0.5%		0.78333
0.0%	minimum	0.7

Summary Statistics	
Mean	0.9531921
Std Dev	0.0361778
Std Err Mean	0.0003214
Upper 95% Mean	0.953822
Lower 95% Mean	0.9525622
N	12674

(d)



Quantiles		
100.0%	maximum	0.97333
99.5%		0.94833
97.5%		0.93333
90.0%		0.91167
75.0%	quartile	0.88833
50.0%	median	0.855
25.0%	quartile	0.80833
10.0%		0.74833
2.5%		0.65
0.5%		0.56229
0.0%	minimum	0.445

Summary Statistics	
Mean	0.8391032
Std Dev	0.0706564
Std Err Mean	0.0006276
Upper 95% Mean	0.8403334
Lower 95% Mean	0.8378729
N	12674

(e)

Figure 4.6 Epitaxial layer distributions for over 10 000 150 mm epitaxial wafers grown in our 8 × 150 mm warm-wall epi reactors; (a) thickness uniformity (% σ/mean), (b) doping uniformity (% σ/mean), (c) Candela CS20, (d) Lasertec System 88 KD4, and (e) KD1 5 × 5 mm useful areas.

entitled device yield is reasonably well predicted by both the total Candela CS20 and Lasertec KD4 counts. Similar to these results, Epi World has generously provided in a private communication (G. Feng and Epi World, private communication) very similar uniformity values of 1.32% and 4.95% for thickness and doping, respectively, and 98% 2 × 2-mm useful areas (projected to be ~88% @5 × 5-mm by the Poisson equation) for over 5000 150 mm epi wafers.

Mauceri et al. [61] reported 30 μm/h growth rates and 10 μm thick 150 mm Schottky wafers with 1.1% thickness and 2.7% doping uniformity with <0.5 defects/cm^2 grown in "less than one hour" utilizing automation and 900 °C hot loads in a LPE PE1O6 hot-wall reactor. In a private communication, D. Crippa [62] relayed that a 200-mm cassette-to-cassette epitaxial reactor will be developed and ready for installation by the second quarter of 2020 as part of the European REACTION project. TEL and users [53, 63] have also reported on 3 × 150 mm automation incorporating hot loads in *Probus*™ horizontal hot-wall reactors but have not yet commented on 200 mm solutions.

In a re-emergence of rapidly rotating single wafer-epi reactors, Tsuchida et al. [64] and later Daigo et al. [51, 65] and Showa Denko (SDK) [52] have adapted single wafer rapidly rotating reactors to incorporate a hot wall with the ceiling apparently sufficiently removed and cool enough to avoid previously experienced Si-condensation, parasitic deposition, and fall down [40]. Regardless of the mechanism, this has resulted in greatly reduced defectivity and reportedly enabled the growth of several millimeters of epi before requiring maintenance at >50 μm/h growth rates. Even though currently *(and probably)* limited to single wafer configuration (150 mm diameter with as of yet unconfirmed plans for 200 mm), the incorporation of automation for very quick (few minutes) and also 900 °C hot loading for short fixed heat and cool cycle times (23 minutes) makes the total time per epitaxial wafer growth 37 minutes for a 10-μm thick layer. As shown in Table 4.1, this suggests throughput is within a factor of 2 of the higher capacity manually loaded multi-wafer planetary reactors. An estimated scaling to 1 × 200 mm would match the throughput of the manual 8 × 150 mm planetary reactor. Moreover, Showa Denko (SDK) recently presented a very impressive 280-μm thick epitaxial wafer with only one visible defect on an entire 100 mm wafer [52] reportedly using a *NuFlare*™ reactor [51].

As mentioned previously, throughput enhancement from automation or hot loads can in theory be equally well applied to a multi-wafer reactor (e.g. an 8 × 150 mm or projected 5 × 200 mm planetary warm-wall reactor in Table 4.1) [50]; however, given the significant capital expense of all production reactors, this will only be cost effective if epitaxial wafer demand supports full epitaxial wafer loads and efficient capacity utilization. Also, if new epitaxial wafer layer requirements cannot be met by any configuration with high yield, this will obviously detract from the basic throughput projections provided here. The yield of key attributes such as epitaxial layer uniformity, reproducibility, flatness, surface roughness, defectivity, and dislocation density to specification can dramatically impact the effective throughput of epitaxial reactors to a required specification (Figure 4.7).

With regard to morphological defectivity and crystallographic dislocations, even with great advances in metrologies, such as confocal optical microscopy

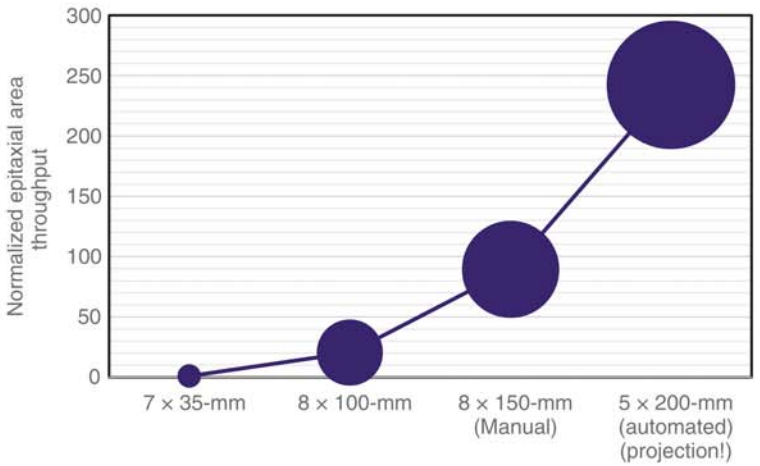


Figure 4.7 Normalized plot of epitaxial area throughput vs. SiC warm-wall reactor generation (data label diameter is proportional to the wafer diameter).

and photoluminescence by Lasertec (https://www.lasertec.co.jp/en/products/environment/sic/sica88.html) and X-ray topography by Rigaku (https://www.rigaku.com/en/products/xrm/xrtmicron), details of which are beyond the scope of this chapter, it is still perhaps not surprising that predicting the suitability of a particular epitaxial layer growth process is not a simple matter. Defects are by nature highly variable in morphology impacting both identification and counting for differing generations of metrology hardware and analysis recipes and subsequent correlation with device yield [15]. There is often sufficient ambiguity and interactivity with various device manufacture processes and design that only the final device yield and performance of a given tuned epi process can conclusively determine the suitability for a particular device type (or even for different manufacturers of the same device type). There are of course cost trade-offs between epitaxial layer yield to needed layer specifications but given that the majority of device processing cost occurs after epitaxy, ultimately these allow little room for epitaxial layer specification relief.

4.9 Summary

The development of SiC epitaxial growth for industrial-scale production has been reviewed from small home-made quartz reactors to modern multi-wafer reactors capable of supporting commercial device production. The highest-throughput device-qualified manual SiC epitaxial growth reactor developed to date is capable of growth upon eight 150-mm wafers at a time at 45 μm/h. The layers produced by this reactor exhibit specular morphology, high purity, and good uniformity. Long-term run-to-run reproducibility is 1.01% for thickness and 5.13% for doping [2].

Epitaxial area throughput has been increased by almost 2 orders of magnitude from that of the earliest 7 × 35-mm configuration while increasing layer quality and

uniformity. Particularly for layers of ~50 μm or less, where epitaxial run cycle time considerations dominate growth rate limitations, thus far the warm-wall planetary configuration has had the superior overall throughput enabling economical SiC device production. It is projected that even a scaled, manually loaded 5 × 200 mm epitaxial reactor could double throughput yet again, and if needed, will likely be capable of growing thicker epitaxial layers for higher voltage power devices [1].

This production capability, however, has now been significantly challenged by epitaxial reactor automation and hot loading even in single-wafer reactors but this too is being developed on multi-wafer reactors for yet higher throughputs. Regardless of the ultimate configuration for 200 mm diameter epitaxial wafer production, and despite ever tightening epitaxial layer requirements, current developments in SiC epitaxial layer reactors and processes still promise factors more epitaxial layer throughputs and hence significant cost reductions over the next few years.

Acknowledgment

The authors appreciate the significant contributions of the hard-working process engineers and technicians who operate and characterize our epitaxial layer wafer production and our internal and external device customers for helping us to build this successful SiC power device market.

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5

Status of 3C-SiC Growth and Device Technology

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5.1 Introduction, Motivation, Short Review on 3C-SiC

The cubic polytype of silicon carbide (3C-SiC) has attracted particular interest since the early days of research and development in the field of SiC technology. Knippenberg [1] elaborated already in the year 1963 in detail stability criteria for the growth of various SiC polytypes and presented process conditions that favorably lead to the formation of 3C-SiC. Later, this work was further elaborated by Fissel [2] who presented in the year 2000 a comprehensive study on thermodynamic considerations of the epitaxial growth of SiC. From the point of view of electronic device applications, the cubic polytype of SiC was considered in the 1980s and 1990s because of the greater electron mobility compared to the hexagonal counterparts, i.e. 4H-SiC and 6H-SiC (Table 5.1).

From a crystal growth point of view, the process development progressed much faster for the hexagonal polytypes 6H-SiC and 4H-SiC which is the main reason that the 4H-SiC is being applied as state of the art in Schottky-junction diodes (SJD) as well as in power switches based on metal oxide semiconductor field-effect transistors (MOSFET). The interest in the cubic polytype, however, remained high throughout the years. The 4H-SiC metal-oxide-semiconductor (MOS) interface exhibits a high defect density in the upper band gap of 4H-SiC and a limited long-term stability. Due to the smaller electronic band gap of the cubic polytype, those interface-related electron traps are mainly located in the conduction band of 3C-SiC and, hence, enable better device performance in the mid-voltage regime of 300–800 V devices [14–16]. Up to date, the major barrier for the application of 3C-SiC in power electronic devices

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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Table 5.1 Physical properties of Si, 3C-SiC, 6H-SiC, and 4H-SiC [3–13].

	Si	3C-SiC	6H-SiC	4H-SiC
Lattice parameter (Å)	5.43 cubic	4.36 cubic		$a = 3.08$ hexagonal
E_G (eV)	1.1	2.36	2.98	3.2
E_B (10^5 V/cm) at $N_D = 5{\cdot}10^{15}$ cm^{-3}	3	15	22	23
n_i (cm^{-3}) at 300 K	$1{\cdot}10^{10}$	$1.5{\cdot}10^{-1}$	$1.6{\cdot}10^{-6}$	$5{\cdot}10^{-9}$
λ (W/cm K)	1.5	3…5	3…5	3…5
v_S (10^7 cm/s)	1	2	2	2
μ_n (cm^2/V s)	1500	900	370	800
μ_p (cm^2/V s)	480	40	80	120
E_D (meV)	45 (P)	48 (N)	71/124 (N)	52/92 (N)
E_A (meV)	44 (B)	242 (Al)	242 (Al)	242 (Al)
ε	11.7	9.7	9.6	9.6
T_S (°C)	1420	2830	2830	2830

is related to the lack of high-quality large wafer material that serves as the basis for the electronic device manufacturing process.

In recent years, further potential applications of 3C-SiC originated that make use of its unique physical properties. 3C-SiC co-doped with the deep boron acceptor and shallow nitrogen donor is a strong candidate for an intermediate band solar cell material that may reach a theoretical light conversion efficiencies above 50% [17, 18]. In addition, p-type doped 3C-SiC using the acceptor aluminum is intensively studied for the application in solar-driven electrochemical water splitting [19, 20]. Beside the hexagonal polytypes, also cubic SiC is under research for the future application in quantum computing [21]. The intentional incorporation and tailoring of point defects during growth of 3C-SiC as well as their annealing behavior have been demonstrated by Schöler et al. [22, 23]. Other important applications of 3C-SiC related to its chemical inertness and mechanical hardness lie in the field of biomedical coating and in general for sensing. In the latter cases, also microcrystalline layers may be applied beside single crystalline materials.

Bulk growth of 3C-SiC that could be performed with some rare, so-called small Lely platelets as seeding material, either using sublimation or solution growth, turned out to be very difficult. However, pioneering work for the nucleation and epitaxial growth of 3C-SiC on Si using chemical vapor deposition (CVD) was already performed in 1983 by Nishino et al. [24]. First attempts to grow bulk 3C-SiC also followed a hetero-epitaxial approach for the seeding process on either (100) oriented 3C-SiC layers that stem from 3C-SiC CVD deposition on Si [25, 26] or as (111) oriented 3C-SiC on (0001) oriented 6H-SiC [27]. In recent years, a number of research teams have elaborated the key process parameters that allow a stable growth of the cubic SiC polytype using sublimation growth [25–37]. Among those

process parameters, a silicon-rich gas atmosphere, a high supersaturation, and a temperature below 2000 °C are most important. The common challenges to realize bulk 3C-SiC are related to the 3C-SiC nucleation and preservation of the 3C-SiC polytype throughout the growth process. Often stacking faults (SFs), double positioning boundaries (DPBs), and anti-phase boundaries (APBs) alter crystalline quality and limit the technological application of 3C-SiC in electronic devices. Regarding the planar defects like SFs and APBs, a significant reduction and even elimination was demonstrated when 3C-SiC nucleation that was carried out on undulant, off-axis (100) oriented Si substrates was already presented [38]. For a review of hetero-epitaxial growth of 3C-SiC layers on Si substrates, see [39].

Merging the above-mentioned knowledge in literature [24–39], it is concluded by the authors of the current work that the growth of high-quality cubic SiC may be achieved by the application of high-quality 3C-SiC template layers initially grown by CVD on (100) silicon followed by a physical vapor sublimation growth method.

In this overview paper, recent progress in the fabrication of large area 3C-SiC substrates and homo-epitaxial layers with a diameter of 100 and 150 mm as well as electronic device processing will be presented. In Section 5.2, the main problems of the hetero-epitaxial process (defects and stress), the evolution of defects and the interaction of different defects, and the effect of these defects on the electrical characteristics of the material will be reported. Section 5.3 discusses the different processes to realize bulk 3C-SiC wafers. In Section 5.4, the main developments on the processing of 3C-SiC for the realization of power devices will be reviewed.

5.2 Nucleation and Epitaxial Growth of 3C-SC on Si

5.2.1 Growth Process

The scientific and technological attraction to 3C-SiC dates back to 1959, when Spitzer et al. [40] published the first report of 3C-SiC growth on a silicon wafer by heating the silicon with a gaseous hydrocarbon. This paper represents the first milestone in 3C-SiC hetero-epitaxy on Si. Later, the real breakthrough in the 3C-SiC/Si hetero-epitaxy was achieved in 1983, when Nishino et al. [24] proposed a multi-step CVD process able to improve the crystal quality in the 3C-SiC epilayers. Their method for the 3C-SiC growth was composed of three different steps: (i) an etching process by flowing HCl at 1100 °C was performed in order to prepare the Si substrate surface; (ii) a buffer layer growth, necessary to obtain good SiC crystal quality, was performed at 1360 °C for a short time under propane (C_3H_8) flow; and (iii) the crystal growth with both silane and propane was carried out at 1330 °C under a flowing H_2 carrier gas. Using this recipe, a single-crystal 3C-SiC layer can be grown on the buffer layer, which is used as the seed for subsequent SiC growth. Coined the “buffer layer method” as used by Nishino revitalized the race toward the ideal material for 3C-SiC electronic applications started in the 1950s. Several universities and semiconductor R&D departments industries tried to improve the scientific knowledge and to develop and optimize an industrial growth process after 1982. Researchers have obtained many improvements due to

their efforts in following many different paths in the labyrinth of 3C-SiC chemical vapor deposition. SiC reactors growing on Si are complicated and a wide range of parameters are involved in the growth process, such as temperature, gaseous precursor composition, pressure, and gaseous partial pressures. A huge number of published works, not only by CVD but also by sputtering or molecular beam epitaxy (MBE) [41, 42], are devoted to the growth of SiC on Si. Over the decades, CVD reactor development involved the enlargement of the reaction chamber allowing epitaxial growth on Si wafers with a diameter of 200 mm (8 in.) [43].

Among many variables, the composition of the *gaseous precursors* is crucial in determining which will be the experimental conditions of several parameters inside the CVD reaction chamber in order to achieve good quality 3C-SiC films. This is of course related to the different behavior of reactants in their dissociation from gaseous phase molecules to solid phase adatoms that will arrive, migrate, and bond with the dangling bonds available at substrate surface steps or terraces. An overview of possible reactions can be found in literature [44–46]. Thus, changes in gaseous precursor chemistries will determine significant differences in the growth temperature range, in the gas partial pressures during the growth, and in the cracking efficiency of reactant species in the gaseous phase. The temperature of gasses determines the rate of production of the various radicals. For instance, in the silane–propane system, a widely used chemistry for SiC CVD epitaxy, silane dissociates at a lower temperature than propane. This means that, as the chamber is heated up to growth temperature, the effective C/Si ratio changes so that the real amount of adatoms to form SiC film is unknown. As a consequence, due to the higher thermal stability of CH species compared to the SiH ones [47], the growth process requires a higher amount of C-containing supply in the gas phase to obtain stoichiometric SiC. On the other hand, being Si the reaction-limited element in the gas phase participating to the reaction, a linear dependence of the growth rate on the Si-precursor gaseous flux is commonly observed.

The dependence of the growth rate with the Si/H_2 ratio is reported in Figure 5.1. From this plot, the linear dependence is clearly evidenced. Moreover, a strong dependency of both parameters with the total pressure can also be observed [49]. In detail, the higher the reactor pressure, the steeper the experimental slope. The higher growth rate at lower Si/H_2 ratio for pressure regime above 200 Torr (eventually at atmospheric pressure) is related to the lower gas velocity and to the longer time that adatoms need to reach the solid surface. When the pressure is reduced, the gas velocity increases and more Si (higher Si/H_2 ratio) is required to maintain the same growth rate.

However, the silane–propane system is affected by homogeneous gas phase nucleation, where solid/liquid particulates (usually of Si) are formed in the gas phase. This phenomenon causes the depletion of the gas phase precursor available for the deposition and the worsening of the surface quality, due to particulates impinging on the deposition surface. To remove the homogeneous gas phase nucleation, the use of chlorinated silicon precursors, or simply the addition of HCl, was suggested [50–53]. Using these precursors, it is possible to obtain a high growth rate (30 μm/h) at low temperature (1370 °C) [54].

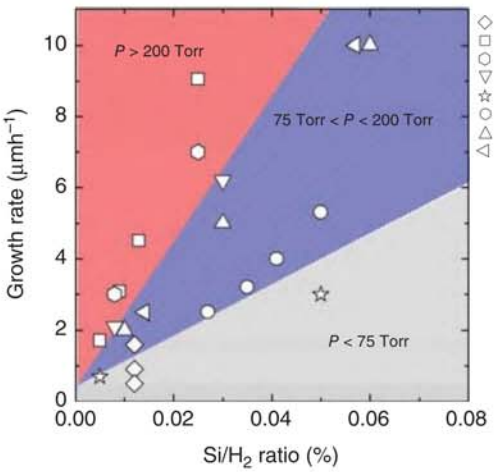


Figure 5.1 Dependence of the growth rate with the Si/H2 ratio. This dependence is strongly influenced by the total pressure within the reaction chamber. Growth temperatures used are similar. Source: Severino [48]. © 2012, Andrea Severino.

Since before Nishino et al. introduced the two-step growth method for the 3C-SiC hetero-epitaxy on Si by CVD, a relevant interest was placed on the effect of a hydrocarbon gas on a Si surface at high temperatures. Different models and experimental observations were proposed in the 1970s, with the evidence that a thin 3C-SiC layer was formed on a Si surface by the conversion of Si into SiC.

Even though single-crystal 3C-SiC films have been obtained by the two-step CVD technique, the SiC/Si interface remains a plague due to the formation of voids in the Si substrate. Voids are usually hollow inverted pyramids, with the shape depending from the orientation of the substrate, lying just beneath the interface. Their presence poses a severe problem in several applications based on 3C-SiC hetero-epitaxy such as hetero-junction bipolar transistors or hetero-junction solar cells with 3C-SiC emitter layer as these devices require an excellent interface morphology. In a work published in 2007 [55], author's group has correlated void density and size with the process temperature and reaction time for 3C-SiC buffer layer formation on differently oriented Si substrates. A statistical study of voids at the interface has been conducted as a function of the process temperature for the buffer layer formation. First, the temperature strongly influences the surface and interface morphology and the film thickness with the observation of an incomplete film formation and occurrence of cavities in the substrate if the temperature is too low. Void shape is, as expected, strictly related to the orientation of the silicon substrate used for the growth. In a diamond cubic crystal structure such as for Si, the atomic lattice packing density and the available bonds in the crystallographic plane strongly affect both the removal and the addition of the atoms on the surface. Voids on the silicon surface during the growth of a 3C-SiC layer could be seen as an etching process of atoms from the substrate contributing to the formation of the growing 3C-SiC layer. The (111) oriented Si surface shows the highest atomic packing density, which is less for the (001) Si surface and is even less dense for the (110) Si surface. Since etch and deposition rates depend on this density, one would expect a faster process in the ⟨110⟩ direction than in the other directions. This assumption is confirmed by measurements, in which the thicknesses of 3C-SiC films grown at 1120 °C are reported as a function

of reaction time and the highest growth rate corresponds to the (110) surface [55]. The trend found here predicts a squared dependence of the thickness vs. the process time, suggesting that the reaction is limited by the diffusion of one of the species (atoms of Si in 3C-SiC buffer layer) involved in the growth.

In a recent paper [56], it has been shown that the main parameter for the reduction of voids at the interface is the C/H ratio. In fact, increasing the C/H ratio the voids density decreases and finally even voids free interface can be obtained. With this process even the density of the carbonization layer increases and the morphology of the layer is largely improved resulting more flat.

Another step that has a large impact on the final quality of the grown layer is the buffer layer grown during the temperature ramp between the carbonization step and the growth one [56]. In fact, it has been observed that the ramp time can have a large impact on the reduction of the final stress, [56] while the C/Si ratio in this step can have an impact on the formation of protrusions in the layer [57].

5.2.2 Defects

Considerable efforts have been made to improve the quality of CVD-grown 3C-SiC. Significant reduction in the defect density in cubic SiC thin films has come with the introduction of a buffer layer [58–60] and the use of patterned Si substrates [38, 61–63], but has also introduced new problems during the growth. The CVD process suffers from an intrinsic drawback, whereby, at typical growth temperatures, between 1550 and 1700 °C, on free-standing 3C-SiC surface diffusion limits the growth rate to approximately 100 μm/h [64]. Instead, growth on Si substrates is limited to temperatures below 1350 °C [65] with correspondingly lower growth rates. High growth temperatures are favorable, as stated above, for the reduction of defects, especially SFs.

Hetero-epitaxial growth of 3C-SiC on Si appears to be an ideal solution to obtain large wafers at low cost, but efforts must be made to reduce the density of crystallographic defects in the 3C-SiC films. Large lattice mismatches (19% at RT) and differences in the thermal expansion coefficients (TECs) (~23% at deposition temperatures and 8% at RT) between the two materials are the causes of defects.

In fact, lattice mismatch produces a misfit dislocation in every fifth SiC plane. The 5 : 4 SiC-to-Si lattice plane matching, defined as the "magic" by Long et al. [66], was reported by Ernst and Pirouz [67] for selected, away-from-voids, regions of a 3C-SiC thin layer. Li et al. [68] reported that when void-free film growth conditions were employed, this 5 : 4 match was extended over the length of the entire layer. Méndez et al. [69] observed with cross-section transmission electron microscopy (TEM) linear misfit dislocations with a density that corresponded to one dislocation on each four [70] Si planes and then on each five [70] SiC planes. These dislocations, as observed by filtered TEM micrographs, are mainly Lömer (90° type) dislocations and spaced about 1.61 nm from each other. Furthermore, the Lömer dislocations are much more efficient than a 60° type for relaxing the strain produced by the 20% lattice mismatch. However, misfit dislocations are not able to

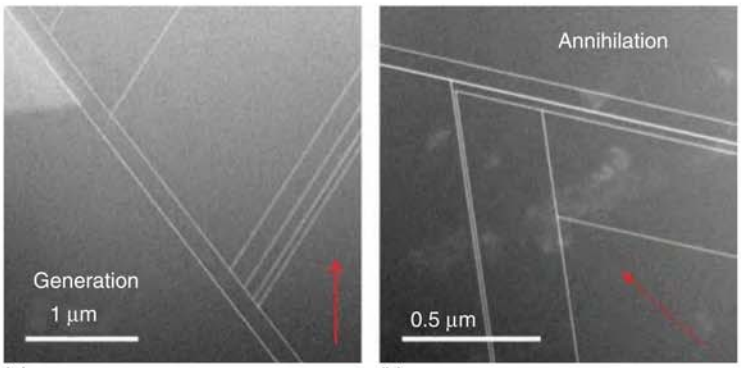


Figure 5.2 (a) STEM cross-section of a sample region where the generation process is evident. The red arrow shows the direction of the growth. (b) STEM cross-section of a sample region where the annihilation process is evident. The red arrow shows the direction of the growth.

completely relieve the residual strain generated, whereby grain misorientations and SF generation are then involved.

The 3C-SiC/Si interface gives rise to a high density of planar and volume defects, such as micro-twins, APBs, and SFs in the epilayer, and voids in Si underneath the hetero-interface. Most of these defects that are considered device killers will however reduce their density, or be annihilated, when very thick (several tens of microns) 3C-SiC epitaxial films are grown. Furthermore, the orientation of the Si substrate strongly influences the defect density and surface morphology.

The SFs are the main defects present in 3C-SiC. Their density is typically very high and, after the fast reduction of their density in the first nanometers from the interface, the density reduction is much less evident and almost a saturation occurs close to 10^4/cm [48]. This saturation occurs essentially because during the growth an equilibrium is reached between the annihilation and the generation of SFs. In Figure 5.2, these two phenomena are evident. In Figure 5.2a, one SF generates several SFs during the growth, while in Figure 5.2b from seven SFs only two survive after the annihilation process.

The SFs can interact in several ways. Two SFs can cross (Figure 5.3a) without annihilation, or a SF can close without interaction with another SF (Figure 5.3b) or finally can interact with a SF of different polarity (Figure 5.3c). Then the behavior and the interactions of these SFs are extremely different and probably depend strongly on the type of SFs and on the surface structure during the growth. A more detailed understanding of the SFs behavior is important to try to reduce this kind of defect that has been shown that has a big effect on the electrical characteristics of the material [61].

The trend of SF linear density (per unit length) as a function of the film thickness is displayed in Figure 5.4. Experimental data reported in the figure show an exponential decaying trend of SF density as the 3C-SiC film thickness increases. The reduction rate of SFs due to their self-annihilation is roughly inversely proportional to their density.

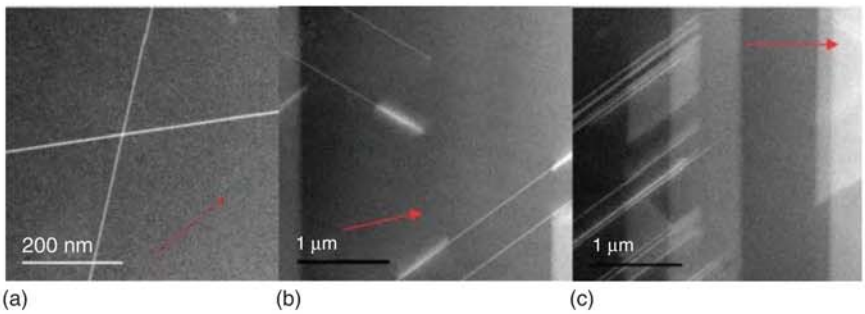


Figure 5.3 (a) STEM cross-section of two SFs crossing. (b) STEM cross-section of two SFs that are closing without annihilation. (c) STEM cross-section of several SFs stopped from a SF of different polarity.

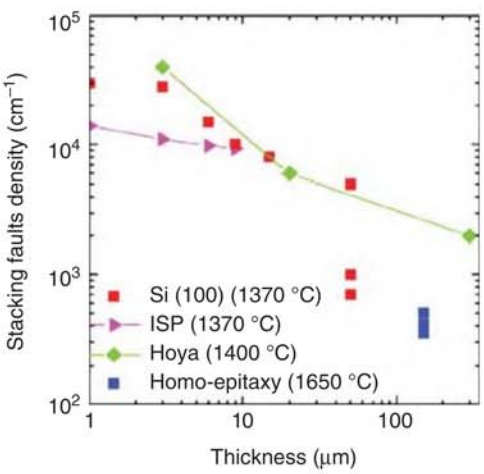


Figure 5.4 Stacking faults density vs. grown thickness. Different processes or different substrates give different SFs densities. Source: La Via et al. [71]. © 2018, Elsevier.

This statement is further supported by Polychroniadis et al. [32], where a detailed study on the propagation of SFs using TEM in cross-section is presented. The annihilation rate of SFs is high where a very dense network of SFs is detected and the mutual closure mechanism is stimulated. As the SF density decreases, SFs are much further each other so that their annihilation rate falls and their density tends to a saturation value. Furthermore, for relatively thin (<5 μm) 3C-SiC films, the APB density is high enough to ensure another closure mechanism to SFs while the density of APB in thicker films is drastically reduced so that their contribution to the reduction of SFs fails.

Using a compliance substrate as inverted silicon pyramids (ISPs)[62], a large reduction of SFs is observed for thin layer because this type of substrate concentrates SFs in small regions increasing the probability of SFs annihilation. After about 10 times the dimension of the silicon inverted pyramid (1 μm), the SFs density saturates at almost the same value of the layers grown on a flat substrate because the concentration of SFs is not working anymore.

Increasing the temperature at 1400 °C, as in the HOYA experiment [32] a further reduction of the SFs density is observed. This reduction is even larger if the silicon substrate is removed and the epitaxy process is realized at temperatures higher than the silicon melting temperature as reported in Figure 5.4 for the samples grown by CVD.

From these data, it is clear that increasing the growth temperature the SFs density decreases. In a previous paper [72], it has been shown by ab initio quantum transport calculations, that SFs give rise to highly dispersive bands within both the valance and the conduction bands that can be distinguished for their enhanced density of states at particular wavenumber subspaces. The consequent localized perturbation potential significantly scatters the propagating electron waves and strongly increases the resistance for n-doped systems. No formation of levels inside the band gap has been observed by these calculations.

In addition, it is not clear which physical mechanism causes a high leakage current when a high density of SFs is observed in the material.

The SFs can interact also with a different kind of defect: the APB. This defect is at the edge of two different domains rotated of 90° between each other.

In order to understand the behavior of the APBs, we followed one of these boundaries through a series of cross view STEM images shown in Figure 5.5 on the right.

The growth direction ([001]) is indicated in the lower part of the image. The SFs lie always in the {111} planes and in cross view STEM images (as in Figure 5.4 right side). SFs lying in the (1−11) and (−111) plane are observed as lines in the ⟨112⟩ directions while SFs in the (111) and (−1−11) are observed as almost trapezoidal shaped bright zones. In the same figure, an APB is shown. APB has different lying planes: the APB lies in (1−11) plane in the bottom image of the series then it changes to (−111) plane in the third image of the series. Moreover, in the fourth image the APB lies in (011) plane and in the top left image it lies again in the (111) plane. It is worth nothing that APBs lying in the (100) plane are also observed. Additionally, in Figure 5.4 we included a STEM plane view of an APB "running" through the surface and interacting with SFs. The plan and cross view images show APBs changing their lying plane. A detailed inspection of the image shows that the APB lying planes are only specific planes (i.e. the {111}, {011}, and {001}) and a process of faceting occurs when a GB curves. In such a way, at low magnification, it is able to "curve" through the sample. Another very important fact that can be understood from this image is that APBs and SFs strongly interact as highlighted with the white circle in the bottom left image.

Another defect that has a large influence on the growth of thick layers is the protrusion [57]. This defect is a small polycrystalline region that starts to grow in the first instants of the growth and becomes bigger and bigger increasing the thickness.

We observed that the presence of the protrusion was not strongly correlated with voids commonly observed at the SiC/Si interface. Instead, we found that seeds for protrusions lie 10 nm into the SiC layer above the SiC/Si interface. This finding indicated that protrusion seeds form during or just after the carbonization process [57].

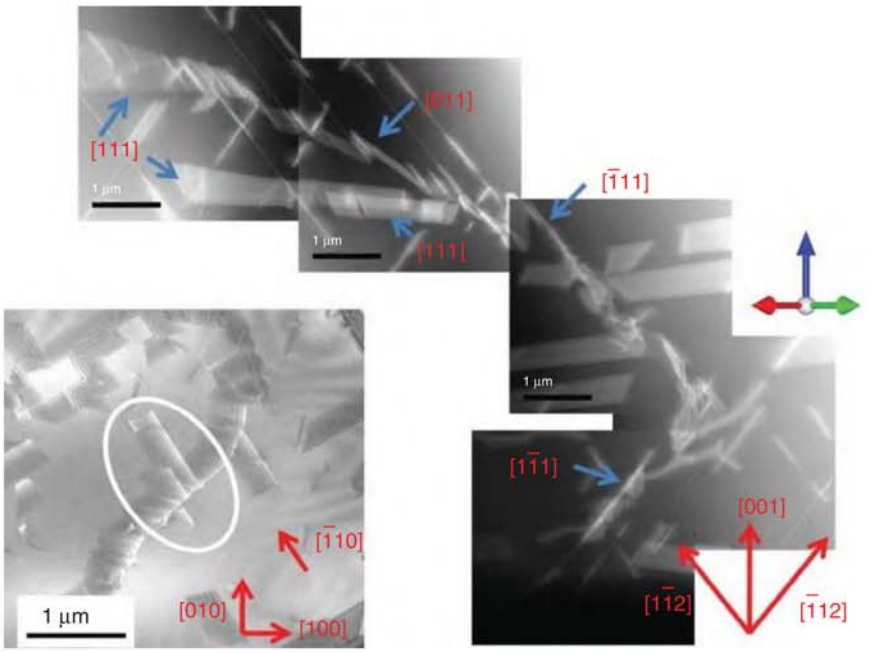


Figure 5.5 The sequence of STEM images shows an APB and its effect on SFs. Image is the projection of the lamellae in the (110) plane. The growth direction ([001]) is indicated at the bottom, the lying plane of the GB for each image is also indicated, and the scale bar is the same for all images. The growth was performed in the [001] direction and (110) is the cross view STEM projection plane. In the left bottom, a plane view STEM image shows an APB interacting with SFs in the highlighted regions.

5.2.3 Stress

Growing 3C-SiC films on a Si substrate inherently means two dissimilar materials are forced together creating several results in the subsequent epitaxy. First, a large strain is generated at the hetero-interface due to a misfit, $\Delta a/a$, of about 19.7% resulting from the difference in bulk lattice parameters of 3C-SiC and Si of 4.3589 and 5.4311 Å, respectively [46]. This strain is called the "intrinsic strain," which contributes to the residual strain field and a high density of crystallographic defects close to the interface is generated in the 3C-SiC film in order to relieve the most of it.

The large mismatch in TECs between Si and SiC is the second contribution to the strain field. The thermal strain acts mainly during the cool down from the growth temperature to room temperature. TECs of Si and SiC at room temperature are 2.77×10^{-6} K^{-1} and 2.57×10^{-6} K^{-1}, respectively, as tabulated by Slack and Bartram [73], leading to a TEC mismatch of about 8% at RT. At growth temperature, the difference in the TECs between SiC and Si increases reaching percentages above 20%, which is dependent on the growth technique used and gaseous precursors involved, but often over 1000 °C. The stress generated during the cooling down from growth temperature is of a tensile nature and causes an upward bending in the wafer and, often, the generation of cracks in the epitaxy and in the substrate. The

bending, referred to "wafer bow," depends on the thickness of the 3C-SiC epitaxy, thickness of the Si substrate, symmetry (orientation) of the epitaxial crystal and substrate, and elastic modulus.

The curvature resulting from the residual stress can be calculated using a modified Stoney equation that takes into account the film elastic relation to wafer bending: [74]

$$\sigma = \frac{M_{film}h}{\Delta R}\left(\frac{1+4mn+6mn^2 4mn^3+m^2n^4}{6mn(1+\mathrm{n})}\right) \tag{5.1}$$

where $m = M_{\mathrm{film}}/M_{\mathrm{sub}}$ is the biaxial modulus ($M = E/(1-\upsilon)$) of the film substrate and $n = t/h$, where t and h are the thicknesses of the substrate and film, respectively. The Young's modulus (E) and Poisson's ratio (ν) are related to the film orientation. ΔR is the change in curvature radius determined from $(1/R) = (1/R_2) - (1/R_1)$, where R_1 is the average radius of the substrate prior to film deposition and R_2 after the film is deposited.

A micro-machined planar rotating probe was developed for residual stress analysis to split the stress into the following two components: (i) the gradient residual stress (σ_1) related to the film defects and (ii) the uniform stress (σ_0) related to the substrate [75]. TEM characterization studies about the defect formation and the defect evolution as a function of thickness on 3C-SiC on the Si substrate revealed the problems due to the incorrect linear stress approximation in a hetero-epitaxial thin film. With FEM, an exponential approximation of the stress relationship was studied, yielding a better fit with the experimental data.

Another important aspect that has been observed in 3C-SiC and that has a large influence on both the bow of the wafer and on the use of this material for micro-electron mechanical systems (MEMS) is the variation of the Young's modulus (E) as a function of the thickness. In fact, due to the presence of a large density of defects at the interface with silicon which is slowly decreasing with the increasing of the layer thickness, the Young's modulus varies from 1.5×10^{11} Pa to 4.1×10^{11} Pa. Then the interface region of the 3C-SiC layer is less rigid with respect to the surface region.

The main parameters for the reduction of the intrinsic stress are the growth rate [76] or the growth time (for the same thickness) and the growth temperature [77]. In fact, it has been observed (Figure 5.6) that decreasing the growth rate and increasing the growth temperature we can observe a decrease of the stress. This effect is probably due to the "creep effect," i.e. the slow, plastic relaxation of the material occurring through the continuous introduction and/or movement of extended defects (SFs, twins, and dislocations) within the material volume, and not only at the growth front.

5.3 Bulk Growth of 3C-SiC

Bulk growth of hexagonal polytypes (4H- and 6H-SiC) using physical vapor transport (PVT) method can be considered mature. Today, wafers with diameters of 200 mm and dislocation densities as low as 2800 cm^{-2} [79–81] can be called

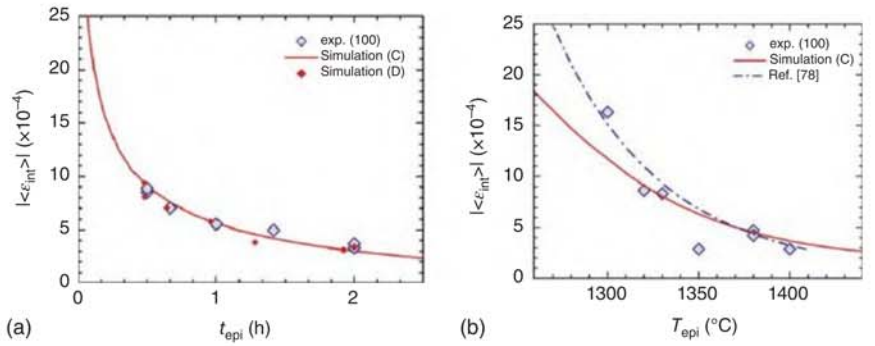


Figure 5.6 Mean intrinsic strain in 3C-SiC(100) as a function of the growth duration t_{epi} (a) and of the growth temperature T_{epi} (b). Source: Zielinski et al. [77]. © 2012, AIP Publishing.

standard for 4H-SiC. However, the method of continuous growth and enlargement as it is performed in PVT growth of hexagonal SiC cannot be employed for 3C-SiC. This is due to the growth conditions required to achieve stable growth of 3C-SiC, namely high vertical temperature gradients and a sufficient supersaturation of the silicon-containing gas phase. Therefore, the epitaxial sublimation growth (SE) method using a sublimation sandwich approach as presented by Tairov et al. [82] in 1976 was implemented and demonstrated the suitability to grow 3C-SiC [26, 83]. Besides that, various other bulk growth processes for 3C-SiC have been presented over the last decades, such as the modified PVT (M-PVT) or the continuous-feed PVT (CF-PVT) method [33, 84]. Up to now, only the epitaxial sublimation growth approach has generated 3C-SiC material with dimensions which can be called bulk [71, 85–88]. All these bulk growth methods have in common that they suffer from a lack of appropriate high-quality seeds, which hindered the development of such approaches for many years. However, such seeding material can be obtained by using 3C-SiC layers, which were hetero-epitaxially grown on silicon substrates by CVD [57, 71, 89]. Even though this approach still faces some challenges in the handling of the fragile CVD-grown seeds, reasonable results could be obtained in recent years [71, 85–88].

Indeed, one of the main challenges for the bulk growth of 3C-SiC by epitaxial sublimation growth, as well as for CVD, lies in CVD growth of the seeding material. Differences in the lattice parameters and TECs between 3C-SiC and silicon lead to CVD layers that feature high levels of stress which can result in the bending of the whole wafer and even cracking of the material. The subsequent processing of such bended layers in order to use them as seeds for SE still slows down the upscaling of this approach.

5.3.1 Sublimation Growth of (111)-oriented 3C-SiC on Hexagonal SiC Substrates

In the past, valuable work has also been done on the growth of (111)-oriented 3C-SiC on hexagonal SiC substrates [31, 37]. It shall be pointed out that this material was of very high crystalline quality. However, the high-quality material could only be

obtained on small areas (<2-in.) as DPBs propagate the material. As DPBs as well as the limitation to (111)-oriented material are not favorable for electrical devices, this approach could not demonstrate its practicability so far.

5.3.2 Sublimation Growth of 3C-SiC on 3C-SiC CVD Seeding Layers

On the other hand, applying epitaxial sublimation growth on CVD-grown seeds led to remarkable results, namely the reproducible growth of (100)-oriented 2-in. 3C-SiC with thickness up to 870 μm as can be seen from Figure 5.7. The growth rates for such layers typically lie between 160 and 320 μm/h. These results represent a milestone in the growth of large area bulk 3C-SiC as such layers with a thickness of approximately 1 mm will in principle allow the consecutive growth using methods like M-PVT or CF-PVT.

The layers depicted in Figure 5.7 represent the first quasi-bulk 3C-SiC material of relevant size produced by sublimation method on a regular base. The optical appearance of all crystals features a bright yellow color which is typical for cubic SiC. X-ray diffraction (XRD) and Raman spectroscopy confirm the growth of 3C-SiC. However, as can be seen from Figure 5.7 the layers still suffer from many defects. The typical defects in (100)-oriented 3C-SiC crystals are SFs, APBs and protrusions. Therefore, the small dark spots on the 3C-SiC layers in Figure 5.7 can be mainly assigned to protrusions which were already present on the CVD-grown seeds and increase in size during epitaxial sublimation growth. Dark areas on the outer edges of the layers can be assigned to defects which were generated by carbon contaminations on the seed surface. Such contaminations originate from the seed-mounting process and insufficient cleaning of the seed. The large dark areas in Figure 5.7b,c arose from areas featuring a burst of the seed layer.

The hot-zone for epitaxial sublimation growth can be realized in a state-of-the-art PVT reactor. In order to meet the aforementioned requirements for stable growth of cubic SiC, the hot-zone for a sublimation sandwich features some typical characteristics [36, 85]. High vertical temperature gradients are realized by a small distance

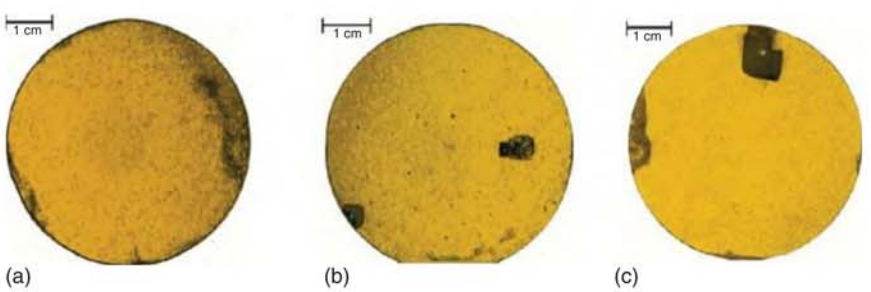


Figure 5.7 Transmitted light images of free-standing 2-in. wafers with thickness of (a) 870 μm, (b) 780 μm, and (c) 500 μm. The small dark spots on the samples can be mainly assigned to defects like protrusions and carbon inclusions. The larger dark areas in (b) and (c) can be assigned to burst areas of the seed layer. Source: Reproduced with permission of Schuh et al. [86].

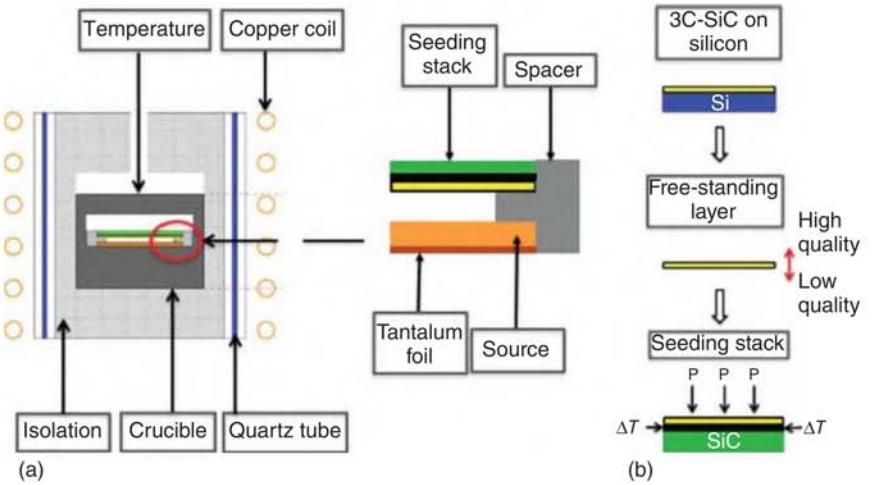


Figure 5.8 Growth-setup for epitaxial sublimation growth and transfer-process for the preparation of seeding-stacks. (a) Schematic of a physical vapor transport (PVT) setup used for epitaxial sublimation growth with the reactor (left) and the hot-zone (right). (b) Schematic manufacturing process for seeding-stacks used in the hot-zone for epitaxial sublimation growth. Source: Schuh et al. [88]. Licensed under CC BY 4.0.

between source material and seed. Usually, both are separated by a thin graphite spacer. A silicon-rich gas phase can be achieved by introducing a carbon getter, namely tantalum, into the growth cell. The supersaturation goes along with the temperature gradient. Hence, starting from the bottom of the growth cell in Figure 5.8a, a tantalum foil lies below the sandwich. On top, a SiC source material, usually polycrystalline SiC, is placed. A graphite spacer determines the distance between source and seeding-stack.

In order to use CVD-grown 3C-SiC layers as seed, a seeding-stack needs to be prepared according to Figure 5.8b. This is necessary to mechanically stabilize the thin (typically 20 µm) 3C-layers and to prevent backside sublimation of the seed during sublimation growth. Starting from 3C-SiC-on-Si wafers that were produced by CVD, a seed of the desired dimensions is prepared by using a multi-pulse laser ablation technique [90, 91]. Subsequently, the silicon substrate is removed using wet-chemical etching by HNA ($HF:HNO_3:H_2O$) resulting in a free-standing 3C-SiC layer with a high-quality growth front and a low-quality former 3C-SiC/Si interface. The free-standing 3C-SiC seed is attached to polycrystalline SiC carrier using a carbon glue. The carrier serves as mechanical support and backside protection. With that transfer process, crystals of 2-in. in diameter have been grown reproducibly. The preparation of 4-in. layers has in principle been demonstrated, too, as can be seen from Figure 5.9. However, at present the transfer of seeding layers with diameters >2-in. is still subject to some difficulties. On the one hand, the handling of the fragile 3C-SiC seeds becomes more difficult with increasing diameter. This obstacle could partly be overcome by a reduction of stress and bow in the CVD seeds. On the other hand, the processing of the seeding stacks for SE growth needs to be adapted for

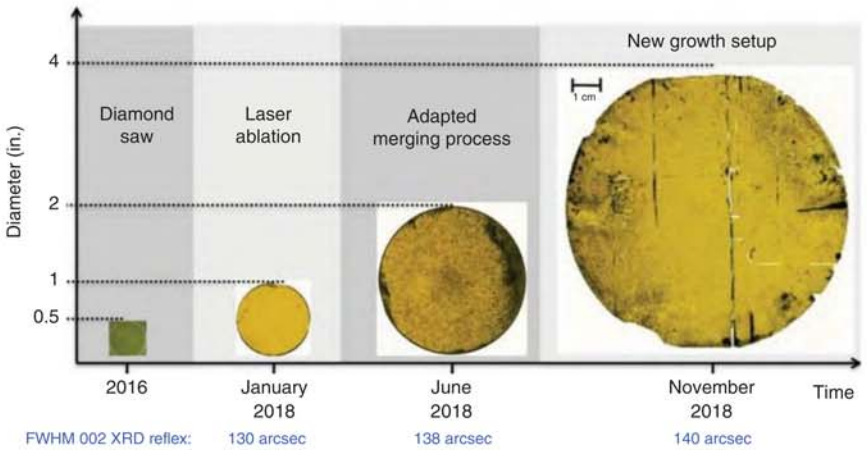


Figure 5.9 Evolution of diameters for bulk 3C-SiC crystals grown by epitaxial sublimation growth. The timeline and the full-width-at-half-maximum (FWHM) values from XRD-rocking curve measurements are indicated.

large diameters. All these challenges are likely to be solved by adaptions concerning the wet-chemical etching procedure and the geometry of the sublimation sandwich.

Even if there are still many defects present in the material, the quality of sublimation grown bulk 3C-SiC can be designated as "high-quality." Raman analysis of a defect-free surface area on a SE-grown material is depicted in Figure 5.10a. For defect-free (100)-oriented on-axis material, the transverse optical (TO) mode is forbidden. If the TO-mode is visible anyway, its position can be used as a measure for the stress within the material [92]. The diagram in Figure 5.10b shows the wavenumbers of the TO-mode for typically stressed CVD-grown material on on-axis and off-axis silicon substrates as it was used as seeds for the aforementioned sublimation grown crystals. From these data, a tensile stress is visible in both materials. In comparison, as-grown SE-material features similar values as CVD material which was grown on on-axis substrates. If sublimation growth on seeding-stacks is applied, a temperature treatment at 800 °C is usually performed after the growth in order to oxidize the carbon glue and remove the SE layer from the remaining part of the carrier. Such material features a reduction of stress toward 797 cm^{-1}, as obvious from Figure 5.10b. Therefore, free-standing sublimation grown bulk 3C-SiC can be considered as quasi stress free.

When it comes to real bulk growth, the thickness of the crystals is the significant value of interest. Therefore, the source-to-seed distance which is set by the spacer determines the maximum achievable thickness. Figure 5.11 depicts calculated values of the supersaturation for different source-to-seed distances (0.75, 2, and 3 mm). The supersaturation which is influenced by the temperature gradient and therefore depends on the source-to-seed distance is the critical parameter in order to evaluate the conditions for stable growth of 3C-SiC. Besides supersaturation, data from Raman spectroscopy and XRD are shown. For the analysis of XRD-rocking curve data, the full-width-at-half-maximum (FWHM) of the 002 reflex is used. Raman

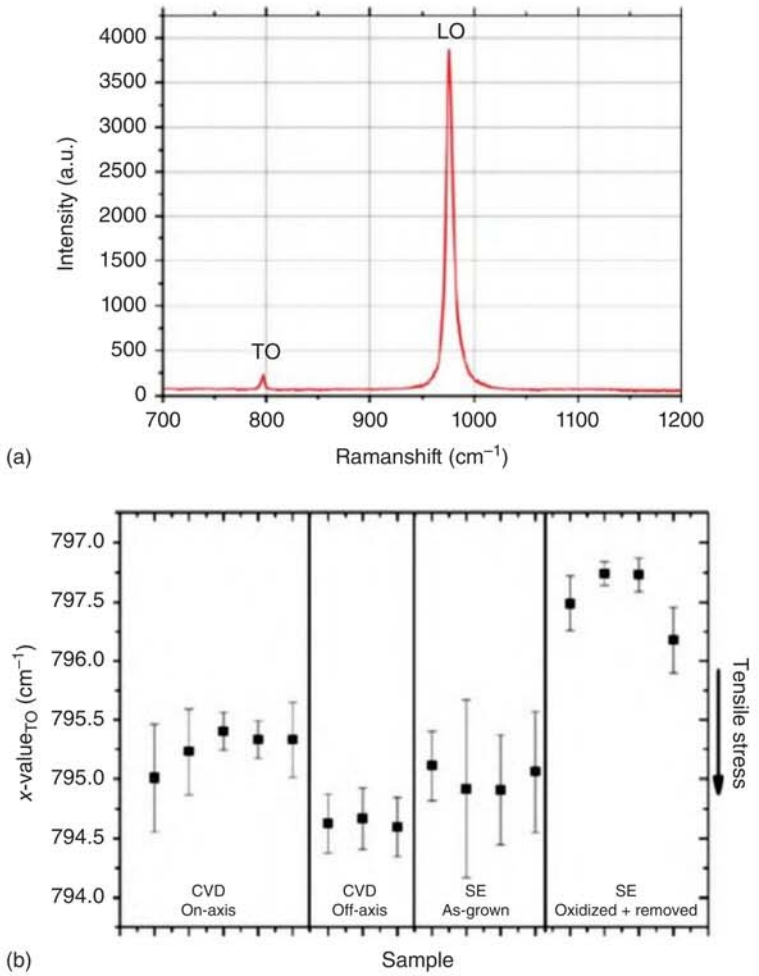


Figure 5.10 (a) Raman spectrum of typical sublimation grown material acquired in a protrusion-free surface area. (b) Comparison of the *x*-value for the transverse optical (TO) Raman mode of 3C-SiC epitaxial layers grown by chemical vapor deposition (CVD) on on-axis and 4° off-axis substrates, homo-epitaxial as-grown material produced by epitaxial sublimation growth (SE), and SE material after temperature treatment. Source: Schuh et al. [86].

results were obtained using the ratio of the intensities of the longitudinal mode (LO) and the TO-mode. From both characterization methods follows a similar trend. A decrease of supersaturation, created by an increase of the source-to-seed distance, results in a decrease of overall material quality. The FWHM values vary from close to 120 arcsec for 0.75 mm spacer to 325 arcsec for 3 mm spacer. In Figure 5.9, the FWHM values for XRD-rocking curve measurements are given for bulk 3C-SiC of different diameters. FWHM values between 130 and 140 arcsec are almost comparable with those of high-quality material grown on hexagonal SiC substrates, which can be lower than 120 arcsec [83].

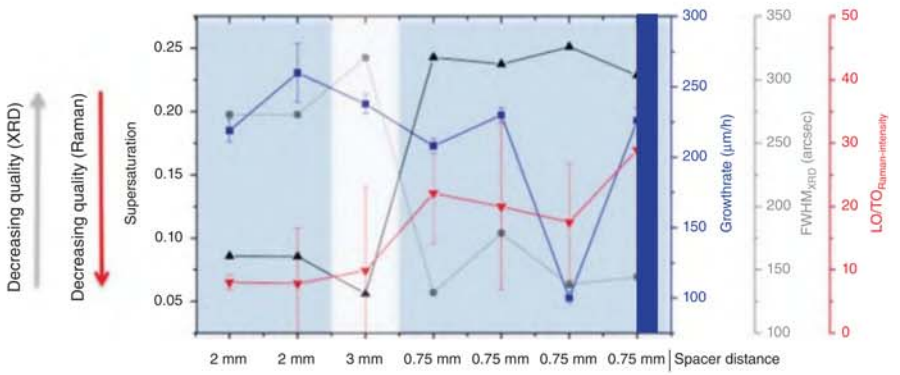


Figure 5.11 Calculated supersaturation of the SiC_2 gas species for experiments with different source-to-seed distances (black). The intensity ratio of the LO and TO-mode from Raman spectroscopy (red), XRD measurements of the 002 peak and the FWHM (gray), as well as the growth rate (blue) is given. Source: Schuh et al. [88]. Licensed under CC BY 4.0.

It should be noted that bulk growth of 3C-SiC by epitaxial sublimation growth is subject to some limitations. Up to now, the main problem is the protrusions defect as already mentioned. This three-dimensional defect occurs during the initial stage of 3C-SiC growth on silicon substrates by CVD. As such material is used as seed for epitaxial sublimation growth, these defects are present in sublimation grown 3C-SiC, too. Zimbone et al. [57] reported that this kind of defect already tends to increase in size with increasing 3C-SiC thickness during CVD growth. This trend can also be observed for subsequent SE growth [93] as the protrusions continue to grow. A set of optical images of SE layers with different thickness are depicted in Figure 5.12a. A continuous increase of protrusion dimensions can be observed for increasing thickness of the bulk material. The diagram in Figure 5.12b shows the length of the protrusion base derived from as-grown surfaces of 3C-SiC vs. the thickness of the layer. At least for the investigated parameter range, a linear behavior can be observed. As a consequence, as long as protrusions cannot be initially avoided, the amount of high-quality protrusion-free material is limited by the density of protrusions on the seeds used for bulk growth of 3C-SiC. Bulk layers with thickness of 2.7 mm have been grown which showed a macroscopic surface roughening due to a complete covering with protrusions. In this context, it is pointed out that keeping stable growth conditions for 3C-SiC, in particular regarding supersaturation, for larger source-to-seed distances is still a matter of research. With numerical simulation, the temperature gradients within the sublimation sandwich can be calculated. Using these gradients, the partial pressure of the growth-limiting SiC_2 gas species can be accessed in order to approximate the supersaturation. Hence, for the growth of 3C-SiC on 3C-SiC seed layers, a supersaturation of 0.1 or above is assumed to be necessary in order to ensure stable growth conditions [88].

While protrusions can be considered a serious issue to be solved in future, the quality of SE layers is quite good regarding SF. If CVD-grown 3C-SiC is used as seed for epitaxial sublimation growth, a defect-rich transition layer is formed between CVD seed and SE layer. Within this area, the SF density increases significantly. However, with increasing 3C-SiC thickness the SF density decreases again during SE growth. As soon as a total thickness of approximately 175 µm is exceeded, the SF density of the SE-layer lies below the value for the used CVD seed (Figure 5.13) [93].

From Raman, XRD, and SF characterization follows, that epitaxial sublimation growth can considerably improve the quality of material grown by CVD. If the density of protrusion defects as well as the wafer bow can be reduced or even avoided in future, the growth of high-quality bulk 3C-SiC comes within tangible reach.

5.3.3 Continuous Fast CVD Growth of 3C-SiC on 3C-SiC CVD Seeding Layers

The main issue to develop the 3C-SiC devices is the lack of available material [71]. Bulk crystal with good crystal quality is not yet commercially available. This limitation is probably due to the fact that almost all of the studies related to 3C-SiC growth were performed using Si as substrate for the epitaxial process. Actually, the hetero-epitaxial system is limited by the high lattice mismatch between SiC and Si

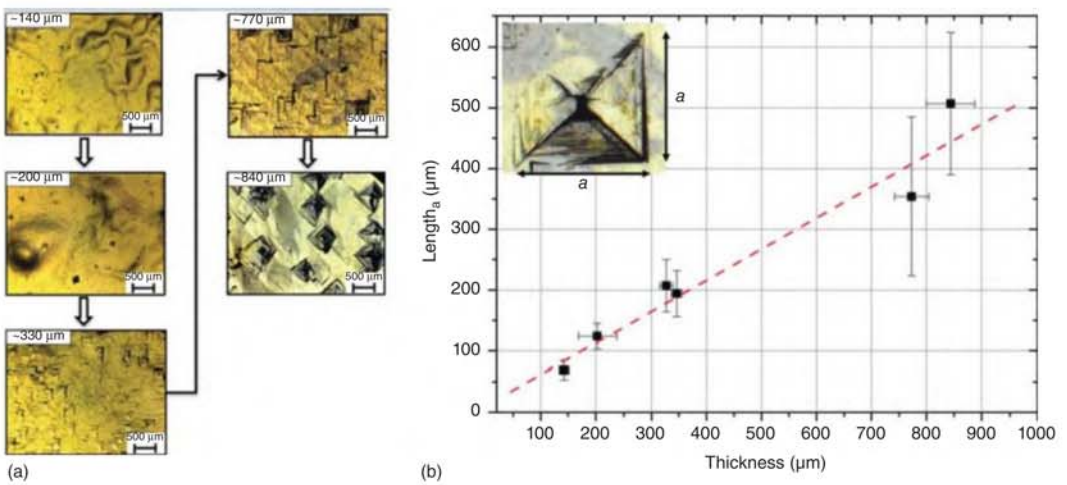


Figure 5.12 (a) Evolution of protrusion dimensions for bulk 3C-SiC layers with different thickness. (b) Edge-length of protrusions plotted vs. 3C-SiC thickness. Source: Reproduced with permission of Schuh et al. [88].

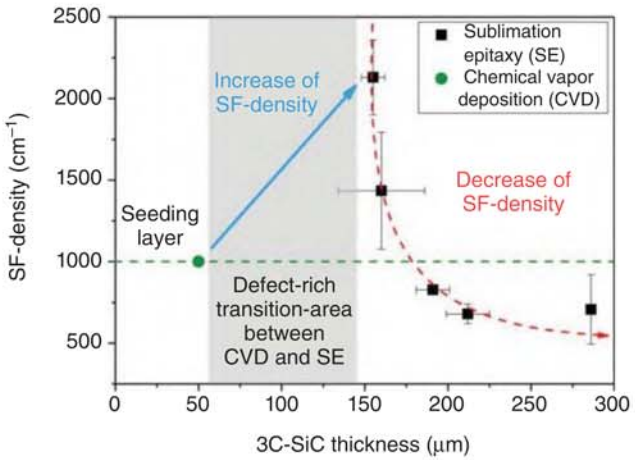


Figure 5.13 Stacking fault (SF) density vs. thickness of SE-grown 3C-SiC layers extracted from KOH etched samples. After an initial rise of SF-density within the transition area between CVD and SE, the density of SFs decreases with increasing 3C-SiC thickness and declines below the value of the used CVD seed. For comparison, the SF-density of HOYA sample grown by Switch-Back-Epitaxy is presented [61]. Source: Adapted from Schoeler et al. [93].

(20%), and the difference in TEC that generates a very high density of defects during the grown of the layers and the cool down, respectively [56, 73]. In the last decades, many efforts have been devoted to search technologic feasible growth techniques to overcome such limitation.

After the initial attempt by Nishino et al. [94], when he proposed a multi-step CVD process able to ensure an improvement in the crystal quality of the 3C-SiC epilayers, and today thick 3C-SiC films have been commonly grown on carbonized Si substrates by CVD. Important progresses have been demonstrated using patterned (undulant) silicon substrates [65] followed by the switch-back epitaxy process. This technique seems to be promising but the wafer bending issue remains unsolved. Another way is to use a silicon substrate with ISPs [62]. Using ISP substrate, a reduction of SFs is observed for thin layer because this substrate allows the probability of SFs annihilation, but the substrate manufacturing is not easy. Different approaches are being developed to find a convincing alternative to 3C-SiC/Si hetero-epitaxial system. In order to grow 3C-SiC bulk material of 4 and 6 in., a new epitaxial reactor chamber has been designed and tested. The main idea is to grow a hetero-epitaxial layer as seed, melt the silicon substrate, and continue the growth at high temperature. In this way, it will be possible to grow a bulk substrate of 3C-SiC with a low density of SFs and low wafer bow. In fact, the bow can be strongly decreased, because by removing silicon, one of the main components of the stress due to the different TEC between the two materials is completely eliminated. The removal of silicon gives also the possibility of a large increase in the growth temperature and in the growth rate, and then thicker wafers and better material can be grown.

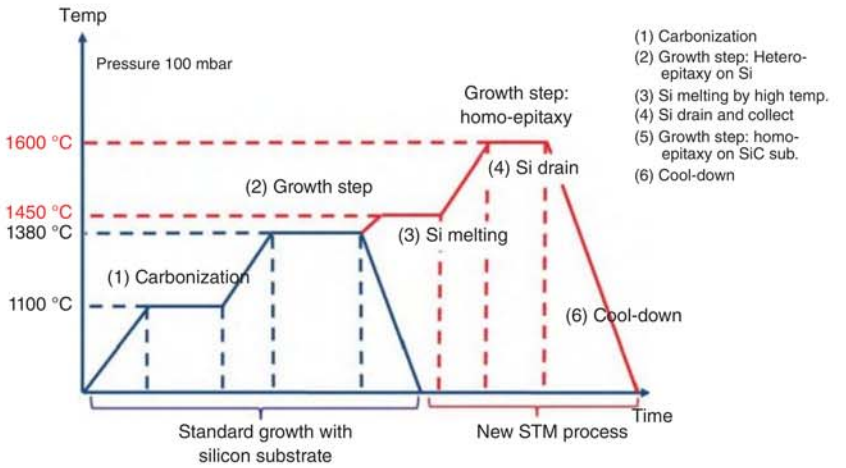


Figure 5.14 Schematic of the new CVD growth process of the 3C-SiC bulk wafer with the silicon melting after the first epitaxial growth on silicon substrate.

In order to grow bulk material of 4 and 6 in., a new chamber for the CVD hot wall commercial reactor has been designed and tested. The main idea described in the patents submitted by STMicroelectronics [95–97], is to grow a thick hetero-epitaxial layer on silicon substrate (4 or 6 in.) with a standard process, melt the silicon substrate by a dedicated new reaction chamber within the CVD reactor, where the Si can drain through the susceptor and continue the growth at high temperature (standard homo-epitaxial process). In this way, it will be possible to grow a bulk substrate of 3C-SiC with a low density of SFs and low bow.

A large set of experiments have been performed to understand how to melt the silicon substrate, how to drain it, how to etch the remaining silicon, and how to grow the homo-epitaxial layer on the 3C-SiC substrate obtained after the silicon melting. In Figure 5.14, a scheme of the entire process is reported. The first two steps are the standard ones (well reported and described in literature). The growth of 3C-SiC seed was performed with a epitaxial CVD process, in a horizontal hot-wall reactor (LPE) on Si(100) substrate. Trichlorosilane ($SiHCl_3$ or TCS), ethylene (C_2H_4), and hydrogen (H_2) were used as silicon and carbon precursors and gas carrier, respectively. The first step (i) is the carbonization steps where, after a vacuum bake of the reactor, to decrease the nitrogen contamination of the reaction chamber and a H_2 etching of the silicon surface is performed at a temperature of 1100 °C for 10 minutes, at the same temperature, the carbonization was performed for a fixed time of 5 minutes with only carbon precursor inside the camber [56, 57]. For the second step (ii), the process was carried out in a low-pressure regime (100 mbar) at a temperature of 1380–1400 °C (very close to the silicon melting temperature).

The growth starts at 3 μm/h, then increases to 6 μm/h and finally further increases to 30 μm/h. With this process, a thick layer of about 90 μm has been grown. Subsequently, the temperature was increased above the melting point of silicon and the Si substrate was completely melted inside the CVD reactor.

The remaining freestanding SiC layer is used as a seed layer for a subsequent homo-epitaxial growth. The processes were obtained in a low-pressure regime at different temperatures in the range between 1600 and 1700 °C. It was used a growth rate of 60 µm/h for two hours to increase the substrate thickness and at 30 µm/h for the last one hour to further improve the quality of the material as previously reported. While the first 20 µm of the last step has been highly doped, the final 10 µm is low doped for device realization. Nitrogen was used as doping species for *n*+ and n-type layers formation. After the homo-epitaxial deposition, the total thickness of 3C-SiC samples was about 200 µm (observed by SEM analysis).

The structural investigation of the entire 200 µm thickness film was performed by SEM in cross-section, where the 3C-SiC film (seed and homo-epitaxial layer) is observed (Figure 5.15). Figure 5.15 shows different layers within the film: starting from the bottom, first the seed of 90 µm and next, the homo-epitaxial layer grown after the fusion of Si. The seed shows different layers with different growth rate, with more defects close to the old silicon interface. With increasing growth rate, the seed exhibits a decrease of the defect density. The seed shows the decreasing of defects increasing the growth rate. The second step is made up of the homo-process that reveals a lower thickness value (around 120 µm) compared to the predicted one (150 µm of Figure 5.15b). From the figure, the change in the doping concentration is also visible close to the film surface (10 µm thickness layer with low doping concentration close to the surface).

The investigation of the temperature influence on the homo-epitaxial process was evaluated by XRD analysis (Figure 5.16). The FWHM on the X-ray rocking curve of the 3C-SiC (002) peak is related to the crystal quality and defect density (decrease the FWHM increases the crystal quality). The figure shows the trend of FWHM as a function of film thickness for different samples growth also in different condition (all the samples at low value of thickness are coming from previous experiments [71]). It is well known that by increasing the film thickness, the quality of the material increases [64]. The first part of the curve (from 0 to about 20 µm of thickness) shows the 3C-SiC samples growth with Si substrate. For such samples, the crystal quality is limited by the present of silicon substrate that starting from about 20 µm of thickness introduces many cracks and extended defects during the cooling down after the growth [71]. The three points between 60 and 90 µm are the 3C-SiC samples without silicon substrate (after Si fusion) with a good crystal quality (around 200 arcsec), comparable with an old 2 in. 3C-SiC wafer provided by HOYA corporation (dotted line). These samples are the substrates used as template for the homo-epitaxial process of this experiment. The stared points (three at 200 µm) are the samples grown by using the new melting technique described in the present work. They are grown at three different temperatures (1600, 1640, and 1700 °C). The graph clearly shows the sample grown at 1600 °C is significantly better than the other two [98]. Indeed, it has a FWHM value of around 100 arcsec that is very promising also compared to a thicker sample (about 400 µm) grown by sublimation epitaxy (PVT reactor) at high temperature [87].

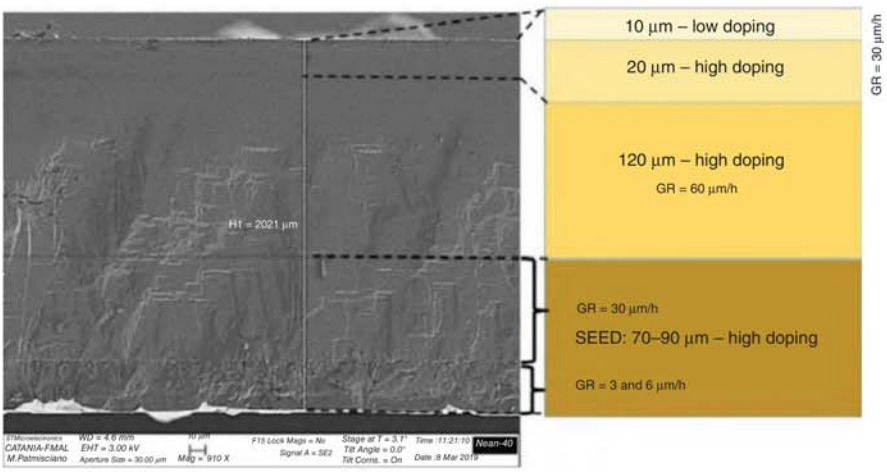


Figure 5.15 (a) Cross-section SEM image of the 3C-SiC wafer (about 200 µm). (b) Schematic representation of the structure: hetero-epitaxial seed and homo-epitaxial layer. Layers have different doping concentration and growth rate. Source: Anzalone et al. [98]. Licensed under CC BY 4.0.

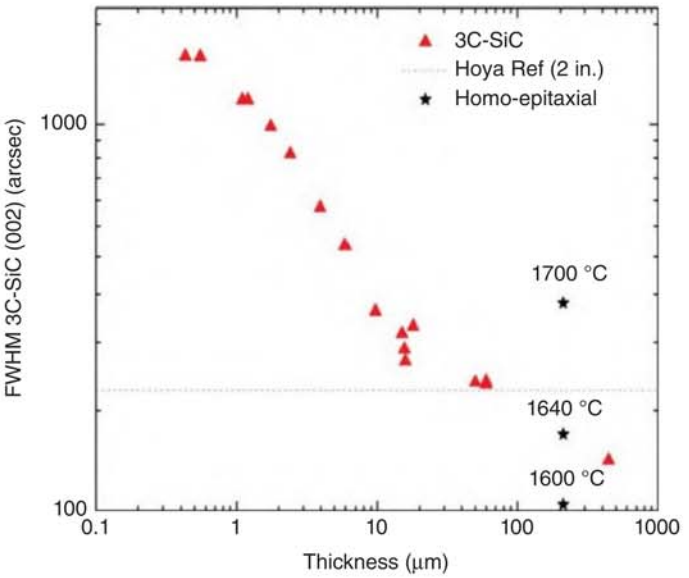
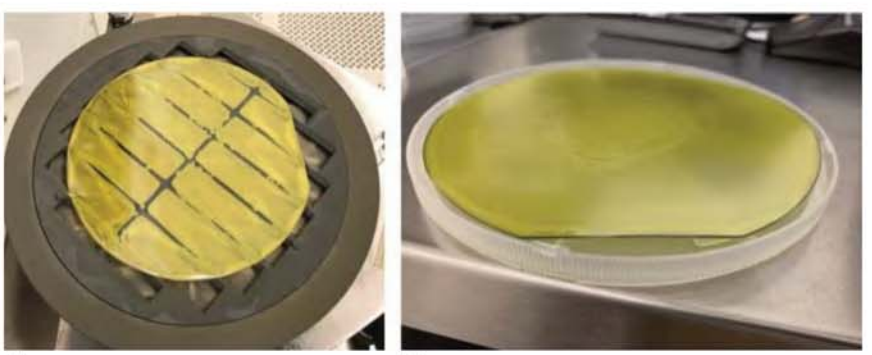


Figure 5.16 FWHM of the X-ray rocking curve as a function of film thickness for different value of temperature and compared with other reference samples. Source: Anzalone et al. [98]. Licensed under CC BY 4.0.



(a) (b)

Figure 5.17 The 3C-SiC 6 in. wafer after the total process. (a) The wafer on the subsector (with silicon not totally melted) and (b) after the total silicon melting.

According to the patent [97], many melting experiments (on 4 and 6 in.) have been performed with the susceptor structure reported in Figure 5.17a. As can be observed in this figure, the main problem observed with this structure was the uncomplete etch of silicon in the internal regions of the wafer (dark zone).

In the successive experiments, using long melting process time and long etching time, it was possible to completely remove this silicon residue.

Finally, with a further susceptor structure tested, a better uniformity of the temperature with respect to the standard structure, the silicon has been successfully removed during the melting and etching process.

It has also been observed that the removal of the silicon substrate releases the tensile stress of the wafer and only the intrinsic stress is present. Then new experiments on the carbonization and growth should be done to decrease this stress and obtain a flat wafer.

5.4 Processing and Testing of 3C-SiC Based Power Electronic Devices

5.4.1 Prospects for 3C-SiC Power Electronic Devices

The past number of years has heralded the dawn of the electric revolution in terms of consumer products, transportation, energy generation, and distribution. Various reports have predicted that 60–80% of global energy demand will be provided in the form of electrical power [99, 100] over the coming decades. This places power electronics at the forefront of technological priorities, with the majority of this electrical energy passing through some form of converter.

It is generally accepted that 3C-SiC can occupy the 600–1000 V range, given its band gap value of 2.4 eV. Although the 3C-SiC band gap is narrower than its 4H-SiC counterpart, this brings about many positives in terms of on-state operation. A narrower band gap lowers the conduction band minimum, resulting in a reduced density of states at the SiO_2/3C-SiC interface.

Therefore, MOSFET fabricated in 3C-SiC have already achieved a channel mobility up to 300 $cm^2/(V\,s)$. This is the highest realized on any of the SiC polytypes, demonstrating the potential reduction in power consumption of these promising switching devices. Furthermore, the bulk mobility for electrons, 1000 $cm^2/(V\,s)$ is slightly higher than that of 4H-SiC, offering a similar drift region resistance. The thermal conductivity is 3–4 W/(cm K) allowing for harsh environment operation with some early reports showing the drift region temperature coefficient (bulk mobility degradation) being 10% lower compared to 4H-SiC (200 °C). This offers enhanced drift region resistance and more realistic junction temperatures.

5.4.2 3C-SiC Device Processing

In spite of these potential advantages, the application of 3C-SiC in power device technology remains limited by the material quality, which in turn is strongly related to the growth techniques [101]. Figure 5.18 shows the cross-section of a typical research-grade 3C-SiC MOSFET fabricated by Li [102]. This device architecture for 3C-SiC is prevalent in the literature and as can be inferred from this figure, the required processing technology is similar to that of conventional silicon and 4H-SiC device topologies. On-going research into the fundamental device building blocks, including the 3C-SiC/SiO_2 interface, ion implantation, and metal/semiconductor contacts, has been reported in the literature. However, these initial studies have been significantly influenced by the quality of the 3C-SiC material (e.g. defect density, surface roughness, surface preparation, etc.) [71].

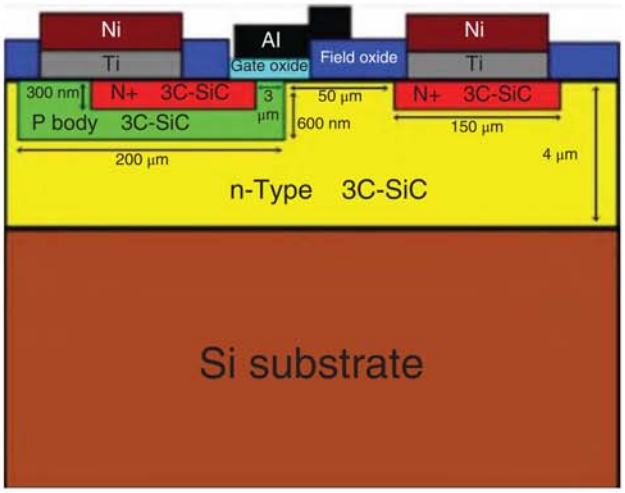


Figure 5.18 A cross-sectional representation of a 3C-SiC LDMOSFET. Source: Adapted from Li [102].

5.4.3 MOS Processing

With its superior electrical properties and the ability to be thermally oxidized, it is no surprise that there is positivity around the prospects for SiC MOS devices. Commercial 4H-SiC is the most prominent SiC polytype. The hexagonal lattice of 4H-SiC means there will be several faces available for oxidation. Most research has been devoted to the (0001) Si-face, the only one available in commercial wafer form. There have been studies suggesting that MOS interface traps for all SiC polytypes are similar [103]; thus, the study on the 4H-SiC/SiO_2 interface also provides a great insight for 3C-SiC. Unfortunately, the 4H-SiC/SiO_2 interface turns out to be quite poor and the electrical performance is not even close to its Si counterpart. The interface trap density (D_{it}) on the as-grown 4H-SiC/SiO_2 interface is typically close to 10^{13} cm^2/eV, which is two orders of magnitude higher than more conventional Si/SiO_2 interfaces [104]. After decades of study, the reasons behind the poor 4H-SiC/SiO_2 interface are still not fully understood. Afanasev et al. [105] discussed the potential origins of this high density of interface traps, with two sources being identified, the first of which is the carbon accumulated at the MOS interface during the SiC oxidation process.

The theory of carbon failing to escape through thicker oxides naturally leads to the idea that there should be less carbon at the MOS interface with respect to thinner oxides. Indeed, a recent study [106] demonstrated an almost ideal SiC/SiO_2 interface with a very thin oxide layer ($\approx$14 nm), the D_{it} value reported was less than 10^{11} cm^2/eV. However, a certain oxide thickness ($\approx$50 nm for SiC MOS devices) is necessary for a reasonable threshold voltage, which renders this thin oxide approach impractical for real device fabrication. Thin thermally grown oxides with a deposited oxide above may be an option but are still not straightforward. This is since a deposited oxide is known to contain many more defects than its more traditional thermally grown equivalent [107]. This leads to the second source of

SiC/SiO_2 interface traps, namely oxide defects. Oxide defect induced traps are essentially the oxide trapped charges. In SiC/SiO_2 studies they are also referred to as "near-interface traps" since they do not actually sit at the interface but instead are located in the SiO_2, very close to the interface. For Si, energy levels of oxide trapped states are in the conduction band, thus not electrically active. For SiC, however, whose band gaps are two to three times wider, many of the oxide trapped charges are located in the band gap, meaning they are electrically active, as has been confirmed by photon stimulated electron tunneling [108]. The near-interface traps have time constants much smaller than the carbon clusters, thus are called fast traps while the latter are known as slow traps.

A schematic representation of the carbon cluster mode is in Figure 5.19 with corresponding energy levels of the specified traps. Due to the significantly low mobility of holes compared to electrons, SiC MOS devices are almost exclusively based on an n-channel design. Therefore, the traps providing the scattering mechanism acting upon electron carriers within the channel are the ones located close to the conduction band edge. Figure 5.19 illustrates the fact that the 4H-SiC conduction band edge is mostly troubled by near-interface traps and π-bonded carbon clusters, with the former more dominant. Both of these traps are accepter-like, namely negatively charged when occupied, which can explain the positive flat band voltage often observed for 4H-SiC MOS devices. On the other hand, 3C-SiC should be free from near-interface traps, attributed to a narrower band gap. However, the $3C\text{-}SiC/SiO_2$ interface is still troubled by π-bonded carbon clusters. These carbon clusters near the 3C-SiC conduction band edge are donor-like, thus positively charged if occupied, which means the resultant flat band voltage may be more negative. Dangling bonds still contribute

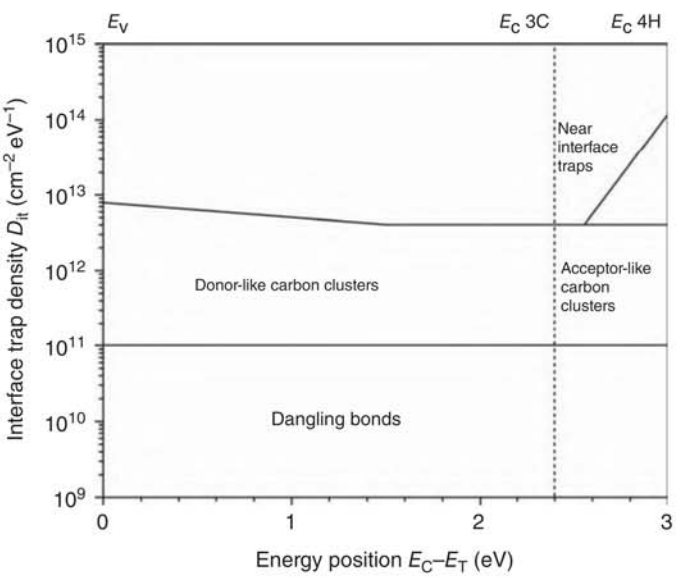


Figure 5.19 Schematic representation of the "carbon cluster model". Source: After Esteve [109].

to some of the interface traps but are merely secondary concerns. Consequently, for SiC, H_2 annealing is not as effective as it is for Si. Other techniques had to be explored for SiC/SiO_2 interface optimization.

5.4.4 3C-SiC/SiO_2 Interface Passivation

The efforts put into improving the SiC/SiO_2 interface can be divided into three directions, namely post-oxidation annealing (POA), channel counter-doping, and high temperature oxidation. Up to this point, nitridation may be the most widely used method to improve the 4H-SiC/SiO_2 interfaces. It is usually achieved by the annealing of thermally grown gate oxides in a nitrogenous trace gas environment (NO or N_2O), called POA. During the annealing process, it is believed that the N—O bond breaks at high temperature and supplies free oxygen which oxidizes 4H-SiC [110], consequently nitridation by POA is accompanied by a further growth of oxide, although this is not significant. Occasionally, gate oxides can be directly grown within such an atmosphere to obtain similar benefits. Previous X-ray photoelectron spectroscopy (XPS) results demonstrated that after NO/N_2O POA, there were fixed nitrogen atoms near the interface with an area density around 1×10^{14} cm^{-2} [111], even after removing all the oxide by thorough HF etching. This suggests that the nitrogen atoms were strongly bonded to the 4H-SiC substrate. There had been evidence showing the nitridation process reduced both carbon-related traps and near-interface traps [112], even though there is still no complete theory established to explain these findings. The near-interface traps are probably reduced by the formation of an oxynitride layer between the 4H-SiC and gate oxide, which redefines the oxide/semiconductor boundary [113] and the oxide trapped charges no longer near the interface. In terms of carbon clusters, they are probably decomposed by inserted nitrogen atoms, which shift the energy levels of remaining clusters deeper into the band gap, further away from the conduction band edge. The result is that these carbon clusters are nullified and are less effective in terms of scattering channel carriers [114]. Apart from N_2O/NO, it was reported that annealing the gate oxide in a phosphorous trace atmosphere ($POCl_3$ [115] or P_2O_5 [116]) also led to a channel mobility improvement. However, this technique introduced severe threshold voltage instability as a result of SiO_2 being converted into phosphor silicate glass. Reducing the number of traps via the introduction of extra atoms into the interface is called passivation, and regardless of the source (N or P), the key-enabler is that enough foreign atoms diffuse through the gate oxide and reach the interface. Certainly higher annealing temperature and time duration will help with that, as long as the SiO_2 crystal structure is still well preserved. However, due to the very low diffusion coefficient of nitrogen in SiC, nitrogen atoms incorporated through POA saturates only within a monolayer deeper into the interface [117], and consequently the mobility value does not increase further and the peak value typically stays around 40 $cm^2/(V\,s)$ [118]. Phosphorous has a higher saturation density than nitrogen in 4H-SiC, but still, the peak mobility value stays around 80 $cm^2/(V\,s)$ [119] regardless of further increased annealing time durations. In summary, the proposed mechanisms for the increased 4H-SiC/SiO_2 channel mobility are defect passivation, channel counter-doping [120–122], and reduced surface roughness scattering [123].

Table 5.2 Recent results on 3C-SiC MOSFET fabrication.

Substrate material	Channel doping	Gate oxidation	Extra treatment	Peak mobility ($cm^2/V\,s$)	References
3C-SiC(001) on Si (CVD)	2×10^{17} cm^{-3} p-type epilayer	O_2 wet oxidation at 1150 °C for 2.5 h followed by Ar annealing at 1150 °C for 30 min	O_2 wet re-oxidation at 950 °C for 2 h	≈165	[127]
Free-standing 3C-SiC(001)	1×10^{16} cm^{-3} p-type epilayer	O_2 dry oxidation at 1100 °C, followed by Ar annealing at 1150 °C for 30 min	O_2 wet re-oxidation at 800 °C for 30 min	≈229	[128]
Free-standing 3C-SiC(001)	7×10^{16} cm^{-3} p-type epilayer	O_2 dry oxidation at 1100 °C for 90 min	O_2 wet re-oxidation at 950 °C for 3 h	5–10	[129]
Free-standing 3C-SiC(001)	1×10^{18} cm^{-3} Al implanted	O_2 dry oxidation at 1100 °C for 90 min	O_2 wet re-oxidation at 950 °C for 3 h	≈40	[130]
Free-standing 3C-SiC(001)	Not known, Al implanted	O_2 wet oxidation at 1150 °C	None	≈150 for [110] and ≈300 for $[\bar{1}10]$	[131]

The 3C-SiC/SiO_2 interface is much less studied when compared to 4H-SiC. The literature revealed the benefits of including hydrogenation processes either during gate oxidation or via POA, which decreases the density of interface states as well as effectively reducing positive fixed charges [15, 124]. Thus, wet oxidation or POA is frequently used in 3C-SiC MOSFET fabrication [124, 125]. Regarding nitridation, extra deep interface traps revealed by the double peak conductance spectra were found from MOS capacitors fabricated using direct N_2O oxidation and pure oxidation on nitrogen implanted films [124, 126]. The inefficiency of the nitridation process for 3C-SiC is curious since according to the carbon cluster model shown in Figure 5.19, the 3C-SiC/SiO_2 interface should be dominated by π-bonded carbon clusters. The effect of which should be reduced by the nitridation process just as 4H-SiC. The electrical performance of fabricated 3C-SiC MOSFET devices is heavily dependent on the quality of the wafer, making it difficult to directly compare. Recent fabrication results relating to 3C-SiC MOSFETs are summarized in Table 5.2. As can be seen, the peak mobility value covers a huge range from as low as 5–229 $cm^2/(V\,s)$.

5.4.5 Surface Morphology Effects on 3C-SiC Thermal Oxidation

As is the case with all semiconductor materials, the surface morphology and corresponding preparation methods have a profound impact on the quality of any

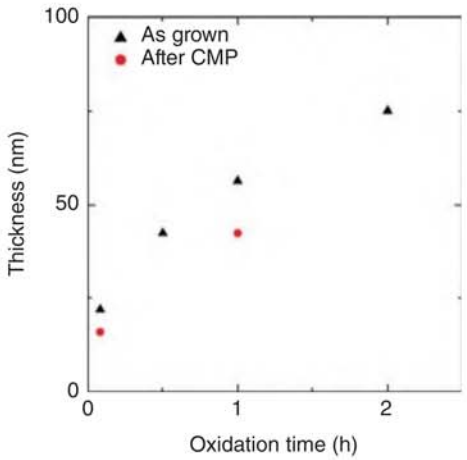


Figure 5.20 Oxide thickness as a function of oxidation time at 1150 °C for as-grown and CMP polished 3C-SiC samples. Source: Fiorenza et al. [132]. © 2019, Trans Tech Publications Ltd.

thermally grown oxide (SiO_2). Moreover, the fact that 3C-SiC typically requires some form of chemical mechanical polishing (CMP) process after hetero-epitaxial growth complicates matters further. Figure 5.20 reports the oxide thicknesses as a function of the oxidation time for as grown and CMP processed 3C-SiC hetero-epitaxial layers [132]. These 3C-SiC layers were grown on 4-in. Si(100) substrates by hot-wall CVD at temperatures in the region of 1350 °C (or above). Silane (SiH_4) and ethylene (C_2H_4) or propane (C_3H_8) are typically used as supplier gases for Si and C, respectively (see section 2). The thickness of these layers was in the range of 5–10 μm. Standard cleaning (SC) was performed on the samples prior to thermal oxidation. Lateral MOS capacitors based on nickel (Ni)/gold (Au) contacts were fabricated and the oxidation rate was estimated by performing a selective oxide wet etch on lithographic patterns and subsequently measuring the height difference between the oxidized and the etched regions with an atomic force microscopy (AFM) microscope. It can be inferred that the oxidation rate follows an approximate linear behavior, at least for the sample without CMP. A similar linear behavior is observed on examination of the two experimental points collected on the sample after the CMP. Observed thickness fluctuations can be due to the large roughness of the 3C-SiC substrate. For this reason, the step height has been averaged between the minimum and maximum values. From Figure 5.20, after the growth of the first 15–20 nm of SiO_2, an oxidation rate of approximately 25 nm/h was estimated.

5.4.6 Thermal Oxidation Temperature Effects for 3C-SiC

Some recently reported results on the temperature varying thermal oxidation properties of 3C-SiC layers are given in this section [133]. Lateral MOS capacitors were fabricated on 14 mm^2 chips. Apart from the solvent and RCA cleans, these samples were subjected to an additional 15 minutes Piranha clean. A unique furnace tube, made from 6H-SiC, so that very high oxide growth temperatures up to 1600 °C could be analyzed, was utilized. For more details surrounding the oxidation conditions, including idle operation, gas flow, and temperature ramp rates, see here [133].

Table 5.3 Gate oxidation processes for the four 3C-SiC/Si lateral MOS capacitors fabricated and information extracted from high frequency *C–V* curves for MOS 1-4.

Sample	Gate oxidation details	POA	Oxide thickness (nm)	Flat-band voltage (V)	Fixed charge density (cm^{-2})
MOS 1	1200 °C O_2 dry oxidation (60 min, O_2 4 slm[a])	N/A	68	−4	1.1×10^{-12}
MOS 2	1300 °C O_2 dry oxidation (20 min, O_2 4 slm)	N/A	73	−6	1.6×10^{-12}
MOS 3	1400 °C O_2 dry oxidation (5 min, O_2 4 slm)	N/A	60	−13	4.5×10^{-12}
MOS 4	1300 °C O_2 dry oxidation (20 min, O_2 4 slm)	1300 °C N_2O anneal (2 h, N_2O, 1 slm)	115	−22	4.0×10^{-12}

a) Standard liters per minute.
Source: Data from Nagasawa et al. [38].

Three samples were oxidized at 1200 °C, 1300 °C, and 1400 °C, respectively. A fourth sample was oxidized at 1300 °C and went through an extra N_2O POA process. More detailed descriptions for oxidation conditions are summarized in Table 5.3.

Figure 5.21 shows the ideal capacitance-voltage (C-V) curves for all four samples plotted against their experimental results. A negative shift of the experimental C-V curves from the ideal ones is observed for all samples, indicating the existence of a positive fixed charge. Only donor-like states are present at the 3C-SiC/SiO_2 interface, and since they are positively charged when empty, these donor-like states may be responsible for the negative flat band voltage shift, extracted from the same data and shown in Table 5.3. Comparing MOS 1, 2, and 3, it can be seen that the flat band voltage shifts negatively with increasing oxidation temperature. This is different from the 4H-SiC case and the reason behind this observation is still not clear. The N_2O annealed MOS 4 has the largest evidenced shift. However, by calculating the fixed charge density for all samples (see Table 5.3), it is seen that MOS 4 does not have the highest fixed charge density. Hence, the significant flat band voltage shift of MOS 4 most likely comes from the counter-doping effect. A sharp peak of nitrogen in MOS 4 compared to all other samples, evidenced by secondary mass ion spectroscopy (SIMS, not shown), demonstrates that like into the 4H-SiC system, nitrogen atoms only accumulate at a very limited depth at or around the 3C-SiC/SiO_2 interface.

5.4.7 Ohmic Contact Metalization

The purpose of this section is to give an overview of the fundamentals of ohmic contacts onto 3C-SiC. Specific and unique contact fabrication processes from the literature will be covered. The basic steps involved in ohmic contact formation to

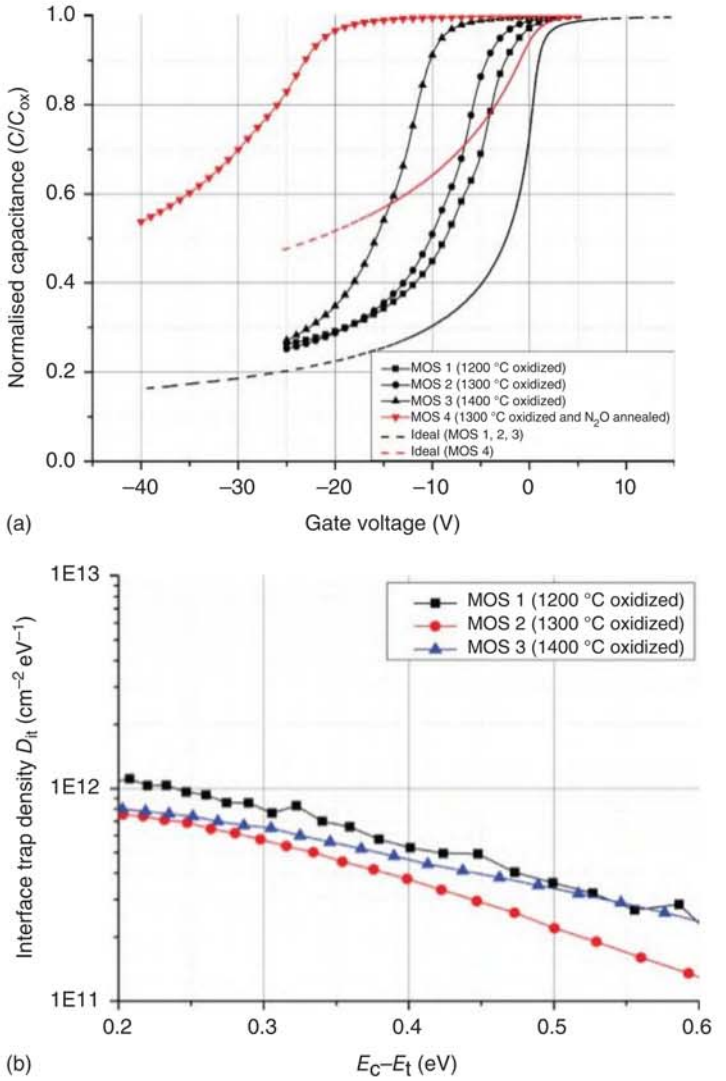


Figure 5.21 Ideal and experimental (1 MHz) normalized $C-V$ curves for MOS 1–4 (a) and interface state density as a function of trap depth beneath the conduction band for MOS 1–3 (conductance method) (b).

3C-SiC and how it differs from silicon and 4H-SiC technology will be covered. Creating a quality ohmic contact to 3C-SiC is challenging for many reasons, mainly the aforementioned material quality issues. It is more difficult to form ohmic contacts to p-type with respect to n-type 3C-SiC due to deeper acceptor levels. The primary challenge here is a limitation in terms of post implantation annealing (PIA) temperatures, resulting in poor dopant activation and ionization since the 3C-SiC is grown on silicon, taking the form of hetero-epitaxy wafers. The result is an ion implantation activation annealing temperature of just below 1400 °C (silicon substrate melting

temperature). As a consequence, there are less carriers (lower activation percentage of acceptor dopants) available for current transport, making it more difficult to achieve a high doping concentration, a precursor required for ohmic contact realization. A high free carrier concentration beneath the metal promotes field emission (FE, tunneling) through the metal-semiconductor junction, that is, generally accepted to be the main current transport mechanism, characteristic of ohmic contacts. Identification of the FE current transport mechanism is prevalent under the ohmic regime and is well understood by understanding the contact resistance variance as a function of temperature. Classic metal-semiconductor theory and characterization have been presented elsewhere [134, 135], whereas the concept of the characteristic energy and doping dependent current transport was introduced by Padovani and Stratton [136].

The most recent study on ohmic contacts applied to epitaxial p- and n-type 3C-SiC layers was given by Spera et al. [137, 138]. Here, Ni metallization to n-type 3C-SiC and Ti/Al/Ni metallization to p-type 3C-SiC were examined. Ohmic behavior could be observed after annealing at 950 °C, with values of the specific contact resistance varying in the range of 10^{-3}–$10^{-5}\Omega.cm^2$, depending on the 3C-SiC layer and on the metal. In general, annealed Ni contacts exhibited a better surface morphology than Ti/Al/Ni ones. However, these latter are more suitable to form ohmic contacts on p-type doped material, owing to the lower work function. Figure 5.22 shows a physical analysis of both n- and p-type ohmic contacts to 3C-SiC utilizing AFM and cross-sectional TEM. Metallic phases were determined using XRD (not shown).

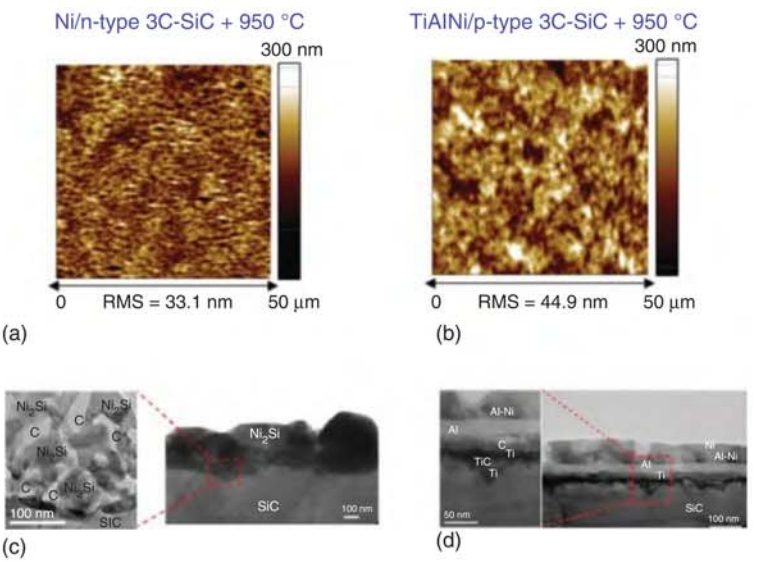


Figure 5.22 AFM images of Ni (a) and TiAlNi (b) ohmic contacts onto n- and p-type 3C-SiC epitaxial layers respectively. Cross-section TEM micrographs of Ni/3C-SiC (c) and TiAlNi/3C-SiC (d) samples after annealing at 950 °C. Source: The figure has been adapted from Ref. Spera et al. [137] with kind permission of Trans Tech Publications Ltd. Copyright ©2019 Trans Tech Publications Ltd.

5.4.8 N-type 3C-SiC Ohmic Contacts

Ohmic contact studies on 3C-SiC have been primarily limited to n-type material with contact resistivity values ranging between 10^{-1} [139] and 10^{-5} Ωcm^2 [137, 140]. Many more reports are available for n-type contact resistance measurements within the literature because activation of p-type dopants has proved troublesome due to the limitation in PIA temperature to just below 1400 °C. As was the case with other semiconductor materials such as 4H-SiC and silicon, two topics have been discussed in detail: surface preparation and contact metals. For WBG semiconductors, another topic attracts more focus, namely post metallization annealing (PMA). Depending on the growth method of the 3C-SiC epilayer, the surface roughness can be quite different from below 1 nm to as high as tens of nm. To obtain a smooth initial semiconductor surface for ohmic contact fabrication, often, CMP is performed before any further processing. Noh et al. [139] showed that when the root mean square (RMS) surface roughness value dropped from 20 nm to 7.5 nm, respectively, the contact resistivity value was reduced by one order of magnitude, from 8.6×10^{-1} Ωcm^2 to 2.8×10^{-2} Ωcm^2. As mentioned previously, actual 3C-SiC device fabrication processing involves a high temperature (> 1400 °C) PIA process, which can potentially degrade the surface further, even if polishing was performed. A thorough discussion was made on the PIA effects on the 3C-SiC surface morphology [140] and how it is related to the resultant specific contact resistivity values. It was noted that although a severe surface degradation can be a major limiting factor, the specific contact resistivity value will not be affected much so long as the surface roughness value stays below 10 nm. Quite a few metals including aluminum (Al), titanium (Ti), Ni, Ni/Ti, Au/Ti, platinum (Pt), tungsten (W), and TiW [101, 139–149] have been studied for 3C-SiC ohmic contact fabrication. Among them, Ni seems to be the most favored, not only because it can achieve a low resistance value, but also the value has been shown to decrease with elevated PMA temperature up to ~ 1000 °C. Even though Ti and Al can achieve the same level or even lower specific contact resistance values, an increase with rising PMA temperature was previously reported for these metals, which is an indication of Schottky barrier height increase [142]. Moreover, both Ti and Al suffer from an ease of surface oxidation during processing.

5.4.9 Ion Implantation

Ion implantation, which includes a mandatory post implantation thermal treatment, is a consolidated technology for the fabrication of regions with different conductivity sign and different conductivity values next to the surface of a SiC wafer. The desired acceptor and donor densities, as well as the desired shape of the doped regions, depend on the device design that is determined by the desired electrical performance. The actual possibility to achieve the desired doping levels and device geometry depends on the ion implantation parameters, the ion implantation mask design, and the PIA treatment. Presently, 4H-SiC and 6H-SiC are the most studied SiC polytypes and the achieved results are benchmarks for setting up an ion implantation technology for 3C-SiC. Common to all, the SiC polytypes are the need of hot ion

implantation processes and of ion implantation masks that takes into account the ion lateral straggling. The latter is significantly large in the case of ⟨0001⟩ 4H-SiC wafers [150]. The heating of the SiC wafer during ion implantation induces a recovery of the lattice disorder as far as such disorder accumulates. Such a dynamic annealing inhibits the formation of heavily disordered regions where the lattice reconstruction of the original SiC polytype is no longer possible during the subsequent PIA [151]. The optimal temperature for hot ion implantation depends on the ion implantation dose rate and the implanted ion species [152]. In the case of the PIA of hetero-epitaxial 3C-SiC/Si, the annealing temperature is limited by the melting temperature of the Si substrate. It has been shown that annealing times of hundreds of hours are necessary to detect the sign of an electrical activation in the case of the ion implanted p-type dopant species Al [153]. The PIA temperature is not limited in the case of homo-epitaxial 3C-SiC. Nevertheless, preliminary experiments have shown that for annealing temperatures equal to or higher than 1700 °C, on bulk 3C-SiC, and very long annealing times at lower temperatures around 1300 °C, in the case of 3C-SiC/Si, the structural quality of the original 3C-SiC material degrades.

5.5 Summary

The presented overview in the state-of-the-art materials growth and processing of SiC clearly indicates the rapid technologic progress in recent years. Based on this, cubic SiC exhibits a realistic chance to be applied in future mid-voltage power electronic devices like they are used, for example, in electric car vehicles.

Acknowledgements

Financial support by the European Union in the frame of the Horizon 2020 program (CHALLENGE project, grant number 720827) is greatly acknowledged.

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6

Intrinsic and Extrinsic Electrically Active Point Defects in SiC

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No crystal is perfect – based on the unit of amount of substance in the International System of Units (SI), the mole [1], we typically assume a prototypical crystal to be composed of the order of 10^{23} atoms. With a density of SiC of 3.21 g/cm^3 and a molar mass of 40.11 g/mol, we arrive at approximately 4.8×10^{22} atoms per cubic centimetres SiC. Typically, SiC-based power devices in the 1.2 kV class employ active layers with a drift layer doping (nitrogen for n-type) in the range of 10^{15} to 10^{16} dopant atoms per cubic centimetres. Hence, the typical desired doping concentration in a power device drift layer is around 6 to 7 orders of magnitude lower than the total amount of atoms and, thus, beyond six sigma level, i.e. 3.4 defects per million (99.999 997% accuracy) [2]! These impurity elements – dopants – are essential for the performance of the devices.

Inevitable, however, are also impurities and intrinsic defects introduced during growth, processing, or even operation that may hamper the application of semiconductor devices. The general characteristics of those defects become relevant at also much lower concentration, as we will show below. The question arises, at which concentration do such defects start to play a role?

Let us first differentiate between intrinsic and extrinsic defects: with the term "intrinsic defects," defects originating in the SiC lattice itself – missing atoms or vacancies, vacancy complexes, stacking faults, etc. – are summarized. "Extrinsic defects" are used for all impurities, i.e. atoms not being silicon or carbon. Furthermore, within this chapter, we focus on "point defects," i.e. defects with a rather local structure involving a single or a pair of atoms. Such point defects may introduce an alteration of its surroundings within the crystal by a change of charge distribution at similar geometry or even forcing a local change of the lattice structure. Dopant impurities, on the other hand, are generally not denoted as "defects." Furthermore, unless stated otherwise, we assume that our prototypical

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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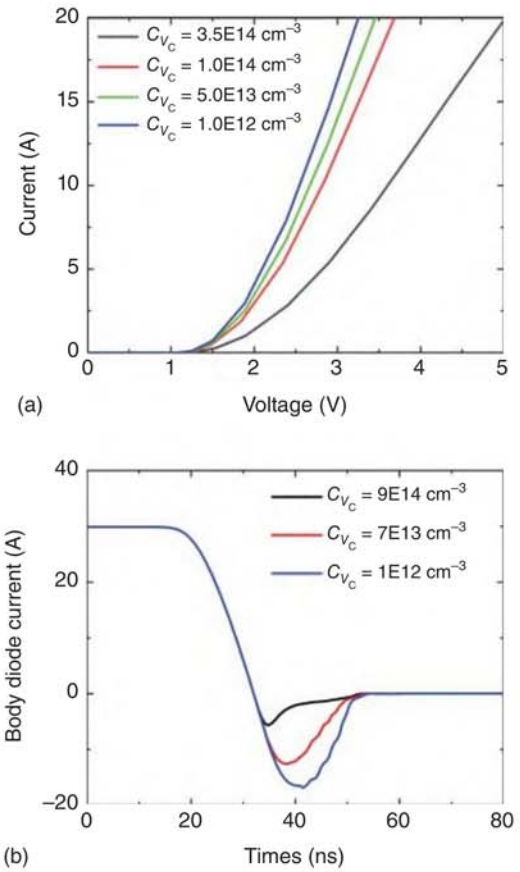


Figure 6.1 (a) TCAD simulation for the forward current of a pin diode, assuming different concentrations of the carbon vacancy, V_C. (b) Reverse recovery of the body diode in a SiC power MOSFET assuming different concentrations of V_C (TCAD simulation).

SiC to be "lightly doped n-type," i.e. exhibiting an effective donor concentration in the range of 3–5 × 10^{15} cm^{-3}, achieved by nitrogen doping during growth.

Now, with these definitions in place, let us get back to our initial question: at which level do impurities and defects in the crystal become relevant – the undesired, performance-altering defects, e.g. generation and recombination centers following Shockley–Read–Hall (SRH) statistics [3, 4], often called "lifetime-killing" defects?

One of the most dominant intrinsic defects in SiC is the carbon vacancy, V_C. In Section 6.2, the current state of the art of the accumulated knowledge on V_C will be presented. We know from experiments that an increasing concentration of V_C is limiting the charge carrier lifetime in n-type 4H-SiC [5].

With device simulations, we can gain further insight on the impact of the V_C concentration on the performance of SiC-based devices: In Figure 6.1, the effect of the change in charge carrier lifetime due to introduction of V_C on the forward current of a pin diode (a) and the reverse recovery current of a body diode of a power MOSFET (b) is shown. The investigation is based on TCAD simulations of a p–n test diode and a MOSFET structure representing a commercial 1.2 kV 4H-SiC-based power MOSFET (C2M0080120D) [6] using Sentaurus Device (S-Device) [7].

A simple p–n-diode is designed, where the thickness of the drift layer is 15 µm and the effective n-type carrier concentration is 3 × 10^{15} cm^{-3}, and simulated with

Sentaurus Technology Computer-Aided Design (TCAD) [7] in order to demonstrate the influence of the V_C concentration on the forward characteristics. Even though the defects cannot be directly incorporated in the simulation model, their effect on the carrier lifetime can be included. Extracted from Ref. [5] for different concentrations of V_C, different carrier lifetimes are used within the SRH recombination model of the device simulation which otherwise uses the default SiC models. The resulting diode current (Figure 6.1a) increases with decreasing defect concentration due to a higher carrier lifetime and thus reduced recombination rate. The effect becomes less significant at higher carrier lifetimes as other factors such as the drift doping and thickness influence the differential resistance of the diode.

Mixed mode simulations of the MOSFET model are performed to assess the influence of the defect concentration, i.e. the carrier lifetime on the reverse recovery behavior of the internal body diode. The test circuit is chosen in accordance to the datasheet of the manufacturer [6]. The default device simulation models provided by Sentaurus [7] are used, while the carrier lifetime of the SRH recombination model is adjusted to represent different V_C concentrations. The resulting body diode current (Figure 6.1b) shows a reverse recovery charge that is decreasing with increasing defect concentration as the recombination rate increases. Due to its additional dependence on drift thickness and doping the reverse recovery is not linearly dependent on the defect concentration.

Based on these rather simple estimates, we can now draw two important conclusions:

- Whereas in the case of the p–n diode the reduction of V_C in the drift layer region is strongly beneficial for achieving a higher forward current at lower bias voltages, a power MOSFET gains from an increased V_C concentration for the drift layer material in order to reduce switching losses, when utilizing the body diode. This is a classical trade-off scenario in power device design. The interested reader is pointed to [8–10].
- The impact of V_C on device performance is already pronounced at concentrations of around 1×10^{13} cm^{-3} – the level determined by Danno et al. [5] as the concentration at which $Z_{1/2}$ (we will later see the direct correlation between the level "$Z_{1/2}$" and V_C) starts acting as a recombination center – a concentration 3 to 4 orders of magnitude lower than the typical doping concentration in commonly used drift layers. Employing a statistical concept widely used in semiconductor industry: we are at a level far beyond six sigma accuracy!

The effect of recombination centers such as V_C becomes even more evident when considering conditions as observed during a short circuit (SC) event, i.e. beyond nominal operation [11]. Here, the effect of recombination on the lifetime of generated charge carriers is visible in the current decay observed after SC operation: SiC MOSFETs may exhibit a leakage current that remains after the turn-off of SC operation, which is common for bipolar Si-IGBTs (the so-called tail current), but unexpected for unipolar power devices such as power MOSFETs. Reducing the lifetimes for holes and electrons (τ_p, τ_n) enhances the SRH generation in the depletion region of the p-base/n-drift junction of the MOSFET. With a larger SRH generation, the total I_{drain} increases as the generated holes flow through the p-base to the base contact, see Figure 6.2.

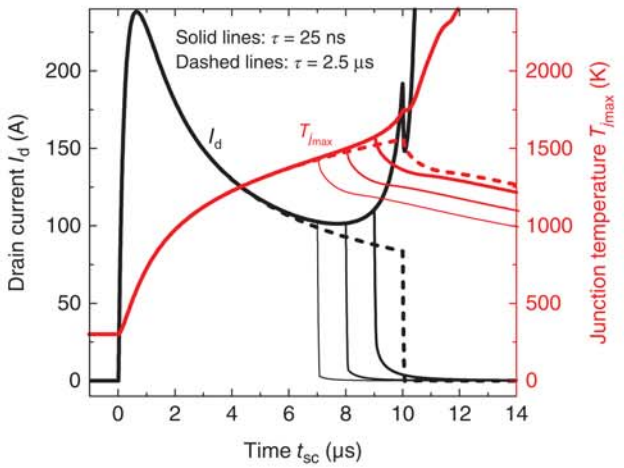


Figure 6.2 Influence of carrier lifetime (τ corresponds to maximum SRH generation lifetime of the electron) on the short circuit current and junction temperature in a SiC MOSFET. Lower generation lifetime increases the leakage current during short circuit leading to an increase of the device temperature. Increasing thickness of the black solid lines corresponds to SC current and temperature with increasing SC time duration (t_{SC} = 7 µs, 8 µs, 9 µs, and 10 µs), showing an increase in tail current at SC turn-off.

Now, one further aspect should be considered: most of the currently used SiC devices are based on material with a rather thin epitaxial "active" layer, typically in the range of some 10 µm, on top of a thicker SiC substrate (typical thickness between 110 and 350 µm), which does not contribute to the active device performance. Hence, the region of interest is the thin, high-quality, rather low-doped layer on top of the wafer. With the boundary conditions we now have established, our search for suitable characterization techniques for identification and characterization of intrinsic and extrinsic electrically active defects should, therefore, be focused on techniques sensitive to probing regions at or at least close to the surface.

The chapter is organized as follows: after a brief recapitulation of the most commonly used techniques to characterize defects in semiconductors, the most sensitive electrical characterization technique, deep level transient spectroscopy (Section 6.1.1) is described. Following, an introduction to muon spin rotation spectroscopy (µSR) is given – a nuclear method involving a short-lived subatomic charged particle highly promising for further analysis of surface-near defects (Section 6.1.2). In addition, the primary theoretical framework for investigating defects in semiconductors is mentioned (Section 6.1.3). Following are a review on recent findings of the two types of vacancies in SiC, the carbon vacancy V_C and the silicon vacancy V_{Si} (cf. Section 6.2), and a collective summary of all unambiguously assigned extrinsic electrically active defects, primarily the ones caused by transition metals (cf. Section 6.3). The chapter is concluded with a suggestion on how the findings presented can be used in current and further SiC research and development, both in science and technology (cf. Section 6.4).

6.1 Characterization of Electrically Active Defects

Very frequently, a very first approach to probe the overall quality of the crystal and its dominant types of defects is an optical method such as photoluminescence. It typically does not require any sophisticated sample preparation and is sensitive to point defects similar to the ones considered here. The investigation of luminescence in materials excited by light date back to the early 1900s, when E.L. Nichols and E. Merritt presented the first results on sidot blende (ZnS) at the meeting of the Physical Society in 1905 [12].

Since then, the method has been further refined and understanding of the spectroscopic response of the materials has improved tremendously; an excellent overview on the technique and data on photoluminescence in SiC can be found in [13] and the references cited therein.

Other techniques utilized for characterization of point defects in SiC are optical absorption, electron paramagnetic resonance (EPR), and optically detected magnetic resonance (ODMR). For more detailed information, we point to the most recent book publication [14] and the references cited therein, as this is not the main focus of this contribution.

These techniques are highly successfully employed for defect characterization, but cannot readily identify electrically active traps or their position in the band gap. Especially optical methods are probing at a completely different region compared to a method depending on capture and emission processes within in a depletion region, such as deep-level transient spectroscopy (DLTS); the incoming laser light in photoluminescence, for example, can excite the entire region of the sample and its detected signal is collected from several 100 μm^3 areas. Furthermore, most available research results using photoluminescence are obtained at fairly low temperatures. In order to avoid the effect of lattice vibrations and to extract clean spectra, most results have been obtained at temperatures below or at about 10 K, and spectra will not exhibit narrow features at temperatures above 100 K. This is in contrast to electrical techniques, which can reliably provide information up to 700 K (see, for example, DLTS studies on near-midgap states of Pt in SiC [15]).

6.1.1 Deep Level Transient Spectroscopy

DLTS is the most sensitive method for the characterization of electrically active defects in semiconductors [16]. It is based on the electron and hole trapping in the Shockley–Read–Hall model [3]. By means of DLTS, it is possible to determine the energetic position and the capture cross section for charge carriers of an electrically active trap in the space charge region of a semiconductor device. In most DLTS studies, Schottky diodes or p–n junctions are used. During a typical DLTS measurement, traps in the space charge region are filled with a pulsing voltage. Upon returning to the reverse bias condition, the traps re-emit the charge carriers due to thermal activation. The measured signal is directly proportional to the number of charge carriers involved in that particular emission.

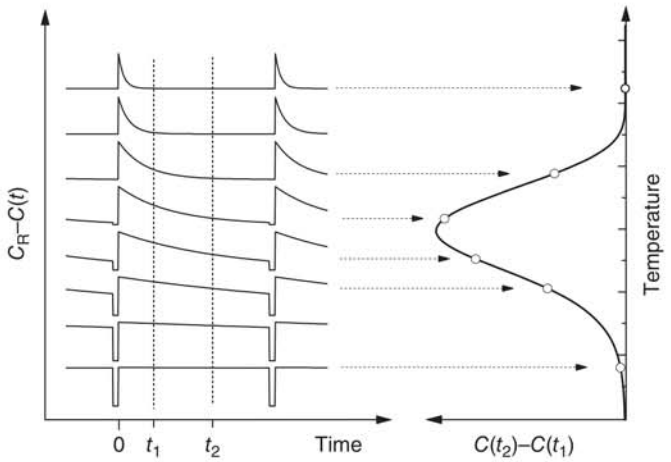


Figure 6.3 From capacitance transients to DLTS spectrum: the capacitance is measured at two different times t_1 and t_2 during the charge carrier emission (left panel). The difference $C(t_2) - C(t_1)$ is stored for each temperature step observed. In the resulting DLTS-signal, a peak can be observed when the emission rate matches the time window (right panel).

The most frequently used technique is the so-called capacitance-DLTS (C-DLTS) that measures the width of the space charge region by observing the diode capacitance. One critical assumption that is made for the evaluation of DLTS data is that the trap concentration is much smaller than the shallow doping concentration. Furthermore, in most cases, it is assumed that the capture cross section does not depend on the energetic position of the trap in the band gap.

The simplest way to determine the emission rate is the so-called box-car method (see Figure 6.3). The capacitance is measured at two different times t_1 and t_2 during the charge carrier emission. The difference $C(t_2) - C(t_1)$ is stored for each temperature step observed. In the resulting DLTS signal, a peak can be observed when the emission rate matches the time window. Applying different time windows t_1 and t_2 leads to different peak positions and the emission rate can be determined by $(t_2 - t_1)/\ln(t_2/t_1)$ at each temperature position. More advanced DLTS systems also use other correlation functions like a sine wave (first Fourier factor) or a double-rectangular function [17]. This may result in spectra with a higher resolution, i.e. narrower DLTS peaks, which may aid to distinguish traps with similar parameters. One should note here that using the capacitance rather than the current transient leads to the effect that the collected charge carrier is not traveling through the junction; therefore, the capacitance-based DLTS is not sensitive to the region close to the junction interface (for a typical drift layer doping this "blind" region is around 100–300 nm thick from the top of the sample/the junction). Application of a forward bias may result in information closer to the surface; however, the validity of all assumptions made in DLTS analysis needs to be ensured.

From the linear regression of the Arrhenius plot of the resulting data, the trap energy is then determined from the slope of the curve. The capture cross section results from the intersection with the $-\ln(T^2t)$-axis. It is important to note that the

latter value represents the product of the entropy factor and the true capture cross section. If the bare capture cross section is to be determined, measurements with a varying duration of the pulse voltage can be performed. Though, this places higher demands on the measurement equipment, i.e. an external pulse generator that is capable of pulses in the order of nanoseconds.

There are multiple descriptions on different flavors of DLTS and a wide range of applications available in the literature. Here, we would like to point the reader to the following, more classical publications aiming at the basics of the technique rather than its application for specific types of samples: [16–19], and, most certainly, [20].

6.1.1.1 Profile Measurements

DLTS is also capable of determining the depth profile of deep levels in the space charge region. One way to observe a depth-dependent concentration is to record the DLTS signal at fixed temperature (isothermal DLTS), varying the reverse and pulse bias and thus the probed region of the device. This is also referred to as double-correlated DLTS (DDLTS).

6.1.1.2 Poole–Frenkel Effect

The electric field in the space charge region affects the emission of charge carriers from a deep donor in an n-type and a deep acceptor in a p-type semiconductor [21]. A deep donor is positively charged after the emission. Therefore, the electron has to overcome the Coulomb barrier. The electric field in the space charge region superimposes the Coulomb field of the donor and thus decreases the barrier. In this case, the emission rate is reduced, and the resulting trap energy determined from DLTS spectra is too low. This is called Poole–Frenkel effect and is often neglected in studies on deep levels. In detailed studies, the Poole–Frenkel effect is determined, e.g. by varying the reverse bias and thus the electric field strength in the space charge region observed. By measuring the emission rate at different electric fields, it is possible to evaluate the correct trap position in the band gap and determine the charge state. In this case, it is necessary to measure the emission rate in a reasonably small part of the space charge region only since the electric field varies with depth. This can also be achieved with DDLTS measurements.

6.1.1.3 Laplace DLTS

Laplace-DTLS has been developed for obtaining a better resolution of major traps in DLTS spectra [18]. Essentially, the data from the capacitance transient are transformed from the time to the frequency domain, enabling an increase in energy resolution by 1 order of magnitude compared to conventional DLTS. The most recent findings, both for V_C and V_{Si}, have been obtained using Laplace-DLTS and will be further discussed in Section 6.2.

All examples given for intrinsic and impurity trap levels in Sections 6.2 and 6.3 are based on one or the other flavor of DLTS analysis, as we deem this technique the most precise for determining activation energy E_a and capture cross section σ for the identification of extrinsic and intrinsic trap levels in the bandgap of a semiconductor, including SiC.

6.1.2 Low-energy Muon Spin Rotation Spectroscopy

In muon spin rotation (μSR) spectroscopy, charge and spin of a short-lived subatomic particle called *muon* are used as sensitive local electronic and magnetic probes of matter. Muon spin rotation (or relaxation or resonance) is a relatively young nuclear method and can be classified between nuclear magnetic resonance (NMR) and diffraction techniques [22]. In contrast to NMR or Mössbauer spectroscopy, μSR does not rely on internal nuclear spins of the target material but can be applied for any type of material in a large variety of environments (e.g. different temperatures, pressures, magnetic and electric fields, …). The fact that the spin polarization of the muons is provided by the laws of particle physics also implies that the magnetic properties of the sample can be studied under zero external field. Muons are instable leptonic particles with an electric charge of $\pm 1\ e$, a spin of 1/2 and a mass of 207 m_e (or 1/9 m_p) [23]. They can be obtained at high-energy proton accelerators through the decay of pions which are produced in nuclear interactions between accelerated particles and nuclear targets. At dedicated muon facilities, muons (in most cases, positive μ^+) are implanted into the material of interest. After a mean lifetime of 2.2 μs, they decay again into a positron e^+ (or electron in case of μ^-) and two neutrinos. The muon decay violates parity, with the result that the positrons are preferentially emitted along the direction of its spin [24]. By measuring the direction of the emitted positrons in a time-resolved fashion using detectors outside of the target material, conclusions on the spatial distribution and dynamical fluctuations of the muons' magnetic environment can be drawn.

A more complete description of μSR and the wide range of applications can be found in a number of books [23, 25–28] and review articles [22, 24, 29–32]].

The main advantages compared to other nuclear methods are the extreme sensitivity of the μSR technique to small internal magnetic fields (reaching down to ~0.1 G) and its unique time window for the study of magnetic fluctuations between 10^4 and 10^{12} Hz, bridging the gap between NMR and neutron scattering techniques. In general, μSR experiments require high muon fluxes of more than 10^3 muons/(s cm^2) which can only be obtained at high-energy accelerators such as the proton accelerator facility at the Paul Scherrer Institute, PSI.

For applications in thin film and surface investigations, muon beams in the range of eV to several keV are needed, yielding implantation depths into the target material ranging from below-nanometer to the order of hundred nanometer [25]. The most successful method to generate low-energy (LE) muons with a decent beam intensity is an approach developed at PSI [33]. This modified μSR technique then also allows probing the region which is otherwise not easily accessible using DLTS, namely, the very surface-near region.

6.1.2.1 μSR and Semiconductors

Depending on the host material, the implanted μ^+ interacts differently with its environment during its short lifetime of 2.2 μs. In metals, the positive charge of the muon is collectively screened by a cloud of conduction electrons and behaves like a free muon. In insulators, semiconductors, or molecular compounds on the other hand,

the muon will usually pick up one electron and form muonium (Mu = μ^+e^-) with the size of the Bohr radius and reduced mass and ionization potential very similar to a hydrogen atom. The evolution of the muon spin during Mu formation is governed by a spin Hamiltonian which includes the interaction between the muon and electron spins as well as the Zeeman interactions between the external field and the electron and muon spins [24, 26].

The muonium formation process varies significantly for different semiconductors and the particularities of each host material have to be considered carefully when interpreting the μSR data.

During the past few years, LE-μSR has been successfully employed for the characterization of V_C [34], V_{Si} [35] as well as the SiO_2/4H-SiC interface region [36]. Considering the recent results, the LE-μSR technique shows great promise for the characterization of defects in SiC, especially close to the surface and including the depth resolution required for the analysis of thin interface structures.

6.1.3 Density Functional Theory

To accompany the aforementioned experimental techniques, an *ab-initio* technique, namely, density functional theory (DFT) is widely used for assessment of potential point defects; one should note, however, that at the beginning of any such simulation there is an assumption on the shape and the characteristics of the investigated defect, which is then rather probed for its likelihood compared to another version rather than enabling a clear identification.

Also, the exact determination of the energetic position of the investigated defect structure in the bandgap requires advanced methods beyond traditional DFT techniques and should, therefore, be carefully reviewed. An excellent example is given by Jose Coutinho et al. [37], whose clear identification of the different transitions of the carbon vacancy in SiC will be discussed in more detail in the later part of this chapter. Here, we would like to turn the focus of the reader on a rather basic problem of DFT-based methods - the choice of the correct setup of the initial supercell to simulate the defect in question and the charge correction required. In Figure 6.4, the effect of the size of the so-called supercell (the collectively treated sum of all unit cells multiplied toward all reciprocal coordinate directions) on the necessary charge correction is presented. As discussed in the very beginning of this chapter, the typical defect concentrations are in the range of 1×10^{12} cm^{-3} to 1×10^{14} cm^{-3}, i.e. up to only approximately 0.0001 defects per million atoms. It is very obvious that both potential corrections of charges as well as the effect of supercells being systematically smaller than real crystals have to be carefully taken into account.

As both optical measurements as well as ab inito simulations are based on completely different areas and even orders of magnitude in size compared to the probed volumes in DLTS or LE-μSR, in most publications on defect characterization using optical or ab initio methods the values obtained may differ compared to the ones obtained by direct electrical measurement using DLTS, complicating the successful correlation to final device performance.

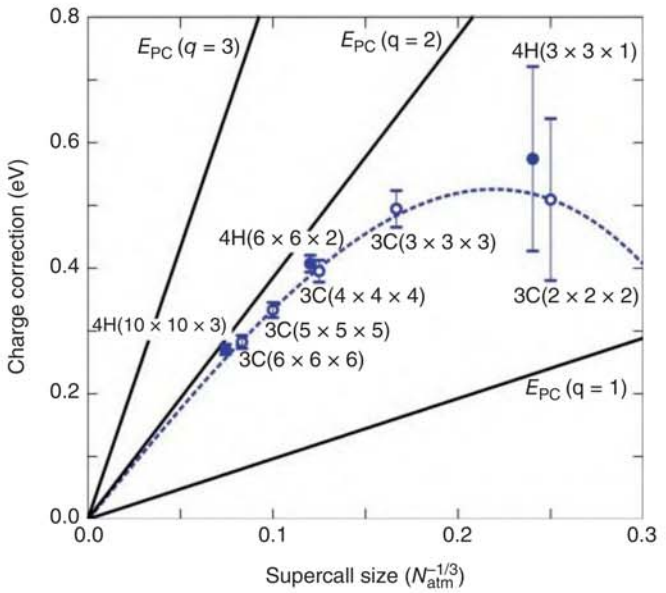


Figure 6.4 Variation of the charge correction, E_{corr}, obtained for a double positively charged carbon vacancy in 4H-SiC (closed circles) and 3C-SiC (open circles) supercells sized by the number of atoms, N_{atm}. Error bars are standard deviations obtained from the averaging of $\Delta\Psi_{PC,ind}$. Integer triplets ($l \times m \times n$) are scaling factors applied to the lattice vectors of each unit cell to obtain the respective supercell. The dashed line represents a function of the form $a\,N_{atm}^{-1} + b\,N_{atm}^{-1/3}$ fitted to the data. Solid lines represent simple point charge corrections for q = 1, 2, and 3. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

6.2 Intrinsic Electrically Active Defects in SiC

In recent years, the understanding of the behavior and stability of the silicon and carbon vacancy in SiC has significantly improved. These two types of intrinsic defects are now very well understood – the focus of this section is, therefore, a careful review of the current state of the art, as found both in experiment as well as theory.

Prior to geometric relaxation, V_{Si} and V_C exhibit a nearly tetrahedral C_{3v} symmetry. Although V_{Si} and V_C initially appear similar, variations in their local environment lead to drastically different behavior.

V_C is surrounded by Si atoms having extended dangling bonds that overlap, and the degenerate ground state makes V_C susceptible to a symmetry-lowering Jahn–Teller distortion. The overlapping Si orbitals neighboring V_C drive a strong inward displacement to increase the overlap, and pairwise Si–Si dimer formation reduces the V_C symmetry to C_{1h} in the neutral charge state [38–42]. As a result, V_C exhibits negative-U characteristics [43] and becomes a deep-level carrier trap responsible for limiting carrier lifetimes in 4H-SiC, thereby lowering the performance of 4H-SiC power electronic devices [44].

V_{Si}, on the other hand, is surrounded by highly localized C orbitals with negligible overlap, similar to the vacancy in diamond. Without nearest- neighbor bonding, there is no driving force for a JT distortion in V_{Si} and a high energetic cost for inward displacement. Instead, the Si–C bonds shorten, yielding a symmetry conserving outward-breathing relaxation. V_{Si}^{-} exhibits $S = 3/2$, long spin coherence times, and single-photon emission [45], in contrast to the low-spin ($S = 0$) and negative-U character of V_C [37, 43]. Owing to these properties, the V_{Si} has been identified as a promising candidate for a wide range of quantum applications, including quantum communication, computing, and sensing [45–47].

6.2.1 The Carbon Vacancy, V_C

The DLTS levels finally assigned to the different charge states of V_C, $Z_{1/2}$ and $EH_{6/7}$ [48], have long been under discussion. Originally, the first description of a deep level in SiC named Z_1 was given in [49]. Over the years, this level has been assigned to V_C^{-} or carbon-interstitial complexes involving nitrogen [50, 51] or hydrogen [52].

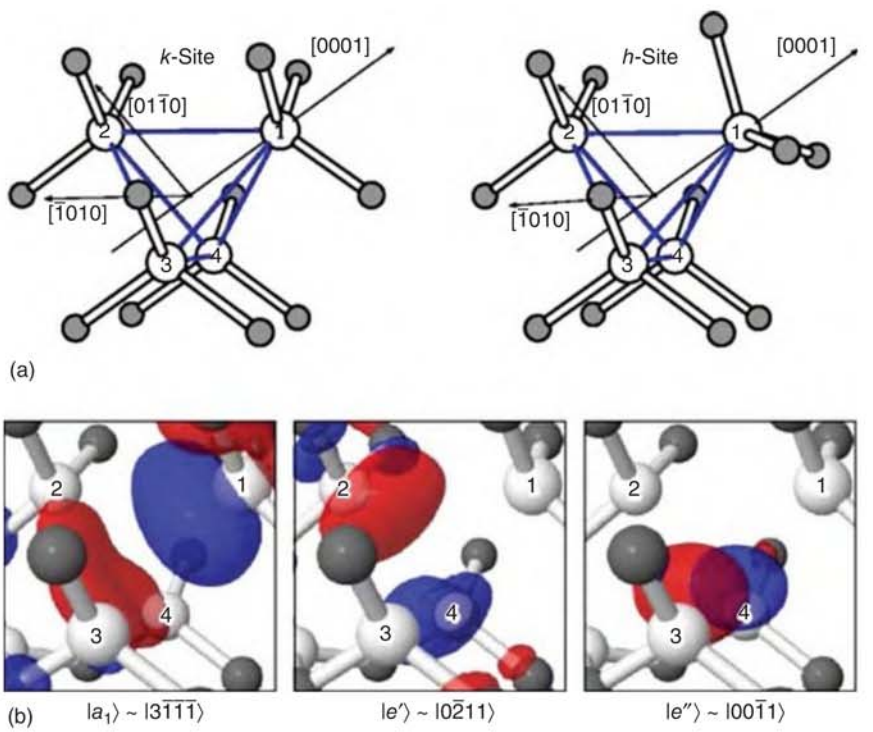


Figure 6.5 (a) Atomic structure of perfect carbon vacancies at *k* and *h* sites of a 4H-SiC crystal. Si and C atoms are white and gray, respectively. Si_1 is axial (located on the [0001] crystallographic axis), whereas Si_{2-4} atoms lie on the basal plane. (b) Representation of the one-electron states in the gap ($a_1 + e$) arising from an undistorted V_C defect at the *k* site. Red and blue isosurfaces denote negative and positive phases, respectively. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

Also, the thermal stability of the trap level was under discussion for a very long time – initial studies even suggested annealing at temperatures as low as 1300 °C [53]. The final assignment of $Z_{1/2}$ and $EH_{6/7}$ to V_C has been presented by Son et al. [43].

Since then, the focus has been on developing further understanding of properties, annealing behavior, and migration. We will start our discussion at the point in time represented in detail in [13] – around 2014. Whereas at this stage the state of the art

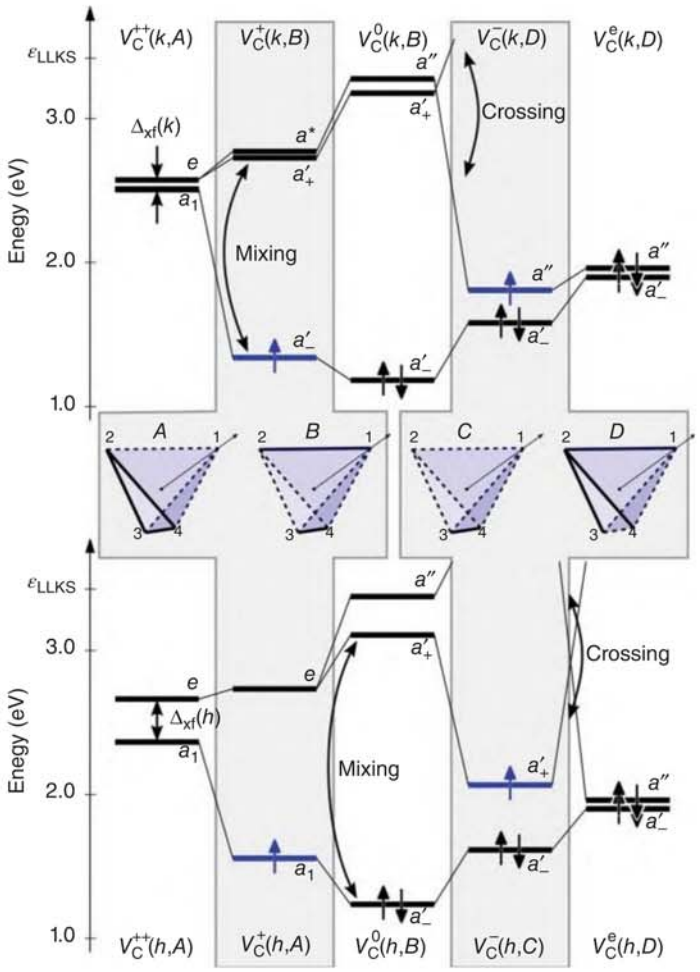


Figure 6.6 Kohn–Sham electronic states at $k = \left(\frac{001}{2}\right)$ for the carbon vacancy at the cubic (upper half) and hexagonal (lower half) sites. The zero of the energy scale is at the ϵ_{HOKS} energy in bulk (using the HSE06 functional). Electrons are represented by upward (spin-up) and downward (spin-down) arrows. Each state is accompanied by symmetry labels (see text for details). The central region displays the structures found for positively charged (*A* and *B*) and negatively charged (*C* and *D*) defects. Contracted/elongated Si–Si distances are represented as solid/dashed lines, respectively. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

was represented by decreasing the V_C concentration using oxidation [56, 57] showed that V_C can also be generated in high-temperature annealing above 1600 °C. From these experiments, kinetics of V_C was determined and the generation rate of V_C, the diffusivity of V_C and carbon interstitials, C_i, was determined to be 6.3, 2.5, and 1.5 eV, respectively [58]. This triggered also a more detailed analysis of the correct treatment of the V_C in DFT calculations, especially with respect to the correct representation of lattice distortions. Starting from the ideal crystal configuration (cf. Figure 6.5), the relaxation and resulting mixing of the different states is determined (cf. Fig 6.6). Finally, the formation energies for the charge states and their dependence on growth conditions (C- or Si-rich) are investigated (see Figure 6.7), and the configuration coordinate diagrams of V_C defects in 4H-SiC are presented (see Figure 6.8).

In a combination of Laplace-DLTS and DFT, the capture and emission behavior of the acceptor states of V_C could then be directly determined with great precision [54]. Interestingly, the suggested fast capture process of the second electron seems to confirm the findings made recently in LE-μSR experiments [35]: Here, a two-electron capture process at the V_C needs to be considered where a Mu^+ forms Mu^- via a short-lived Mu^0 state (Figure 6.9).

Migration of V_C was further investigated in [55]; the V_C shows a different migration pattern for *a*-cut vs. *c*-cut SiC wafers. Diffusion of V_C along the *a*-direction is found to exhibit a lower activation energy than migration along *c*-direction. Furthermore, although the formation energy of V_C is lower than the one for C_i, the energy required for diffusion is higher for V_C than for C_i.

The authors find that although V_C has a lower formation energy than C_i, it is still less mobile, so that self-diffusion of carbon in SiC is most likely governed by carbon interstitial migration (Figures 6.10 and 6.11).

In summary, the recent advances in understanding of the carbon vacancy in SiC have been achieved by the combination of various experimental and theoretical

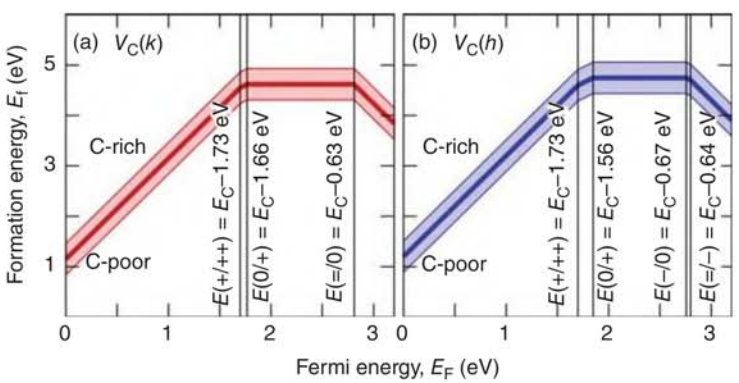


Figure 6.7 Formation energy (E_f) of the carbon vacancy at the cubic (a) and hexagonal (b) sites as a function of the Fermi energy (E_F). Lower, central, and upper lines represent E_f values for crystals grown under C-poor (or Si-rich), stoichiometric, and C-rich conditions. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

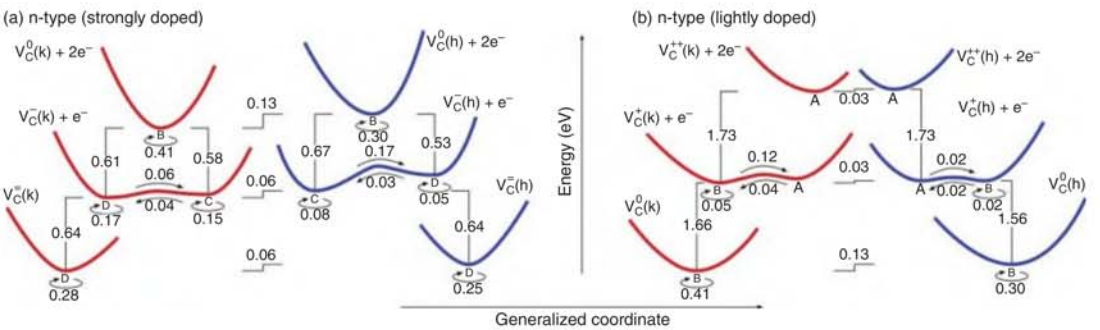


Figure 6.8 Configuration coordinate diagram of V_C defects in 4H-SiC. Acceptor and donor transitions are shown in (a) and (b), representing strongly doped and lightly doped n-type material, respectively. Electronic transitions (up in energy) involve the emission of one electron to the conduction band (e^-). Insets (a) and (b) include two diagrams, one for each sublattice site. Energies (in eV) are accompanied with guidelines for better perception. Forward/backward transformation and rotation barrier energies are indicated by right/left and spinning arrows, respectively. Steplike guidelines indicate the energy difference between ground states of defects in *k* and *h* sites. Minima of the potential curves represent stable/metastable structures and are identified with labels A–D. Source: Reprinted with permission from [37]. Copyright (2017) by the American Physical Society.

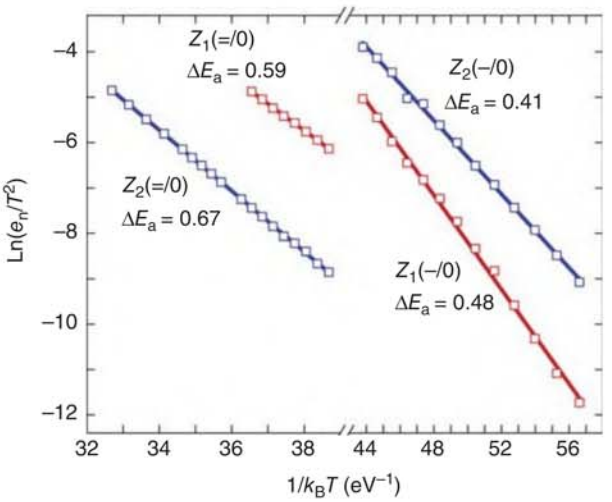


Figure 6.9 Arrhenius plots of electron emission rates for $Z_1(=/0)$, $Z_2(=/0)$, $Z_1(-/0)$, and $Z_2(-/0)$ transitions in 4H-SiC obtained by L-DLTS measurements. Activation energies for electron emission are also shown for each peak. The horizontal axis is broken and separates double from single emissions. Source: Reprinted from [54], with the permission of AIP Publishing.

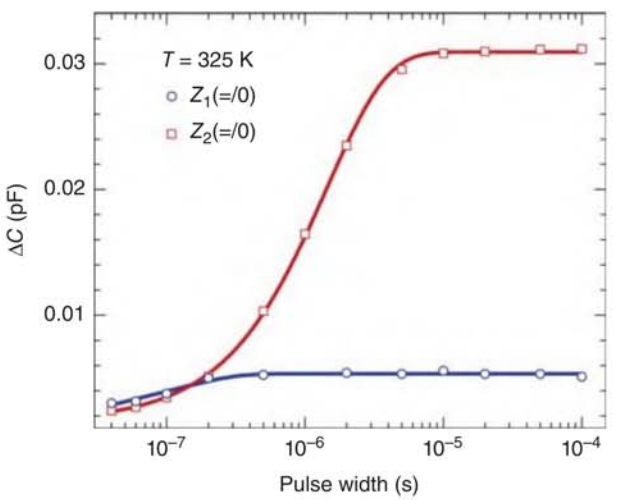


Figure 6.10 Capture kinetics measured for $Z_1(=/0)$ and $Z_2(=/0)$ transitions by L-DLTS at $T = 325$ K. Data points are the magnitude of the L-DLTS peaks for different durations of the filling pulse. Source: Reprinted from [54], with the permission of AIP Publishing.

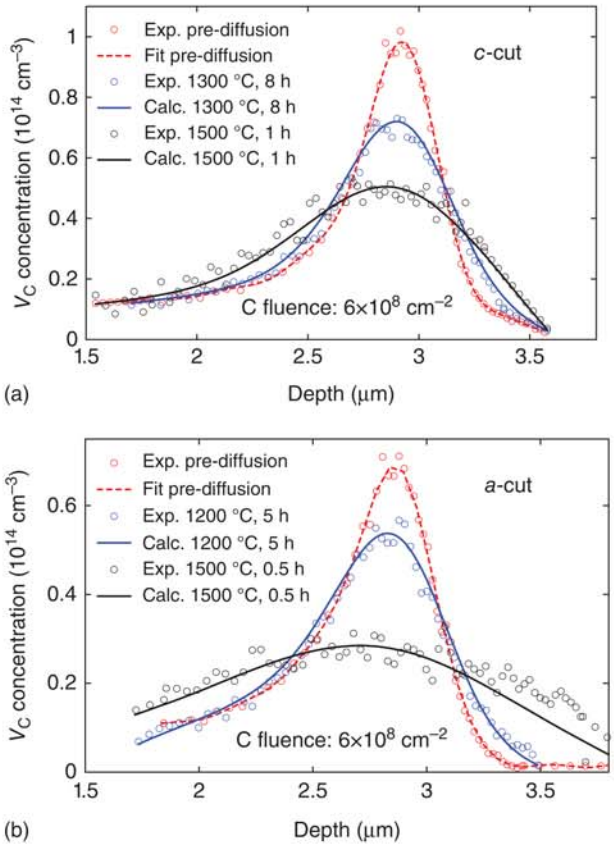


Figure 6.11 V_C concentration vs depth profiles along the (a) *c* and (b) *a* direction before (red) and after (blue and black) annealing at temperatures between 1200 and 1500 °C. Circular marks represent experimental data, red dashed lines are fits to the initial profiles, and solid lines are the diffused profiles calculated by solving the diffusion equation. Source: Reprinted with permission from [55]. Copyright (2019) by the American Physical Society.

approaches. V_C has been unambiguously correlated to the well-known $Z_{1/2}$ and $EH_{6/7}$ levels as seen in DLTS. The fast capture process also has been observed experimentally using LE-μSR, and the theoretical framework developed in the course of the various studies allows the correct prediction of formation and activation energy. This has enabled also a good understanding of annealing conditions where either a generation or an annealing of V_C can be expected, delivering a useful processing method toward lifetime control in power devices (Figure 6.12).

6.2.2 The Silicon Vacancy, V_{Si}

For a very long time, the electronic signature of the Si vacancy was unknown. In photoluminescence spectroscopy, the V_{Si} exhibits a well-known fingerprint [60, 61]. Only very recently, the DLTS signature of the silicon vacancy in 4H-SiC has been identified [59].

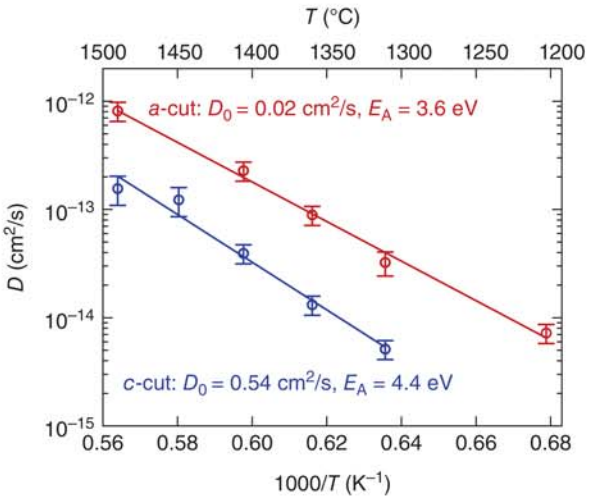


Figure 6.12 Temperature dependence of V_C diffusivity (D) along the c direction (blue) and a direction (red), with D clearly obeying Arrhenius behavior. Circular marks represent D, and solid lines are linear fits to the data. The extracted fitting parameters (D_0 and E_A) are included in the figure. Source: Reprinted with permission from [55]. Copyright (2019) by the American Physical Society.

A so-called S_1 level has first been observed in 4H SiC after electron irradiation with 2 MeV electrons [62]. This first study raised a lot of questions as the defect appeared to be comparably unstable in irradiation and subsequent annealing experiments (especially compared to what we now know to be the signature of V_C). Hence, in a further study [63], the trap level was named "S" (as in sporadic, not Si), and the behavior remained a "mystery" for quite some time. In retrospect, a truly visionary choice of naming this level! S_1 and S_2 have first been identified as different charge states of one and the same defect in [64] and were further investigated in [65].

A definite assignment of S_1 and S_2 to V_{Si} and the identification of the $(-/2-)$ and $(2-/3-)$ charge transition levels of V_{Si} using DLTS and a combination of proton irradiation, photoluminescence and DFT was presented by Bathen et al. [59].

LE-μSR investigations show that a μ^+ in the vicinity of V_{Si} is captured to form an isolated and stable Mu^0, which does not interact further with the environment [35], an effect corroborated by the stability of the hydrogen-V_{Si} complex found recently [66].

From optical measurements and DFT calculations, V_{Si} has for a long time now attracted a lot of attention as a high-spin qubit candidate with long spin lifetimes. From recent Laplace-DLTS, two contributions for the S_1 state were identified, assigned to the hexagonal and cubic lattice site (see Figure 6.13). With the identification of the electronic signature, it is now possible to access the V_{Si} also electrically, as shown in Figure 6.14 and [59]. This may allow a good electrical spin control in a spintronic application in the true sense of the word.

6.3 Transition Metal and Other Impurity Levels in SiC

Transition metals (TM) are a common impurity in semiconductor material, often introduced during growth (see also other chapters in this book). Furthermore, intended doping with transitions metals is aimed at formation of recombination

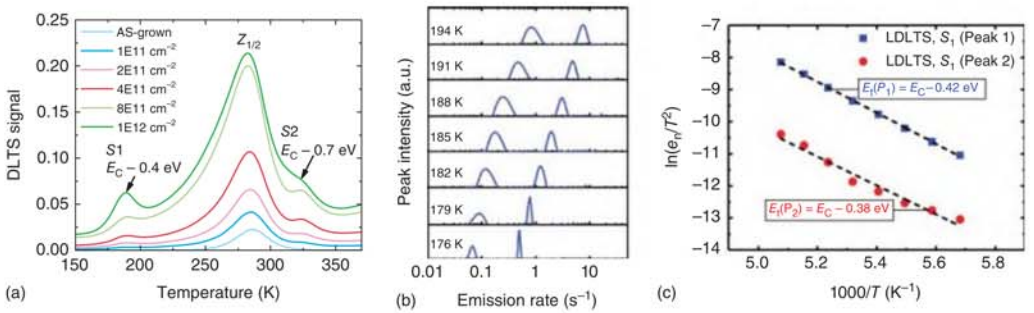


Figure 6.13 Experimental characterization of V_{Si} charge state transitions. (a) DLTS spectra of proton-irradiated n-type 4H-SiC samples, evidencing an increase in S_1, $Z_{1/2}$, and S_2 intensities with proton fluence. (b) Temperature-dependent Laplace-DLTS measurements of the S_1 peak, demonstrating that S_1 contains contributions from two defect centers, likely $V_{Si}(h)$ and $V_{Si}(k)$. (c) Arrhenius behavior of the two contributions to S_1 revealed by the Laplace-DLTS measurements. The confidence intervals for the activation energies are approximately ±0.01 eV for E_t(P1) and ±0.02 eV for E_t(P2). Source: Reprinted with permission from [59] under the terms of the Creative Commons CC BY license. Copyright 2019, Springer Nature.

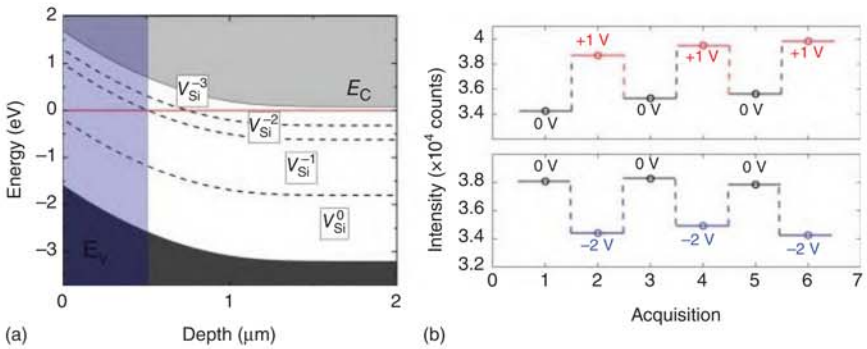


Figure 6.14 (a) Simulation of a Schottky barrier diode using Sentaurus S-device [7], without applied bias and at 100 K and depiction of the different charges states of V_{Si}. (b) Selective switching of the V_{Si} luminescence intensity is experimentally demonstrated for the forward- and reverse-biased Schottky barrier diode. The sample has been irradiated with a proton fluence of 1×10^{12} cm^{-2}. For each acquisition cycle, the intensity level on the plot represents an averaged value over 201 measurements, resulting in minimal standard deviation (within the marker size). Source: Adapted from [59].

centers for fast switching devices. Other transition metals are interesting for use in spintronic applications, e.g. for formation of diluted magnetic semiconductors. In Tables 6.1–6.3 and Figure 6.15, all unambiguously identified trap levels in SiC are summarized. The experienced reader will notice that the list of impurities and references is limited compared to the data collection presented in [13] and other reviews. We justify this approach by the careful analysis of the available data and publications. All data and references included in this work have been obtained by direct electrical measurements using DLTS, most of them using radiotracer DLTS, allowing an unambiguous assignment of the trap level to the impurity element, i.e. avoiding misinterpretation due to incompletely annealed radiation or any other processing damage. Also, the collection does not contain data from any optical method such as photoluminescence. As discussed above, the comparison between charge transitions as observed in photoluminescence with the capture and emission directly measured using DLTS is not straightforward and may be misleading. Furthermore, we did not include data where the original reference was not retrievable.

It should be pointed out here that this extreme approach does not allow us to provide any information on the following elements, which have been presented elsewhere: molybdenum, manganese, and oxygen. We hope that the reader acknowledges this rigor and that we can provide a truly reliable database for the years to come.

Table 6.1 Transition metal impurities in SiC–parameters identified by DLTS.

Element	4H				6H				15R				3C			
	E (eV)	σ (10^{-14} cm^2)	Site	References	E (eV)	σ (10^{-14} cm^2)	Site	References	E (eV)	σ (10^{-14} cm^2)	Site	References	E (eV)	σ (10^{-14} cm^2)	Site	References
Cr (−/−)	−0.14	0.1		[1,2]												
	−0.18	0.1		[1,2]												
Cr (−/0)	−0.74	0.2	k/h	[1,2]	−0.53	2	k	[4]	−0.45	1	k	[5]				
					−0.55	2	h	[4]	−0.47	1	h	[5]				
Cr (+/++)	0.54	0.2	h	[3]												
	0.63	1	k	[3]												
V (−/0)	−0.96	1	k	[1,2]	−0.71	0.04	k	[4]	−0.7	0.2	k	[1,2]				
	−0.98	1	h	[1,2]	−0.75	0.1	h	[4]	−0.72	0.2	k	[1,2]				
									−0.74	0.01	k	[1,2]				
									−0.76	0.01	h	[1,2]				
									−0.8	0.01	h	[1,2]				
Ti (0/−)	−0.13	1		[1,2]												
	−0.17	1		[1,2]												

Negative values of E_a denote values measured from the conduction band edge, positive values of E_a denote values measured from the valence band edge.
References: [1–5, 67–71]

Table 6.2 Transition metal impurities in SiC–parameters identified by DLTS.

	4H				6H				15R				3C			
Element	***E*** **(eV)**	σ **(10^{-14} cm^2)**	**Site**	**References**	***E*** **(eV)**	σ **(10^{-14} cm^2)**	**Site**	**References**	***E*** **(eV)**	σ **(10^{-14} cm^2)**	**Site**	**References**	***E*** **(eV)**	σ **(10^{-14} cm^2)**	**Site**	**References**
Ta (0/+)	−0.66	5	*h*	[1]	−0.46	10	*h*	[2,3]	−0.42	10	*h*	[2,3]				
	−0.69	5	*k*	[1]	−0.49	10	*k*	[2,3]	−0.45	10	*k*	[2,3]				
Ir (−/0)	−0.82	7		[4]												
Pt (−/−)	−0.81	0.4		[4]												
Pt (−/0)	−1.46	0.3		[4]												
Ru (−/0)	−0.87	1		[5]												
Pd (−/0)	−1.03	0.1		[5]												
W (−/0)	−0.17	50	*k*/*h*	[6]												
	−1.43	100	*k*/*h*	[6]	−1.16	60	*k*/*h*	[6]	−1.14	60	*k*/*h*	[6]	−0.47	10		[7]
Fe	−0.39	0.2		[8]												
	1.46	3		[8]												
	0.97	0.07		[8]												

Negative values of E_a denote values measured from the conduction band edge, and positive values of E_a denote values measured from the valence band edge.
References: [1–8, 15, 72–78]

Table 6.3 Other impurities in SiC–parameters identified by DLTS.

Element	4H				6H				15R				3C			
	E (eV)	σ (10^{-14} cm^2)	Site	References	E (eV)	σ (10^{-14} cm^2)	Site	References	E (eV)	σ (10^{-14} cm^2)	Site	References	E (eV)	σ (10^{-14} cm^2)	Site	References
Be (−/0)	1.06	5	k/h	[1]												
Zn (+/0)					1.16	1.4		[2,3]								
Cd (++/+)	1.19	0.02	k/h	[2]												
Er (+/0)	0.75	2	k/h	[4]	0.78	2	k/h	[4]								
Gd (+/0)	0.94	4		[5]	0.95	4		[5]								
Eu (+/0)	0.86	4…7		[6]	0.88	4…7		[6]								

Negative values of E_a denote values measured from the conduction band edge, and positive values of E_a denote values measured from the valence band edge.
References: [1–6, 79–84]

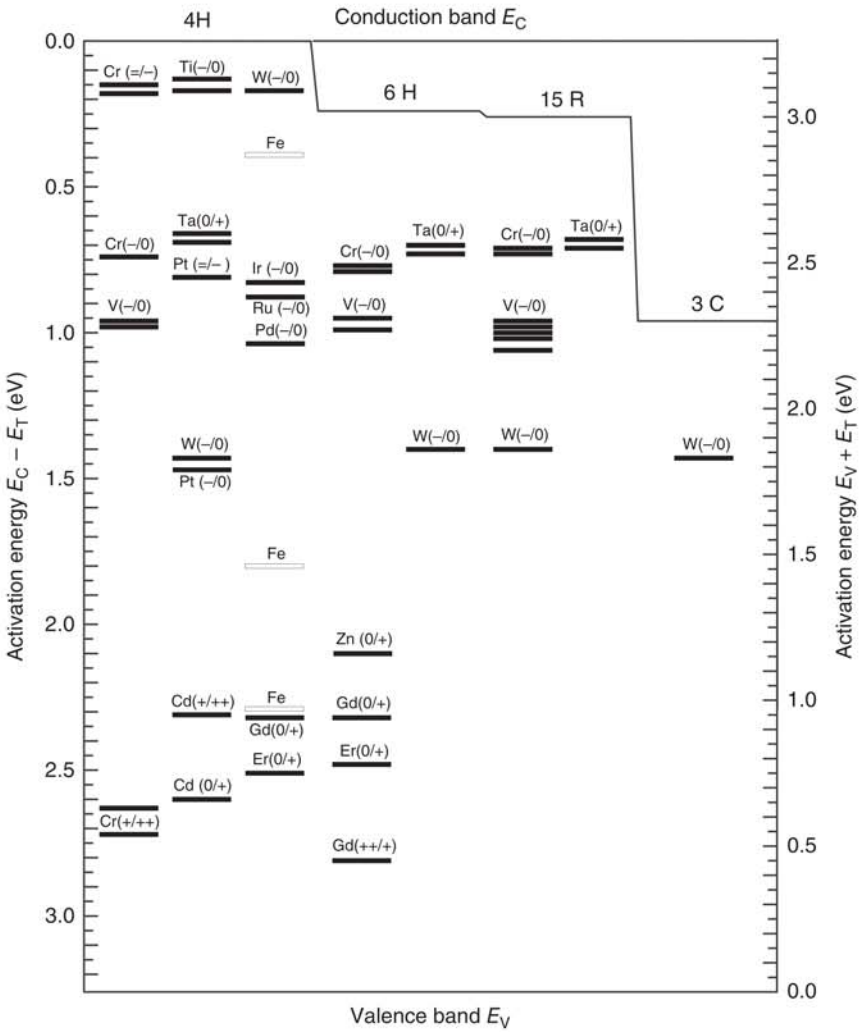


Figure 6.15 Overview of all, by means of DLTS, directly measured trap levels caused by impurities, which have been unambiguously assigned to the respective element and have been measured in the respective polytype. Detailed data and the corresponding references are listed in Tables 6.1–6.3.

6.4 Summary

To conclude this chapter on electrically active defects in SiC, let us briefly summarize our findings first.

For both V_C and V_{Si}, the electrical signatures have now been clearly identified. This enables not only a much clearer picture on how these intrinsic defects behave but it also allows the cross pollination toward a variety of very targeted new studies and the development of new and exciting applications.

Furthermore, it is impressive how the combination of methods such as DLTS, LE-μSR, photoluminescence spectroscopy, and DFT can deliver insights into the capture and emission processes of charges in these intrinsic defects. A μ^+ in the vicinity of V_{Si} is captured to form an isolated and stable Mu^0, which does not interact further with the environment. The capture of μ^+ at V_C may also result in the formation of Mu^0, but interactions between V_C and the environment are strong, prompting the capture of a second electron and the formation of delayed Mu^-. This is similar to electron localization in V_{Si}^-, where weak interactions between V_{Si} and the surroundings result in long spin coherence times and a weak outward breathing motion of the neighboring carbon atoms. Conversely, the neighboring atoms surrounding V_C collapse inward following a symmetry-lowering path, leaving a smaller lattice void for the muon to fill in V_C compared to V_{Si}. The strong electron–phonon coupling of V_C leads to a prominent Jahn–Teller distortion of the surrounding geometry, which may be indirectly probed via the Mu formation process of the implanted μ^+. This interpretation is also supported by DFT calculations, where the geometric relaxation surrounding $(V_{Si}\text{-Mu})^-$ is almost identical to that of V_{Si}^-, while introducing a muon into V_C^0 and forming $(V_C\text{-Mu})^+$ yields significant interactions between μ^+ and the lattice.

Laplace-DLTS has further revealed the exact activation energies for the different charge states of V_C and V_{Si}, along with small capture cross sections in the range of 10^{-15} cm^2 to 10^{-16} cm^2 for V_C [54] and 10^{-17} cm^2 to 10^{-15} cm^2 for V_{Si} [65].

This is in contrast to what we often read as a description of "shallow levels" as formed by dopants [20]. Here, higher concentrations are used (see discussion in the very beginning of this chapter) and, therefore, there is a higher probability of overlapping charges. The term "deep levels," on the other hand, is commonly used for levels with activation energies away from the two band edges, and, more importantly, with localized wave function (and, hence, small capture cross sections). Keeping this strong localization of electrons for both V_C and V_{Si} in mind, let us further assess also the available information on extrinsic electrically active defects.

A large variety of elements have been investigated for their impact on SiC and its bandgap. In Figure 6.16, all presently available information is collected in a more graphical manner. In this graph, the information is given for 4H-SiC; the results presented in Figure 6.15 and in the Tables 6.1–6.3, however, represent the collective amount of unambiguously confirmed impurity levels in the respective polytype, as available (4H, 6H, 15R, 3C).

For a very long time now, the alignment of transition-metal-induced traps in the bandgap of SiC has been discussed and is experimentally verified (see also Section 6.3). This alignment has initially been suggested in [85] for transition metals in III–V heterostructures. In addition, the reader shall also be reminded of one of the first theoretical attempts to assess the electronic properties of transition metals in SiC: The site preference for a variety of 3d-transition metals [86].

These early results have shown two aspects: a pronounced difference in the charge configuration of V_C and V_{Si} and, consequentially, a pronounced difference

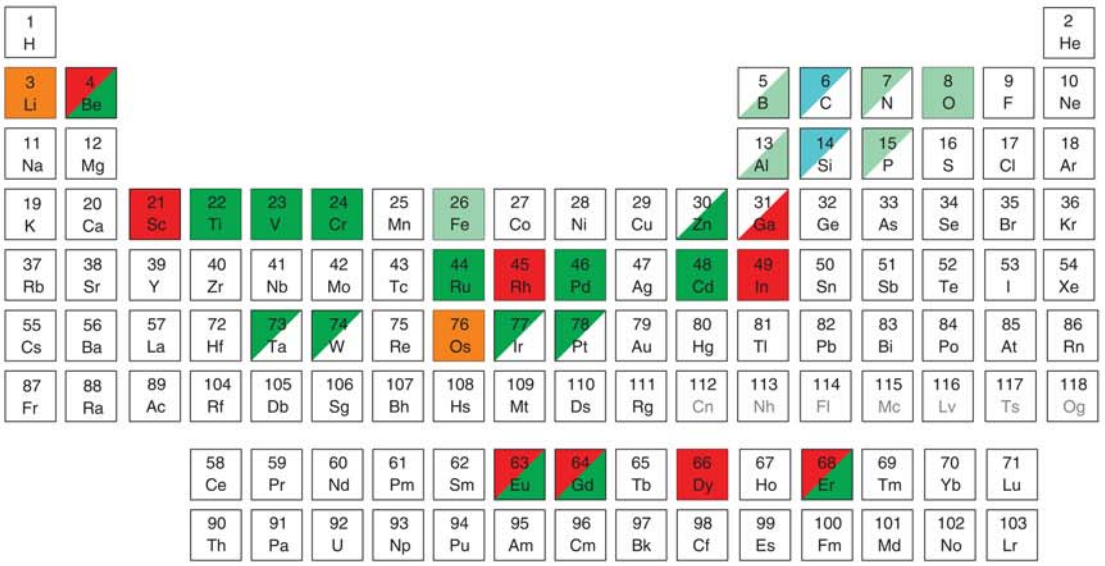


Figure 6.16 Depiction of the table of elements: elements marked green have unambiguously been assigned to electrically active defects in 4H-SiC; light green denotes a confirmed assignation using conventional DLTS (POSITIVE), full green an assignation obtained by chemically sensitive radiotracer DLTS (TRUE_POSITIVE). Marked in full red are the elements that have been investigated, but no trap level has been detected (TRUE_NEGATIVE). Orange are the elements that have been investigated, but the assignation may be influenced by recoil effects (potentially FALSE_NEGATIVE). Light blue are the intrinsic defects V_C and V_{Si}, which have been unambiguously identified using a combination of different methods (POSITIVE). In any case, upper triangles indicate traps in the upper half of the bandgap, denoting states measurable in n-type SiC; lower triangles indicate traps in the lower part of the bandgap, i.e. in p-type SiC.

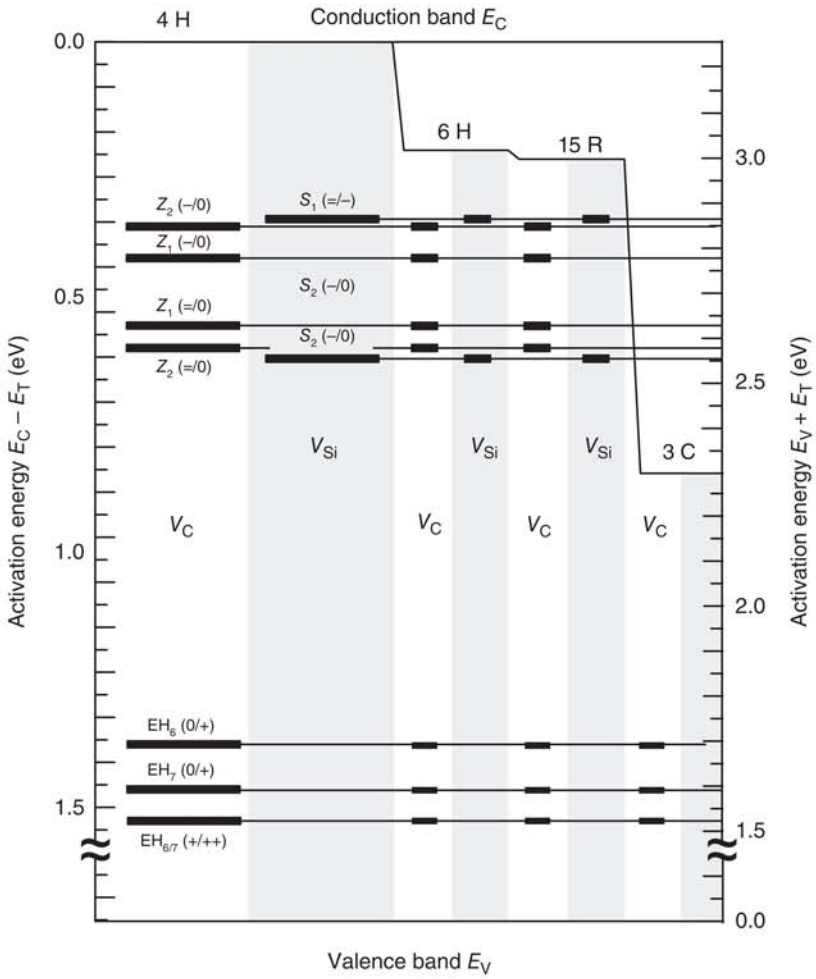


Figure 6.17 Suggested positions for V_C and V_{Si} in the 4H, 6H, 15R, and 3C polytype, assuming the validity of the assignment for 4H-SiC and their alignment according to [85].

in bonding of impurity 3*d* elements: "*… the TMs surrounded tetrahedrally by four Si atoms experience a large crystal field splitting while the tetrahedral C environment does not give rise to a significant crystal field splitting at all. It is only in the latter case that high-spin configurations are predicted.*" [86].

Let us now put the findings from this early study in context with our current discussion and recapitulate: The Rule of Langer and Heinrich [85] is fully confirmed and accepted for extrinsic defects exhibiting primarily rather small capture cross sections. The identification of the electronic signature for V_C (i.e. the correct assignment of the levels previously named $Z_{1/2}$ and $EH_{6/7}$) and V_{Si} (i.e. S_1 and S_2, respectively) allowed further characterization and verification of the local charge relaxation behavior and confirmed a similarly small capture cross section as for transition metals.

These considerations now allow us to make a very firm statement toward the alignment of the intrinsic defects, namely, V_C and V_{Si}, in different SiC polytypes, similarly to the ones of transition metals. This alignment has been suggested before for the DLTS level $EH_{6/7}$ but could not be further confirmed or assigned to either of the vacancy types [87].

Figure 6.17 shows the proposed alignment of the electrically active states of the two intrinsic defects considered in the context of this work.

The collected results are now concluded for their impact in applications. A focus on V_C concentration for tailoring charge carrier lifetime in power devices is, once more, confirmed to be crucial. For emerging application involving spin control, the focus can be on the V_{Si}, at least for 4H-SiC and up to temperatures slightly below room temperature. For integration of spintronics on 3C-SiC; however, the use of a transition metal impurity is required. Here, the focus should be on an element substituting for an Si atom (i.e. the site of the V_{Si}), as otherwise the formation of a high-spin configuration is unlikely.

And last but not least, for all applications, the position of the Fermi level for the respective operating point should be considered …

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7

Dislocations in 4H-SiC Substrates and Epilayers

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7.1 Introduction

Silicon carbide (SiC), chiefly the 4H polytype, is a wide bandgap semiconductor highly suited for electronic and optoelectronic devices operating under high temperature, high power, high frequency, and/or strong radiation conditions, where conventional semiconductor materials such as silicon, GaAs, and InP are considered to have reached their limits [1]. SiC-based devices require the production of high-quality thin films, which in turn require high-quality substrates. Commercial SiC wafers are obtained from bulk crystals predominantly grown by physical vapor transport (PVT, also called seeded modified Lely growth) [2], while homoepitaxial growth of SiC on these substrates is commonly achieved by chemical vapor deposition (CVD) directly from the gas phase [3–6]. The high-temperature chemical vapor deposition (HTCVD) process [7, 8] can also yield thicker films and higher growth rates while halide CVD has also received much attention due to the lower decomposition temperature of halide precursors [9]. Solution growth methods such as the top-seeded solution growth (TSSG) method [10] are also being developed for bulk growth of SiC.

During both bulk and epitaxial growth, management of the various growth parameters including thermal profile of the growth system and resultant thermal gradient stresses within the growing crystal are critical to control the nucleation and propagation of various defects. Crystalline imperfections, such as growth dislocations of screw character with closed-cores and hollow-cores (micropipes [MPs]), deformation-induced basal plane dislocations (BPDs), parasitic polytype inclusions, planar defects (stacking faults, microscopic twins and small angle boundaries), and hexagonal voids, affect the device performance to different extents [11–14], and the lowering of their densities is a primary goal of the SiC crystal growth community. Synchrotron white beam X-ray topography (SWBXT) and synchrotron monochromatic beam X-ray topography (SMBXT) [15] have played a

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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key role in revealing the detailed configurations of these defects and have been able to shed much light on their origins [16, 17], thereby enabling the development of strategies for their elimination.

7.2 Dislocations in Bulk 4H-SiC

7.2.1 Micropipes (MPs) and Closed-core Threading Screw Dislocations (TSDs)

Screw dislocations lying along the [0001] axis have Burgers vectors equal to nc with hollow cores becoming evident with $n \geq 2$ for 6H and SiC $n \geq 3$ for 4H SiC [18]. Using back-reflection geometry in SWBXT, both closed- and hollow-core (MPs) screw dislocations (Figure 7.1a) are revealed [19]. Possible mechanism for nucleation of MPs involves the incorporation of inclusions, which could be, for example, graphite particles, silicon droplets or even voids, into the crystal lattice [20–24]. Recent improvements in the growth process have effectively eliminated the nucleation of MPs in 4H-SiC, but Figure 7.1a TSDs are always present. Regarding the nucleation of screw dislocations with predominantly c-component Burgers vectors, the highly anisotropic hexagonal structure of 4H (or 6H) SiC may play a critical role. Normally, the relief of external stresses such as those occurring during crystal growth occurs by the process of deformation, i.e. nucleation and motion of dislocations. In 4H-SiC, the basal plane is the predominant deformation plane, and dislocations with Burgers vectors of type $1/3\langle 11\bar{2}0\rangle$ are involved to relieve stresses within the basal plane. Prismatic slip on the $\{1\bar{1}00\}$ planes also involves dislocations with the same Burgers vector type, i.e. $1/3\langle 11\bar{2}0\rangle$ and thus displacements are limited to the basal plane. Since no deformation-induced dislocations contribute to relief of stresses outside the basal plane, threading screw dislocations (TSDs) and threading mixed

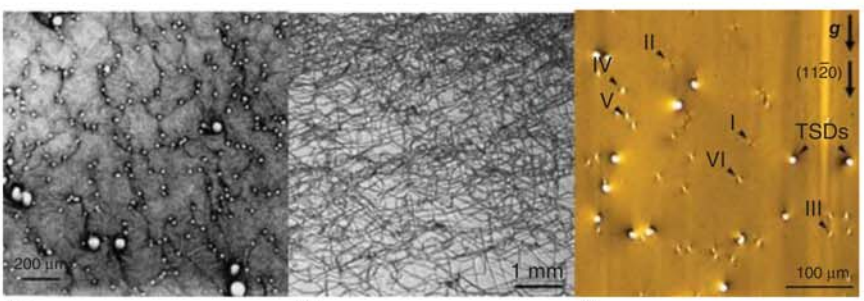


Figure 7.1 (a) Back-reflection X-ray topograph images of closed-core (smaller white spots) and hollow-core (large white spots) screw dislocations in a (0001) 6H SiC wafer; (b) transmission X-ray topograph of 4H-SiC substrate showing network of BPDs; (c) monochromatic beam X-ray topograph ($g = 11\bar{2}8$) showing the images of six types of TEDs in 4H-SiC; (I) $b = 1/3[\bar{1}2\bar{1}0]$; (II) $b = 1/3[\bar{2}110]$; (III) $b = 1/3[\bar{1}\bar{1}20]$; (IV) $b = 1/3[1\bar{2}10]$; (V) $b = 1/3[2\bar{1}\bar{1}0]$; (VI) $b = 1/3[11\bar{2}0]$.

dislocations (TMDs) that have Burgers vectors perpendicular to or at large angles to the basal plane provide the displacements to accommodate local high stress concentrations. Such stress concentrations while present around inclusions also exist at the seed–crystal interface thereby resulting in nucleation of TSD or TMD pairs.

7.2.2 Basal Plane Dislocations (BPDs)

BPDs are glissile dislocations with both line directions and Burgers vectors (i.e. $1/3\langle 11\bar{2}0\rangle$) in the basal plane (0001) (Figure 7.1b). Detailed Burgers vector analysis of these dislocations can be easily performed using the **g.b** and **g.b×l** criteria similar to TEM. Observation of the morphologies of the BPD loops clearly indicates that they are deformation induced and appear to have been nucleated both at the crystal edges and at the sites of MPs/screw dislocations [16].

7.2.3 Threading Edge Dislocations (TEDs)

In 4H-SiC, threading edge dislocations (TEDs) are dislocations with line directions roughly parallel to *c*-axis and Burgers vectors in basal plane, i.e $1/3\langle 11\bar{2}0\rangle$. TEDs are one of the major components of low-angle grain boundaries (LAGBs). The six different directions of the TED Burgers vector in 4H-SiC (Figure 7.1c) can be unambiguously identified by comparing their image features to their corresponding ray tracing simulated $(11\bar{2}8)$ grazing-incidence topograph images [25].

7.2.4 Interaction between BPDs and TEDs

7.2.4.1 Hopping Frank–Read Source of BPDs

Studies of the configurations and behavior of BPDs in wafers cut from PVT-grown SiC boules have enabled identification of the operation of single-ended Frank–Read sources which are interconnected on different basal planes [26]. Figure 7.2 shows an example of a final configuration of a BPD which has developed into a sequence of diamond-shaped loops on different basal planes connected by TED segments sufficiently long enough to reduce their mutual interaction forces. The dislocation has a Burgers vector of $1/3[11\bar{2}0]$ with the segments comprising the loops along $\langle 1\bar{1}00\rangle$ line directions.

A macrostep deflection of the surface outcrop of the TED onto the basal plane creates a segment of BPD (Figure 7.2b). If the BPD segment is in screw orientation, further advancement of the macrostep will replicate the BPD in the direction of step flow (7.2c). If the advancing macrostep encounters a step advancing in the opposite direction, for example, a spiral step from a screw dislocation, the dislocation will be re-deflected into the threading direction as shown in the schematic cross sections in Figure 7.2d. At a later stage of growth, if the outcrop of the re-deflected TED encounters another advancing macrostep, the whole process can be repeated (Figure 7.2e). As soon as the TED is deflected onto the basal plane, a single-ended Frank–Read (marked as no. 1) source will begin to operate (Figure 7.3a). The deflected BPD segments move away from screw orientation and is expected to

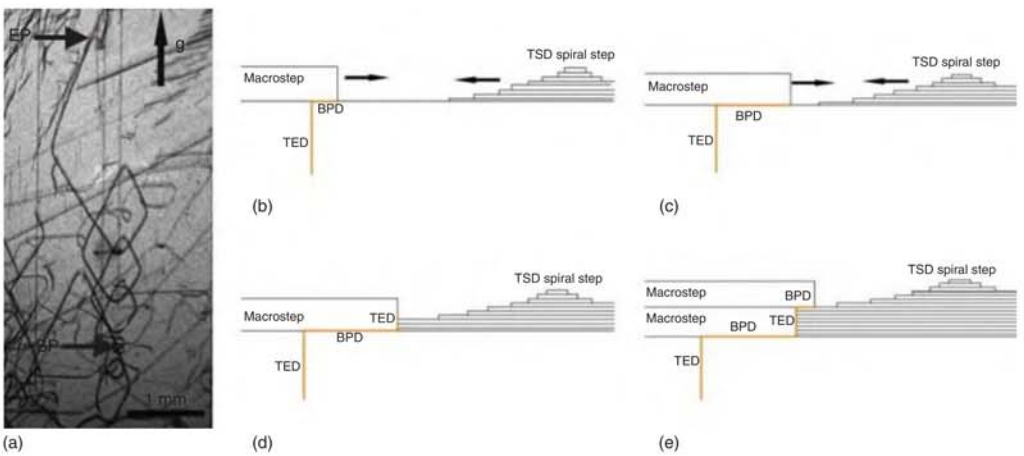


Figure 7.2 SWBXT transmission image ($g = 11\overline{2}0$) showing a diamond-shaped BPD loop (SP – starting point; EP – ending point). (b)–(e) Schematic cross-sectional view of the deflection of a TED onto the basal plane by a macrostep followed by re-deflection up into threading orientation through the encounter between macrostep and a TED spiral advancing in the opposite direction.

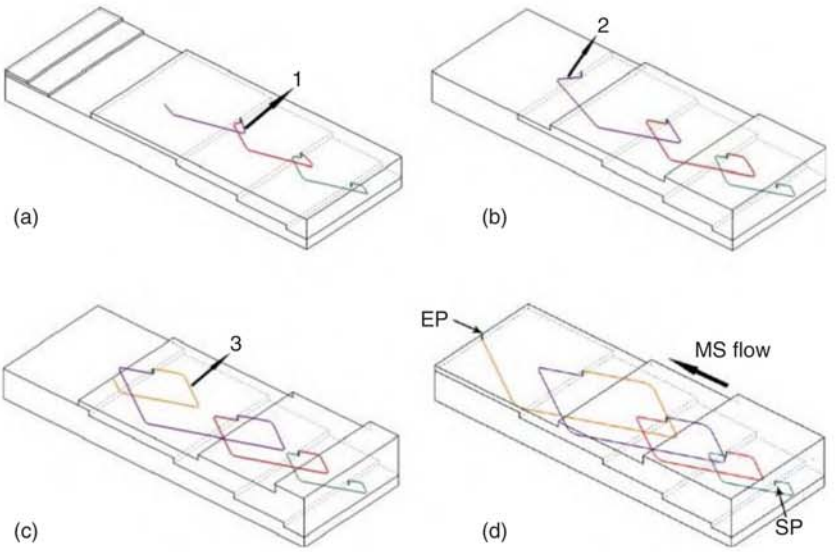


Figure 7.3 (a)–(c) Schematic of the formation of a single-ended Frank–Read source through the deflection of a TED into a BPD and back again. The TED segments act as pinning points for the BPD glide; (d) the final configuration of the loops produced by the Hopping Frank–Read source. "SP" indicates the starting point, and "EP" end point. Source: Wang et al. (2014). Characterization of Defects in SiC Substrates and Epilayers. ECS Transactions, 64(7), 145–152.

become more susceptible to conversion into a TED segment. When the BPD is re-deflected into threading orientation, a second single-ended source (marked as no. 2) will initiate at that point. As this new TED segment in deflected again onto the basal plane, a third single-ended source (marked as no. 3) will initiate (see Figure 7.3c). For these latter two sources to be able to operate independently the BPD segments on parallel basal planes must be separated by a distance large enough that their mutual repulsive forces can be overcome. If the distance is too small, the gliding BPDs will simply continue to draw out the dislocation dipole which will remain locked in place (Fig 7.3a). On the other hand, if the separation is large enough, the two BPD arms can effectively behave independently of each other as single-ended sources (Figure 7.3b). Thus, the resultant BPD configuration effectively behaves like a series of single-ended Frank–Read sources which "hop" from one slip plane to other parallel slip planes through a process of double deflection involving overgrowth by macrosteps followed by impingement of the overgrowing macrostep on a step moving in the opposite direction. This behavior is termed as a Hopping Frank–Read source mechanism.

7.2.5 Threading Mixed Dislocations (TMDs) in 4H-SiC

In addition to MPs and pure screw dislocations where the Burgers vectors are one to several times c, 4H-SiC crystals also contain threading dislocations with both c and a components [27, 28]. Figure 7.4a shows an SWBXT image ($g = 0004$) from

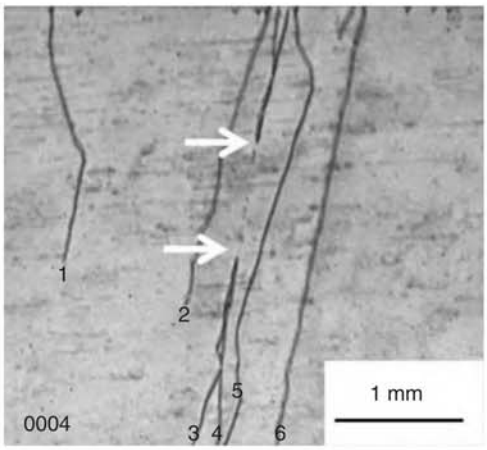


Figure 7.4 Transmission topograph ($g = 0004$) shows dislocation contrast from 1 to 6.

Table 7.1 **g·b** values for dislocations from 1 to 6 in Figure 7.9.

g·b g b	0004	$0\bar{1}10$	$1\bar{2}10$	$01\bar{1}1$	$0\bar{1}11$	$10\bar{1}5$
1&6: $1/3[1\bar{2}13]$, $c+a$	4	1	2	0	2	−5
3: $1/3[\bar{1}\bar{1}23]$, $c+a$	4	1	1	0	2	−5
4: $1/3[\bar{1}\bar{1}2\bar{3}]$, $-c+a$	-4	1	1	−2	0	5
2&5: $\langle 0001 \rangle$, TSD	4	0	0	1	1	−5
Arrow: $2/3[\bar{1}\bar{1}20]$, $2a$	0	2	2	−2	2	−2

an axial slice where segments of six threading dislocations labeled **1–6** are visible although dislocations **3** and **4** appear to have interacted such that parts of their length have apparently annihilated. By carrying out detailed contrast analysis on multiple reflections (see Table 7.1), the Burgers vectors of these dislocations are estimated.

The exact Burgers vectors are revealed through the interactions between the threading dislocations with *c*-component of Burgers vector. Two closed-core threading dislocations with opposite *c*-component experience a strong attractive force but the reaction is difficult via slip but can be achieved by interaction with non-equilibrium concentration of vacancies (i.e. climb). These reactions are summarized later.

7.2.5.1 Reaction Between Threading Dislocations with Burgers Vectors of $-c + a$ and c + a Wherein the Opposite *c*-Components Annihilate Leaving Behind the Two *a*-Components

In Figure 7.4, a segment of dislocation lines **3** and **4**, marked with arrows, appears to have annihilated and shows no contrast. As illustrated in Figure 7.5a, dislocation **3** and **4** have opposite sign *c*-components and these *c*-components annihilate while the two *a*-components are left behind. Figure 7.5b shows a section topograph superimposed onto a 0004 projection topograph. From the sense of the mutual shift between the bimodal image components, it can be seen that dislocation **3** and **4** have

right-handed and left-handed screw components, respectively, and thus annihilate when they meet.

7.2.5.2 Reaction Between Threading Dislocations with Burgers Vectors of $-c$ and $c + a$ Leaving Behind the a-Component

Figure 7.5d shows a reaction between $-c$ and $c + a$ dislocations. The $-c$ TSD annihilates with the opposite sign c-component of the $c + a$ dislocation leaving a single a-component behind (Figure 7.5d). TSD dislocation **7** is visible in Figure 7.5e and out of contrast in Figure 7.5f while dislocation **8** is visible in both images, which suggest that it has both c- and a-components. The annihilated segment, marked by arrows, is invisible in Figure 7.5e and visible in Figure 7.5f, which indicates that the annihilated segment has only an a-component of Burgers vector.

7.2.5.3 Reaction Between Opposite-sign Threading Screw Dislocations with Burgers Vectors c and $-c$

Figure 7.5g shows a typical helical morphology of a TSD and when two dislocations like this are close to each other, the interaction between TSDs with opposite signs of Burgers vectors will occur, as shown in Figure 7.5h where some segments annihilate leaving others in the form of trails of stranded loops comprising closed dislocation dipoles.

7.2.5.4 Nucleation of Opposite Pair of $c + a$ Dislocations and Their Deflection

Figure 7.6a shows a pair of $c + a$ dislocations nucleated from an inclusion. To satisfy Burgers vector conservation, these two dislocations originating from an isolated inclusion inside a perfect crystal region must have opposite sense of Burgers vector. This is evident from Figure 7.5b that shows a section topograph, which shows the sense of the mutual shift between the bimodal image components, it can be seen that dislocation **1** has right-handed screw component while dislocation **2** has left-handed which confirms that dislocations **1** and **2** have opposite c-components.

Overgrowth of an inclusion during step flow crystal growth creates a closure failure which is accommodated by the nucleation of the opposite sign pair of screw dislocations [29]. Similarly, when an inclusion is overgrown by growth steps on the growth face, dislocations of opposite sense are created to accommodate the misalignment that has magnitude equal to $c + a$. Two possible surface configurations at the growth front after the generation of the opposite sign pairs are shown Figure 7.6c. Two extra half-planes are associated with a-component of $c + a$ dislocations and the surface outcrop at the dislocation core is associated with c-component of the dislocations.

Occasionally, partial deflection of $c + a$ dislocation is observed, in which the a-component of $c + a$ dislocation deflects onto basal plane and c-component continues growing along the growth direction; as a result, $c + a$ dislocation diverges into a BPD with $\mathbf{b} = a$ and a TSD with $\mathbf{b} = c$, as shown in Figure 7.7. A pair of opposite sign $c + a$ dislocations described above propagates along growth direction, and later at some level, a-component of the dislocation on the left is deflected onto the basal plane and the c-component continues to propagate while the $c + a$ dislocation on

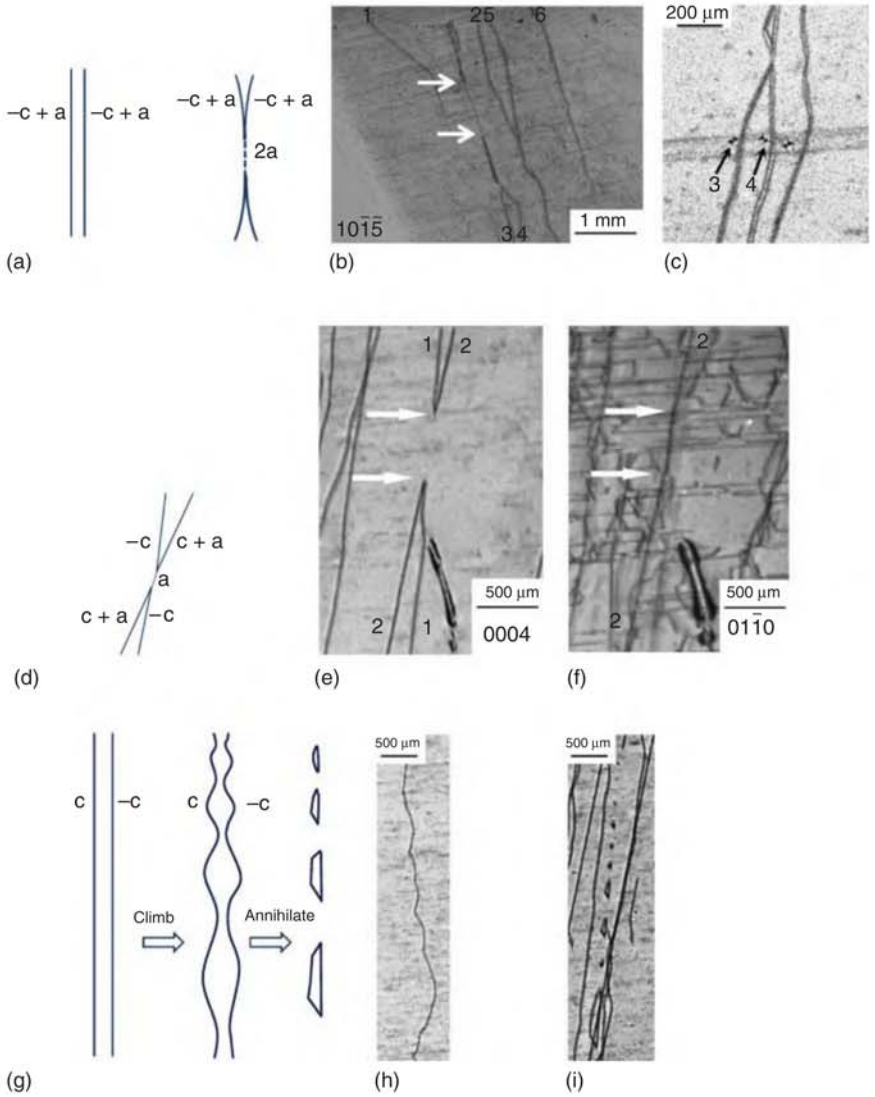


Figure 7.5 (a) Illustration of the reaction between $-c+a$ and $c+a$ dislocation; (b) overlapping 0004 section topograph on projection topograph shows opposite signs of dislocation **3** and **4**, since their screw arrangements are mirror images. (d) Illustration of the reaction between $-c$ and $a+c$ dislocation; (e) SWBXT image of 0004 reflection showing the annihilation of $-c$ and $c+a$ dislocation, named **7** and **8**, respectively; (f) $01\bar{1}0$ reflection showing the strong contrast of dislocation **8** as well as "the annihilation segment," and absence of dislocation **7**. (g) Illustration of the reaction between c and $-c$ dislocation; (h) SWBXT image of 0004 reflection showing curved slightly helical morphology of c dislocation; (i) 0004 reflection at different regions showing annihilation of c and $-c$ dislocation at some segments leaving others in the form of stranded loops comprising closed dislocation dipoles. Source: Wang et al. (2014). Characterization of Defects in SiC Substrates and Epilayers. ECS Transactions, 64(7), 145–152.

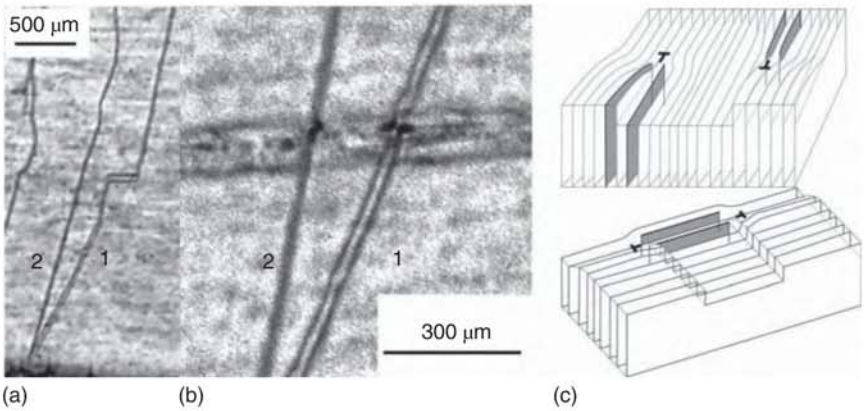


Figure 7.6 (a) SWBXT transmission image of 0004 reflection; (b) a section topograph superimposed on a projection topograph revealing the sense of the opposite sign dislocation pairs. (c) two possible configuration of the opposite sign $c + a$ dislocations being nucleated

the right is completely deflected onto the basal plane and later redirected back into the growth direction. The deflection process here is strongly related to the advancement of macrosteps.

7.2.5.5 Deflection of Threading $c + a$, c and Creation of Stacking Faults

Three types of stacking faults have been observed to date in 4H-SiC: Shockley faults, Frank faults and those which comprise some kind of combination of these two. Such faults can arise from the deflection of c-axis threading dislocations of Burgers vector **c** and **c** + **a** onto the basal plane [30, 31]. If the spiral step risers of such dislocations divide into $c/4$ and $3c/4$ increments, overgrowth can be facilitated by the simultaneous dragging of one of the Shockley partials associated with the core structure of the original dislocation by the overgrowing macrostep. This acts like an interfacial Shockley partial and adds the Shockley component to the $c/4$ Frank component of fault vector. Stacking faults vectors can be determined by X-ray topography by analyzing the contrast from stacking faults on multiple X-ray topographs which arises from the phase shift experienced by the X-ray wavefields as they cross the fault plane [32]. This phase shift has been computed to be equal to $\delta = (-2\pi g \cdot R)$, where g is the active reciprocal lattice vector for the reflection and R is the fault vector.

Formation of these faults can be understood by considering two processes. First is the overgrowth of TEDs onto the basal plane in the step flow direction and the second involves the overgrowth of dislocations of the type $c + a$ (i.e. both c and a components are anchored at the dislocation outcrop). This result in the deflection of extra half planes associated with "a" component to deflect onto basal plane, but in this case, the Shockley partial dislocations are separated by the step height of the "c" dislocation. The deflected dislocations under thermal shear stress glides creating large faults, with the leading partial faulting and trailing partial unfaulting the plane in case of TEDs and in case of $c + a$ dislocations the partials cannot move in tandem as they are separated by step height due to which depending on direction of force

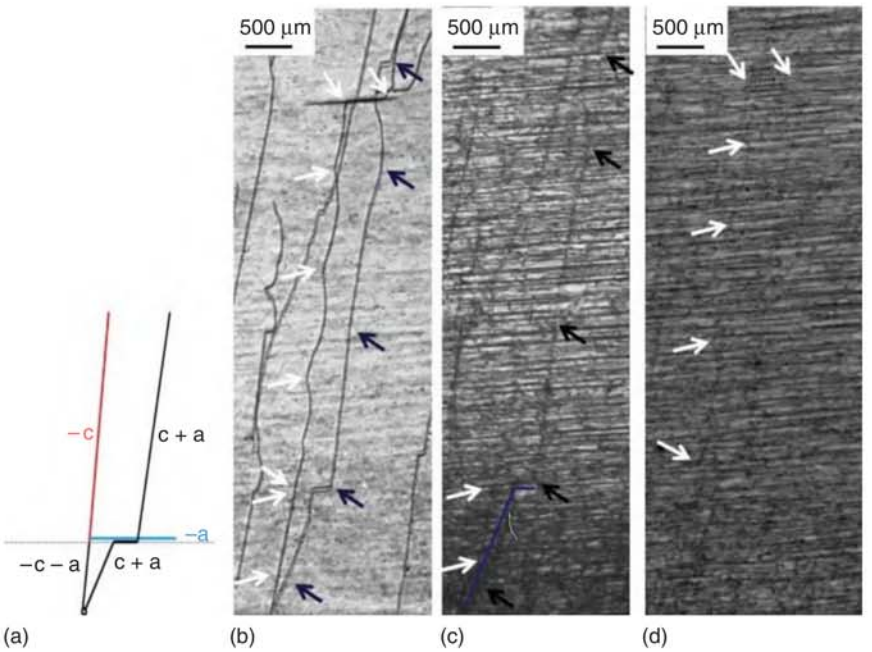


Figure 7.7 (a) Illustration of partial deflection of threading $c+a$ dislocations shown in (b)–(d); (b) 0004 reflection shows a pair of opposite-sign threading $c+a$ dislocations as well as a segment of pure screw dislocation; (c) $01\bar{1}0$ reflection shows contrast from the segments of $-c-$a dislocation marked by white arrows and $c+a$ dislocations marked by black arrows; (d) $01\bar{1}1$ reflecion shows contrast from the segment of pure screw dislocation marked by white arrows.

one partial glides creating faults while the other partial gets locked. Based on these two models, four fault vectors have been determined described as follows:

Type I: Frank Fault: Frank faults are "in-grown" stacking faults and result from the overgrowth of *c*-axis screw dislocations whose surface growth spiral steps were separated into *c*/2 increments. Figure 7.8a shows SWBXT image in transmission geometry of such a fault. Detailed analysis of the contrast from different reflections shows the fault vector is $\frac{1}{2}[0001]$.

Type II: Shockley faults: Figure 7.8c is a SWBXT image recorded from a section of a $n+$ 4H-SiC crystal showing stacking fault configurations which has one straight edge corresponding to the sessile partial and the other being curved corresponding to the glissile partial. In this case the step has an integral number of unit cells high, the resultant expanding fault will be a Shockley fault (since the out-of- plane component is *nc*, where n is an integer). Detailed analysis of the fault contrast revealed the fault vector to be $1/3[01\bar{1}0]$ which corresponds to a Shockley fault. Figure 7.8d is an illustration showing the integral number of step height, where the glissile partial lying below the step has created faults while the sessile partial at the top gets locked.

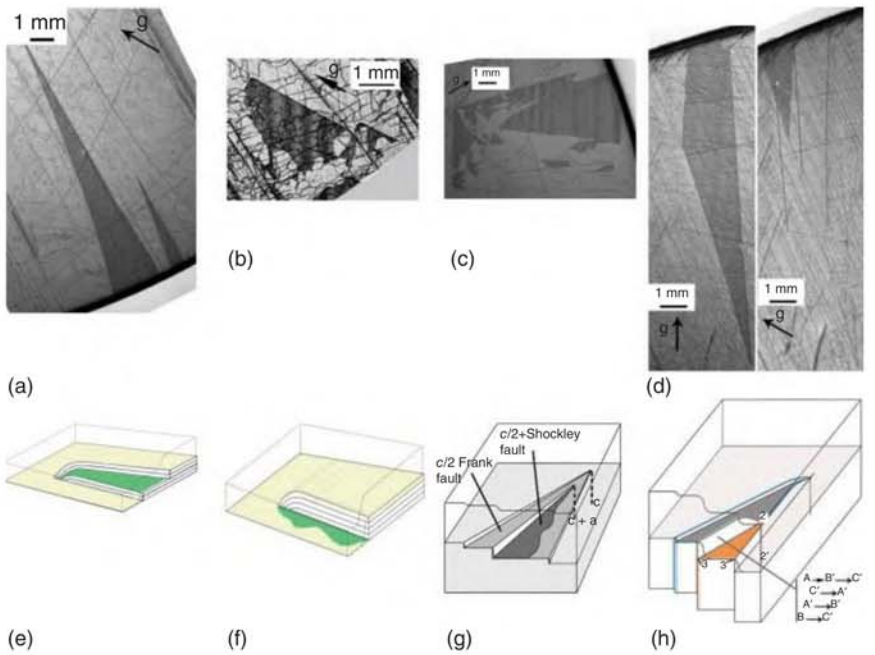


Figure 7.8 Transmission SWBXT images from 4H-SiC crystals showing stacking faults with fault vector: (a) $R = 1/2[0001]$ (Frank fault); (b) $R = 1/3[1\bar{1}00]$ (Type I Shockley fault); (c) $R = 1/6[20\bar{2}3]$ vector ($S + c/2$); (d) $R = 1/12[\bar{4}043]$ (i) and $R = 1/12[\bar{4}403]$ (ii) (vector $S + c/4$). Illustration of the stacking faults: (e) Frank-type stacking fault resulting from the overgrowth of a c-axis screw dislocation which has separated into two $c/2$ step heights. The area between the two demisteps corresponds to the Frank fault; (f) Type I Shockley fault vector showing integral number of step height with the glissile partial lying below the step and the sessile at the top which is locked; (g) Overgrowth of c dislocation and formation of the $c/2$ Frank-type fault within which a $c + a$ dislocation with one sessile Shockley partial and one glissile Shockley partial converts some part of the fault to $c/2$ plus a Shockley type; (h) overgrowth of $c + a$ dislocation with a c-height step converting it into a Frank dislocation plus two Shockleys with one sessile and the other glissile. Overgrowth of $c + a$ dislocation 11′ with $c/4$ and $3c/4$-height steps which has second 22′ with c-height spiral step protruding onto the terrace between these two step risers. Stacking sequences are indicated, the "interfacial Shockley" converts A layer into B', allowing overgrowth by the A′ layer at the bottom of the macrostep. Following overgrowth the Shockley associated with the deflected 22′ dislocation located at 23 glides under stress until it reaches the edge of the step 23′ creating the fault of type A shown in (d). Source: Wang et al. (2014). Characterization of Defects in SiC Substrates and Epilayers. ECS Transactions, 64(7), 145–152.

Type III: Combination of Shockley and Frank fault with fault vector $S + c/2$: These faults are a combination of Shockley and Frank faults resulting from the overgrowth of c-axis screw dislocations whose spiral steps have divided into two $c/2$-high demisteps and which has several $c + a$ dislocations with c-height spiral step risers protruding onto the terrace between the two demisteps. Figure 7.8e shows a SWBXT image of stacking faults in a 76 mm wafer. Overgrowth of c-axis screw dislocation and $c + a$ dislocations which has protruded the terrace created

by two demisteps results in both $c/2$ Frank fault and Shockley fault associated with $c + a$ to lie on the same basal plane.

Type IV: Combination of Shockley plus a Frank fault with Fault vector $S + c/4$: Type IV is also a combination of Shockley and a Frank fault but of the type $S + c/4$, where the c-axis screw dislocation has divided itself into $c/4$ and $3c/4$ step heights. Such faults can arise from the deflection of c-axis threading dislocations of Burgers vector $c + a$ onto the basal plane. If the spiral step risers of such dislocations divide into $c/4$ and $3c/4$ increments, overgrowth can be facilitated by the simultaneous dragging of one of the Shockley partials associated with the core structure of the original dislocation by the overgrowing macrostep. This acts like an interfacial Shockley partial and adds the Shockley component to the $c/4$ Frank component of fault vector. Figure 7.8g shows a SWBXT image taken in transmission geometry showing the area marked C is a fault with $R = 1/12[44\bar{6}03]$ which is a combination of Shockley and c/4 Frank fault and similarly area marked D in 7.8g corresponds to $R = 1/12[\bar{4}043]$ which is due to a second $\mathbf{c} + \mathbf{a}$ dislocation protruding the terrace. Such deflection process generally leads to exit of the threading dislocations through the crystal sidewalls and provide a mechanism by which the density of threading dislocations in the boules can be lowered.

7.2.6 Prismatic Slip during PVT growth 4H-SiC Boules

Prismatic dislocations are dislocations with Burgers vector $1/3\langle 11\bar{2}0\rangle$, generated and gliding on the $\{1010\}$ planes. They are mostly generated from the same sources that BPDs are generated from, such as crystal edge, MPs, etc. Figure 7.9a shows a prismatic slip band (marked with red arrow) nucleated from a MP. In addition, the gliding of TEDs on the prismatic planes can generate prismatic dislocation half loops as well. Examples of TEDs gliding on prismatic planes are shown in Figure 7.9b.

6″ 4H-SiC commercial wafers often reveal an inhomogeneous distribution of prismatic slip with only two sets of prismatic slip systems activated in each of the 12 regions around the periphery of the wafer as shown in the enlarged X-ray

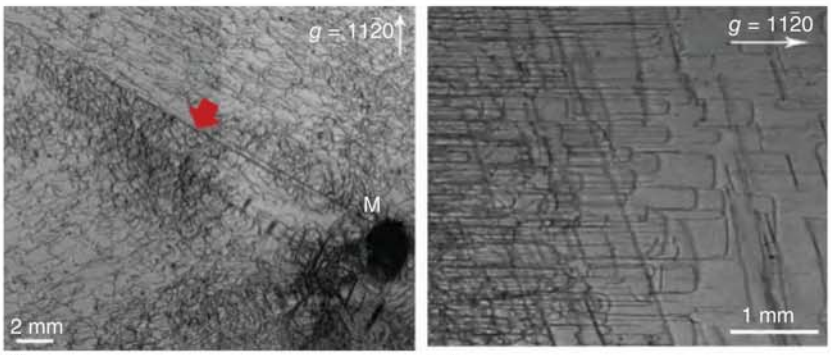


Figure 7.9 SWBXT images recorded from 4H-SiC samples showing (a) a prismatic slip band emanating from a MP in a commercial wafer and (b) the gliding of TEDs on prismatic plane generating a lot of prismatic dislocation half loops (this image is recorded from an axially-cut sample).

topographs in Figure 7.10 [33]. Such non-uniformity clearly indicates that the resolved shear stresses caused by radial temperature gradients that induced the dislocation nucleation in different prismatic slip systems were also distributed non-uniformly. By thermal modeling of the temperature distribution in the boule during PVT growth, the radial temperature gradient and resultant thermal stresses was determined at any location in the crystal boule. The corresponding resolved shear stress on each prismatic plane was calculated and the distribution plotted. The regions where the resolved shear stress exceeds the critical resolved shear stress are determined, and predicted distribution of prismatic dislocations for the three different slip systems is shown in Figure 7.10. Clearly, the predicted distribution is in excellent agreement with the observed distribution on the SWBXT topographs. Clearly, thermal stresses induced by radial temperature difference play a key role in the activation of prismatic slip in 4H-SiC crystals grown by PVT.

7.2.7 Relationship Between Local Basal Plane Bending and Basal Plane Dislocations in PVT-grown 4H-SiC Substrate Wafers

During PVT growth of 4H-SiC boule, internal stresses due to non-uniformity of temperature field results in basal plane bending that is accommodated by the inhomogeneous distribution of BPDs during cool down and persists in wafers sliced from the boule. Nature of basal plane bending measured by high-resolution X-ray diffraction (HRXRD) was compared with net BPD distribution across the whole diameter range of different wafers [34]. On synchrotron monochromatic beam X-ray topographs recorded in grazing incidence geometry, ray tracing principle denotes that black contrast BPD is created when diffracted X-ray beams converge from concave-shaped basal plane (extra half plane of edge dislocation facing way from surface), while white contrast BPD is created when diffracted X-ray beams diverge from a convex-shaped basal plane (extra half plane facing toward the surface). Thus, the net BPD distribution can be indicative of nature of basal plane bending, i.e. if black contrast BPDs are predominant, basal plane is bent in a concave manner, if white contrast BPDs are predominant, basal plane is bent in a convex manner. Figure 7.11b,d shows results of such BPD distribution measurement along the $[11\bar{2}0]$ and $[1\bar{1}00]$ for a 6″ 4H-SiC wafer, respectively. Comparison of the net BPD variation with the peak shift on HRXRD measurements shows good agreement qualitatively (Figure 7.11a,c). To quantitatively estimate the basal-plane tilt angle, from the dislocation measurement, the following equation can be applied [35]:

$$\frac{\delta\phi}{\delta x} = nb \tag{7.1}$$

where n is the net BPD density on the plane perpendicular to the basal plane, b is the Burgers vector, $\delta\theta$ is the total peak shift in an interval δx. Calculated values matches well with experimentally determined values from HRXRD [34].

7.2.8 Investigation of Dislocation Behavior at the Early Stage of PVT-grown 4H-SiC Crystals

The behavior of defects during the early stages of PVT growth in large diameter (6-in.) 4H-SiC crystals was investigated, especially nucleation and multiplication that form the basis of the overall dislocation distribution during subsequent growth

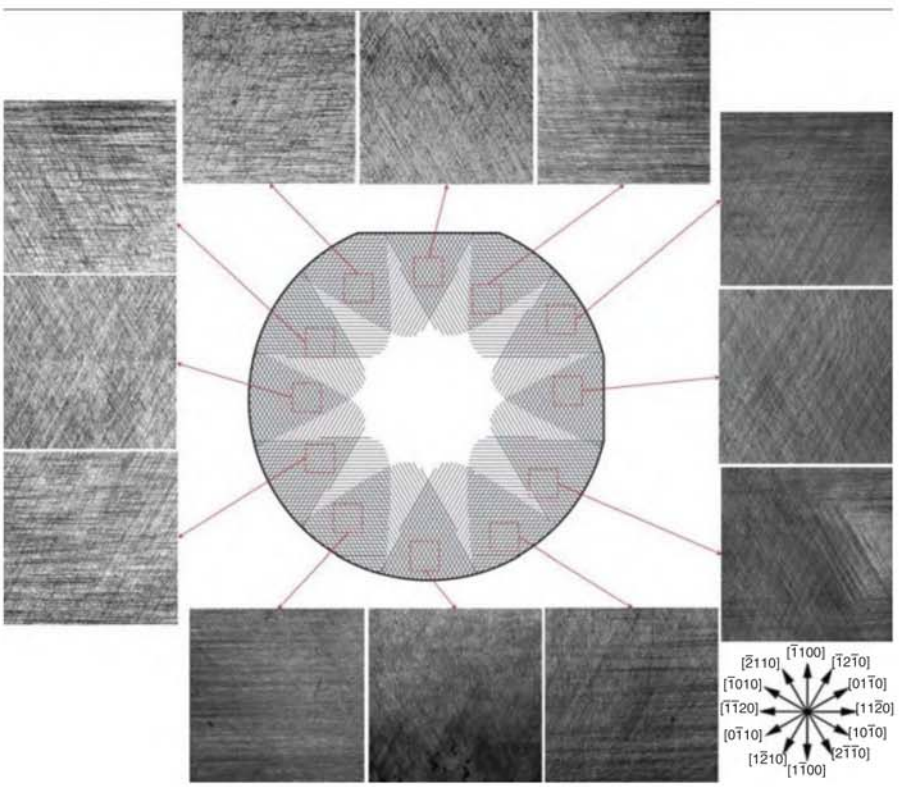


Figure 7.10 Correlation of wafer map (middle) showing the predicted distribution of prismatic dislocations for the three different slip systems with SWBXT images from the corresponding areas of the 150 mm 4H-SiC wafer showing excellent agreement. Source: Based on Guo et al. [33].

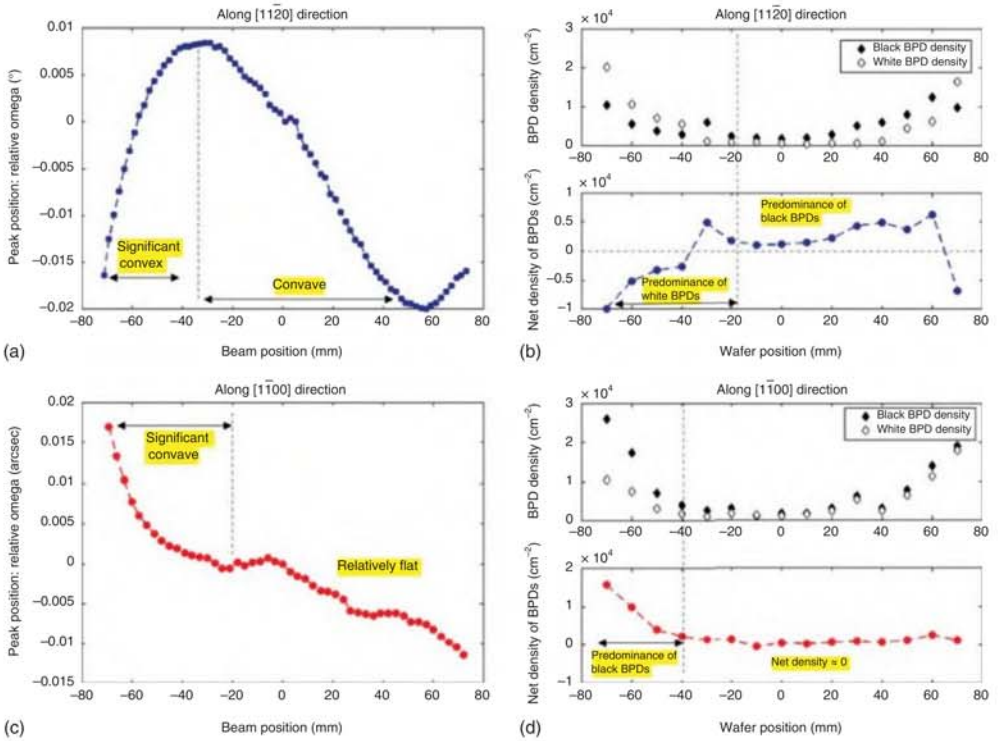


Figure 7.11 (a, c) X-ray rocking curve peak position as a function of the beam position across the diameter of 6 in. 4H-SiC crystal (wafer#1). Scan direction is along [11$\bar{2}$0] (a) and [1$\bar{1}$00] (c), respectively. (b, d) Results from black/white contrast BPD density analysis along [11$\bar{2}$0] (b) and [1$\bar{1}$00] (d) directions. Source: Based on Guo et al. [33].

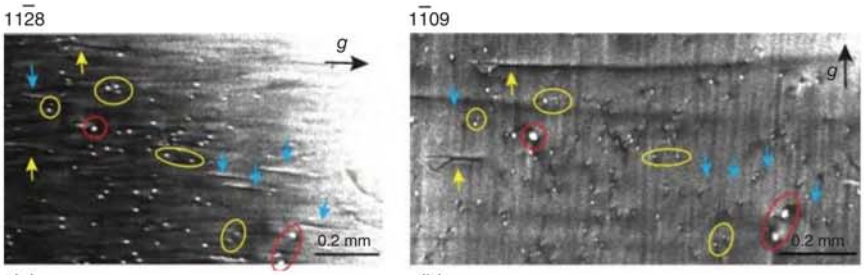


Figure 7.12 Grazing incidence X-ray topographs recorded from the same area of early grown 4H-SiC wafer in different diffraction vectors (a) $g = 11\bar{2}8$, (b) $g = 1\bar{1}09$. Blue arrows indicate straight BPD segments showing contrast in (a) but out of contrast in (b) proving these are screw-oriented BPDs.

of the full boule [36]. Studies from initial grown seeded layers with thickness of several hundred microns by synchrotron X-ray topography reveals the deflection of TEDs and TMDs with same or opposite sign pairs nucleated from the seed with unique configurations as shown in Figures 7.12–7.14. Configurations observed include the deflection of TEDs into screw-type BPDs (Figures 7.12), deflection of pairs of TEDs with same or opposite sign of Burgers vector by macrosteps followed by glide of resultant BPDs (Figure 7.13) and the deflection of TMDs followed by separation of the **a** component (Figure 7.14).

7.3 Dislocations in Homoepitaxial 4H-SiC

7.3.1 Conversion of BPDs into TEDs

During homoepitaxial growth on 4H-SiC substrates, BPDs intersecting the surface are replicated into the epilayer and are susceptible to recombination enhanced dislocation glide (REDG) during device operation (see Section 7.3.2). However, by conversion of BPDs to TEDs, this can be prevented. One way to facilitate this is by engineering the substrate surface prior to CVD growth, i.e. defect preferential etching. Etch pits produced at BPD outcrops can facilitate lateral growth over step flow growth within the pits resulting in TED conversion [37]. See Figure 7.15 for schematic of this conversion and Figure 7.16 for examples of this observed in 4H-SiC crystals by monochromatic X-ray topography.

7.3.2 Susceptibility of Basal Plane Dislocations to the Recombination-Enhanced Dislocation Glide in 4H Silicon Carbide

Dissociation of BPDs into mobile silicon-core (Si-core) partial dislocations and subsequent expansion of Shockley stacking faults (SFs) associated with advancement of these partial dislocations under forward bias causes forward voltage drop

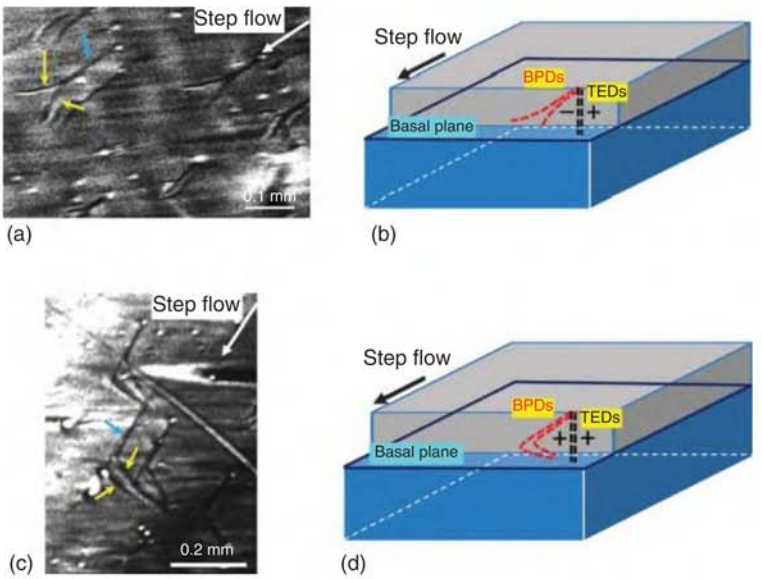


Figure 7.13 Dislocations with unique shapes are observed in grazing incidence X-ray topograph ($g = 11\bar{2}8$). (a, c) Stationary segments of the dislocation marked with blue arrows are along the step flow direction. Dislocation segments marked with yellow arrows refer to two gliding segments, which are separated parts of opposite sign deflected TEDs gliding toward opposite directions in (a), while two segments in (c) are associated with two deflected TED segments with same sign of Burgers vector. Formation mechanism is illustrated in (b) and (d), respectively. Source: Based on Guo et al. [33].

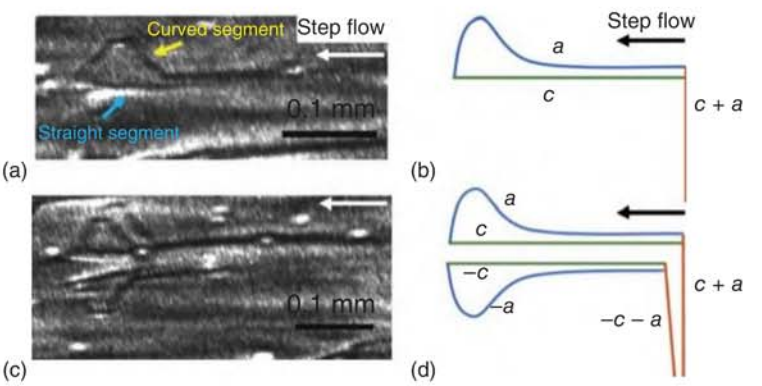


Figure 7.14 (a, c) Grazing incidence X-ray topographs of one or a pair of deflected TMDs with Burgers vector of $c + a$ in $11\bar{2}8$ reflection. Straight segment corresponds to c component while gliding segment corresponds to a component. (a) Deflection of one single TMD. (c) Deflection of a pair of TMDs with opposite sign Burgers vectors. (b, d) Illustration showing the deflection process for single or oppoiste sign pair of TMDs. Source: Based on Guo et al. [33].

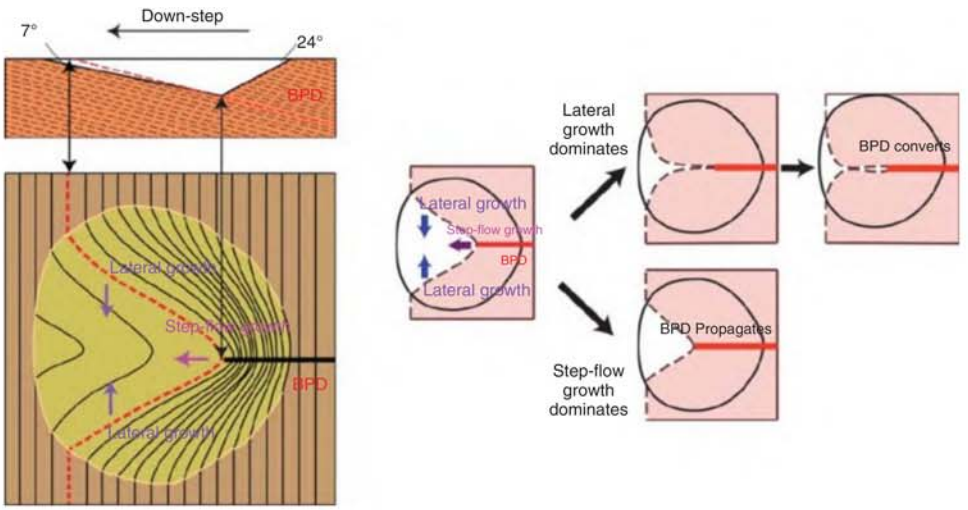


Figure 7.15 (a) Cross section of the BPD etch pit along the line bisecting the sector-shaped plane. The parallel dotted lines illustrate the basal planes. Schematic of steps in and around the pit; (b) schematics of the basal plane in which the BPD lies; evolution of the basal plane during epitaxy if lateral growth dominates, and evolution of the basal plane during epitaxy if step-flow growth dominates. Source: Based on Zhang and Sudarshan [37].

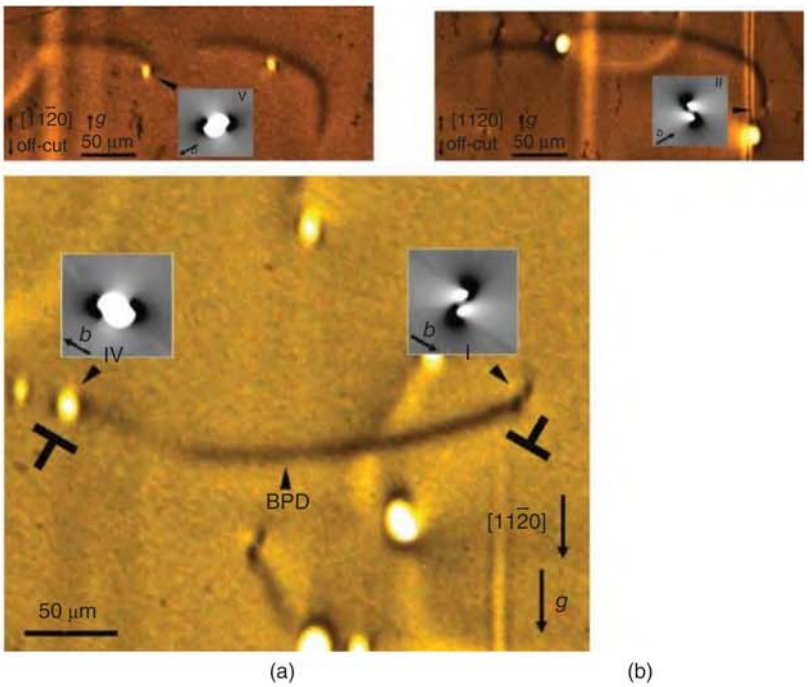


Figure 7.16 SMBXT images showing the conversion of BPDs to TEDs. Burgers vectors of TEDs are determined by comparison to simulated contrast from ray tracing simulations.

and reduced lifetime of silicon carbide (SiC) based bipolar devices [14]. Such expansion of basal SFs is activated by the electron–hole REDG process [38–40]. Through detailed X-ray topography analysis of a dislocation configuration formed after stacking fault expansion under forward bias, the susceptibility of BPDs to REDG is shown to be determined by the counterclockwise angle θ from the line direction to its Burgers vector (Figure 7.11a). Figures 7.11b–f shows the X-ray topographs and schematic configuration (g) after the advancement of the mobile partial. During the advancement of the partial, it interacted with a few TSDs, and the final configuration obtained is shown in Figure 7.11g. The Burgers vector $\boldsymbol{b}$ of the original BPD is determined to be $1/3(\bar{1}\,\bar{1}20)$. Thus, the original BPD is screw oriented ($\theta = 0°$), and it is dissociated into a C-core and a Si-core partials. The BPDs with $30° < \theta < 150°$ are most BPDs detrimental, as both partials will advance under forward bias. If $-30° < \theta < 30°$ or $150° < \theta < 210°$, only one partial advances. Both partials are immobile if $210° < \theta < 330°$ [41] (Figure 7.17).

In summary, the susceptibility of the BPDs to REDG process is determined by the counterclockwise angle θ from the line direction to its Burgers vector. The BPDs with $30° < \theta < 150°$ are most detrimental, as both partials will advance under forward bias. If $-30° < \theta < 30°$ or $150° < \theta < 210°$, only one partial advances. Both partials are immobile if $210° < \theta < 330°$.

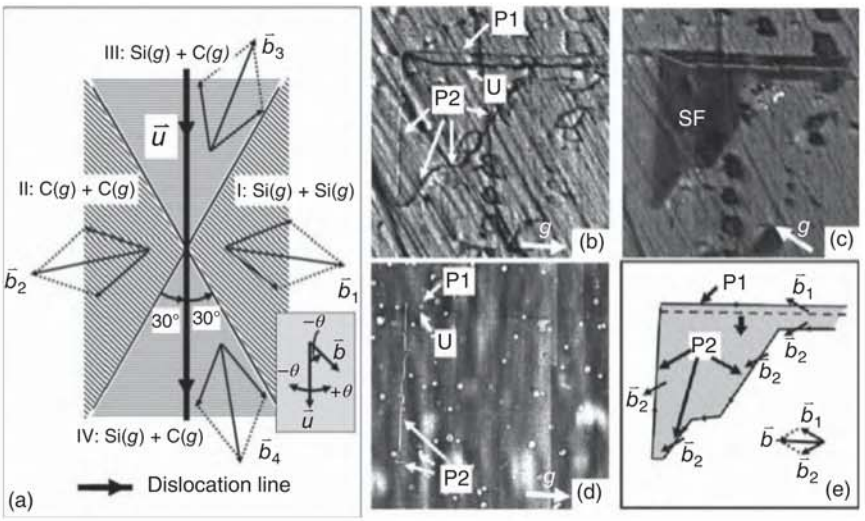


Figure 7.17 Schematics showing Shockley partial dislocations of different core structures dissociated from a perfect BPD. Four regions are defined, according to the direction of Burgers vector with respect to the line direction of the dislocation, assuming Si-face is facing up; Region I: $30° < \theta < 150°$, the BPD is dissociated into two Si-core partials; Region II: $210° < \theta < 330°$, the BPD is dissociated into two C-core partials; Region III: $150° < \theta < 210°$, one Si-core and one C-core. Region IV: $-30° < \theta < 30°$, one Si-core and one C-core; θ is defined in the inset of (a). REDG activated SF after forward bias from a screw-oriented BPD. (a) $(11\bar{2}0)$ transmission topograph showing the partials (P1 and P2) bounding the SF. The SF area is out of contrast since $\boldsymbol{g}\cdot\boldsymbol{R}$ is equal to an integer. Source: Zhang et al. [43]; (b) $(\bar{1}010)$ transmission topograph showing the SF; (c) P2 is out of contrast in $(2\bar{1}\bar{1}0)$ transmission topograph, indicating its Burgers vector of $1/3(0\bar{1}10)$; (d) P1 is out of contrast in $(1\bar{2}10)$ transmission topograph, indicating its Burgers vector of $1/3(\bar{1}010)$; (e) (0008) back-reflection topograph. The sign of P1 and P2 can be determined; (f) schematics showing the SF configuration. The SF is obtained via expansion of Si-core partial toward the bottom edge of the view (see the dashed line) and interaction with TSDs. The Burgers vector of each partial segment is labeled; the Burgers vector $\boldsymbol{b}$ of the original BPD can be obtained and it is screw-oriented. Source: Modified from Chen et al. [41].

7.3.3 Nucleation of TEDs, BPDs, and TSDs at Substrate Surface Damage

Subsurface damage associated with surface scratches on the substrate, residual from polishing act as dislocation nucleation sites during epitaxial growth. X-ray topography and chemical etching studies suggest that the scratches on the substrate surface act as dislocation nucleation centers during the growth. TED-TED pairs, TED-BPD pairs, TSD-TSD pairs, and Carrot defects are generated at scratches [42]. It is observed that the orientation of the scratch with respect to the off-cut direction exerts influence over the nucleation process. When scratches are parallel to the off-cut direction (Figure 7.18a,b), they manifested themselves as a single, dense row of TEDs. For scratches inclined to the off-cut direction (see Figure 7.18c–f), in addition to a single, dense row of TEDs, linear features verified as BPDs are

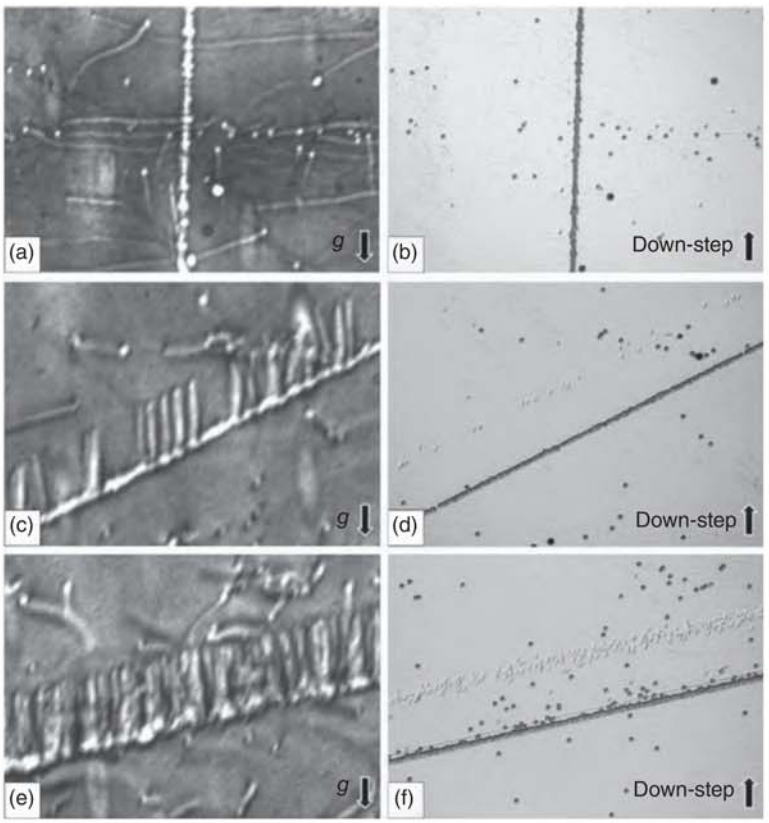


Figure 7.18 Synchrotron X-ray topographs ((a), (c), and (e)) and corresponding etch pit patterns ((b), (d) and (f)) recorded from epilayers grown on a scratched substrate surface. Panels (a) and (b) show a scratch parallel to the off-cut direction while panels (c)–(f) show scratches inclined to the off-cut direction.

observed. The density of the BPDs associated with the scratch increases with the angle between the scratch direction and off-cut direction.

TSDs can also be nucleated along substrate surface scratches as seen in the case of two scratches shown in Figure 7.19a,b. On the topographs, both scratches have linear features attached to them which project along the off-cut direction. X-ray topography reveals the lower one as a single white band similar to the cases discussed above. Compared with the etch pit pattern, it is clear that only TEDs and BPDs nucleated along it. But the upper one manifested itself on the topographs as a single but wider white band of contrast. The corresponding etch pit pattern confirmed that some other dislocations whose pits are bigger and deeper than TED etch pits were also nucleated along the scratch. Figure 7.19c shows an enlarged area, and it is observed that these dislocations appear as large hexagonal pits which correspond to elementary TSDs.

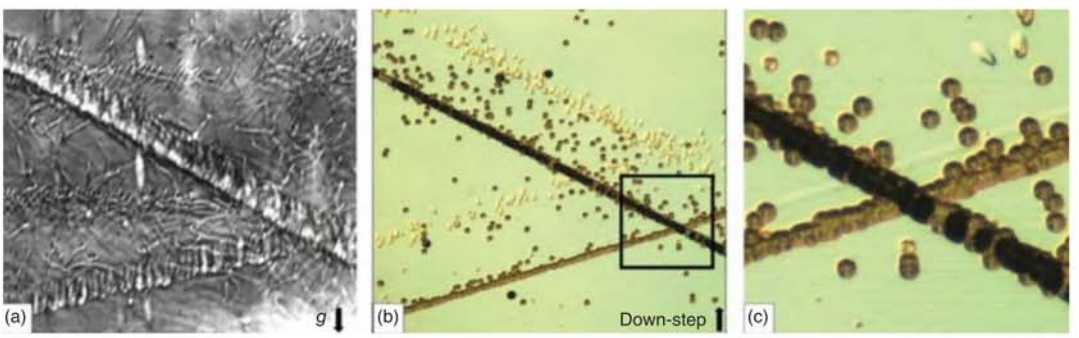


Figure 7.19 (a) SMBXT image recorded from an epilayer grown showing defects nucleated at two residual scratches on the substrate surface; (b) corresponding etch pit pattern; (c) enlargement of the framed region in (b).

7.3.4 Nucleation Mechanism of Dislocation Half-Loop Arrays in 4H-SiC Homo-Epitaxial Layers

BPDs in the 4H-SiC homepitaxial layers largely result from the replication, during growth, of BPDs which intersect the surface of the off-cut SiC substrates. BPDs which intersect the surface in screw orientation are observed to nucleate half loop arrays. By recording the behavior of a half-loop arrary (HLA) from a Si-face epilayer using ultra violet photoluminescence (UVPL) imaging, a model has been developed to explain the formation of HLAs [43]. Figure 7.20a shows a screw-type BPD with Burgers vector $1/3[11\bar{2}0]$ intersecting the surface of the substrate which is expected to be replicated during epitaxy in contrast to those with significant edge components which are likely to be converted into TEDs. As soon as the epilayer exceeds critical thickness, as per the predictions of Matthews and Blakeslee [44], the threading segment of the screw-oriented BPD will be forced to glide sideways leaving a trailing interfacial segment in its wake at or near the substrate/epilayer interface. During this glide process, the mobile threading segment adopts more edge character near the growth surface (see Figure 7.20b) rendering it susceptible to conversion to a TED during continued growth. The sessile TED segment pins the surface intersection of the mobile BPD segment. During further growth, the TED segment is replicated while the mobile

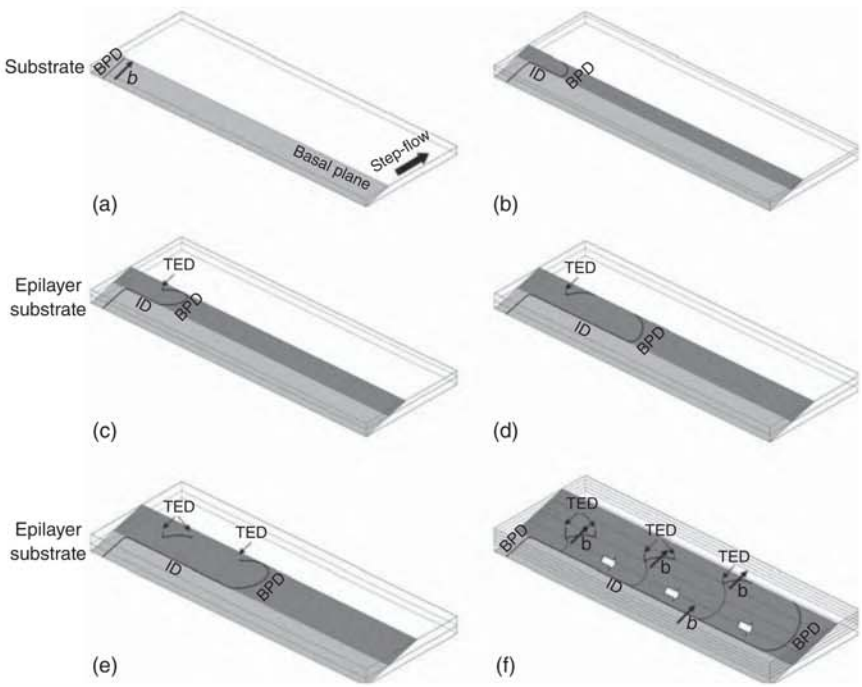


Figure 7.20 Schematic diagram showing the formation mechanism of a HLA. (a)–(e) sequential stages in the process; (f) summary of process. The lighter shaded planes in (a)–(f) indicate the basal plane on which the BPD lies in the substrate, while the darker one lies in the epilayer. See text for details of mechanism. Source: Zhang et al. [43].

basal segment of dislocation pivots about the pinning point as shown in Figure 7.20c. At this juncture, part of the mobile BPD segment can escape through the epilayer surface (creating a surface step of magnitude equal to the Burgers vector), as shown in Figure 7.20d leaving two further BPD surface intersections which, since they are not in screw orientation, are susceptible to conversion to TEDs. Upon conversion, one of these TEDs is connected via a short BPD segment to the TED segment created in Figure 7.20b, thus creating a half loop comprising two TEDs and a connecting BPD. The other TED again acts as a pinning point for the still mobile segment of threading BPD, as shown in Figure 7.20e, as the process repeats during continued growth as the TED segments further replicate and the threading BPD segment continues to glide. The net result of this process is an array of half loops with short, large edge component BPD segments, all deposited on the exact same basal plane. The direction of the array is nearly perpendicular to the off-cut direction as summarized in Figure 7.20f. The value of this angle depends on the competition between the growth rate and the rate of sideways glide of the threading BPD segment.

In addition to the above mechanism, HLAs are also observed to be generated from epilayer surface-nucleated half-loops of BPD, BPD half-loops generated from 3C inclusions in the epilayer, and from BPD half loops emanating from substrate/epilayer interface scratches as shown in Figure 7.21 [45].

7.3.5 V- and Y-shaped Frank-type Stacking Faults

Grazing incidence synchrotron white beam X-ray topographs showing V- and Y-shaped features (Figure 7.22) are revealed to be ¼[0001] Frank-type stacking faults [46]. Geometric analysis of the size and shape of these faults indicates that they are fully contained within the epilayer and nucleated at the substrate/epilayer interface. Detailed analysis shows that the positions of the V shape stacking faults match with the positions of *c*-axis threading dislocations with Burgers vectors of c or $c + a$ in the substrate and thus appear to result from the deflection of these dislocations during epilayer growth. Similarly, the Y-shaped defects match well with the substrate surface intersections of *c*-axis threading dislocations with Burgers vectors of $\mathbf{c}$ or $\mathbf{c} + \mathbf{a}$ in the substrate which were deflected onto the basal plane during substrate growth. For the V-shaped defects, this is based on the overgrowth of the surface spiral steps associated with the surface intersections of the threading dislocations (Figure 7.23a–c). For the Y-shaped defects, this is based on overgrowth of the special configurations of steps at the surface intersections of the threading dislocations that were deflected onto the basal plane during substrate growth (Figure 7.23d–f).

7.4 Summary

By applying synchrotron X-ray topography techniques in conjunction with complementary characterization techniques, information on different dislocation types in bulk and thin film SiC materials has been obtained. Analysis of the behavior of these dislocations and their interactions during crystal growth has provided valuable information to either eliminate defects or engineer their structures to minimize their impact.

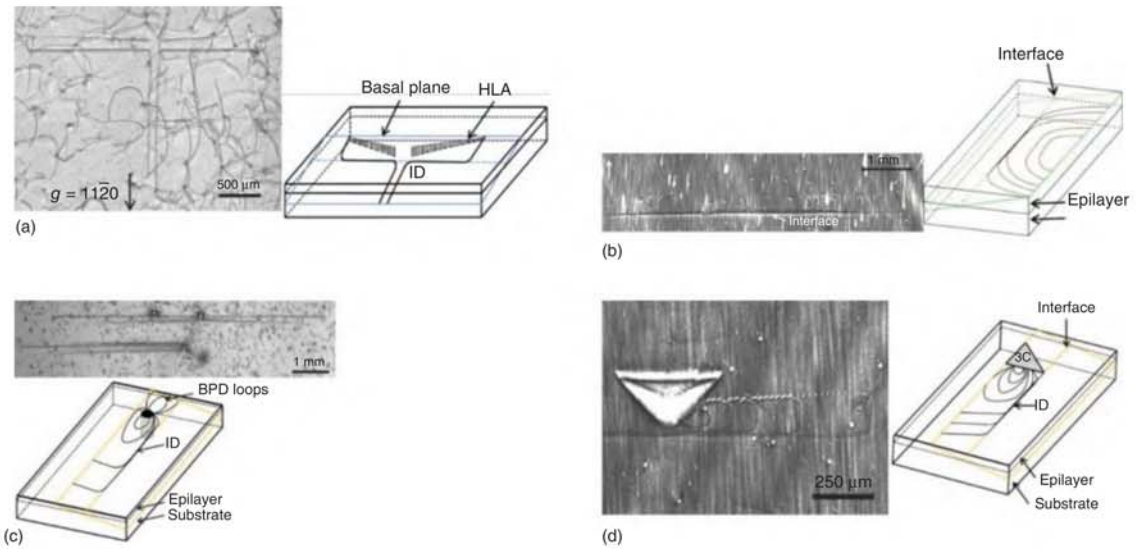


Figure 7.21 X-ray topographs and corresponding schematics of formation of interfacial dislocations and associated HLAs during (a) epilayer growth, (b) on epilayer surface, (c) micropipes and (d) 3C polytype inclusions. Source: Wang et al. [45].

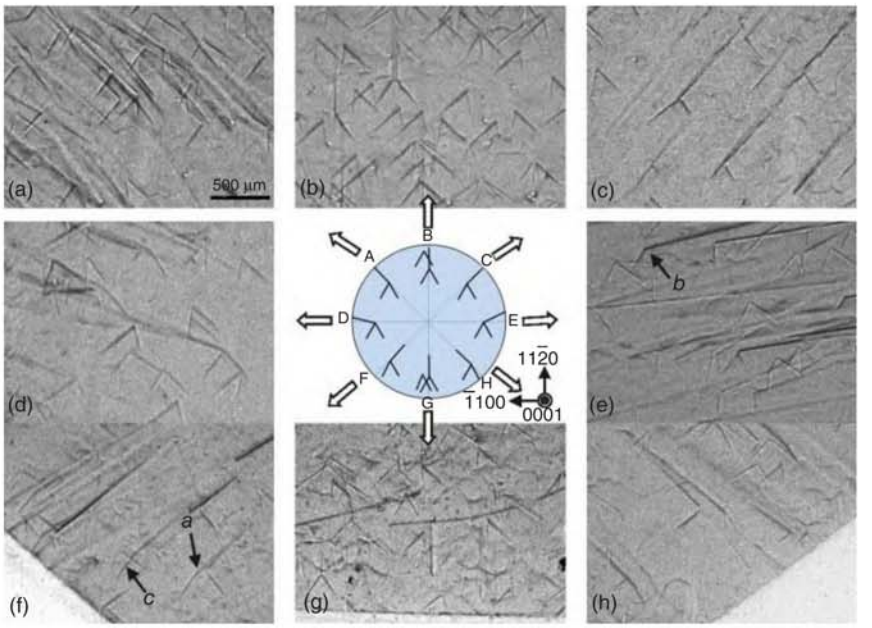


Figure 7.22 Grazing incidence X-ray topographs of V and Y shape defects around the periphery of the 4H-SiC wafer. Schematic in the middle shows how the V and Y shape defects distribute around the periphery of the wafer. Source: Wang et al. [46].

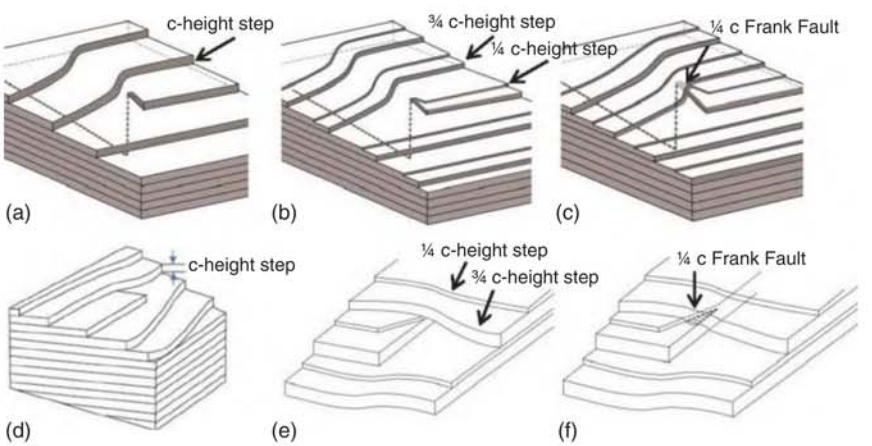


Figure 7.23 (a, c) The formation mechanism of V shape stacking fault during epitaxial growth; (d–f) the formation mechanism of Y shape stacking fault during epitaxial growth. Source: Wang et al. [46].

Acknowledgments

This work supported by Dow Corning, then Dupont (now SK Siltron). Topography experiments were carried out at the Stony Brook Synchrotron Topography Facility, Beamline X-19C, at the NSLS (DOE Office of Basic Energy Sciences Contract no. DE-AC02-76CH00016), Brookhaven National Laboratory. This research used resources of the Advanced Photon Source (Beamline 1-BM), a U.S. DOE Office of Science User Facility operated for the DOE Office of Science by Argonne National Laboratory under Contract No. DE-AC02-06CH11357. The Joint Photon Sciences Institute at Stony Brook University provided partial support for travel and subsistence at the Advanced Photon Source.

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8

Novel Theoretical Approaches for Understanding and Predicting Dislocation Evolution and Propagation

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8.1 Introduction

Dislocations in semiconductors have been studied extensively for Si and GaAs, both of which have a face-centered cubic crystal structure. Such crystal boules are grown from the melt using the Czochralski and floating zone method in the case of Si and liquid-encapsulated Czochralski and vertical gradient freeze method in the case of GaAs. The application of the so-called Dash necking technique [1] allows the reduction of the dislocation density in Si during the initial seeding growth stage down to a zero dislocation density value and then to retain this state throughout the complete growth process. Si ingots of up to 450 mm in diameter and wafers cut from those with a dislocation density of 0 cm^{-2} nowadays can be considered state of the art. GaAs as compared to Si has different thermoelastic properties and exhibits a greater brittleness, which is why the growth of "zero dislocation GaAs succeeded only up to a crystal diameter of roughly 70 mm [2]. GaAs crystal boules with a diameter >100 mm exhibit dislocation densities of approximately 100–3000 cm^{-2}. There, dislocations often cluster or form dislocation networks, sometimes termed *dislocation patterns*, that consist in a inhomogeneous dislocation distribution with regions of very low density bounded by strongly localized regions of very high densities. Due to the performance killing impact of dislocations on electronic devices, their propagation, multiplication, and annihilation have been studied in many aspects. Usually, the study of dislocation behavior during bulk growth is related to thermoelastic strain in the growing crystal. For a recent overview, please refer to the "Handbook of crystal growth – bulk growth edited by P. Rudolph [3] and to the recent work [4, 5] which particularly considers the formation of cellular dislocation networks also in SiC. Besides high dislocation densities and small-angle grain boundaries, also micro-pipes and super-screw dislocations with Burgers vectors larger than the c-lattice parameter are an important issue in SiC growth [6]. Last but not least stacking faults together with the occurring partial dislocations of different

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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core structures form extended defects, especially in non-cubic semiconductors such as nitrides and SiC [6]. This makes SiC a particularly interesting model system for defects in non-cubic semiconductor crystals.

In the following, we first introduce the state of the art in terms of modeling and simulation approaches. After that we concentrate on continuum modeling approaches for dislocation emphasis on two specific model classes, the Alexander–Haasen model and continuum dislocation dynamics (CDDs) models. This is followed by numerical examples that demonstrate different features of evolving dislocation structures: the first example shows that the ability to represent the flow of dislocations is important; the second example deals with dislocation motion between dislocation veins which act as strong obstacles for the motion of dislocations. We then summarize our work and put it into the perspective of ongoing research.

8.2 General Modeling and Simulation Approaches

There are many modeling and simulation approaches for defect-related phenomena on (sub) nanometer length scales. e.g. in the context of defects in semiconductors, Łażewski et al. [7] used density function theory for investigating the electrostatic barrier near the core of a pair of edge dislocations, and a number of authors, among them Rao et al. [8], Oren et al. [9], Zhou et al. [10], Chen et al. [11] applied molecular dynamics simulation for simulating dislocation in various materials such as, e.g. B3-GaN. However, such simulations are – for reasons of computational cost – not appropriate for simulating the structure–property relation of specimens on a macroscopic length scale. Discrete dislocation dynamics (DDDs) simulations [12–17] have been used only in rare cases with simulation codes from the metal plasticity community [18] and also suffer from a large computational cost. Nonetheless, they are able to simulate larger volumes/numbers of interacting dislocations than atomistic simulations. In the field of metal plasticity, phase field methods for dislocation dynamics gained some popularity [19, 20]. They do not resolve individual atoms but are still able to represent the dislocation core energy in some physical detail – unlike the DDD methods most of which are based on linear elasticity approaches. So far, there have been no applications to the domain of semiconductors.

Most of the (commercially) available software for macroscopic modeling on the device scale of semiconductors usually is only able to computes thermal stress during the growth process and, based on this, to roughly estimates the dislocation density based on a resolved shear stress; neither strain hardening nor details of the nucleation process or the flow of dislocations can be considered. Among the most commonly used phenomenological model is the Alexander-Haasen (AH) model [21], which is utilized in a range of different formulations to semi-quantitatively describe dislocation structures. Yonenaga and Sumino [22, 23] developed an elastic-viscoplastic type of constitutive equation for predicting the quantity of dislocation density. Ide et al. [24] analyzed the influence of oxygen diffusion on dislocation density during crystal growth and during the cooling processes. State-of-the art

simulation methods furthermore embed the AH model into a crystal plasticity finite element model [25–27] and thereby also consider the influence of the crystallographic orientations and slip systems on the resolved shear stress.

A novel type of continuum models is motivated by work that, so far, has been undertaken only within the small-scale metal plasticity field. The so-called Continuum Dislocation Dynamics (CDD) theory [28–32] is a strongly enhanced continuum crystal plasticity formulations in terms of additional microstructural information (i.e. detailed geometrical information of dislocation) and their nonlocal evolution equations (describing dislocation flow). The result is a continuum theory that is almost as detailed as a DDDs model but that does not suffer from the same computational restriction [33]: the computational time in DDD simulations scales almost quadratically with the number of interacting line segments, while for the CDD theory the number of dislocations has no influence, which allows for computational models that can eventually reach length and time scales comparable to experimental ones. As opposed to other continuum approaches, CDD can naturally differentiate and convert between straight and curved dislocations, as well as between "geometrically necessary dislocations (GNDs) and "statistically stored dislocations (SSDs) [29, 31].

8.3 Continuum Dislocation Modeling Approaches

Continuum models for predicting the evolution of dislocations have been used for more than half a century. The popularity is a result of the fact that continuous representations do not resolve each individual dislocation but rather operate with continuous density fields. The benefit is that the computational cost can be strongly reduced due to the fact that a density, i.e. the *dislocation line length per volume* is just a single number regardless how many dislocations are present. Thus, the computational cost does not scale with the number of interacting dislocations or atoms. The drawback is that a density value is not able to represent all details of the potentially complex dislocation microstructure [34–36]. In the following, we will introduce the theoretical background of two different models, the Alexander–Haasen model and the CDDs theory.

8.3.1 Alexander–Haasen Model

The Alexander–Haasen (AH) model [21] is based on the standard assumption of additive decomposition of the total strain rate $\dot{\boldsymbol{\epsilon}}$ into an elastic part $\dot{\boldsymbol{\epsilon}}^{\mathrm{el}}$, a thermal part $\dot{\boldsymbol{\epsilon}}^{\mathrm{th}}$, and a plastic contribution $\dot{\boldsymbol{\epsilon}}^{\mathrm{el}}$ as, $\dot{\boldsymbol{\epsilon}} = \dot{\boldsymbol{\epsilon}}^{\mathrm{el}} + \dot{\boldsymbol{\epsilon}}^{\mathrm{th}} + \dot{\boldsymbol{\epsilon}}^{\mathrm{pl}}$. Thermal loading causes thermal eigenstrains $\dot{\boldsymbol{\epsilon}}^{\mathrm{th}}$, while the mechanical loading gives rise to elastic strains $\dot{\boldsymbol{\epsilon}}^{\mathrm{el}}$, and additionally, the presence of dislocations causes eigenstrains $\dot{\boldsymbol{\epsilon}}^{\mathrm{pl}}$. Explicitly solving the (anisotropic) elastic boundary value problem yields stresses $\boldsymbol{\sigma}$. Projecting those by application of the symmetric projection tensor $\boldsymbol{M}_s = \boldsymbol{n} \otimes \boldsymbol{s}$, with the slip plane normal vector $\boldsymbol{n}$ and the slip direction $\boldsymbol{s}$ gives resolved shear stresses τ_{res} in the local coordinate system of the respective slip systems s. The plastic

shear strain contribution to $\varepsilon^{\mathrm{pl}}$ in the slip coordinate system is obtained from the Orowan equation, $\dot{\varepsilon}^{\mathrm{pl}} = \rho_{\mathrm{m}} b v$, with the modulus of the Burgers vector b, the density of mobile dislocations ρ_{m}, and the velocity of mobile dislocations v. The latter is phenomenologically given as a function of temperature and local effective stress

$$v = v_0 \left(\frac{\tau_{\mathrm{eff}}}{\tau_0} \right)^m \exp\left(-\frac{Q}{k_{\mathrm{B}} T} \right) \mathrm{sign}(\tau_{\mathrm{res}}) \tag{8.1}$$

where k_{B} is the Boltzmann constant, Q is the activation enthalpy, T is the temperature, and m is a fitting parameter. Furthermore, the effective shear stress is

$$\tau_{\mathrm{eff}} = \left\langle |\tau_{\mathrm{res}}| - \tau_{\mathrm{y}} \right\rangle \quad \text{with} \quad \langle \cdot \rangle = \begin{cases} \langle \cdot \rangle \text{ for } \langle \cdot \rangle > 0 \\ 0 \text{ for } \langle \cdot \rangle \leq 0 \end{cases}. \tag{8.2}$$

Therein, the yield stress τ_{y} governs dislocation interactions and is given by the so-called Taylor relation [37], $\tau_{\mathrm{y}} = aGb\sqrt{\rho_{\mathrm{m}}}$, with a constant a typically in the range of 0.2–0.5 and the shear modulus G. The yield stress acts like a friction stress which has to be overcome for plastic activity to take place. The set of equations is completed by a constitutive rate expression for the dislocation density of the form

$$\dot{\rho}_{\mathrm{m}} = K \left(\frac{\tau_{\mathrm{eff}}}{\tau_0} \right)^{\lambda} \rho_{\mathrm{m}} |v|, \tag{8.3}$$

with parameters λ and τ_0. Model extensions may separately consider evolution equations for mobile and immobile dislocations but are not able to convert the former into the latter quantity, or vice versa (cf. [38] for a discussion of the shortcomings of these models).

This macroscopic constitutive model might be used for obtaining a rough estimate of the order of magnitude of dislocation density in situations where homogeneous plasticity can be assumed. However, it is generally not possible to decide a priori whether homogeneous plasticity can be assumed or not. The AH model fails to predict fluxes of dislocations since it is a local model, given as an ordinary differential equation. It therefore also cannot represent, e.g. loss of dislocations through surfaces, as has been investigated in more details in [39]. Another consequence is that it fails to predict the peculiarities of occurring heterogeneous dislocation microstructures as, e.g. during dislocation cell structure formation. Thus, the AH model has only a limited range of applicability.

8.3.2 Continuum Dislocation Dynamics Models

Any version of a CDDs model is a nonlocal model which was obtained by coarse graining the geometrical properties and the motion of discrete dislocations (the so-called *kinematics* of dislocations). As such, it is based on a set of continuous variables and describes at least the *flux* of dislocation density by a set of transport equations. These models have been developed for and so far mainly used in the domain of metal plasticity [29, 31, 40–43].

8.3.2.1 The Simplest Model: Straight Parallel Dislocation with the Same Line Direction

In the particular case of straight dislocations of the same line direction, running along the y direction of a Cartesian coordinate system and that move in a slip system with $\boldsymbol{n} = \boldsymbol{e}_z$, the continuum dislocation kinematics is described by a scalar evolution equation of dislocation density ρ

$$\partial_t \rho = -\partial_x (\rho v), \tag{8.4}$$

where $\partial_i(\cdot) \equiv \partial(\cdot)/\partial i$. For a constant dislocation velocity v, this would be a pure convection equation. It is accompanied by the Orowan equation

$$\partial_t \gamma = \rho v b \tag{8.5}$$

where b is the magnitude of the Burgers vector and γ is the plastic shear strain in the respective slip system. γ, as an eigenstrain, serves as the connection to the elasticity theory, similar as in the AH model. The resulting stresses reflect in the velocity function v as detailed below.

8.3.2.2 The "Groma" Model: Straight Parallel Dislocations with Two Line Directions

Among those who established a more general continuum model in the dislocation community were [44] as well as I. Groma et al. [28, 45] who additionally investigated how the interaction of dislocations can be described in terms of continuum variables. The evolution equation Eq. (8.4) is then replaced by a set of evolution equations for the total and signed GND densities as,

$$\begin{aligned} \partial_t \rho_{\text{tot}} &= -\partial_x(\rho_{\text{gnd}}\, v) \\ \partial_t \rho_{\text{gnd}} &= -\partial_x(\rho_{\text{tot}}\, v). \end{aligned} \tag{8.6}$$

Dislocation densities still describe only straight (edge) dislocation, but this model allows for two different line orientations. The positive and negative dislocation densities, ρ_+ and ρ_-, are then defined as the number of dislocations with positive or negative line direction per averaging area. Thus, the total and GND density can be alternatively expressed as

$$\rho_{\text{tot}} = \rho_+ + \rho_- \tag{8.7}$$

$$\rho_{\text{gnd}} = \rho_+ - \rho_-. \tag{8.8}$$

Figure 8.1 shows a sketch of two different dislocation configurations highlighting the need for *two* different density variables. In the Groma model, it is possible to represent a so-called SSD content inside an averaging volume, e.g. the volume contains both an edge dislocation with positive line orientation and an edge dislocation with negative line orientation. As a consequence, positive and negative densities can move past each other without being annihilated, i.e. as if on different slip planes inside the averaging volume.

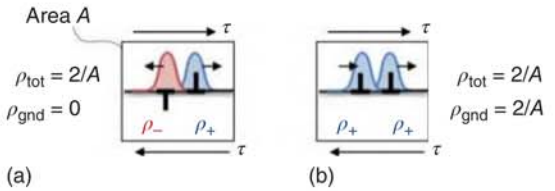


Figure 8.1 (a) An averaging area containing two edge dislocations with opposite line directions. (b) Same averaging area containing two edge dislocations with the same line direction. Both systems have the same total density but differ in the net GND content. τ is the applied shear stress under which action a positive edge dislocations moves in positive x direction (here: to the right), a negative edge moves toward the left, as indicated by the small arrows.

8.3.2.3 The Kröner–Nye Model for Geometrically Necessary Dislocations

A different approach is based on the Kröner–Nye tensor [46] which is defined as

$$\boldsymbol{\alpha} = \operatorname{curl} \boldsymbol{\beta}_{\mathrm{pl}}, \tag{8.9}$$

where $\boldsymbol{\beta}_{\mathrm{pl}}$ is the plastic distortion. This representation is only valid if all dislocations in an averaging volume share the same line direction $\boldsymbol{l}$, which is why there is an alternative formulation based on the GND density,

$$\boldsymbol{\alpha} = \rho_{\mathrm{gnd}} \boldsymbol{l} \otimes \boldsymbol{b}. \tag{8.10}$$

If the coordinate system is aligned with the Burgers vector direction and the edge orientation, the individual coefficients of the Kröner–Nye tensor contain the edge and screw GND contributions. One of the main differences to the above introduced two models is that here dislocations can also be curved. A serious drawback of this quantity is that once the assumption of GND content is violated, e.g. an averaging volume contains dislocations of opposite line orientation, the dislocation content would be "annihilated." This is nonphysical in particular in situations where averaging volumes are larger than the annihilation distance which for metals has a typical order of magnitude of a few Burgers vectors. Combining the advantage of the Groma model to handle SSD densities with opposite line orientations with the ability of the Kröner–Nye model to handle arbitrarily curved lines leads to extended CDDs models that can also work in truly three-dimensional situations.

8.3.2.4 Three-dimensional Continuum Dislocation Dynamics (CDD)

Representing dislocation microstructures as only straight edge dislocations in 2D or as GND structures has many limitations and is therefore not suitable to be used as basis for 3D models:

(i) Curved dislocations may bow out and thereby increase the line length contained in the system, while straight dislocations can only translate [40]. However, the resulting densities and the plastic slip are very different.
(ii) While only GNDs give rise to internal stresses [32, 45], *all* dislocations need to be considered because due to the motion of dislocations they can change their "character," e.g. a GND configuration may become a dipole configuration with a zero net GND content.

(iii) Real dislocation microstructures are intrinsically three dimensional and may include many complex phenomena such as junctions or locks that can only be represented in truly three-dimensional models. A detailed comparison of CDD models of varying complexity can be found in [38].

To alleviate the above shortcomings, a more advanced CDDs model was introduced by Hochrainer et al. [29], which also can be generalized to three-dimensional systems. Similar to the above models, the dislocation velocity drives the evolution of the dislocation microstructure in each slip system, which in the case of Hochrainer's CDD is represented by four field variables: the total density ρ_t (which upon volume integration gives the total line length inside the volume), a vector of "geometrically necessary dislocation density $\boldsymbol{\varrho} = [\varrho_s, \varrho_e]$, e.g. of screw ($\varrho_s$) and edge ($\varrho_e$) dislocations, a curvature density q_t (which upon volume integration gives the number of closed dislocation loops as multiple of 2π) and the plastic strain γ. The temporal change is governed by evolution equations in the form of partial differential equations (PDEs) which have the character of transport equations

$$\begin{aligned}
\partial_t \rho_t &= -\nabla \cdot (v\boldsymbol{\varrho}^{\perp}) + v q_t \\
\partial_t \boldsymbol{\varrho} &= -\nabla (v \rho_t) \\
\partial_t q_t &= -\nabla \cdot (-v\boldsymbol{Q}^{(1)} + \boldsymbol{A}^{(2)} \cdot \nabla v)
\end{aligned} \tag{8.11}$$

and which are, for each slip system, completed by the Orowan equation for the rate of plastic strain $\gamma = \rho_t b v$. Therein, a dot denotes the scalar product, $\boldsymbol{\varrho}^{\perp} = [\varrho_e, -\varrho_s]$ is the 90° rotated GND density vector. As stated in [36], we assume that,

$$\boldsymbol{Q}^{(1)} = -\boldsymbol{\varrho}^{\perp} q_t / \rho_t \tag{8.12}$$

$$\boldsymbol{A}^{(2)} = \frac{\rho_t}{2} \left[(1 + \Psi)\, \boldsymbol{l}_{\varrho} \otimes \boldsymbol{l}_{\varrho} + (1 - \Psi)\, \boldsymbol{l}_{\varrho^{\perp}} \otimes \boldsymbol{l}_{\varrho^{\perp}} \right] \tag{8.13}$$

where $\boldsymbol{l}_{\varrho^{\perp}}$ is the unit vector perpendicular to $\boldsymbol{l}_{\varrho}$ and $\boldsymbol{l}_{\varrho} = \boldsymbol{\varrho}/|\boldsymbol{\varrho}|$ is the average line direction, and Ψ is approximated as

$$\Psi \approx \frac{\left(|\boldsymbol{\varrho}|/\rho_t\right)^2 \left(1 + \left(|\boldsymbol{\varrho}|/\rho_t\right)^4\right)}{2} \tag{8.14}$$

[29] showed that it is possible to construct CDD formulations that additionally include higher-order equations, which was analyzed for a number of formulations by Monavari et al. [38]. However, [47] showed that already the above set of equations is well able to represent many important features of DDD simulations.

The velocity v in the above equations needs to be specified in terms of a constitutive equation through which elastic interactions enter the model,

$$v = \begin{cases} \frac{b}{B} \left(|\tau_0| - \tau_y \right) & \text{for } |\tau_0| > \tau_y \\ 0 & \text{otherwise} \end{cases} \tag{8.15}$$

where $\tau_0 = \tau_{ext} + \tau_{int}$ is the summation of the external shear stress (τ_{ext}) and the long-range (or "internal) interaction stresses (τ_{int}) which have to be obtained from the additional solution of a dislocation eigenstrain problem [32, 48, 49]. τ_y is as above the Taylor-type yield stress.

8.4 Example 1: Comparison of the Alexander–Haasen and the Groma Model

8.4.1 Governing Equations

In the following, we only want to study the difference due to the transport character of the evolution equations. To make the two models comparable, we will use the same phenomenological source term for dislocation multiplication of the AH model for the Groma model. By adding the right-hand side of Eq. (8.3) into the transport equations Eq. (8.6) with the assumption that $\rho_{\mathrm{tot}} \equiv \rho_{\mathrm{m}}$, the evolution equations Eq. (8.6) then simply become

$$\begin{aligned} \partial_t \rho_{\mathrm{tot}} &= -\partial_x(\rho_{\mathrm{gnd}} v) + S \\ \partial_t \rho_{\mathrm{gnd}} &= -\partial_x(\rho_{\mathrm{tot}} v) \end{aligned} \tag{8.16}$$

with

$$S = K\left(\frac{\tau_{\mathrm{eff}}}{\tau_0}\right)^{\lambda} \rho_{\mathrm{tot}}|v| \tag{8.17}$$

where v is again given by Eq. (8.1). The subscript "m" in the AH model indicates that only mobile and no sessile dislocations are considered; the Groma model does not have to differentiated between the two "types" of dislocations. However, since in our model no, e.g. junction formation can take place, all dislocations could be considered as mobile.

8.4.2 Physical System and Model Setup

The considered physical system is a hexagonal 4H-SiC crystal as, e.g. grown by the physical vapor transport (PVT) technique. The crystal is assumed to have $h = 45$ mm and the radius $r = 30$ mm, as shown by the gray-shaded region in Figure 8.2a. As a simplification, we only consider a two-dimensional cross-section as indicated by the blue rectangle in the same figure. There, the basal plane that is characterized by a normal pointing into the z direction is the only active slip system. As mechanical boundary conditions the crystal is fixed in the x and z directions at point C_1 and only in z direction at point C_2. For simplicity, we do not consider cooling, heating, or heat fluxes, only a time-independent symmetrical temperature field is prescribed during simulation. The resulting resolved shear stress distribution is shown in Figure 8.2. The same geometry setup is used for the AH model and the Groma model. The simulations are based on the following material parameters and constants: $b = 3.073 \times 10^{-10}$m, $v_0 = 8.5 \times 10^{-15}$m/s, $K = 2.0 \times 10^{-5}$ m^{-1}, $Q = 3.3$eV, $\lambda = 1.1$, $m = 2.8$, $a = 0.425$, and the Boltzmann constants is $k_{\mathrm{B}} = 8.617 \times 10^{-5}$ eV/K. For the mechanical problem, the thermal expansion coefficient is temperature dependent [50] as shown in Figure 8.3; also the components of the stiffness tensor

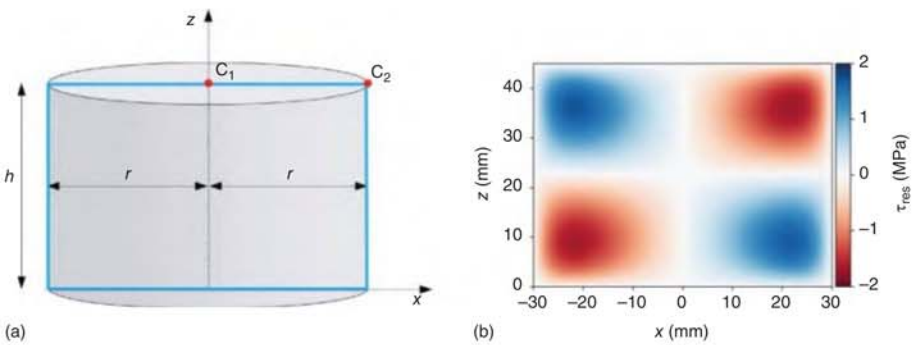


Figure 8.2 (a) 2D crystal geometry and (b) initial distribution of the resolved shear stress τ_{res} at $t = 0$ seconds in the plane indicated by the blue lines in (a).

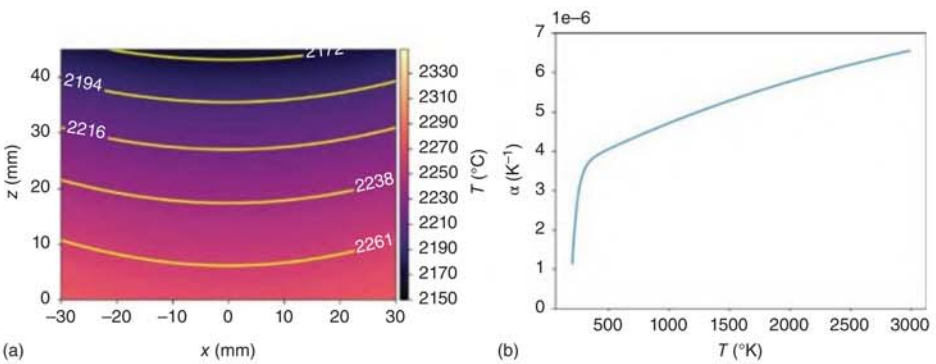


Figure 8.3 (a) Prescribed temperature field, (b) Thermal expansion coefficient.

are temperature dependent [51]. In Voigt notation, they read for hexagonal SiC: The temperature-dependent shear modulus is taken as the elastic constant C_{44}.

$$\begin{bmatrix} C_{11} \\ C_{12} \\ C_{13} \\ C_{33} \\ C_{44} \end{bmatrix} = T \times \begin{bmatrix} -0.025 \\ -0.011 \\ -0.011 \\ -0.025 \\ -0.007 \end{bmatrix} \frac{\text{GPa}}{\text{K}} + \begin{bmatrix} 486.6 \\ 101.3 \\ 59.02 \\ 528.9 \\ 150.3 \end{bmatrix} \text{GPa} \tag{8.18}$$

For the numerical solution of this time-dependent, multiphysics problem which consists of a mechanical part, a thermal part and the dislocations part, the finite element method is used. For the numerical discretization, triangular elements with quadratic shape functions were used for both the elastic and thermal problem; for the CDD dislocation problem, we used cubic shape functions so that all derivatives are approximated properly.

8.4.3 Results and Discussion

The simulation results of the AH model and the Groma model are shown in Figure 8.4 and include dislocation density, resolved shear stress, and plastic shear strain at a total time of $t = 3000$ seconds. There, the plots in the left column display the result from the AH model, the middle column shows the results from the Groma model, and the last column are the corresponding results along the red, dashed line. The difference between these two model is then easily observable with both the magnitude of dislocation density (Figure 8.4a,b) and the qualitative shape of the plots themselves (see Figure 8.4c). The AH model shows a growing patch of increasing dislocation density (see Figure 8.4a) where the resolved shear stress is highest while the Groma model exhibits smaller patches of dislocation density (see Figure 8.4b) at the surface ($x \approx 30$ mm, label C) and around the crystal axis ($x = 0$ mm, label A). The maximum dislocation density values of the Groma model are observed to be close to the surface with values of roughly 2500 cm^{-2} and a value of 600 cm^{-2} around the axis, while the AH model has a maximum value of approximately 1500 cm^{-2}. In a way, the two models behave opposite to each other. The difference between the two models is also obvious in the results of the resolved shear stress. Figure 8.4d,e shows the resolved shear stress τ_{res} field for the basal slip system with respect to the dislocation density distribution in Figure 8.4a,b. In the AH model, ρ_{m} will initially increase at the four stress hot spot (see Figure 8.2b) and then decrease as a consequence of plastic relaxation which can be observed in the shape change (compared Figure 8.2 and Figure 8.4d); it reaches the state shown in Figure 8.4d. As a result of this "stress transfer," a substantial increase in dislocation density by nucleation of new dislocations takes place in regions where originally the initial stress was low. As opposed to that, in the Groma model, dislocation accumulations occur close to the surface and close to the crystal axis. The reason for this behavior is that dislocations are nucleated where the stress is highest, but then move away, driven by shear stresses. They accumulated where the shear stress is low (see Figure 8.4e,f) and form quasi-stationary pile-up structures. It ultimately

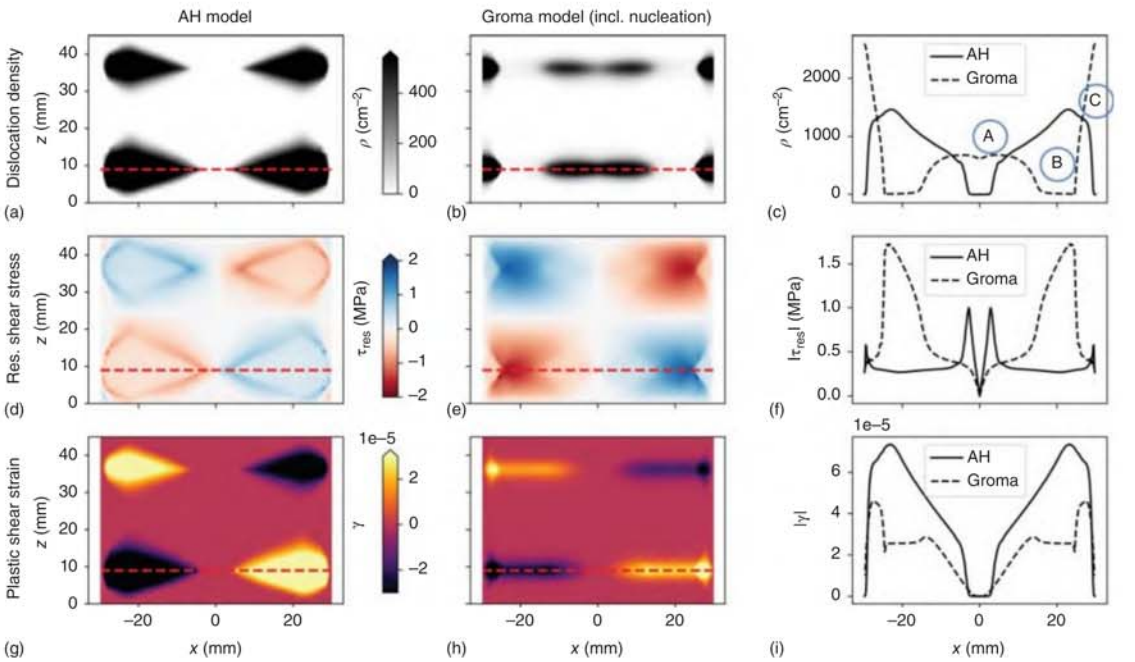


Figure 8.4 Comparison between AH model and Groma model including a source term: the top row shows the density, the middle row the resolved shear stress, and the bottom row depicts the plastic strain. The left column are results for both models plotted along the red, dashed lines.

leads to a depleted zone where in the AH model the density is highest (see label B in Figure 8.4c).

Is this consistent with the results for the plastic shear? For the AH model, plastic strain co-evolves with the nucleation of dislocation density, and therefore, as expected, has roughly the same shape as the dislocation density (see Figure 8.4g,i). The Groma model behaves quite differently as the AH model. In the Groma model, the plastic strain is caused by dislocation *motion* and is high in the regions which were swept by dislocation (see Figure 8.4h,i). These are, for this example, exactly the regions where no dislocations are present any more. This is the expected behavior which is consistent with basic dislocation dynamics. Thus, the comparison of the two different simulations revealed that the flow of dislocation in the crystal during growth cannot be neglected, as it is done in the AH model. The dislocation motions controls the distribution of dislocation inside the crystal and makes it possible that dislocations can move even to places where originally the stress was low, such as the surfaces or the central region. However, the Groma model has some limitation, as already above stated: e.g. the source term is just an approximation which cannot capture the whole mechanisms of dislocation nucleation; furthermore, dislocations are only assumes to be straight lines. And last but not least, the simulation only considers basal plane dislocation while there are many more types of dislocations in reality that also need to be taken into account.

8.5 Example 2: Dislocation Flow Between Veins

8.5.1 A Brief Introduction to Dislocation Patterning and the Similitude Principle

Under certain conditions, it is observed that dislocations tend to form heterogeneous but regular structures, some of which are termed "dislocations patterns." They are observed both in metals as well as in semiconductors. The micrographs in Figure 8.5 show examples of such structures. These dislocation patterns can occur, e.g. as approximately periodic dislocation agglomerations or sharply distinguishable cell (e.g. Figure 8.5c) or "labyrinth" structures (Figure 8.5h). The common feature is that all of these structures are characterized by clusters of very high dislocation density alternating with regions of very low (or zero) density. These dislocation formations are usually "metastable structures which mostly persist upon unloading. One of the remarkable features is that the cell sizes Λ – regardless material, loading condition or temperature – are always related to the applied stress τ_{ext} through the "law of similitude [52, 53] by $\Lambda = DaGb/\tau_{\text{ext}}$, where usually the constant $D = 10$–20 and G is the shear modulus, and $a \approx 0.3$ is the nondimensional coefficient relating flow stress and dislocation density ρ in the Taylor relationship $\tau = aGb\sqrt{\rho}$. This has been known for plastically deformed metals for about half a century [54] but is also observed in semiconductors as pointed out more recently by Rudolph [4, 5]: e.g. in GaAs dislocations arrange themselves in experimentally observable cellular structures of diameter in between 100 and 1000 μm. Although

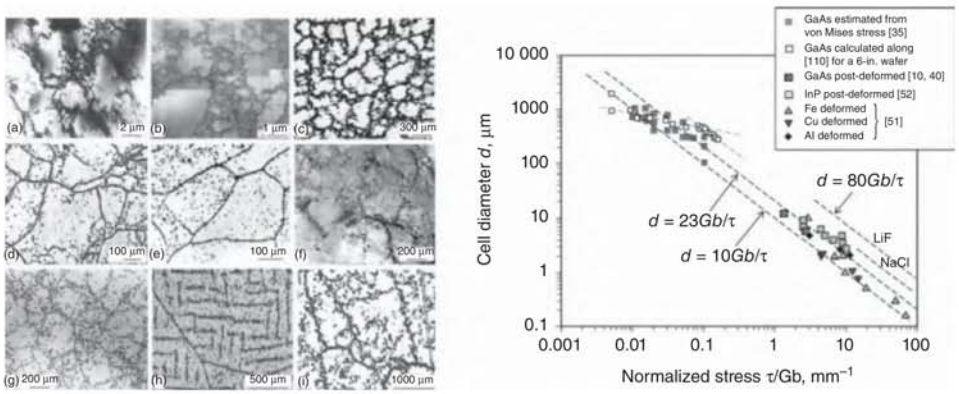


Figure 8.5 Dislocation organizes themselves into patterns as, e.g. cell structure, independent of the material or loading condition (A). The cell size is related to the applied stress through the "similitude relation (B). Images taken with permission from [4].

the regular (sometimes fractal) appearance is visually interesting, these dislocation structures deteriorate the electronic and mechanical properties of semiconductors, and their formation needs to be prevented as far as possible. Hence, understanding the mechanisms leading to the occurrence of patterns is crucial for being able to prevent such structures. Rudolph [4] suggested to relate the origin of this phenomenon to the same mechanisms as in the case of metals (where cells form roughly in the 1–10 µm size range, see Figure 8.5A). The different cell size regimes, i.e. mm-range for semiconductors and µm-range for metals, is related to the very different dislocation densities at saturation which result in different stresses due to the Taylor relationship (8.5B). In the case of SiC dislocation, cell structures have also been reported in the past for materials exhibiting dislocation densities in the mid $10^4\,\mathrm{cm}^{-2}$ to low $10^5\,\mathrm{cm}^{-2}$ range; however, basically no attention has been paid to describe the dislocation microstructure in terms of such networks or cells. At lower dislocation densities in the mid $1\times10^3\,\mathrm{cm}^{-2}$ range as it is typical for best commercial SiC wafer materials, the cell structure is difficult to visualize and mainly occurs in defective areas where dislocation bundles occur. So far, no detailed theoretical concept or computational model of dislocation cell formation in semiconductor materials exists. There is, however, a great need to explain and therefore to be able to take countermeasures against the formation of dislocation entanglements, which also has been recognized in the literature: for instance, the 2014 edition of the book *Extended Defects in Semiconductors* by Holt and Yacobi [55] strongly emphasizes within the last sentence of the section *Major Persisting Issues* "… The need for a theoretical framework for this phenomenon [cellular dislocation structures]…". Encouraged by this general viewpoint, we take it as an worthwhile task to transfer modeling of dislocation patterning from metals to the semiconductor case.

8.5.2 Physical System and Model Setup

Approaches that are able to predict dislocations patterning are – even in the modeling community for dislocation mediated metal plasticity simulation – very scarce: even discrete simulation methods are due to the computational cost generally not able to predict the evolution of dislocation patterns. This is why in the following a CDD model will be used to demonstrate some of the most important mechanisms involved during formation of dislocation patterns. The first stage, i.e. the formation of such stable dislocation agglomerations has already been investigated in [34] and for a different formulation also in [56] where it was shown that the above CDD model is indeed able to simulate this.

As a model system, we now assume that already a stable wall-like structure (e.g. a cell wall or the wall of a persistent slip band, PSB) exists. A dislocation dynamics model must then be able to represent the motion of dislocations between these constraining walls, similar to the situation investigated in [38]. The experimental results from [57] shown in Figure 8.6a illustrate the walls structure in a so-called persistent slip band (PSB) which consist of dipolar edge dislocation configurations. The dislocations gliding in the channels between the walls have mainly

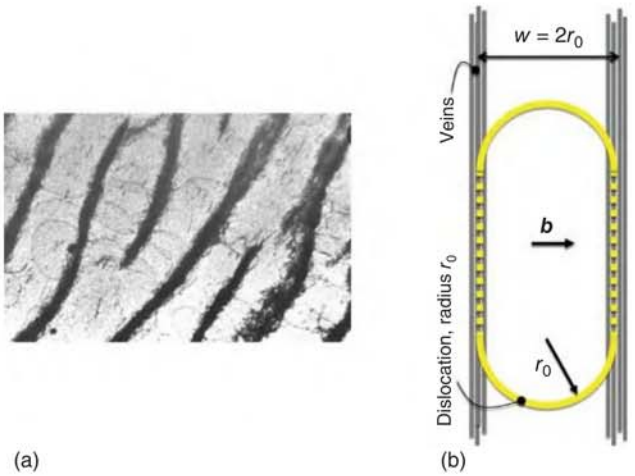


Figure 8.6 (a) TEM micrograph showing walls of PSBs (dark) [57] and gliding of screw segments between walls; (b) schematic of dislocation vein structure made up of extended edge dipoles and glide screw dislocation of radius r_0. The channel width is $w = L_x$. Source: Hael Mughrabi. Cyclic slip irreversibilities and the evolution of fatigue damage. Metallurgical and Materials Transactions B, 40(4):431–453, 2009. Source: Hael Mughrabi. Cyclic slip irreversibilities and the evolution of fatigue damage. Metallurgical and Materials Transactions B, 40(4):431–453, 2009.

screw orientation. In cell structures, the cell walls may have a different dislocation content; however, the ability to represent bowing out of dislocations and glide in between the walls is equally important. In what follows we will now demonstrate that the CDD model is able to represent the bowing-out/gliding mechanism, which is a prerequisite for predicting the formation for cell or wall structures.

8.5.3 Geometry and Initial Values

The geometry is chosen to be rectangular with the channel width L_x and the channel length L_y (see Table 8.1 for all numerical values and used material parameters). The system is periodic in y direction, i.e. dislocations exiting the system at the top will flow back in at the bottom. In horizontal direction, the boundaries are

Table 8.1 Parameters for dislocation flow between veins.

Parameter	Value
System size L_x	1×10^{-5}m
System height L_y	2×10^{-5}m
Loops radius r_0	2×10^{-6}m
Standard deviation s	7×10^{-6}m
Burgers vector modulus b	0.256×10^{-9}m
Drag coefficient B	5×10^{-8}Pa s
Shear modulus G	128×10^{9}Pa

impenetrable for dislocations, which are modeled by a horizontal velocity profile that is zero directly at the boundaries, constant inside the channel with a value of v_0, and has a smooth transition in between:

$$v = v_0 \left(\frac{2}{1 + e^{-(x+L_x/2)\beta}} - 1 \right) \left(\frac{2}{1 + e^{-(L_x/2-x)\beta}} - 1 \right) \tag{8.19}$$

with $v_0 = 0.4\,\mathrm{ms}^{-1}$, $\beta = 0.004$. Within the present work, we ignore all dislocation interactions and concentrate exclusively on the "kinematics that is, how curved and connected lines move and evolve in space and time without interactions.

In order to consistently representing a system of curved and connected lines in a coarse-grained continuum manner, we obtain dislocation density distributions (such as ρ_t) by first defining a distribution of a number of mathematical dislocation loops. This is followed by convolution along the loops' lines with a Gaussian normal distribution function $\left(s\sqrt{2\pi}\right)^{-1} \exp\left(-\xi^2/2s^2\right)$, where s is the width of the distribution and ξ is the distance perpendicular to the loop. This effectively "smears out" the line perpendicular to it. By multiplication of the dislocation density with the normalized radial unit vector or division by its radius, r, we can determine the dislocation density vector $\boldsymbol{\varrho}$ or the curvature density $q_t = \rho_t/r$, respectively. CDD initial values are obtained by summing up the individual fields. Initial values with two dislocation loops and 50 dislocation loops for our simulation are shown in Figures 8.7 and 8.8. The curvature, i.e. 1/radius of a line is obtained in a postprocessing step from $k = q/\rho$; it is not defined in regions where the density is zero (compare the right most plot in Figure 8.7). More details on the process of creating consistent initial values can be found in [33, 34].

8.5.4 Results and Discussion

Because of the zero velocity in the walls and the smooth transition from $v = 0$ to a constant velocity v_0 further away from the wall, the velocity field acts such that dislocations are first slowed down on their way toward the walls and eventually freeze

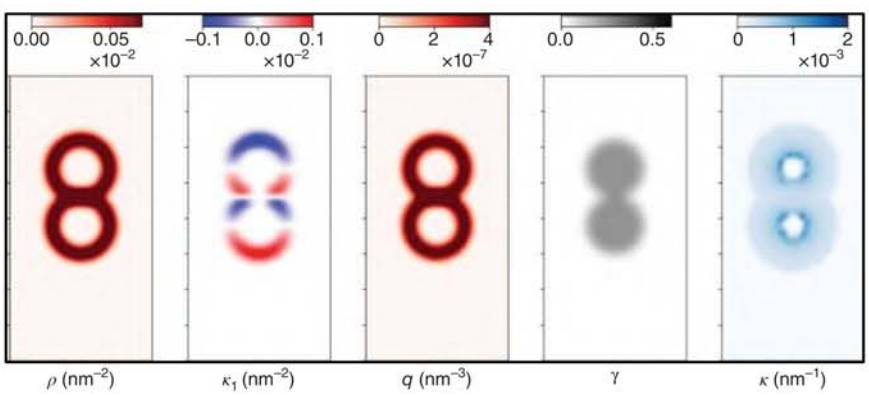


Figure 8.7 Initial CDD field values for two quasi-discrete dislocation loops. From left to right: total density, edge GND density component, curvature density, plastic slip, curvature.

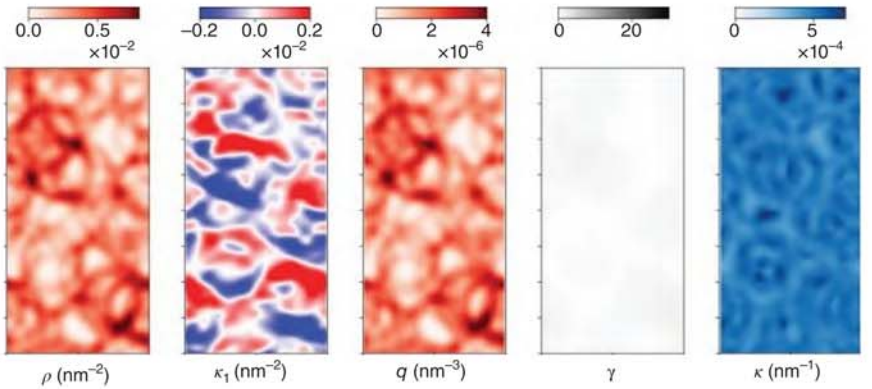


Figure 8.8 Initial CDD field values for a distribution of 50 dislocation loops. From left to right: total density, edge GND density component, curvature density, plastic slip, curvature.

in their motion so that they cannot enter the walls. Figures 8.9 and 8.10 present the relations among the four CDD variables during dislocation evolution. The two-loop system is not fundamentally different from the 50-loop system but makes it easier to understand the meaning of the different fields. Initially, one can observe free loop expansion inside the domain because of the constant velocity. Since we neglect interaction between dislocations and assume that they or on different but near-by slip planes in their respective averaging volumes, they will pass through each other during expansion. Later, at time $t = 0.01$, we can observe that dislocation will reach the left and right boundaries and begin to a pile-up at these walls while they still expand in the vertical direction (see Figures 8.9 and 8.10). An interesting feature is the formation of pile-ups of bent lines at walls: when expanding dislocation loops touch the left and right boundaries, they bend and adjust to the shape of the walls. Because of that, the values of curvature density q at these areas are larger than inside area. Line pile-ups of dislocation density can be seen in the left and right boundaries and even clearer as a banded structure at time $t = 0.025$. The dislocation density ρ has a high value in the vicinity of the walls because of the density from piled-up dislocations. The threading edge segments, i.e. density with approximately horizontal orientation, are segments from expanding loops. Therefore, they become more straight, which also shows in their reduced curvature (last column of Figures 8.9 and 8.10). Investigating the curvature $k = q/\rho$, because of the impenetrable walls we observe that the screw segments are straight with the curvature value $k = 0$ at walls and we find a nonzero curvature shortly before the surface where dislocations need to bend strongly.

The plastic slip γ – which is the pendant of the plastic strain on the level of the individual slip plane – shows clearly that it is proportional to the slipped area. Where two loops overlap, the value of γ is doubled. The system with 50 loops, on the other hand, shows nearly homogeneous plasticity in the inside of the channel and a larger accumulation of plastic slip directly at the boundaries. This is due to the fact that the high curvature density scales is responsible for additional line length production.

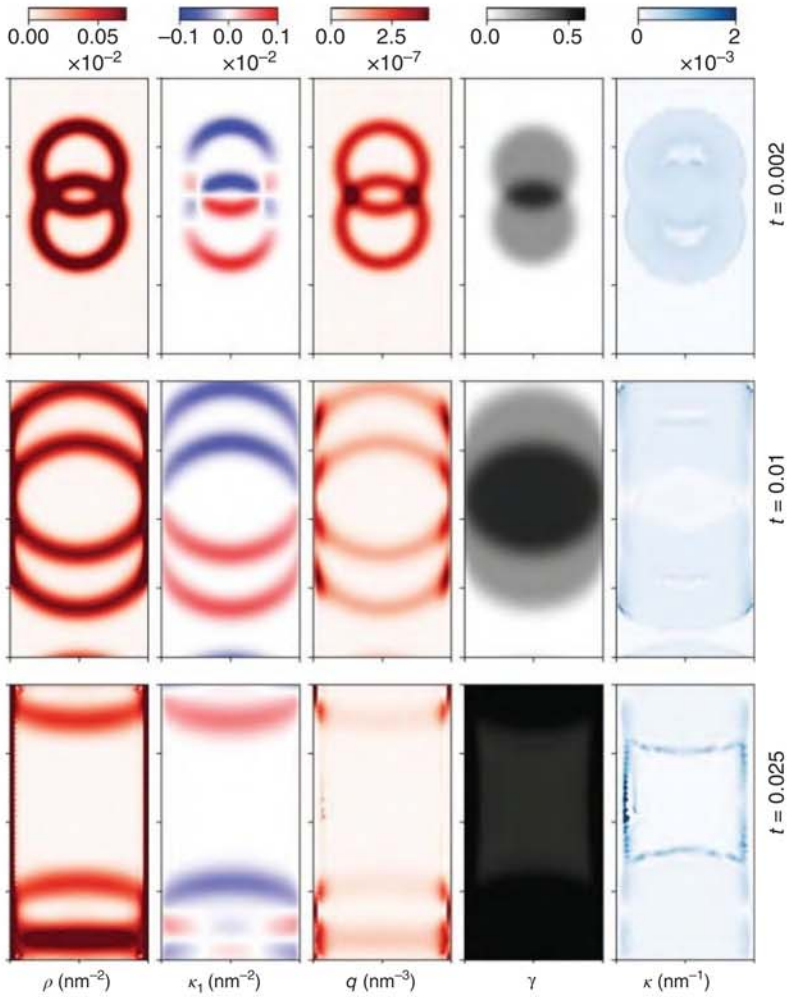


Figure 8.9 Two mobile dislocation loops expansion in the channel.

How do these microscopic field variables relate to average quantities on the macroscopic system scale? Figure 8.11 shows the total dislocation line length $l = \int_A \rho \, \mathrm{d}A$ versus time. To validate our model results, we construct two extreme cases:

(i) There is only free loops expansion as if no boundaries and interactions are present. This results in a linear line length increase $L = N_\mathrm{d} 2\pi \left(r_0 + vt\right)$ (with N_d the number of loops and v the velocity) and is shown as the tangent in Figure 8.11a.

(ii) Loops have a very large radius such that the threading edge segments can be considered as straight. Then these segments move and at the same time deposit straight screw segments at the boundaries, as if it were a rectangular loop. This yields a line length of $L = N_\mathrm{d} \left(\pi w + 4vt + 2w\right)$ with w the width of the channel. This is shown as the tangent in Figure 8.11b.

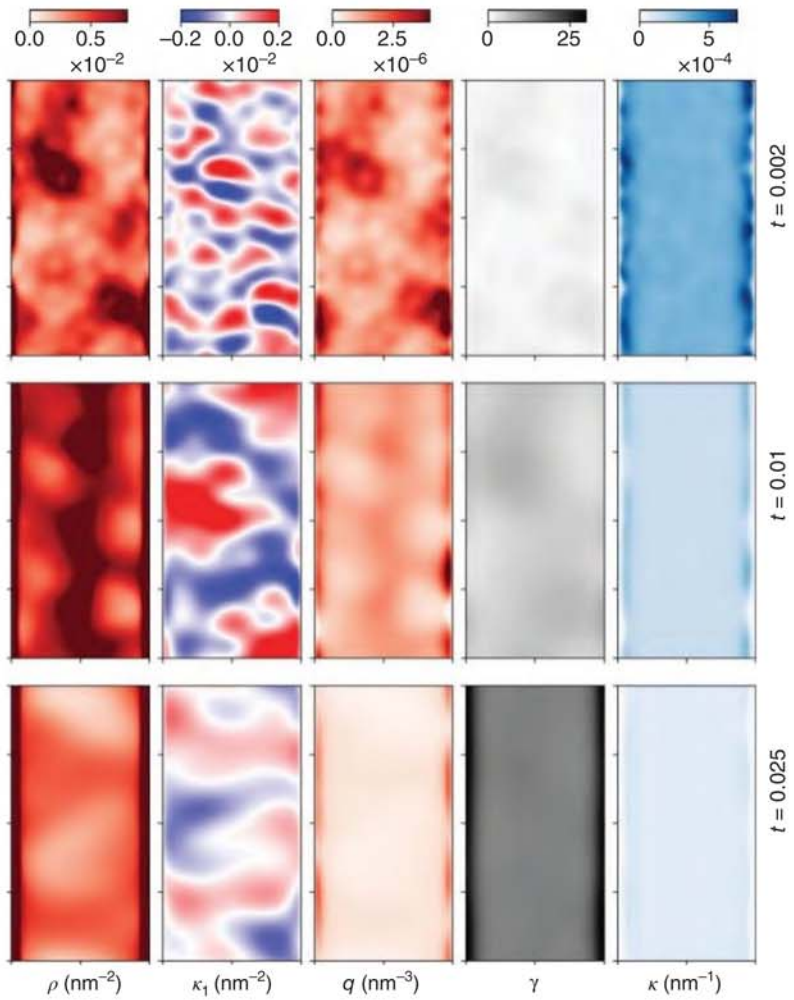


Figure 8.10 Fifty mobile dislocation loops expansion in the channel.

One can observe that the simulation reproduces the correct rate of line length at the beginning of the simulation and toward the end, in between is a larger transition region. This clearly demonstrates that the complex interplay between dislocation loop expansion, dislocation motion, line bending, and deposition at a boundary can all be predicted by this CDD model. Additionally, without dislocation interactions, the system is just a superposition of individual loops, even in cases where the individual loops can no longer be distinguished. Using just the Groma model could not work because the line length production due to the threading edge dislocations cannot be represented and the total line length in the system would stay constant. How would the AH model have performed? A direct comparison is difficult because the CDD model can operate even without stresses and just by prescribing a velocity. Assuming a constant shear stress, the AH model would not be able

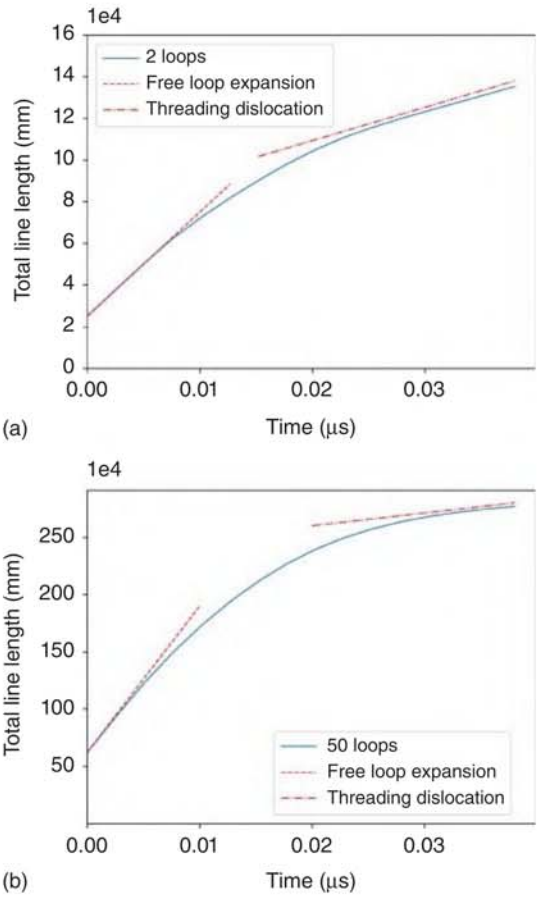


Figure 8.11 Total line length vs. time. The two tangents denote the line length assuming (i) only free loop expansion without any boundaries and (ii) only straight edge segments that are connected by straight screw segments as in a rectangular loop.

to represent the deposition of density at the boundary, similar to what was shown in Figure 8.4. Furthermore, it would not be possible to interpret the resulting density or plastic strain configuration in terms of geometrical properties of dislocations lines. Since dislocations are the carrier of plastic deformation, we see the lag of interpretability as one of the big drawbacks of any purely phenomenological continuum model – irrespective of the quality of the overall predictions.

8.6 Summary and Conclusion

An overview over current state of the art modeling techniques for predicting defects in semiconductors has been presented. Putting a focus on systems of dislocations, it was discussed that it might be very lucrative to apply simulations methods from the metal plasticity domain to the domain of semiconductors. In this context, a number of state-of-the art methods for predicting the dislocation dynamics in a continuum frame work were introduced and critically discussed. In particular, the comparison with one of the most established simulation model used in the

semiconductor domain, the Alexander–Haasen model demonstrated that it is very important to be aware of the limitations and the range of applicability of a model: the Alexander–Haasen model is not able to predict fluxes of dislocations, which in many applications might be a strong limitation.

Discussing modeling approaches in the context of dislocation pattern formation, we demonstrated that the introduced CDD model is able to represent many important dislocation features that also can be clearly interpreted in terms of geometrical features of curved lines. Nonetheless, the current CDD theory still has not been applied to general system in three dimensions. This will require detailed work on extracting data from DDD and MD simulations that can then be used as input for dislocation interaction formulations. Nonetheless, a continuum model that operates on length and time scales comparable to experimental ones also might be very well able to act as a link between theory, modeling, and experiment. In particular, experimental data is, of course, the ultimate benchmark for any model. Therefore, one might be tempted to say that a good simulation model need not exactly reproduce experimental results; rather, a good simulation model is a model that can be easily interpreted as well as parameterized and directly validated by experiments, both on the microscopic and macroscopic scale.

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9

Gate Dielectrics for 4H-SiC Power Switches: Understanding the Structure and Effects of Electrically Active Point Defects at the 4H-SiC/SiO_2 Interface

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9.1 Introduction

At the heart of every metal oxide semiconductor field effect transistor (MOSFET) is the interface between the oxide and the semiconductor. The field effect may create a conducting channel between the source and the drain of the transistor [1] which makes up an electronic switch. Especially in the field of power transistors, designed to block source–drain voltage above 600 V, silicon carbide (SiC) has become an important semiconductor in recent years. However, there was a 10-year delay between the introduction of the first SiC diode and the first SiC MOSFET [2]. This delay can partially be attributed to SiC specific manufacturing challenges for MOSFETs. Among them, it was crucial to be able to control the detrimental impact of electrically active point defects at the four layer hexagonal SiC (4H-SiC)/silicon dioxide (SiO_2) interface which impacted the performance and reliability of SiC MOSFETs.

Here, we summarize previous research on a few SiC specific electrical effects of interface traps on the performance and reliability of SiC MOSFETs. In Section 9.2, we describe the electrical characteristics and how they are efficiently characterized with electrical measurements. In Section 9.3, we discuss possible microscopic origins for the individual electrical effects.

9.2 Electrical Impact of Traps on MOSFET Characteristics

It is rather obvious that point defects at or near the SiC/SiO_2 interface have a potentially detrimental impact on the performance and reliability of SiC MOSFETs. However, it is difficult to draw a connection between a group of electrically active point defects to a certain electrical effect in state-of-the-art MOSFETs. Here, we list a handful of electrical effects which can be described independently and can be assigned to a group of electrically active point defects.

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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9.2.1 Sub threshold Sweep Hysteresis

The subthreshold sweep hysteresis has been found in 2016 by comparing the transfer characteristic (drain current–gate voltage ($I_D V_G$)) of trench SiC MOSFETs measured with upward vs. downward gate voltage sweep direction [3], see Figure 9.1. It occurs only if the upward sweep starting gate voltage is a few volts negative and thus at the onset of the accumulation of holes at the interface. When the gate bias is then swept into the positive direction to turn on the transistor, a small drain current starts to flow already at negative gate biases. This also leads to a small but measurable drain current at zero volts gate bias [2]. However, when staying at zero gate bias after a previously negative gate bias phase, the drain current slowly decreases and eventually vanishes completely, as can be seen in Figure 9.2. When continuing the gate bias sweep to more positive voltages, the difference between up- and downward sweep vanishes nearly completely. The remaining few mV hysteresis at positive gate biases can be attributed to the charging/discharging of oxide defects, similar to what has been measured two decades ago on SiC metal oxide semiconductor capacitors (MOSCAPs) [4].

The amount of SH depends strongly on the sweep starting voltage, as depicted in Figure 9.3. The larger the negative sweep starting bias, the larger the hysteresis, until a saturation level below approximately −15 V. When defining a small drain current level for a V_{TH}^{sub}, one can use the oxide capacitance to calculate a number of charges at the 4H-SiC/SiO_2 interface as $N = C_{ox}\Delta V_{TH}^{sub}/q$, where q is the elementary charge. It is found that the number of charges leading to the few volts of SH is in the range of 10^{12}cm^{-2}. The same effect occurs on Si-face (planar) and a-face (trench)

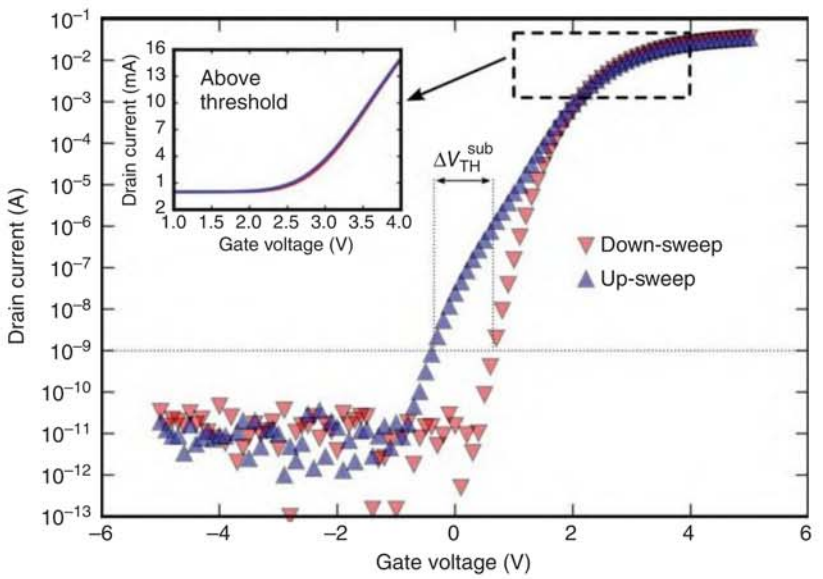


Figure 9.1 Example for the sub-threshold sweep hysteresis (SH) for a sweep starting gate voltage of −5 V. The inset shows that above the V_{TH} the hysteresis is negligibly small [3].

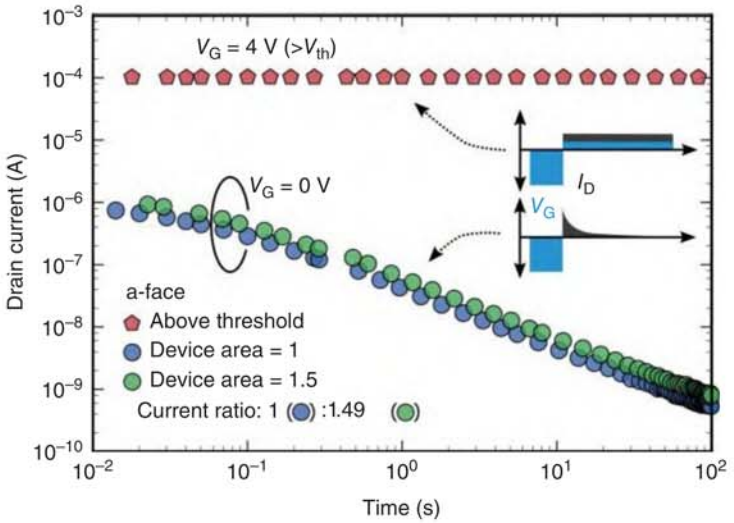


Figure 9.2 At the V_{TH}, the drain current shows negligibly tiny transient variations. At 0 V, after a negative gate bias pulse, the drain current decreases slowly over time. The current scales with the device area, indicating a uniform distribution of the drain current on the whole device area [3].

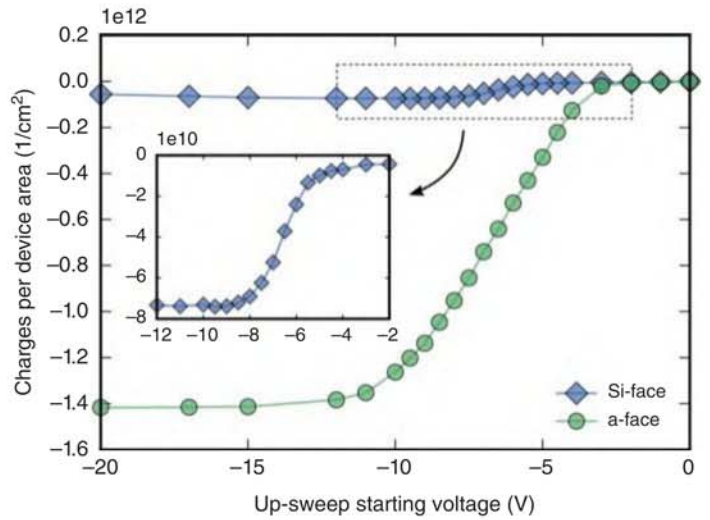


Figure 9.3 Dependence of the amount of SH on the upward-sweep starting voltage for silicon (Si)-face (planar) and a-face (trench) MOSFET devices [3].

MOSFET devices but is about ten times larger on trench MOSFETs. This finding is fairly independent of the manufacturer and its particular technology, as depicted in Figure 9.4.

SiC MOSFETs are often used in half-bridge configuration where the gates of the two transistors are switched with e.g. 50kHz. When the low level of the gate signal

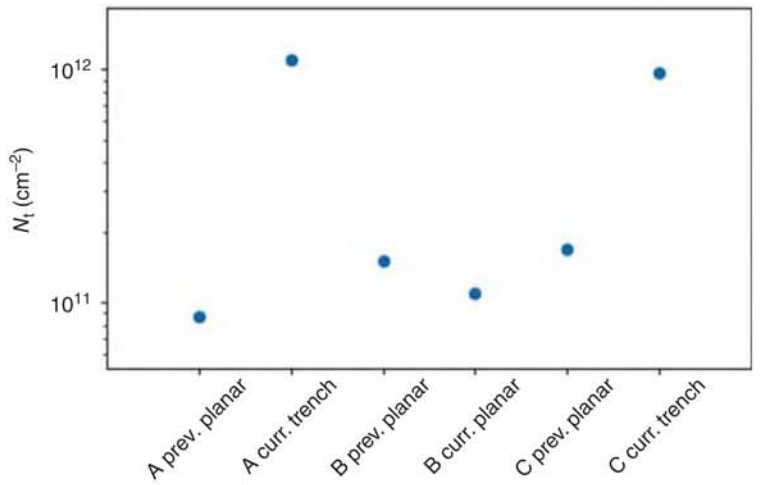


Figure 9.4 Comparison of the amount of SH for different manufacturers (A, B, and C), their current (curr.) and previous (prev.) generation, and whether the device technology is planar (Si-face) or trench (a-face) [5].

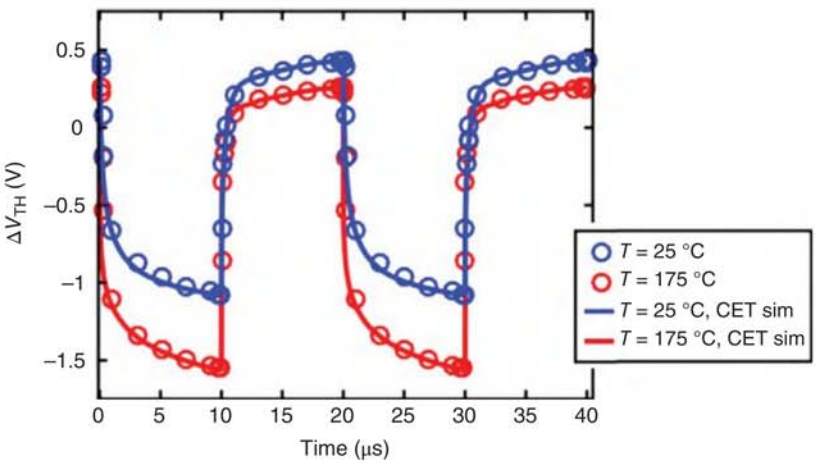


Figure 9.5 Evolution of the ΔV_{TH} during the application of a bipolar alternating current (AC) signal on the gate between −5 and 25 V [6]. Symbols are measurements, lines are calculations from the corresponding capture-emission time (CET) map.

to drive the transistor in off-state is negative, the actual V_{TH} of the device varies a few volt in these small time frames [6], see Figure 9.5. In order to measure this effect, a dedicated setup which switches from the applied gate voltage to a quick V_{TH} measurement and back within less than 1 μs is needed [6]. Then, the charging and discharging of the traps within μs and ms can be seen. Figure 9.6 shows the change of V_{TH} during a negative gate bias application as well as right after this period at a positive gate voltage close to the V_{TH}. Independent of the duration of the negative

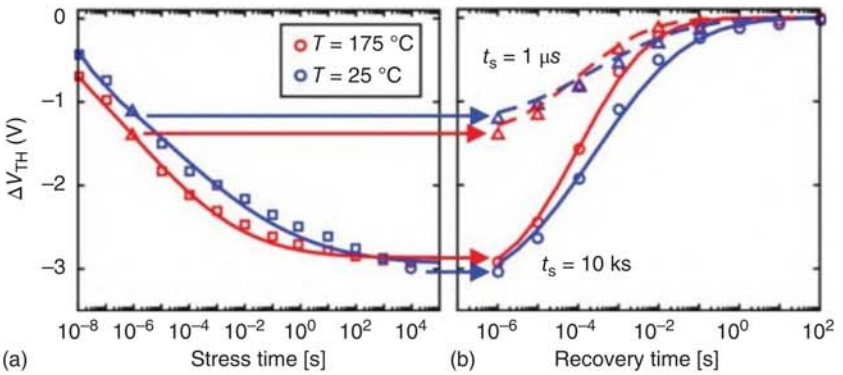


Figure 9.6 (a) Decrease of the V_{TH} by the application of a negative gate bias of −5V. (b) Recovery of the V_{TH} shift by the application of the V_{TH} voltage at the gate. No matter if the negative bias has been applied 1 µs or 10 ks, the V_{TH} variation vanishes after about 100 ms [6].

bias applied to the gate (1 µs or 10 ks in Figure 9.6), the negative V_{TH} shift vanishes after about 100 ms at the V_{TH}.

The time and voltage dependence of this charging and discharging processes can fully be modeled and calculated employing the concept of capture-emission time (CET) maps [6, 7]. A large number of traps all having the same electron capture time constant τ_c would cause a drain current transient of the form

$$I_D(t) = I_{D,0} \exp\left(-\frac{t}{\tau_c}\right) \tag{9.1}$$

thus giving a single exponential transient which would span over about two to three decades in time. The experimentally observed transient (as depicted in Figure 9.6b) spans over about four to six decades. Therefore, it cannot be due to a single capture time constant but has to have a wider distribution of capture time constants. This distribution of time constants can be obtained by performing an multi exponential analysis (MEA) on the drain current transient data (see also Section 9.2.3). The resulting density function of the number of traps with a certain capture time constant can be displayed vs. the density of the emission time constants from the inverted process. The resulting contour map is thus a different way to display the transient behavior of a SiC MOSFET at negative gate voltage and is called a CET map. It essentially gives the number of charges with a certain capture and emission time constant. A particular measurement procedure compiles to a certain occupation of the CET map [8]. The easiest example being a finite stress duration at negative gate bias and subsequent readout at the V_{TH} is a rectangular integration of the CET map of the lower right corner [7]. The perfect agreement between experiment and CET map-based simulation in Figures 9.5 and 9.6 (circles are experimental values and lines are the corresponding calculation/simulation) is nearly obvious, indicating solely the correct derivation of the CET map from previous measurements. However, having obtained the correct CET map, any arbitrary gate bias evolution can be input and the resulting change of the V_{TH} be calculated. This allows to calculate

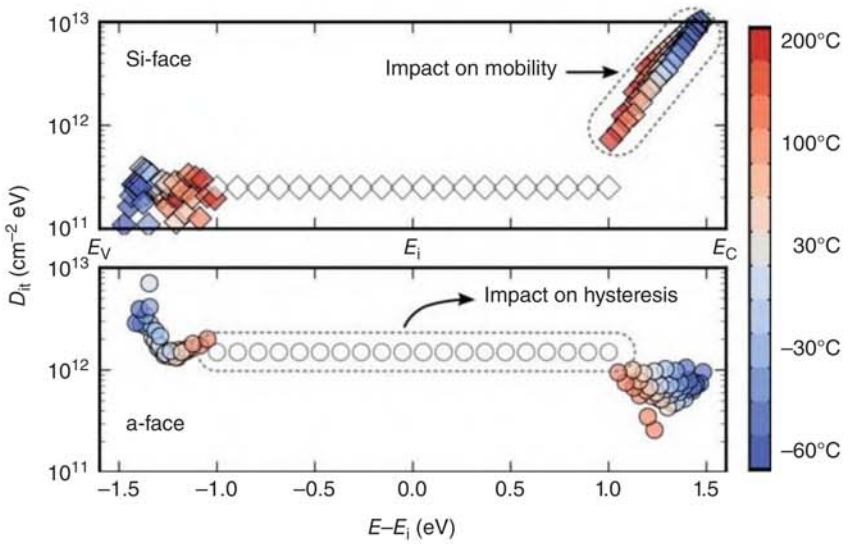


Figure 9.7 Density of interface traps for similar planar (top) and trench (bottom) SiC MOSFETs [3].

and model the fast transient behavior of the V_{TH} for various application scenarios and the actual V_{TH} value can be determined at every time instance [9].

To understand the reason for the observed SH and fast V_{TH} transient, further physical analysis have been performed. The ten times larger SH effect on a-face devices compared to Si-face devices has been investigated by employing charge pumping (CP) measurements [3]. Figure 9.7 shows the density of interface traps D_{IT} for the two device types obtained by spectroscopic CP at temperatures ranging from −60 to 205 °C. Si-face devices have a small D_{IT} near the valence band edge E_V and around mid-gap and a large increase toward the conduction band edge E_C. a-face devices do not show the increase toward E_C but have an increased density around mid-gap. This larger mid-gap density is attributed to the occurrence of SH. By applying negative biases to the gate, the Fermi level gets close to E_V which can charge these interface traps positively, resulting in shift of the V_{TH} toward negative infinity. The large increase of the D_{IT} toward E_C for the Si-face device can explain the reduced apparent channel mobility of these devices compared to a-face devices (see Section 9.2.4 for details).

Further investigation of the SH revealed even more interesting physical details to the charging/discharging effect [10]. By analyzing the decrease of the drain current over seven decades in time, it could be proved that electron capture into interface traps obeying the Shockley–Read–Hall (SRH) theory is the physical reason for this effect. The maximum amount of chargeable interface traps could be determined to be $4.2(1) \times 10^{12}\text{cm}^{-2}$. The distribution of time constants spans over 3.7 decades in time and has a capture cross section of $2.5(3) \times 10^{-19}\text{cm}^{-2}$. The extraction of these parameters allows for consistent inclusion of this dynamic trapping process into device simulations.

9.2.2 Preconditioning Measurement

Having understood the electrical effects due to continuous charging and discharging of interface traps from the Section 9.2.1, the need for adapted measurement procedures, different from those developed for Si technology, becomes evident for the throughout characterization of 4H-SiC MOSFETs. While measurement procedures for Si-based MOSFETs had been standardized by a few organizations several decades ago, new standards for SiC-based devices are under development e.g. in the JEDEC Solid State Technology Association (see www.jedec.org).

A very promising approach to differentiate between recurring charging/discharging processes of interface traps and the creation of new traps has been proposed recently [11]. The heart of the approach is a specific evolution of the bias applied to the gate as depicted in Figure 9.8, together with instructions concerning the voltage applied to the drain and rough timing specifications. The first pulse to negative gate voltages (marked red in Figure 9.8) drives the MOSFET into accumulation, and thus, charges interface traps positively. The measurement of the threshold voltage directly after (n_0) measures thus a very small or even negative V_{TH}. Afterwards, a positive preconditioning pulse, larger than the V_{TH}, is applied to invert the SiC in the channel region and bring the interface traps back to a neutral charge state. p_0 gives a V_{TH} value close to the real V_{TH} of the device because the interface traps are neutral during normal operation around the V_{TH}. This positive preconditioning pulse is a minimum requirement for a reproducible V_{TH} measurement and has to be done prior to every V_{TH} measurement. Before the stress phase, a sweep of the gate voltage may be performed to obtain the full transfer characteristic of the device. After the stress, the same measurement procedure is applied again, leading to the two threshold voltage values n_1 and p_1.

The impact of the stress phase can now be separated between a change of the V_{TH} and a change of the SH. For the change of the V_{TH}, one best uses the shift

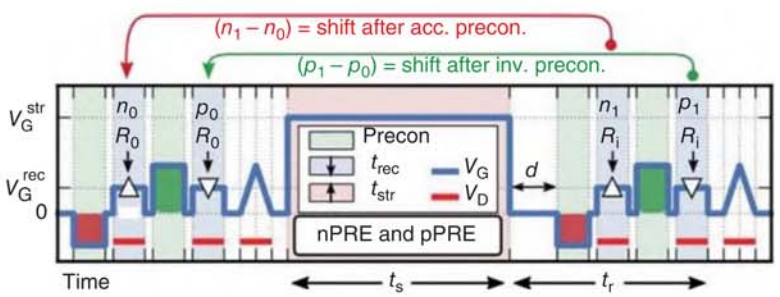


Figure 9.8 Evolution of the voltage applied to the gate (V_G) and drain (V_D) with respect to the source for a preconditioning measurement [11]. V_G^{rec} and V_G^{str} are the gate voltages for recovery and stress phases, respectively. With this approach, the impact of the stress phase can measured with preconditioning after an accumulation phase (acc. precon., negative gate bias) or after an inversion phase (inv. precon., positive gate bias).

after positive preconditioning ($p_1 - p_0$), since p_0 and p_1 are very independent on the timing of the measurement. These values are easier to measure and easier reproducible than n_0 or n_1. The amount of SH can be obtained before ($p_0 - n_0$) and after the stress ($p_1 - n_1$). The difference between these values (ΔSH) indicates a change of the amount of interface traps due to the stress phase. An example result of constant gate bias stress of 5 MV/cm is compared to conventional JEDEC Solid State Technology Association (JEDEC)-like measurements (similar to what is defined in the JEDEC **J**ESD241 document) in Figure 9.9. The comparison reveals that JEDEC-like measurements, as they had been developed for Si-based MOSFETs, do not properly account for the charge state of interface traps and overestimate the amount of threshold voltage shift for 4H-SiC MOSFETs. Using the preconditioning measurement approach, it is revealed that a large fraction of the shift which is observed in the standard JEDEC test is a recurring charging/discharging process of interface traps which cannot be accounted as degradation of the device.

Another key benefit of the method is that arbitrary delays between the end of the stress and the readout of the V_{TH} shift (time duration d in Figure 9.8) become irrelevant. This is especially beneficial in an industrial environment, where delay times between e.g. a minute and the duration of a weekend may occur. Figure 9.10 displays the dependence of the threshold voltage shift on the recovery time for different measurement approaches. JEDEC-like measurements show a large dependence on the recovery time (cf. lines with JED in Figure 9.10). The V_{TH} measurements after a negative preconditioning pulse do have a time dependence (green lines in Figure 9.10) but it cancels out when the time delay is the same before and after stress

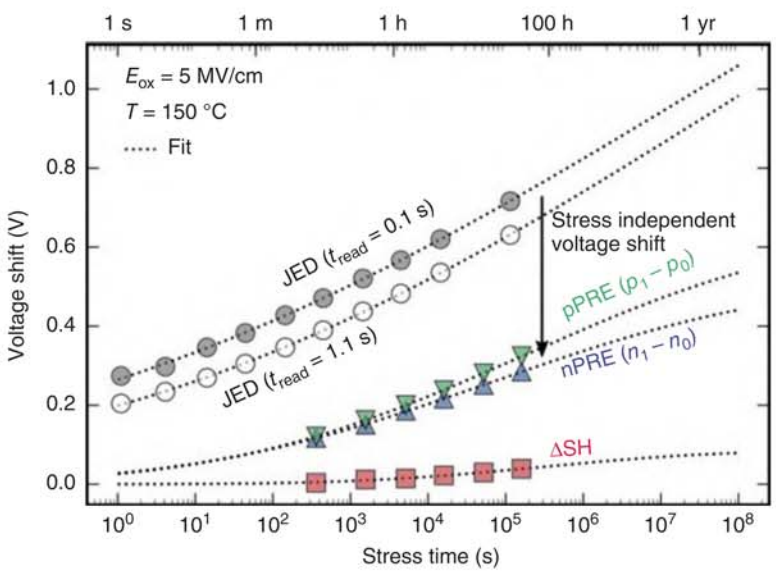


Figure 9.9 Voltage shift of a SiC–MOSFET due to constant gate bias stress [11].

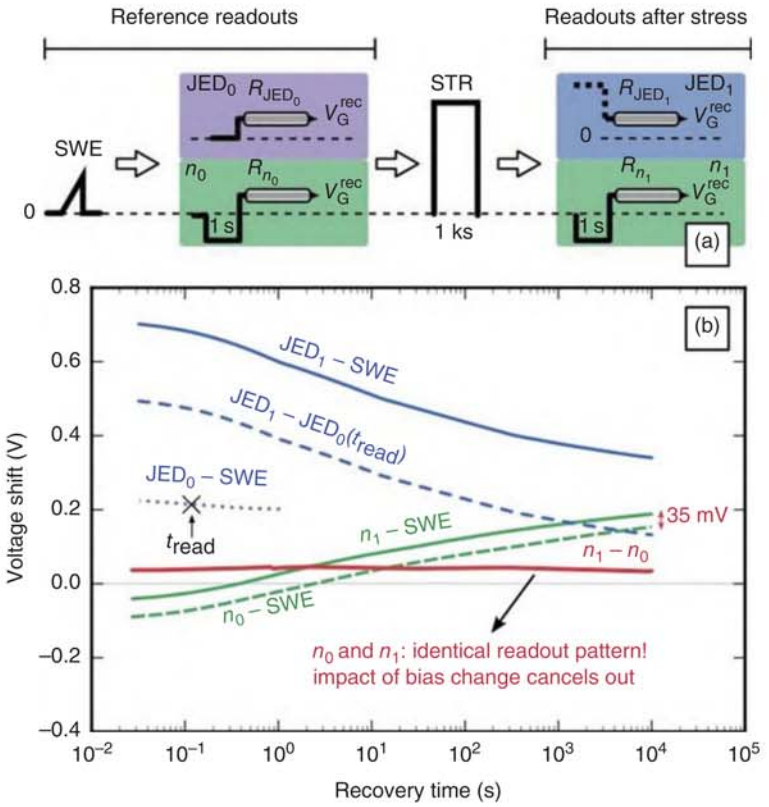


Figure 9.10 (a) Measurement procedures and (b) their corresponding dependence of the threshold voltage shift on the recovery time [11].

(red line in Figure 9.10). As such, ensuring always the same time delay (it may also be as large as e.g. 10 ks ≈ 3 h) is sufficient to obtain reproducible voltage shift results.

9.2.3 Bias Temperature Instability

With the aforementioned preconditioning measurement procedure, the drift of the threshold voltage under positive bias temperature stress (PBTS) or negative bias temperature stress (NBTS) can be cautiously characterized. The positive and negative preconditioning pulses are therefore applied before and after a bias temperature stress (BTS) phase of a certain duration and temperature and give the impact on the V_{TH} as well as a possible change of the SH. Figure 9.11 depicts an exemplary drift as a function of stress time. The change of the V_{TH} depends approximately logarithmically on the stress time for the given durations and is nearly independent of the preconditioning pulse polarity. The change of the SH is about an order or magnitude smaller.

The apparent logarithmic dependence of the ΔV_{TH} on the stress time is a result of the broad distribution of activation energies of point defect

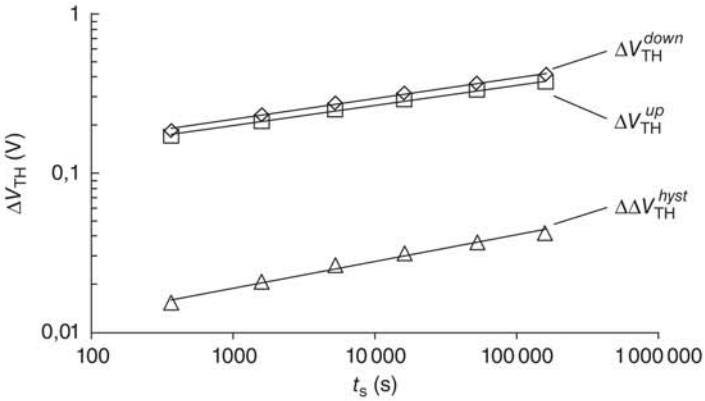


Figure 9.11 Drift of the threshold voltage over BTS time. $\Delta V_{TH}{}^{down}$ denotes the change of V_{TH} after a positive preconditioning pulse and $\Delta V_{TH}{}^{up}$ after a negative one. $\Delta\Delta V_{th}{}^{hyst}$ is the change of the SH [2].

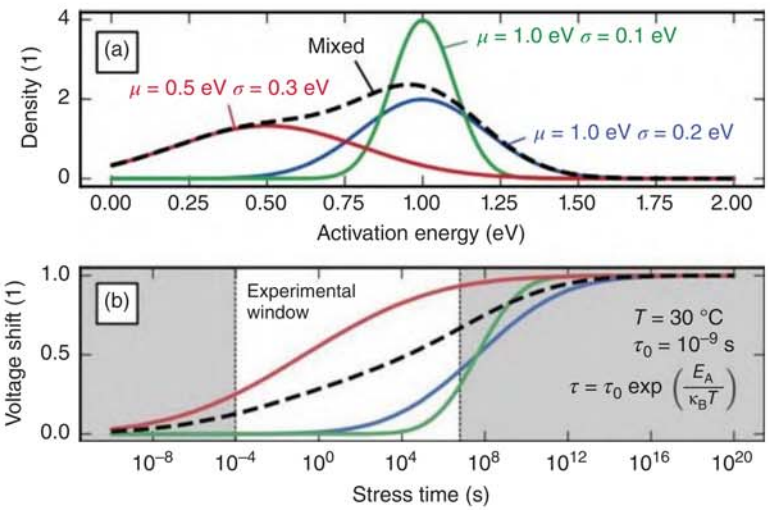


Figure 9.12 (a) Calculated probability density function over activation energy. Green, red, and blue are hypothetical normal distributions which sum up to the black dashed line. (b) The resulting time dependence of the V_{TH} shift for the different distributions. Highlighted is the typical experimental window for electrical measurements.

charging/discharging/creation processes in the dielectric at or near the interface to SiC. Figure 9.12 depicts an assumption of the distribution of activation energies and the resulting time dependence of the V_{TH} shift. The resulting ΔV_{TH} transients appear logarithmically dependent on the stress time within narrow experimental windows.

To calculate the result of charging processes of individual point defects, a number of physical models are needed. The most basic idea is that a point defect can be in two charge states: either neutral or charged. A defect whose charged state is

positive is called donor-like defect, one with a negative charge state acceptor-like. The second important assumption is that the state of the defect is only dependent on its current state and not any previous states (Markov chain of first order). These two simple assumptions result in an exponential function of the time dependence of the probability of having the defect in one charge state as $p(t) \propto \exp(-t/\tau)$ [12]. The characteristic time constant τ for a Markov process is calculated from the transition rates (probability per unit time) from one charge state to the other. For physical or chemical processes, the time constant τ is inversely proportional to the reaction rate constant which quantifies the rate of a given chemical reaction. In our case, the chemical reaction is the possible rearrangement of the amorphous network of Si and oxygen (O) (or potentially other elements) surrounding the point defect in SiO_2. Exactly, this rate constant obeys Arrhenius' law and thus the time constant is temperature activated as

$$\tau = \tau_0 e^{\frac{E_A}{k_B T}} \tag{9.2}$$

The measured ΔV_{TH} transient is the result of a superposition of a large number of single exponential functions and the superposition can be easily calculated by summing the individual components. The inverse problem, the identification of the underlying distribution of time constants from the resulting transient is called multi exponential analysis (MEA) and is an important and challenging problem for many different scientific fields [13]. This inverse problem has a unique solution only in the case of zero noise, id est (latin, read as *that is to say*) (i.e.) for real-world measured transient data there is no unique solution [14]. Some parameters of the distribution of time constants have to be assumed and still only an approximation of the distribution can be derived. Important methods to perform MEA can be found in these references [13–18].

The identification of the point defect in the SiO_2 which causes the bias temperature instability (BTI) cannot be easily performed from ΔV_{TH} transient data alone. Due to the broad distribution of time constants, it is difficult to study the temperature dependence of an individual time constant which would allow an Arrhenius analysis and thus the identification of the activation energy. To identify single defects, the active area of the MOSFET has to be around 100 nm × 100 nm such that the impact of a single charge on the drain current is sufficiently large [19]. Such small devices exist for Si technology where the charging/discharging processes have been extensively studied employing time-dependent defect spectroscopy [20, 21]. For SiC, such small devices do not exist yet. But without the basic information of the barrier energy for the defect charging process, it becomes nearly impossible to compare with ab initio calculations of defects in SiO_2. For the time being, one has to assume that similar defects are responsible for BTI in both Si- and SiC-based MOSFETs. Further discussion on this topic can be found in Section 9.3.3.

9.2.4 Reduced Channel Electron Mobility

The mobility μ of electrons in a semiconductor is the proportionality factor between the electric field and the electron drift velocity. For bulk 4H-SiC, the mobility may

have values between 10^2 to 10^4 cm^2/V s, depending on the doping level and the temperature [22]. For all semiconductors, the mobility decreases with increasing impurity concentration (because of increased scattering probabilities [1]) and with increasing temperatures (increased phonon scattering [1]). A typical value for the bulk mobility of 4H-SiC (at room temperature and for a typical doping level of 10^{17} cm^{-3}) is around 700 cm^2/V s [22], measured by employing the Hall effect.

For MOSFETs, the channel electron mobility is usually calculated by fitting the output characteristic of the MOSFET in the linear regime (small V_D) employing

$$I_D = \frac{W}{L}\mu_{FET}C_{ox}\left(V_G - V_{TH}\right)V_D \tag{9.3}$$

where I_D is the drain current, W and L are the MOSFET channel width and length, respectively, μ_{FET} is the MOSFET channel electron mobility, C_{ox} is the oxide capacitance, V_G is the voltage at the gate, V_{TH} is the threshold voltage, and V_D is the drain voltage. A peculiarity of SiC is a heavily reduced electron mobility in the MOSFET channel, down to values as low as 10^{-3} cm^2/V s [23]. With such low μ_{FET} values, it would be unreasonable to build a power MOSFET because the resulting $R_{DS,on}$ would not be competitive with available Si-based transistors (especially insulated gate bipolar transistors [IGBTs]).

The apparent strong reduction of μ_{FET} is only to a tiny part due to a reduction of the actual electron mobility itself [24–26]. In fact, the free electron density n_{free} decreases through trapped electrons, which reduces the drain current of the transistor. Since the free electron density is not considered in (9.3) the reduction is caught by μ_{FET} as a fitting parameter. To separate between MOSFET channel mobility and free carrier density, Hall effect measurements are most useful. But also the fitting of the transfer characteristic of the MOSFET under the assumption of a particular energetic distribution of the interface trap density allows to obtain n_{free} and μ independently [24, 27].

By using an POA after the oxidation (or deposition) of SiO_2 in nitrogen (N) containing atmospheres, the MOSFET mobility is increased to values ranging from 10^1 to 10^2 cm^2/V s. Typical gases for the POA are nitric oxide (NO), nitrous oxide (N_2O), and ammonia (NH_3), usually mixed with dinitrogen (N_2). N_2 alone normally does not lead to significant improvements in the MOSFET mobility. Most efficient is usually the annealing in NO at temperatures around 1150 °C [28].

The particular reasons for the remaining reduction of the channel electron mobility beside the effect of the n_{free} reduction are still under debate [29]. The decreased mobility values in Hall measurements could be due to a natural reduction of the interaction of channel electrons with acoustic phonons, ionized impurities, and other known physical effects [1]. However, the impact of the mobility change is very small compared to the impact of the n_{free} reduction and is thus not of utmost importance. The overall topic of an increased $R_{DS,on}$ because of the two effects remains, however, of very high importance, because the channel resistance is the part of the MOSFET where most improvement is possible. Solving this issue would allow to build competitive SiC MOSFETs for the voltage class below approximately 1.2 kV [30].

9.3 Microscopic Nature of Electrically Active Traps Near the Interface

The electrical effects mentioned in Section 9.2 all occur due to charging/discharging/creation processes of point defects near the SiC/SiO_2 interface. Here, we give an overview about the research toward the identification of the microscopic composition and nature of these defects. In the following, we will formulate hypotheses for likely defect candidates for each aforementioned electrical effect.

9.3.1 The P_{bC} Defect and the Subthreshold Sweep Hysteresis

The SH effect in SiC MOSFETs has been summarized in Section 9.2.1. In order to identify the microscopic defect responsible for the SH effect, electron paramagnetic resonance (EPR) experiments have been combined with ab initio density functional theory (DFT) calculations [23, 31].

EPR employs the Zeeman effect: the energy level of an unpaired electron splits in a magnetic field into two levels. If the energy difference between these two levels is exactly matched by electromagnetic radiation, a resonance condition occurs. Because the local magnetic field at a nucleus is also impacted by neighboring nuclei, one can draw conclusions on the structure of the surroundings of the electron (hyperfine interaction). Conventional EPR experiments give information of all paramagnetic centers within a sample. This is naturally a weakness of the method for the investigation of defects in MOSFETs because the SiC/SiO_2 interface region is only a few nm thick compared to the several orders of magnitude larger sample thickness. Furthermore, the method cannot easily be applied to fully fabricated MOSFETs because the metal layers lower the quality factor of the standing electromagnetic wave in the resonator cavity.

Employing electrically detected magnetic resonance (EDMR) instead of EPR can circumvent these problems. Using EDMR, the current through the transistor changes due to the resonance condition and gives a similar defect fingerprint as in an conventional EPR experiment. The signal is, however, only due to carrier recombination centers at the SiC/SiO_2 interface and is insensitive to centers energetically close to the valence or conduction band edges. The method thus gives information on defects responsible for the SH but not those which limit the MOSFET mobility.

As already stated in Section 9.2.1 (and depicted in Figure 9.7), the larger SH effect in trench MOSFET devices compared to planar devices can be attributed to a larger density of interface traps around mid-gap for a-face compared to Si-face. Consistently, also the EDMR signal was generally larger for trench MOSFET devices compared to standard planar devices. This supports the argument that interface traps energetically close to the center of the band gap cause the SH effect.

For full identification of the defect causing the SH effect, a significant increase of the signal-to-noise ratio for EDMR experiments was important to allow for reasonable resolution of the hyperfine side peaks. This could be reached by employing the

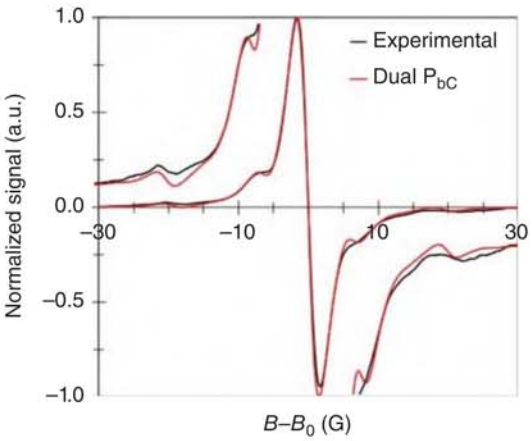


Figure 9.13 Example normalized EDMR spectrum with zoomed in lines for better visibility of the hyperfine side peaks at about ±7G and ±20G. The red line is a simulated spectrum for dual-P_{bC} [31].

bipolar amplification effect (BAE) [32]. Figure 9.13 gives an example EDMR spectrum of SiC MOSFET with the resolved hyperfine peaks.

The hyperfine peaks are of particular importance because they allow for a direct comparison with DFT calculations. For the identification, several steps were needed. First, a defect-free interface model was designed, as depicted in Figure 9.14. This is possible because in the case of the Si-face of 4H-SiC, there exists a connection scheme for an ideal interface to SiO_2 [33]. Into this model, all possible point defects near the SiC/SiO_2 interface were introduced, including all sorts of vacancies, interstitials, anti-site pairs in SiC, and their variants with neighboring nitrogen atoms. From all these possible defect candidates, a short list was created by removing all defects with unreasonably large formation energy. These remaining defects were investigated in more detail and their average hyperfine splitting was calculated. By calculating the relative intensity of the peaks based on the isotopic abundance of the spin active nuclei, the EDMR spectrum can be calculated and compared to the experimental observation (red vs. black line in Figure 9.13).

The occurrence of the hyperfine side peaks at the same magnetic field value is a very strong indication that the P_{bC} defect family [23, 31, 34, 35] is responsible for a recombination current in SiC MOSFETs. However, there is an indication that the type of interface defect visible in EDMR is process dependent, because variants of the defect have been identified, namely the silicon vacancy near the interface [36] and the carbon P_b center [37]. However, this does not exclude even more defects or other defect types to cause recombination processes at the SiC/SiO_2 interface, since they could be not paramagnetic and thus simply not visible in the EPR experiment.

9.3.2 The Intrinsic Electron Trap and the Reduced MOSFET Mobility

A summary about the smaller MOSFET mobility compared to the bulk electron mobility has been given in Section 9.2.4. The majority of the apparent reduction of the MOSFET mobility is a misinterpretation because of the reduced free electron density in the MOSFET channel. Here, we summarize the hypothesis that the microscopic defect causing the large number of trapped electrons close to the channel is

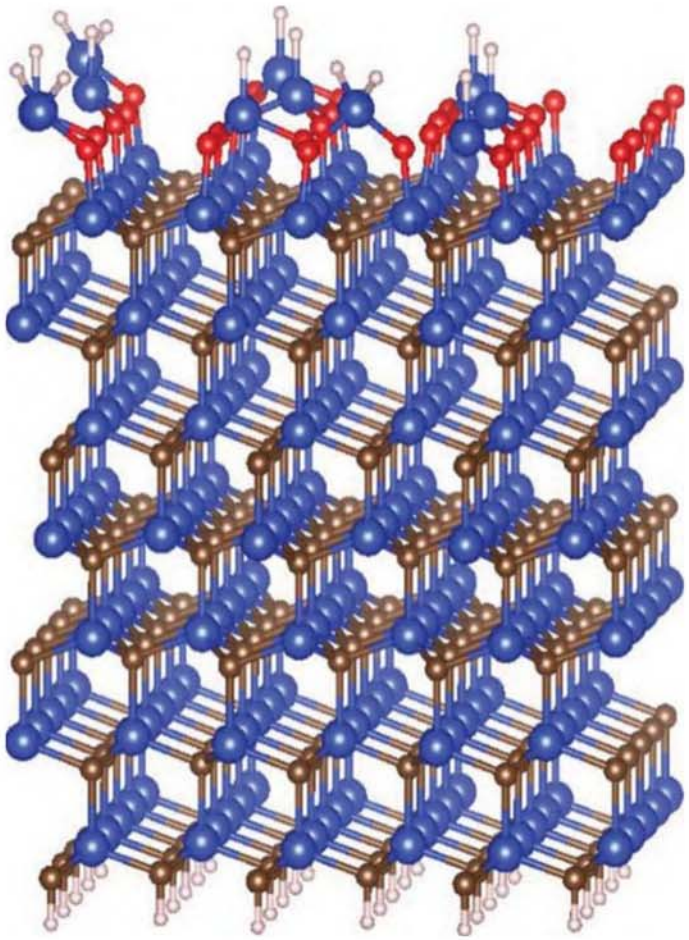


Figure 9.14 Atomistic model of 4H-SiC with one layer of SiO_2 on top.

the intrinsic electron trap in amorphous SiO_2 [38], favored against other defects as e.g. the Si_2–C–O structure [39].

Ab initio calculations of amorphous silica SiO_2 revealed trapping of an electron in preexisting structural precursors. The precursor sites are characterized by wide (greater than 130°) O–Si–O angles. These sites can occur randomly distributed in the SiO_2 network because of distributions of bond angles and lengths in the amorphous crystal, resulting in a density of approximately $5 \times 10^{19} cm^{-3}$. The calculated energetic trap level is approximately 3.2 eV below the bottom of the conduction band of SiO_2 [38]. Figure 9.15 shows an example for the spin density upon charge capture of an intrinsic electron trap.

The intrinsic electron trap can be correlated especially with experimental findings which had utilized photon stimulated electron tunneling [40]. Therefore, the energy difference between the trap level and the SiO_2 conduction band edge was determined by optical excitation of the trapped electrons under an applied electric field. The

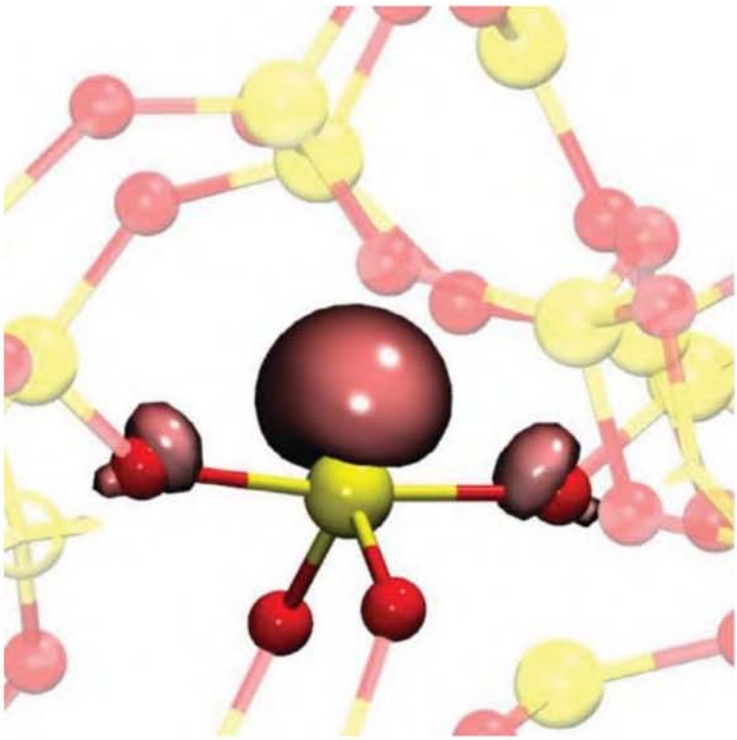


Figure 9.15 Charged intrinsic electron trap with the spin density of the trapped electron (Si atoms yellow, O atoms red).

value for the trap energy level was determined as 2.8 eV. Specifically, the energy level is independent of the underlying semiconductor material (4H-SiC, 6H-SiC, or even Si). This is a strong argument for the intrinsic electron trap, since other defect candidates, like e.g. the Si_2–C–O structure, involve carbon and are thus very unlikely to occur in Si–SiO_2 structures.

The experimental trap energy level is 2.8 eV and thus smaller than the theoretically suggested value of 3.2 eV. However, calculations also show that the trap energy is significantly smaller for crystalline α-quartz (2.5 eV). As such, the strained environment for this defect in SiO_2 close to the interface a semiconductor may cause a different energy trap level, besides a possibly increased density [41]. Mind that the conduction band edge of 4H-SiC is 2.7 eV below the conduction band edge of SiO_2 and thus populating the intrinsic electron trap works most efficient for 4H-SiC compared to other SiC poly types or other semiconductors.

9.3.3 Point Defect Candidates for BTI

Research concerning bias temperature instability (BTI) in SiC MOSFETs benefits from the research previously performed for Si-based MOSFETs. However, also for Si-based MOSFETs the exact microscopic point defect causing BTI has not yet been

unambiguously identified, but many candidates exist. In Si MOSFETs, the only defect type which is unambiguously created during BTS is the dangling bond on a Si atom at the Si–SiO_2 interface (P_b center) [42–46]. It becomes most probably created through dissociation of a neutral hydrogen atom passivated dangling bond on a silicon atom at the silicon-silicon dioxide interface (P_bH complex). The identification was done by performing EDMR measurements before and after BTS.

However, for SiC MOSFETs, the similar defect type P_{bC} is not changed in its density through NBTS [47]. Even more, the EDMR signal did not change at all despite a very large change of the V_{TH}, thus indicating that the defects charged or created during NBTS in SiC MOSFETs are not spin dependent. This is again similar to Si MOSFETs where EDMR after NBTS shows only the increase of the P_b signal, but no other additional defect has been unambiguously identified. Few reports claim signatures of a dangling bond on a silicon atom bonded to three oxygen atoms within the silicon dioxide (E′ center) after NBTS [42].

As no direct evidence of the defects created through NBTS appears possible as they could be diamagnetic, alternative approaches have to be employed. For Si MOSFETs, a very promising approach has evolved in recent years by studying the charge state of individual defects. In nanometer-sized devices, the change of the V_{TH} due to BTS occurs in discrete steps of several millivolt [48]. The step height is a fingerprint of a particular defect in the device because of the lateral distribution of the current through the transistor and the individual impact of a single defect charge state on the overall current [49]. Because of this possibility to identify the response of a single defect on temperature, time, and bias, the time dependent defect spectroscopy (TDDS) can give physical properties of the defects contributing to BTI. These properties, such as the barrier energy for charging/discharging or its charge transition level with respect to the valence and conduction band edges, may then be compared to the results of ab initio calculations employing DFT.

One important property which has been found for defects contributing to BTI in Si MOSFETs is the bistability in every one of the two charge states. This means that there have to exist at least two configurations in e.g. the neutral charge state, where only one of the two configurations allows a transition to the say positive charge state [50]. This property of a defect leads to effects like temporarily activated random telegraph noise (RTN) during the recovery after BTS or the volatility of defects in repeated stress/recovery BTI experiments [51]. Since the bistability of the charge states has been observed consistently in Si-based MOSFETs, possible defect candidates have been screened to have more than two states (as well as a charge transition level close to the center of the SiO_2 band gap) [50]. The remaining candidates are the oxygen vacancy, the hydrogen bridge, and the hydroxyl E′-center [50, 52], where the latter is currently most promising. An example of the defect is given in Figure 9.16.

Considering the dynamics and overall behavior, BTI in SiC MOSFETs is similar to BTI in Si MOSFETs [53]. However, there are a few peculiarities and differences which have to be considered. The bistability criterion does not necessarily need to be important for SiC MOSFETs. This could render the list of possible defects for BTI in SiC MOSFETs much longer compared to Si MOSFETs. As such, it is important to

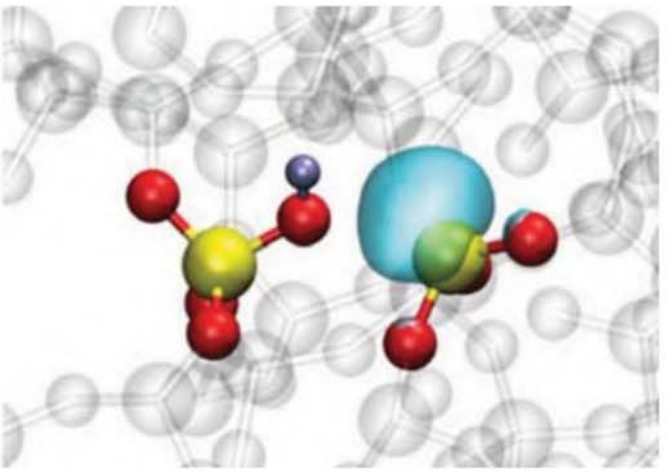


Figure 9.16 Example configuration of the hydroxyl E′ center in the neutral charge state [52]. Hydrogen, silicon, and oxygen atoms are silver, yellow, and red, respectively.

obtain physical properties of the defects contributing to BTI in SiC MOSFETs additionally to the information given from Si MOSFETs. Nanometer-sized devices are not yet possible with SiC technology, so the response of an ensemble of defects on BTS has to be analyzed (see also Section 9.2.3). The obtained BTI measurement data have to be modeled in a compact framework where the physical defect parameters are calculated individually but the computational effort is kept low by calculating the semiconductor/insulator system macroscopically. Such a simulator has been written and released [54] and has been applied to SiC MOSFETs [9]. The result reveals two electron and one hole trap band close to the conduction and valence band edges of 4H-SiC, respectively. The shallow electron trap band has thereby similar parameters as for Si MOSFETs, suggesting the existence of an electron trap intrinsic to SiO_2, just as previously submitted by DFT calculations alone (as described in Section 9.3.2). Given the complexity of deriving physical parameters of an ensemble of defects contributing to BTI, additional research is necessary to identify and eventually remove the defect responsible for V_{TH} shifts following BTS.

9.4 Conclusions and Outlook

It is obvious that the natural mismatch of the crystal structure between SiC and SiO_2 will naturally cause many different point defects near the interface of these two materials. Through improved high temperature processes, many of these defects have been completely removed or rendered electrically inactive, because their charge transition levels have been shifted outside the SiC band gap. It is, however, not obvious how these remaining electrically active defects impact the performance and reliability of MOSFET devices which employ the SiC/SiO_2 interface as the central element for electronic switches.

We think the effect of a hysteresis between the upward- and downward transfer characteristic sweep with negative start gate voltages is due to interface traps, energetically located close to the center of the band gap. A possible defect candidate for this effect is the P_{bC}, a dangling bond at a carbon atom directly at the interface. In order to have these interface traps in a defined charge state whenever the transistor is characterized by measuring the threshold voltage, the preconditioning measurement method should be used. Therefore, a preconditioning gate voltage pulse to deep accumulation or inversion is used to have most interface traps either charged positively or neutral, respectively. This allows to be able to study the impact of e.g. BTS with reliable and reproducible measurements. Investigating the instability of SiC MOSFETs due to BTS by using this measurement method reveals a very broad distribution of capture time constants, presumably due to a broad distribution of charging barrier energies of the individual defects. Several point defects may cause BTI in SiC or Si MOSFETs, but recently mostly discussed for Si is the hydroxyl E′-center.

The smaller MOSFET mobility compared to the bulk mobility value of SiC is due to a misinterpretation of the strongly reduced free electron density in the MOSFET channel. The majority of electrons are trapped and thus immobile and do not contribute to the drain current in unpassivated devices. A possible candidate for this effect is the intrinsic electron trap in SiO_2, wide angle O–Si–O bonds occurring naturally in the amorphous SiO_2 and eventually more frequent near the SiC/SiO_2 interface because of localized strain.

The summary gives only a few candidate point defects for different electrical effects in SiC MOSFETs. It cannot be a definitive answer on the nature of interface traps, as e.g. other recombination centers could be more prominent but are simply not paramagnetic. Also, even though BTI is comparable between Si and SiC MOSFETs, the defects responsible for BTI in SiC-based MOSFETs could be different from those in Si devices because of possibly carbon-related defects. As such, further research is needed to fully clarify the role of point defects near the SiC/SiO_2 interface for the operation of SiC-based MOSFETs.

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10

Epitaxial Graphene on Silicon Carbide as a Tailorable Metal–Semiconductor Interface

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10.1 Introduction

The discovery of monolayer graphene growth on silicon carbide (SiC) [1–4] provides a unique opportunity to rediscover the very fundamental concept of a metal–semiconductor interface [5, 6] providing an accurately defined structure with atomic precision. This chapter summarizes recent experiments and technological concepts that benefit from this exceptional monolithic material system. We start with a review of the formation of the graphene layer and its tailorable interface, and we continue by discussing the basic electronic functionality, which can immediately be used to define diodes, transistors, and electronic circuits. These devices open up opportunities to study the very fundamentals of semiconductor textbook physics in a new context, in particular, with unprecedented access to the high-frequency limit of electronic information processing. Key to these experiments is the optical transparency of graphene electrodes. This can further be exploited for solid-state quantum technology with SiC.

10.2 Epitaxial Graphene as a Metal

Graphene is an atomically thin material [7], the single layer version of the well-known material graphite. After its discovery, graphene attracted a lot of attention (including the Nobel prize 2010 in physics) because of its unusual quantum mechanical structure that roots in the honeycomb sp^2 lattice and its symmetry. Its electronic bands merge conically in six points at the edge of the Brillouin zone (Dirac cones) and, hence, graphene has no electronic bandgap, but is a (semi-) metal. A figure of merit in semiconductor technology, the charge-carrier mobility reached unprecedented values up to $10^6\,\mathrm{cm}^2/\mathrm{V\,s}$ in graphene flakes, which raised wishful fantasies with regard to this novel electronic material [8, 9].

For this manuscript, the special properties of the Dirac electrons (“relativistic electrons”) and the high mobility are unimportant, but we focus instead on the

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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simple fact that graphene is an atomically thin metal. Different to standard 3D metals, which are charge neutral in the bulk and can have excess charge only at their surfaces, graphene, being a surface-only material, can be entirely electron charged (n-type) or hole charged (p-type), but remains metallic.

10.3 Fabrication and Structuring of Epitaxial Graphene

10.3.1 Epitaxial Growth by Thermal Decomposition

It is known since the early days of SiC material research that heating SiC leads to a decomposition of the surface and the formation of graphitic structures [10, 11], which means sp^2 hybridized carbon. With the advent of graphene as an interesting atomically thin and truly two-dimensional material that is uniquely formed of sp^2 carbon [7, 12], an interest was raised to fabricate graphene on SiC single crystal wafers, both on their carbon face (C-face) [13, 14] and on their silicon face (Si-face) [3, 15]. While the results on the C-face are highly interesting, but did not result in a controlled monolayer growth, it turned out that the Si-face is perfectly suited for this purpose. A recent review is given in Norimatsu et al. [4]. When SiC(0001) is heated up to approximately 1100 °C under ultrahigh vacuum conditions, a decent local graphene monolayer growth can be observed, however, with rather rough surfaces that contain graphene islands, multilayer graphitic areas, voids, and structural defects [15, 16]. The problem under these conditions is that the silicon loss is fast and kinetically driven, but the remaining material remains far from annealing conditions and cannot reconfigure structurally. For the latter, higher annealing temperatures are required, but the silicon loss has to be balanced. The solution turned out to be the use of inert gas at ambient pressure during annealing, in particular argon (Ar). Under these conditions, the thermal decomposition of the SiC surface is slowed down kinetically and can be performed at approximately 1700 °C, which meets nicely the annealing conditions of SiC. The result is a nearly intact SiC bulk crystal with a sharp and atomically flat interface to a monolayer (or few layers) material that consists entirely of carbon on macroscopic or even wafer scales [3, 17]. The first grown layer is an atomically thin carbon layer that looks in top view like the honeycomb lattice of graphene.

A closer look, however, reveals that it has still out-of-plane bonds to the underlying Si atoms of the SiC crystal (among those Si atoms, there are numerous sites that are not saturated with carbon and provide dangling bonds, cf. Figure 10.1a). The carbon atoms of this so-called buffer layer have, hence, both sp^2 and sp^3 contributions [19]. As a consequence, the π electronic band typical for graphene is missing and this layer is therefore electronically insulating [15]. On top of this buffer layer, under appropriate conditions, a second layer is formed which is the desired pure sp^2 graphene layer. Its electronic band structure has been determined by angular-resolved photo electron spectroscopy (ARPES) [15]. Note that this graphene layer is not charge neutral; because of the electron-donating interface it is charged with a typical charge density of 10^{13} cm^{-2}, which corresponds to a Fermi energy of $\Delta E_F \approx 350$ meV above the

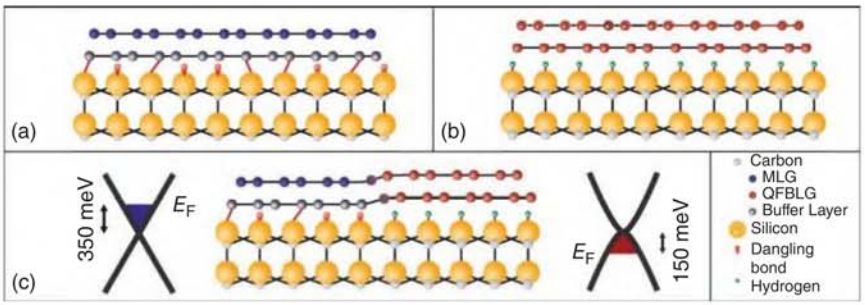


Figure 10.1 Scheme of epitaxial graphene on SiC. (a) Epitaxial graphene on SiC as obtained from thermal decomposition. The graphene layer (blue) is formed on top of an insulating carbon buffer layer (black). This material is negatively charged (n-type) and is termed monolayer graphene (MLG). (b) By high-temperature hydrogen treatment, the buffer layer is converted into a graphene layer, such that quasi-freestanding bilayer graphene (QFBLG) resides on the substrate. This material is positively charged (p-type). (c) Employing milder intercalation conditions, it is possible to fabricate both materials side by side in a closed sheet. This junction links n-type MLG with p-type QFBLG without interruption of the carbon layers. Values for E_F are deduced from Hall measurements under ambient conditions. Source: Reprinted with minor adaptions from Sorger et al. 2015 [18], license: CC BY 3.0.

Dirac point (see Figure 10.1c left). The charge carrier mobility at room temperature is typically limited to $\mu_e = 1000\,\mathrm{cm^2/V\,s}$. The mobility rises toward low temperatures to about $2000\,\mathrm{cm^2/V\,s}$, which corresponds to mean free paths of approximately 50 nm [3]. This limitation can be traced back to line defects in the graphene plane, more precisely stacking faults with respect to the underlying buffer layer [20, 21]. The temperature dependence of the mobility stems from electron–phonon interaction with particularly strong influence of the buffer layer phonons [22]. Significantly higher values of the mobility can be achieved when the open surface of graphene is chemically doped such that the charge carrier density approaches zero [23]. The described monolayer graphene (MLG) is atomically flat on atomically flat substrate terraces, which may be up to 3 µm wide and >100 µm long on nominally on-axis substrates. They are interrupted by substrate steps. There, interestingly, the graphene grows uninterruptedly like a carpet over the steps, with an additional graphene layer in vicinity of the step such that there, effectively, bilayers or even multilayers are observed [3]. Fabricating MLG means, therefore, creating a continuous layer of large area epitaxial graphene, which includes bilayer contributions of about 20%.

This fabrication is predominantly temperature controlled. The temperature can be chosen such that (nearly) exclusively buffer layer is produced. At somewhat higher temperatures, MLG is formed, and at even higher temperatures, bilayer graphene (BLG) can be fabricated. It should be mentioned, however, that the MLG process is most reliable; buffer layer growth is more critically dependent on a subtle choice of growth parameters and initial surface morphology.

10.3.2 Intercalation

Starting from MLG, the application of hydrogen at temperatures around 900 °C provides an interesting tool to modify the material. Initially applied to terminate the

dangling bonds, it turned out that hydrogen also cuts the covalent bonds between SiC and the buffer layer [24, 25]. The result is the conversion of the electrically inactive buffer layer into a truly sp^2 graphene layer, while additional graphene layers remain unchanged (see Figure 10.1b). This leads to the following conversion scheme: buffer layer only is converted to quasi-freestanding monolayer graphene (QFMLG), MLG is converted to quasi-freestanding bilayer graphene (QFBLG), and so on. The terminology of *quasi-freestanding* indicates that the interaction with the substrate is substantially released. In particular, the charge carrier mobility of the quasi-freestanding material is independent of the temperature; the electron–phonon scattering is suppressed [25]. Also, the negative charge induced by the buffer layer is removed; however, another mechanism becomes dominant. The static electric dipole moment of the hexagonal SiC crystal (absence of inversion symmetry) requires a positive termination of the surface and, therefore, charges quasi-freestanding graphene species with a hole density in the range of $(10^{12}–10^{13})\,\mathrm{cm}^{-2}$ [26], a typical value for the Fermi energy under ambient conditions is $\Delta E_\mathrm{F} \approx -150\,\mathrm{meV}$ below the charge-neutrality point (cf. Figure 10.1c right). Note that intercalation of this interface has turned out to be a rich research area in itself (see e.g. [27, 28]). Recently, even 2D metallic sheets have been stabilized as an interface layer [29, 30]. In the course of this paper, we consider only the "simplest" hydrogen intercalation, with which, however, striking effects can be demonstrated.

10.3.3 Structuring of Epitaxial Graphene Layers and Partial Intercalation

Starting with a continuous large-area graphene layer, device fabrication requires lateral structuring. An obvious strategy is to cover graphene with resists, in particular polymethyl methacrylate (PMMA) or photo resists, which is then patterned by electron beam or optical lithography. Unwanted graphene areas are subsequently removed by oxygen plasma etching at mild conditions. This technique has previously been applied to exfoliated graphene [31, 32] and epitaxial graphene on the C-face of SiC [14] and leaves the charge carrier mobility mainly unaffected. The resist materials can be nearly completely removed. However, even little resist residues can be problematic for specific applications if the graphene surface is key to functionality (e.g. sensors). Strategies to remove contaminations are described by Algara-Siller et al. [33] and Yager et al. [34].

While the lateral patterning of the graphene sheet is common to all graphene materials (e.g. exfoliated graphene, chemical vapor deposition [CVD] graphene [35]), a specialty of epitaxial graphene is the opportunity to tailor the epitaxial interface by intercalation. This intercalation can even be performed locally such that the electronic properties of a continuous graphene layer can laterally be varied (see Figure 10.1c). Conceptually, the intercalation process, which on the wafer scale was thermodynamically driven, must be controlled kinetically.

For this purpose, edges or voids are defined by lithography techniques [18, 36]. Under relatively mild conditions (approximately 500 °C), hydrogen cannot diffuse through the closed layer, but creeps underneath graphene from the predefined

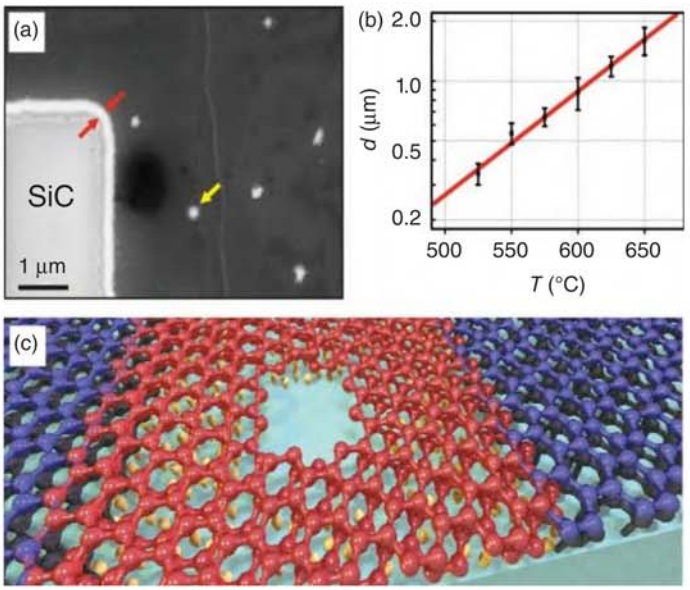


Figure 10.2 Partial intercalation of epitaxial graphene. (a) Scanning electron micrograph of a graphene edge exposed to hydrogen (530 °C for 30 min). The bright strip along the edge (indicated by red arrows) corresponds to locally intercalated graphene. The spots in the closed graphene areas (yellow arrow) indicate unintended conversion at pinholes. (b) Measurement of the intercalation width d as a function of temperature T for 90 minutes exposure time. An exponential dependence is observed indicating a temperature-activated process. (c) Artist's view of alternating n-type and p-type graphene stripes: the red layer indicates p-type QFBLG (hydrogen termination of the substrate in yellow). The blue layer represents n-type MLG with the buffer layer (black) underneath. Source: Reprinted with minor adaptions from Sorger et al. 2015 [18],, license: CC BY 3.0.

edges (see Figure 10.2a). The intercalation depth is then temperature controlled; application time is less critical (see Figure 10.2b). This technique allows for side-by-side fabrication of MLG and QFBLG on the very same chip and even within one continuous graphene sheet. Note that this offers the opportunity of graphene p–n junctions (p-type QFBLG and n-type MLG; sketched in Figures 10.2c and 10.1c), which differ, however, from semiconductor p-n junctions because graphene provides no electronic bandgap. Thus, graphene p-n junctions are essentially metallic with linear I–V characteristics.

10.4 Epitaxial Graphene as Tailorable Metal/Semiconductor Contact

In general, a metal/semiconductor contact forms a space-charge region, which originates from the different work functions of the metal and the semiconductor. As a consequence, a Schottky barrier is formed [6] providing nonlinear current–voltage characteristics through the interface. In the case of an n-type semiconductor, the Schottky barrier vanishes only if the metal's work function is smaller than that of the

semiconductor. This is the textbook case of a flat-band ohmic contact with linear I–V characteristics. The typical work function of SiC, which consists of the electron affinity ($\chi_{4H\text{-}SiC} = (3.4\text{–}3.6)\,eV$ or $\chi_{6H\text{-}SiC} = (3.85\text{–}4.0)\,eV$ [37–39]) and the Fermi energy $\Delta E_F = E_C - E_F$ (typical values ≈ 0.1 eV), is small. As a consequence, no flat-band ohmic metal/SiC contact is known (Schottky barrier heights of typical metal/SiC contacts range between 1.0 and 1.8 eV [40]).

As outlined earlier, graphene essentially behaves like a metal due to the absence of a bandgap. It turns out that epitaxial graphene being the combination of graphene, SiC and their common interface behaves very similarly to the metal/semiconductor textbook case. The fact that the metal is only atomically thin does not provide a conceptual change. The interaction between graphene and SiC is now controlled by the interface layer that has been described above as buffer layer plus dangling bonds (as illustrated in Figure 10.1a). It turns out that its properties determine the band alignment through Fermi level pinning and can be purposefully controlled by intercalation.

10.4.1 Ohmic Contacts

As-grown epitaxial graphene on n-type 6H-SiC(0001), i.e. MLG, provides an excellent ohmic contact. This is an astonishing observation that is depicted in Figure 10.3a. Even when comparing it with technologically relevant ohmic contacts [41, 42], MLG outperforms those. Whereas the use of bulk metals for ohmic contacts always requires high contact doping of the semiconductor and sophisticated recipes including annealing, the ohmic contact with MLG is close to the flatband case. This becomes particularly evident at low semiconductor doping concentrations, where nickel (Ni) or other metals always result in rectifying Schottky contacts, whereas MLG/SiC remains nicely ohmic (see Figure 10.3a). This remarkable fact is determined by the atomically thin interface layer between graphene and SiC (see Figure 10.1a). The buffer layer and the dangling bonds jointly provide a rich density of electronic interface states, which results in the well-known effect of Fermi-level pinning [6] with three consequences: (i) Strong electron doping of the MLG layer [3]. (ii) Consequently, a reduced work function for MLG. (iii) Screening of MLG from vertical electric fields originating in the semiconductor [43]. An important consequence of this situation is that the charge density in MLG sticks to $n = 10^{13}\,cm^{-2}$ as mentioned previously, independent of temperature, doping of the semiconductor, electric fields in the semiconductor, etc. The second important consequence is the robust ohmic behavior on n-type 6H-SiC. A closer look by photoelectron spectroscopy reveals a small Schottky barrier height of $\Phi_B = 0.3$ eV of the MLG/6H-SiC contact [44], which does not influence the electrical characteristics.

For the technologically more relevant polytype 4H-SiC with its larger bandgap and thus smaller electron affinity, the band alignment is less pronounced resulting in a slightly higher Schottky barrier height of $\Phi_B = 0.6$ eV [44]. This leads to deviations from perfect ohmic characteristics at low doping levels. In turn, little contact doping is sufficient to recover the ohmic MLG/4H-SiC characteristics. The described properties have been studied in depth using the transfer length method (TLM) [45].

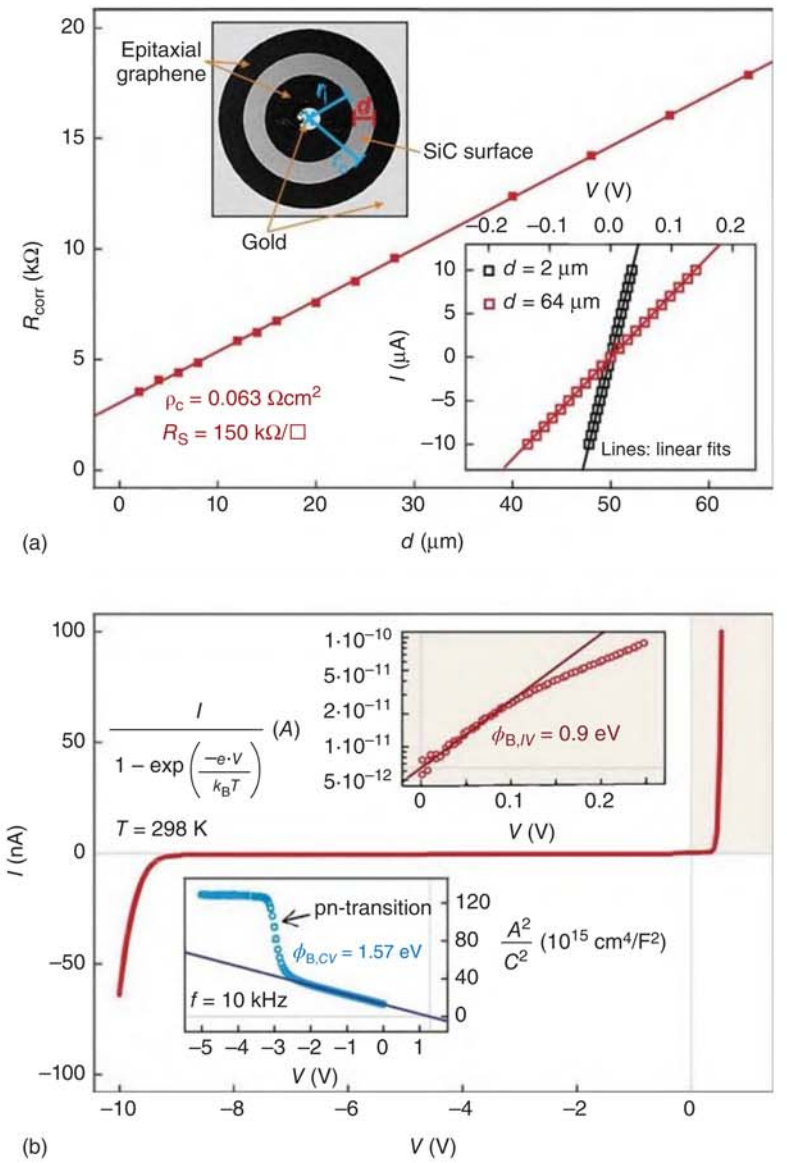


Figure 10.3 Epitaxial graphene as ohmic and Schottky contacts to SiC. (a) MLG ohmic contact: transfer length method (TLM) measurement using a circular contact geometry (see scanning electron micrograph). MLG has been covered with gold to reduce series resistances. Despite a very low doping concentration of the SiC ([N] = 1×10^{15} cm^{-3}), the I–V characteristics of the MLG contacts are perfectly ohmic (see inset). (b) QFBLG Schottky contact: I–V characteristics of a QFBLG/SiC junction, which clearly displays rectification. A Schottky barrier height $\Phi_{B,IV}$ = 0.9 eV is extracted from the forward characteristics (shaded area, same data shown in upper inset). $\Phi_{B,CV}$ = 1.57 eV is extracted from C–V data (lower inset) on the same device. Source: Reprinted from Hertel et al. 2012 [36], license: CC BY-NC-SA 3.0.

Table 10.1 Comparison of specific contact resistances ρ_C: MLG ohmic contacts vs. conventional metal ohmic contacts.

Polytype	Doping (cm^{-3})	Contacts	$\rho_C(\Omega\ cm^2)$	References
6H-SiC	1.0×10^{15}	MLG	6.3×10^{-2}	[45]
	1.0×10^{15}	Ni	Not ohmic	[45]
	4.5×10^{17}	Ni	1.7×10^{-4}	[46]
	7.4×10^{18}	Ni	3.6×10^{-5}	[42]
	$(7–9) \times 10^{18}$	Ni	5.0×10^{-6}	[47]
	1.0×10^{19}	MLG	5.9×10^{-6}	[45]
	4.5×10^{20}	Ni	1.0×10^{-6}	[48]
4H-SiC	4.2×10^{18}	Ni	6.4×10^{-5}	[49]
	7×10^{18}	Ni	4.8×10^{-5}	[50]
	1.6×10^{19}	MLG	5.6×10^{-5}	[45]
	1.6×10^{19}	Ni	4.1×10^{-4}	[45]
	1×10^{20}	Ni	5.3×10^{-4}	[51]

The results are summarized in Table 10.1 and underscore the advantageous properties of MLG in terms of ohmic contact performance.

10.4.2 Schottky Contacts

It was already mentioned that the modification of the interface via intercalation has significant impact on the charging of the graphene sheet. In particular, hydrogen intercalation leads to a positive charge density in the graphene layer, cf. Figure 10.1c. This indicates that the band alignment between graphene and SiC strongly changes after intercalation [52]. A measurement of the Schottky barrier height can be performed by photoelectron spectroscopy, leading to a value of at least 1.5 eV [18]. Electrical measurements on large-scale QFBLG/SiC contacts indeed prove the rectifying diode behavior (Figure 10.3b) [36]. However, a closer analysis (inset in Figure 10.3b) rather indicates a smaller Schottky barrier height of 0.9 eV, which is substantially lower than the X-ray photoelectron spectroscopy (XPS) result. To resolve this discrepancy, it is instructive to determine the Schottky barrier height via capacitance–voltage (C–V) measurements on the very same junction, from which $\Phi_B \approx 1.5$ eV is obtained again [36]. The difference originates from the fact that both C–V and XPS techniques probe the area-averaged barrier height, whereas the I–V analysis is sensitive to the lowest barrier height in the contact region, even if it is only in a small spot (pin hole).

The origin of these pinholes can be investigated more systematically by using nanocharacterization techniques. At first, QFBLG/SiC Schottky contacts were fabricated with a large span of contact diameters from 200 µm down to 0.5 µm, the smallest being electrically contacted using the tip of a conductive atomic force

microscope (C-AFM). It was observed that the Schottky barrier height increases with decreasing contact diameter and finally saturates at $\Phi_B \approx 1.5\,\text{eV}$ for the smallest contacts. This can be better understood by C-AFM current maps and their immediate comparison with the topology. It turns out that the Schottky barrier height lowering occurs at the step edges of the SiC substrate terraces. Hence, these line defects provide the pinholes. When they are avoided, the Schottky diodes display the Schottky barrier height of 1.5 eV even in I–V analyses [53]. Note that the terrace widths strongly depend on the off-cut angle of the SiC substrate [53] and the step-bunching effect, which occurs under certain annealing conditions [54].

10.5 Monolithic Epitaxial Graphene Electronic Devices and Circuits

10.5.1 Discrete Epitaxial Graphene Devices

Provided with graphene ohmic and Schottky contacts, and further with recipes for their side-by-side fabrication on the very same wafer, resistors, diodes, as well as transistors are feasible.

We focus here on the transistors, which are of the metal-semiconductor field-effect transistor (MESFET) type. The metal is fully substituted by epitaxial graphene; we term this transistor, therefore, epitaxial graphene-silicon carbide field-effect transistor (GraSFET) [36, 55]. Notably, all metallic contacts can be established by epitaxial graphene; the gate contact being of the Schottky type (QFBLG/SiC) and the source and drain contacts being of the ohmic type (MLG/SiC). As all components are carved out of a single root SiC material, we termed the overall devices *monolithic*.

The situation is graphically sketched in Figure 10.4a. Blue graphene layers indicate MLG with the underlying (black) buffer layer; the red double layer corresponds to QFBLG with hydrogen atoms (yellow) saturating SiC's dangling bonds. The SiC consists of a layer structure: the top layer (light blue) is n-type and conductive, whereas the underlying layer is either semi-insulating or p-type to suppress unwanted current pathways through the substrate. Current can flow from the source contact (left MLG contact) via the n-type SiC layer to the drain contact (right MLG contact). The current flow can be controlled by the gate contact (QFBLG contact in the middle) with its underlying space-charge region. The depth/width of the latter is enlarged by driving the Schottky contact in reverse direction (negative voltage applied to the gate). When the n-type SiC channel is fully depleted, i.e. all current paths are squeezed off, the transistor is fully switched off. In turn, when releasing the negative voltage, the channel is opened allowing for an electrical current from source to drain.

Figure 10.4b displays a scanning electron microscopy (SEM) image of an actual implementation of a GraSFET. We now describe the manufacturing processes. It starts with high-purity semi-insulating on-axis 4H-SiC into which nitrogen is implanted to define the conductive transistor channel volume (n-type well). Subsequently, MLG is grown, a step that includes the post-implantation annealing. In the next step, partial intercalation of the gate contact is prepared by defining voids in the

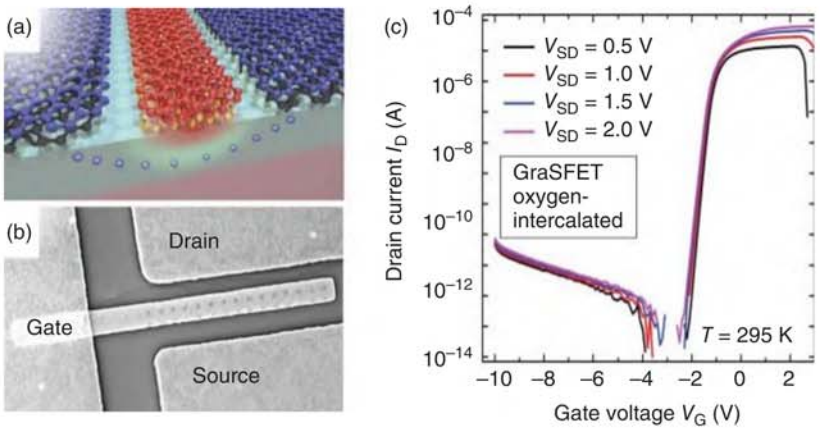


Figure 10.4 Monolithic epitaxial graphene/SiC transistor (GraSFET). (a) An artis's view of a monolithic epitaxial graphene transistor. Current can flow from MLG (blue hexagonal grid with underlying bufferlayer in black; source electrode) through the n-doped SiC (light blue) to a second MLG electrode (drain). The current path is confined by a non-conducting layer underneath (purple). The voltage applied to the Schottky gate provided by QFBLG (red) opens or closes the channel. (b) Scanning electron micrograph of an improved GraSFET implementation. The conductive transistor channel is defined by nitrogen implantation between source and drain contacts. To reduce series resistances, contact areas have received an additional contact implant and MLG is covered by Ti/Au. Note that the graphene gate finger has intentionally been placed onto a single substrate terrace, which reduces gate leakage currents. (c) Transfer characteristics of a normally-on oxygen-intercalated GraSFET with improved device design. A large on/off ratio of 10^8 with a subthreshold swing of 110 mV/dec is achieved. Source: (a) Reprinted from Hertel et al. 2014 [56], with the permission of WILEY-VCH, ©2014 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. (b) Reprinted with minor adaptions from S Hertel 2016 dissertation, urn:nbn:de:bvb:29-opus4-72024, license: CC BY-SA 3.0.

appropriate graphene area using electron beam lithography and subsequent oxygen plasma etching. When exposing the sample to hydrogen under mild conditions, partial intercalation takes place only in the predefined area around the voids. The residue of this void pattern can be seen in Figure 10.4b (gate finger). Subsequently, source, drain, and gate contacts are defined by electron beam lithography and metal deposition of gold (Au) or titanium/gold (Ti/Au) (cf. also [57]). The metal layer serves as an etch mask for the final oxygen plasma etch. This ensures that the graphene electrodes to SiC are carved out congruently with the metal layer. Hence, in contrast to the artist's view, all graphene areas with their rather high series resistances are additionally covered with metal. This reduces the sheet resistances of the leads from kΩ/□ down to below Ω/□ and, thus, improves the transistor performance.

Further improvement can be achieved when substituting the hydrogen intercalation by oxygen intercalation in water vapor [58], which again allows partial

intercalation when using mild conditions. The oxygen intercalation is more stable. Moreover, recent long-term experiments with hydrogen-intercalated QFBLG have revealed that hydrogen atoms are replaced by oxygen when storing the sample in ambient air for several months [58].

The transfer characteristics obtained with such a device for various source–drain voltages V_{SD} at room temperature are shown in Figure 10.4c. They display a remarkable on–off ratio up to 10^8 with a subthreshold swing of 110 mV/dec. The threshold voltage can be engineered: the implantation depth of the n-type well defines the zero-gate voltage channel thickness, which may be chosen normally-on or normally-off. Here we display a normally-on case with a threshold voltage of ≈ -1 V. The on-state current obtained for this small test device is in the order of 100 µA; it can be extended by adjusting geometry and channel doping. GraSFET devices are able to operate at high temperatures [58]; the temperature limit is rather determined by the increase of leakage current than by material instabilities. QFBLG (including the intercalation) is stable at least up to 800 °C; this is particularly valid for oxygen-intercalated QFBLG [58].

10.5.2 Monolithic Integrated Circuits

Having resistors, diodes, transistors, and interconnects at hand, integrated analog and digital circuits with monolithic epitaxial graphene devices become feasible. Here we demonstrate two very elementary logic components in the simplest realization (resistor–transistor-logic).

Figure 10.5a displays the circuit of a simple logic inverter; the chip layout is sketched in Figure 10.5b. All components are monolithically made of epitaxial graphene (partially hydrogen intercalated). The channel of the GraSFET is chosen to be normally-off with a threshold voltage around 0.25 V. The circuit was operated with a supply voltage of 0.5 V. The logic input is denoted as A and the logic output as Y. Figure 10.5c presents the logic signal transfer characteristics of this device, which shows nicely the inverter operation. The output voltage lies perfectly within the noise margin ensuring stable operation of subsequent logic components.

Another important device is the NAND gate. With a NAND gate at hand, a full logic becomes possible according to de Morgan's theorem [59]. A demonstrator of a NAND gate can easily be achieved by extending the described inverter circuit with a second gate contact in the GraSFET (see Figure 10.5d,e). Figure 10.5f displays the corresponding measurement obtained on such a device. The input voltages V_A and V_B are plotted on the vertical and horizontal axes, respectively, while the output voltage V_Y is color coded. The NAND logic can immediately be seen: the output becomes low only if both inputs are high at the same time. The noise margins are indicated as rectangles in the plot; again, the output voltages lie perfectly within the noise margins ensuring stable logic operation. These findings on a single inverter and NAND gate demonstrate that the GraSFET architecture is suited to build up any logic circuit.

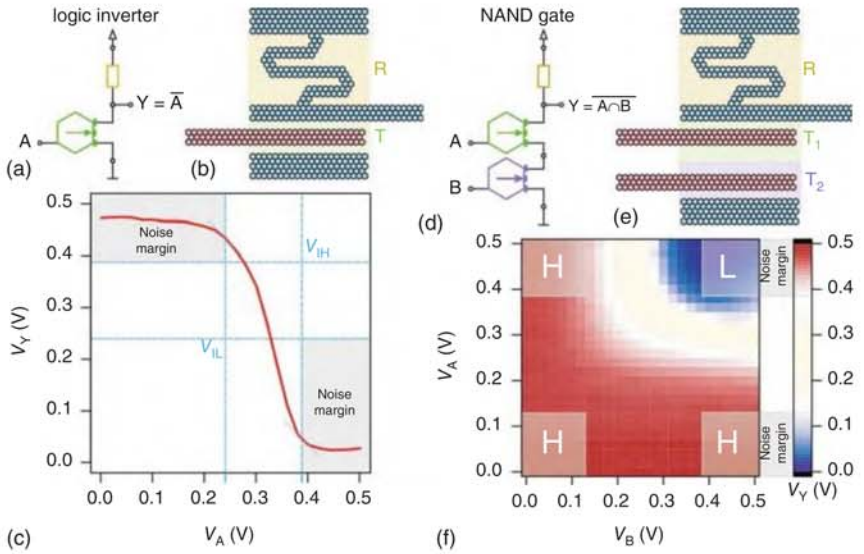


Figure 10.5 Monolithic integrated logic circuits. Logic inverter: circuit (a) and schematic implementation (b) of an inverter built in transistor-resistor logic by a monolithic epitaxial graphene transistor together with a graphene resistor (blue hexagons indicate MLG, red hexagons indicate QFBLG). (c) Voltage transfer characteristics of the inverter showing output voltages clearly within the noise margins. NAND gate: circuit (d) and schematic implementation (e) of a NAND gate; the circuit is similar to the logic inverter, but the GraSFET is equipped with a double gate connected to the NAND inputs A and B. (f) Color-coded output voltage as a function of the two input voltages. NAND function is visible with output voltages well within the noise margins. Source: Reprinted from Hertel et al. 2014 [56], with the permission of WILEY-VCH, ©2014 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

10.6 Novel Experiments on Light–Matter Interaction Enabled by Epitaxial Graphene

10.6.1 High-Frequency Operation and Ultimate Speed Limits of Schottky Diodes

We now guide our attention to an elementary process in electronics that is rectification by a diode. Common wisdom tells that the speed of Schottky diodes is governed by *RC* limitations of their parasitic environment. Little, however, is known about intrinsic limitations of Schottky diodes for timescales faster than the *RC* limit. It turns out that epitaxial graphene Schottky diodes are an interesting prototype for the investigation of such very fundamental speed limits of Schottky rectification [60].

Notably, the metallic (graphene) layer is only one atom thick. We start the description with experiments in the THz spectral range ($\gtrapprox$100 GHz). THz radiation is coupled via logarithmic periodic antennae (Figure 10.6a) to a Schottky diode, which is fabricated similar to the abovementioned procedures and schematically displayed in Figure 10.6b. Here, Schottky and ohmic contacts are defined side by side both using MLG on 4H-SiC(0001) with its rather low Schottky barrier height; the ohmic

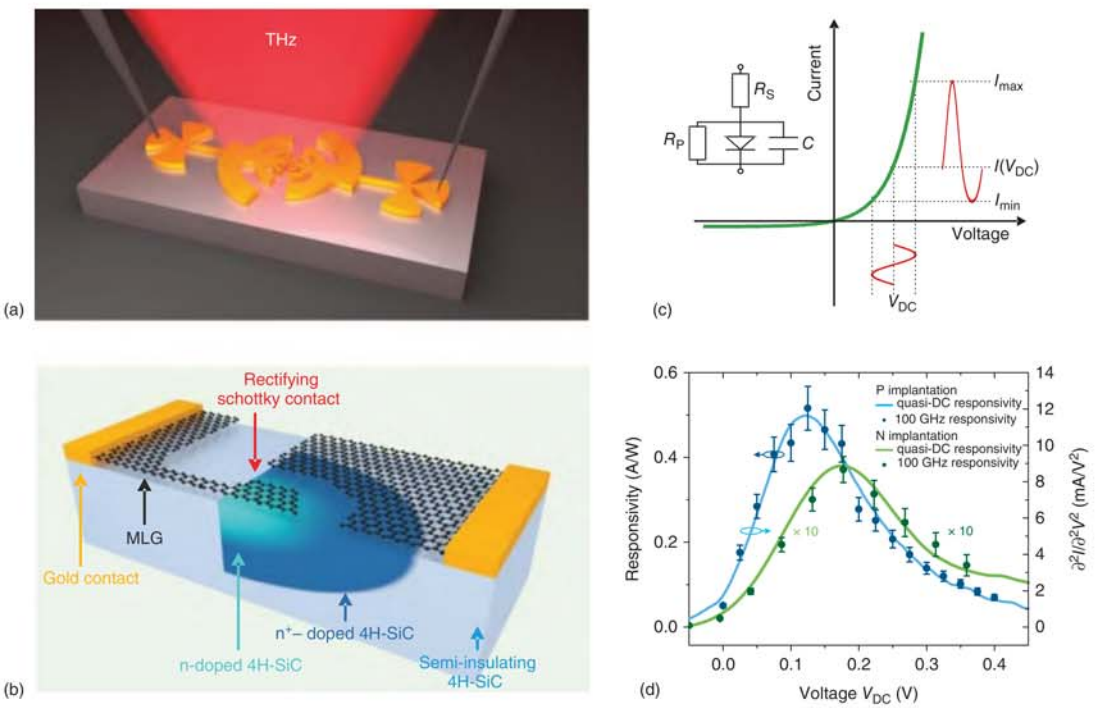


Figure 10.6 Detection of THz radiation with epitaxial graphene/SiC Schottky diodes. (a) The Schottky diode is connected in the center of a logarithmic periodic antenna. The THz radiation is transformed by the antenna into a THz voltage V_{AC} which is rectified by the device. The resulting time-averaged current $\langle I(t)\rangle$ is proportional to the square of the field amplitude of the THz radiation. (b) Close-up of the Schottky diode. MLG forms the metal of the Schottky contact, the semiconductor is n-doped SiC. By increasing the doping level, an ohmic contact between the two materials is achieved. (c) Schematic of rectification in a Schottky diode and its equivalent circuit: an incident voltage V_{AC} superimposed on bias voltage V_{DC} translates via the curvature into an asymmetric AC current response that increases the time-averaged (DC) current. (d) Responsivities calculated from quasi-static $I-V$ characteristics (solid lines) and THz responsivities (at 100 GHz, symbols) as a function of the bias voltage obtained on two Schottky diodes with phosphorous (P) or nitrogen (N) doping, respectively. Remarkably, the quasi-DC responsivity and the THz responsivity are barely distinguishable. Source: Reprinted with minor adaptions from Schlecht et al. 2019 [60], license: CC BY 4.0.

contact differs only by a significant contact implantation. We first present a DC electrical characterization (Figure 10.6c), which corresponds to a typical textbook I–V characteristic of a diode with a non-vanishing serial resistance. The equivalent circuit is depicted in the inset. Now, THz radiation is applied to the diode from a homebuilt cw-THz source based on n-i-pn-i-p superlattice photomixers [61] via the antennae. As the resulting oscillating voltage V_{AC} is rather small, it provides an oscillation around the operating point V_{DC}. In forward direction with its strongly nonlinear characteristics, an oscillation in V_{AC} results in an oscillating current I_{AC} that is non-sinusoidal. Hence, a Taylor expansion immediately results in higher-order corrections. In particular, the time-averaged signal of $I(t)$ deviates from I_{DC} such that

$$\langle I(t)\rangle = I_{\mathrm{DC}} + \frac{1}{2}\frac{\mathrm{d}^2 I}{\mathrm{d}V^2}\hat{V}_{\mathrm{AC}}^2 + \cdots .$$

As a consequence, the response to the THz radiation (quantified by its power) can simply be measured as DC current with a proportionality constant that is termed responsivity. Figure 10.6d shows the central result of this setup for n-type SiC which is doped by either phosphorous (P) or nitrogen (N). With increasing bias voltage V_{DC}, the responsivity increases first exponentially (due to the curvature of the exponential increase of $I(V)$). It has a maximum at a few hundred millielectronvolt and is then reduced because the series resistance suppresses the curvature. While the responsivity of the device is competitive with state-of-the-art Schottky diode detectors, the more interesting aspect is the comparison of the quasi-DC responsivity (i.e. the second derivative of the static I–V characteristics) and 100 GHz responsivity: their shape is barely distinguishable. From this observation, we conclude that the epitaxial graphene Schottky diode behaves nearly identically on extremely different time scales: between 1 Hz for the quasi-DC characterization and the 100 GHz, the physics apparently does not change despite 11 orders of magnitude differing frequencies. In this setup, however, the *RC* limitation is still important: the cutoff frequency is at 580 GHz.

To access even faster time scales, different strategies must be chosen that entirely avoid *RC* limitations. We chose a femtosecond excitation with a laser. Photoelectrons are charge-neutral excitations within graphene that rapidly establish non-equilibrium to the diode without *RC* delays in electrical leads. Again, epitaxial graphene Schottky diodes turn out to be the ideal choice for such experiments. Not only they withstand highest laser intensities because of the outstanding robustness of both graphene and SiC but also SiC is entirely transparent while graphene absorbs about 2.3% of the incoming light pulse [62].

For the experiment a photodiode with a Schottky barrier height of 0.8 eV is chosen (cf. Figure 10.6b). It is operated in reverse bias conditions and illuminated with ultrashort pulses (5.5 fs) perpendicular to the graphene plane. Via internal photoemission, which is considered to be prompt, high-energy electrons are generated, which have now two options: either they tunnel though the barrier (prompt internal photoemission, PIPE) or they exchange energy with other photoelectrons, which leads to an increased electronic temperature after the pulse. As a consequence of the latter, there are electrons at even higher energies that can travel over the barrier

(photothermionic current, PTI). The measured quantity is the overall photocurrent, which consists of both PIPE and PTI electrons. When the laser power is enhanced, the ratio of PIPE and PTI rates with their characteristic power dependencies can be identified.

As it turns out, an even more meaningful quantity is the saturation absorption. When the laser power is increasing, the photocurrent increases as well, but only up the point where optical saturation is reached. At this point, there are so many excited electrons filling the limited electronic graphene density of states that additional photons cannot excite further electrons (Pauli blocking). This is a remarkable regime that can only be reached because of the extreme robustness of epitaxial graphene and is indeed detected in our experiments. It turns out experimentally that the saturation absorption of the photocurrent depends on the bias applied to the junction. This guides the attention to a counteracting mechanism: subsequent to photoexcitation, there is a time scale after which a hot electron is extracted from the graphene plane toward SiC, the charge transfer time τ_{ct}. The shorter τ_{ct}, the more laser power is required to saturate the electronic excitation. Hence, the bias voltage controls via τ_{ct} the saturation absorption process. From a detailed numerical analysis of the photocurrent as a function of laser power *and* bias voltage across the diode (including PIPE, PTI and saturation absorption) meaningful timescales for τ_{ct} can be extracted. It yields $\tau_{ct} \approx (300 \pm 200)$ as (attoseconds), which is the fastest time ever observed for electrons that are transferred from one material to another. Hence, with ultrafast optical excitations, a Schottky diode can resolve timescales faster than femtoseconds, i.e. Petahertz [63].

10.6.2 Transparent Electrical Access to SiC for Novel Quantum Technology Applications

In recent years, SiC has been identified as a promising material for quantum technology applications such as quantum sensors and single photon sources required for quantum communication and quantum cryptography [64–67]. Key elements are optically excitable and luminescent point defects that are often termed color centers. They are similar to single atoms regarding their quantum mechanical properties, but they are contained in a well manageable solid host material. Most experiments in this novel field, which brings together quantum optics, solid-state physics, and material sciences, have been performed on the NV center in diamond (see e.g. [68–70]). Compared to diamond with its technological shortcomings, SiC has significant advantages like a mature process technology and large-scale wafer availability. Most importantly, various luminescent point defects in SiC have been identified with excellent properties for quantum applications, and recipes have been developed for their fabrication [71–75].

Since point defects in a solid host material are subject to interactions with the crystal environment, the detailed properties of individual defects vary even though they are nominally of the same type. On the other hand, precise spectral matching is required when two or more color centers shall be coupled for quantum communication [76]. As a consequence, a handle is needed for fine-tuning the spectral

properties of individual color centers into resonance. Stark tuning is a promising strategy because electrical fields can be generated locally using electrodes in the vicinity of the defects, which need to be spectrally fine-tuned [77].

Here, SiC inherently brings along epitaxial graphene with the unprecedentedly useful properties of being an atomically flat and one-atom thick transparent metal [62] in epitaxial registry to the SiC surface. These properties are of great importance because luminescent defects are typically read out by optical means, i.e. they should be located surface-near and not be obscured by other materials like metal electrodes or surface contamination. We recently demonstrated the use of epitaxial graphene electrodes for Stark tuning spectral lines of the silicon vacancy defect V_{Si} in 4H-SiC, which were created between and underneath the electrodes [78]. Employing the transparent properties of epitaxial graphene contacts, it was possible to observe spectral fine-tuning or line splitting in symmetry-conserving axial electric fields or symmetry-breaking basal electric fields, respectively. This allows for both Stark effect analysis of defect symmetries [79] and spectral matching of several remote single-photon sources paving the way for integrated quantum technology.

10.7 Conclusion

Graphene that grows out of SiC(0001) provides an unprecedented material system. Graphene in many aspects behaves like a standard metal but is atomically thin, ultrarobust, and optically nearly fully transparent. Different to bulk metals, the full graphene sheet can be charged either with electrons or holes not only by gating (which is not considered here) but also even more interestingly by defining via intercalation the epitaxial interface to SiC with atomistic control. In turn, this interface influences the electronic properties of the underlying SiC as well. Epitaxial graphene and SiC thus provide a monolithic metal/semiconductor system with atomic precision. This is not only very elegant but also extremely powerful: epitaxial graphene/SiC Schottky contacts and ohmic contacts can be prepared side by side and functionality up to the level of logic inverters and NAND gates is demonstrated. Epitaxial graphene/SiC Schottky diodes show unchanged operation even at 100 GHz. Hence, we see SiC as an upcoming material for applications in the THz spectral range. Further, relying on the extreme robustness of the combined material system, experiments under extreme conditions can be carried out. For example, extreme ultrashort laser pulses can be used to explore charge transfer in a diode on the (sub-) femtosecond time scale. Finally, SiC provides opportunities as a quantum technology platform. Here, epitaxial graphene electrodes can solve the problem of compensating even finest spectral differences of luminescent point-like quantum objects.

We foresee a bright future for SiC and epitaxial graphene. This unique material system paves the way for many future applications well beyond pure electronic functionality.

Acknowledgments

The authors would like to thank the young colleagues who carried out the experiments at the Chair of Applied Physics (FAU Erlangen-Nürnberg), A. Albert, M. Albrecht, L. Bergmann, A. Finkler, M. Hauck, S. Hertel, J. Jobst, F. Kisslinger, F. Krach, K. Meil, C. Ott, S. Preu, S. Reshanov, M. Rühl, M. Schlecht, C. Sorger, K. Ullmann, D. Waldmann, and Y. Wang, further our colleagues from the Chair of Technical Physics (FAU Erlangen-Nürnberg), K. Emtsev, M. Hundhausen, L. Ley, J. Ristein, T. Seyller, and F. Speck, and from the Chair of Laser Physics (FAU Erlangen-Nürnberg), Ch. Heide, T. Higuchi, P. Hommelhoff. Special thanks also to S. Reshanov and A. Schöner, P. Giannazzo and F. Roccaforte as well as S. Maier. The authors acknowledge financial support from the Deutsche Forschungsgemeinschaft (DFG) within SFB 953, project 182849149, priority program 1459, and WE 3542/7-1.

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11

Device Processing Chain and Processing SiC in a Foundry Environment

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11.1 Introduction

Silicon carbide (SiC) metal–oxide semiconductor field-effect transistors (MOSFETs) became commercially available in January 2011 to satisfy the demand of a higher voltage, lower on-resistance, and faster device. Since then, the availability of larger substrates, lower epitaxial defect density, mature process technology, higher demand by the electric vehicle, renewable market and the growth of commercial foundries have helped to put the SiC technology on a rapid growth curve. This chapter describes the fabrication process for a SiC vertical power DMOSFET. The process flow is meant to provide a starting point for existing 150–200 mm Si foundries which are rapidly becoming obsolete and wish to add another 10–15 years to their productive life. The cost of SiC power MOSFETs will reduce in time due to increase in volume by commercial foundries and reduction of prices for substrate and epitaxial layers. This will create a healthy growth curve for SiC technology for the next 20–30 years.

11.2 DMOSFET Structure

Silicon carbide DMOSFET is used as a vehicle to describe the process integration in SiC technology. Other devices such as Schottky diode will use a sub-set of these steps. A cross-sectional view of a vertical power DMOSFET is shown in Figure 11.1. This name comes from the Si technology where both P-well and N^+ source are formed by diffusing p-type and n-type impurities through the open areas in the mask (diffused MOSFET). Although SiC technology uses double implantation instead of diffusion process as discussed later, this name is still used for the technology. DMOSFETs include two main areas: active and termination, as shown in Figure 11.2.

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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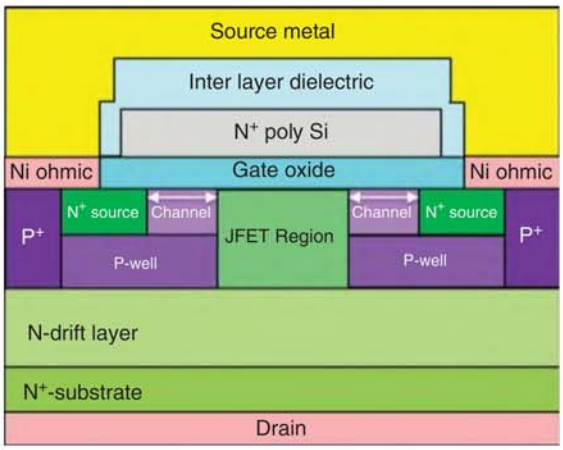


Figure 11.1 Cross-sectional view of a vertical power DMOSFET cell.

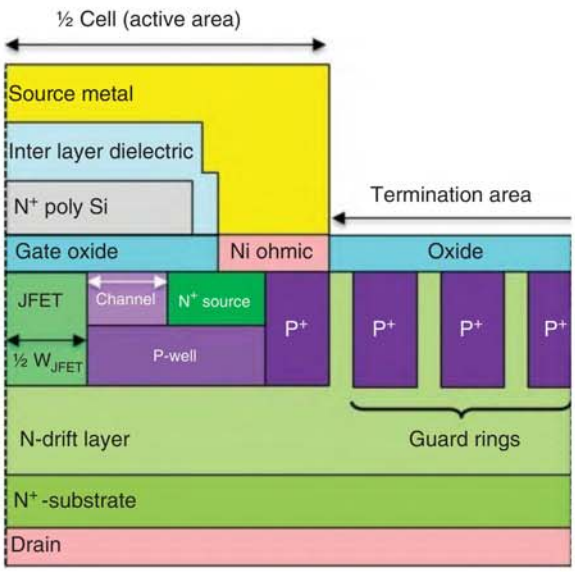


Figure 11.2 A cross-sectional view of a vertical power DMOSFET including active and termination areas.

The operation of an n-channel DMOSFET is based on applying a positive voltage to the gate. This results in formation of an inversion layer (n-type) in the P-well close to the SiO_2/SiC interface. By applying a positive voltage to the drain, the electrons can move from the source through this channel, passing through the junction gate field-effect transistor (JFET) region (sandwiched between two P-wells), the N-drift layer and collected by the drain.

In the active area, all DMOSFET cells are in parallel and connected to each other by overlayer metallization. It should be noted that different cell geometries can be utilized for the DMOSFETs such as linear, square, hexagonal, and orthogonal [1, 2]. Figure 11.3 shows a top view and cross-sectional view of three linear cells in the active area.

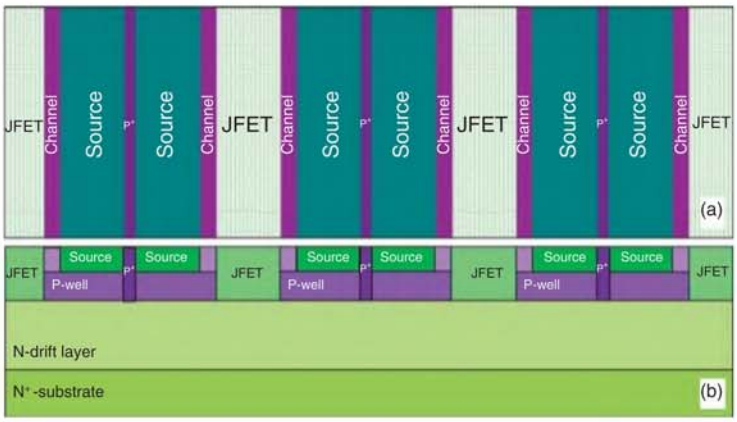


Figure 11.3 (a) Top-view and (b) cross-sectional view of three linear cells in the active area.

Different types of terminations such as guard rings (GRs) or junction termination extensions (JTEs) or combinations of these can be utilized for these devices. The GRs have an advantage over the JTEs with respect to reduced number of ion implantation steps. The GRs can be formed along with the P^+ formation with the same mask and implantation.

11.3 Process Integration of SiC MOSFETs

SiC DMOSFET processing includes several main steps such as dry etching, ion implantation, implant activation anneal, thermal oxidation, surface passivation, poly-Si deposition, metallization, and polyimide coating. In this section, we first provide an overview of the process integration of SiC DMOSFET. This section is adapted from [3]. Then, all the unit steps are discussed further in Sections 11.3.1–11.3.9.

Figure 11.4 shows a cross-sectional view of a nominal 1.7 kV SiC vertical DMOSFET. All the doping concentrations and thicknesses of this structure have been carefully simulated utilizing 2D simulator Silvaco Atlas at the Ohio State University. The last P^+ region at the periphery of the device is needed to be wider in order to provide enough space for gate runner. The gate runner is connected to the gate pad not shown in Figure 11.4.

Figure 11.5 shows a mask layout of a 1.7 kV 4H-SiC DMOSFET, including 46 GRs for termination of the device, which gradually reduce the electric field for a stable breakdown voltage. Each GR has a width of 2 μm, and a gap between each GR is 0.8 μm. The source and gate pads are used for wire bonding in the packaging step. The channel stop ring is made by N^+ implantation and forms along with the N^+ source with the same mask. This ring is used to terminate any shallow depletion layers formed near the surface and thus to eliminate leakage paths. It stops the electric field from extending up to the edge of the chip. The source and gate pads are used

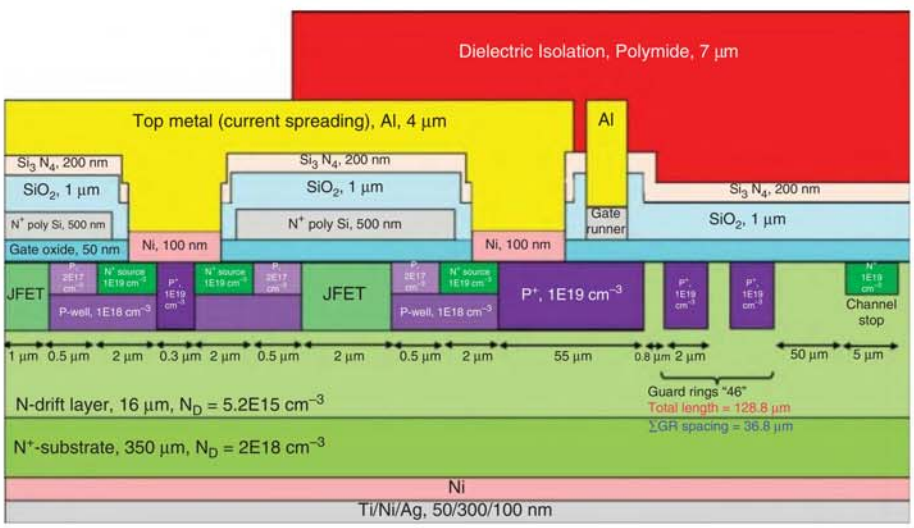


Figure 11.4 A cross-sectional view of 1.7 kV SiC vertical power DMOSFET.

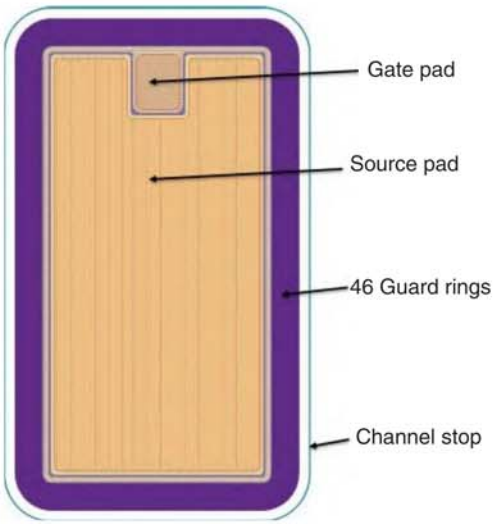


Figure 11.5 A top-view of a vertical power DMOSFET.

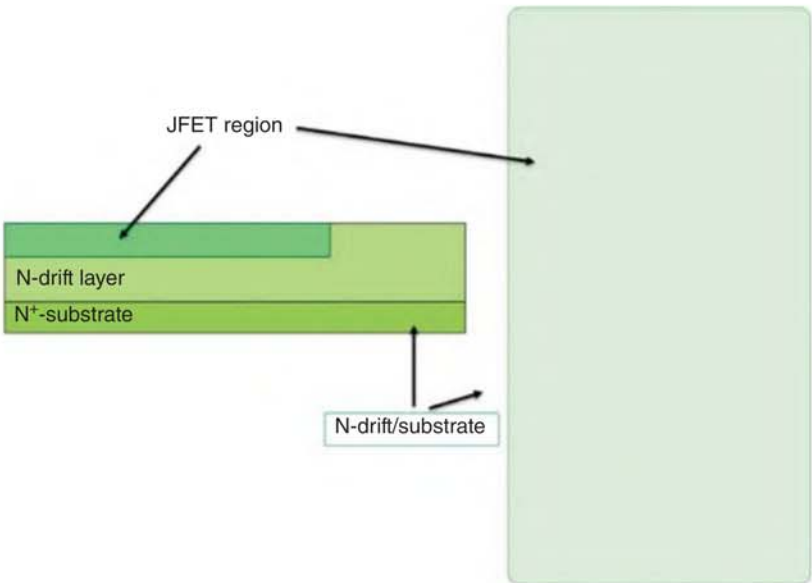


Figure 11.6 (Right) Mask #2: JFET mask and (left) a cross-sectional view of the wafer including the JFET region within the drift layer.

for wire bonding in the packaging step. Ten masks are needed for the fabrication of this MOSFET.

The first mask step is to create alignment marks by dry etching. Different structures are designed for these marks based on the lithography tool utilized in the clean room.

Figure 11.6 shows Mask #2 for forming an n-type JFET region within the drift layer. Nitrogen (N) implantation with several energies is performed at room

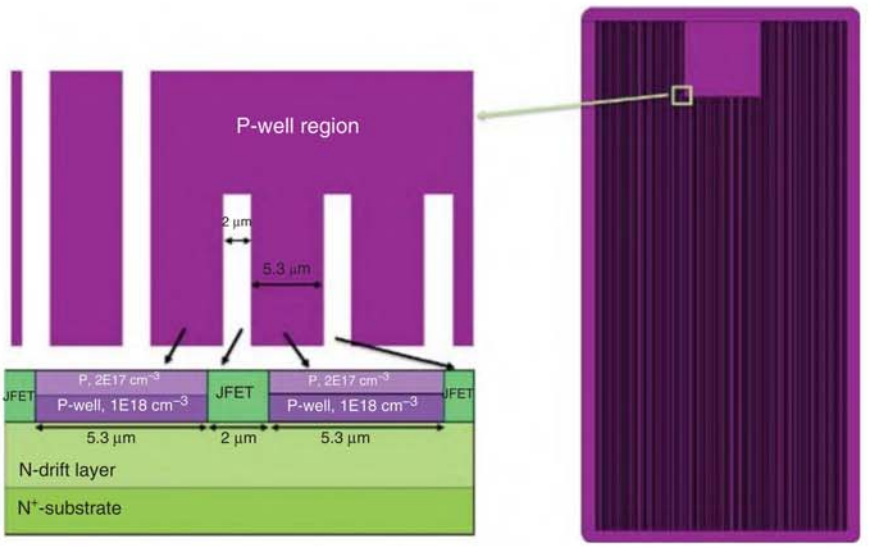


Figure 11.7 Mask #3: P-well mask along with a cross-sectional view of the wafer (bottom left).

temperature (since the dose is below 10^{15} cm^{-2}) with a photoresist masking layer (see Section 11.3.3). Aluminum (Al) implantation with several energies at high temperature (~600 °C) with an oxide mask is utilized for forming the P-well (Mask #3) as shown in Figure 11.7. Woongje Sung et al. reported how two different channels (accumulation vs. inversion modes) can be formed by the P-well implants, which result in different channel mobilities as well as threshold voltages [4].

Similarly, N and Al series implants at high temperature (~600 °C) are used for forming the N^+ source (Mask #4) and P^+ (Mask #5), respectively (see Figures 11.8 and 11.9). It should be noted that the channel stop and all the GRs are also made at the same time with Mask #4 and Mask #5, respectively. To prevent electric field crowding at the corners, all corners at the periphery of a high-voltage device are rounded. As a rule of thumb (confirmed by simulations), the radius of the first corner is set to be three times the thickness of the drift layer (see Figure 11.10). Figure 11.11 shows all the masks together for making JFET, P-well, N^+ source, and P^+ in the drift layer. However, a high-temperature annealing process is required to electrically activate all implanted dopants. A capping layer is generally used to reduce surface roughness during the activation annealing. A graphite-cap layer on the surface can be formed by coating the wafer by a suitable photoresist followed by high-temperature bake as shown in Figure 11.12. Then, activation annealing is done in Ar ambient at temperatures around 1600–1700 °C for 10–30 minutes. After the activation anneal process, the capping layer is removed by ashing in O_2 plasma.

To clean the surface after ion implantation followed by high-temperature annealing, sacrificial oxidation is performed by a thermally grown oxide layer followed by removal with HF acid. Growth of a high-quality SiO_2 gate oxide layer (40–50 nm) followed by post-oxide annealing (POA) with Ar and NO to reduce fixed oxide

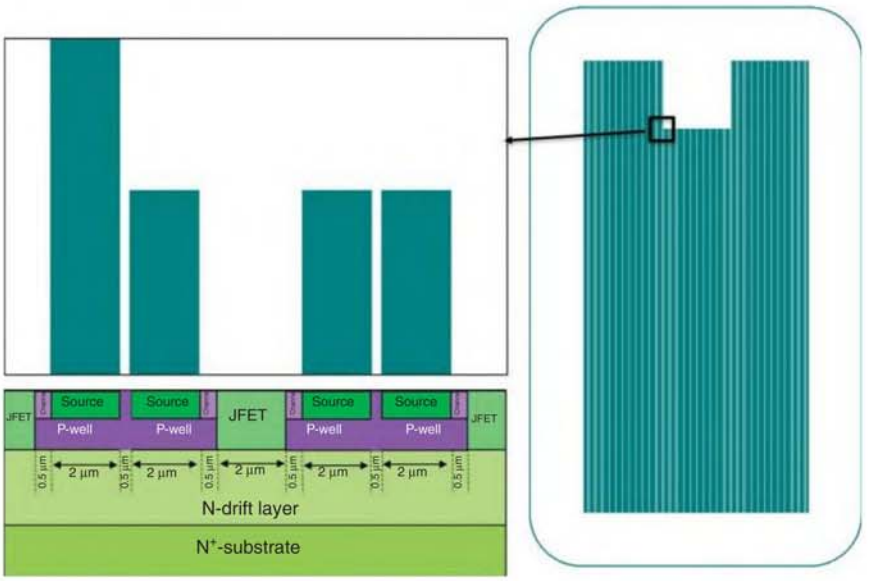


Figure 11.8 Mask #4: N^+ source mask along with a cross-sectional view of the wafer (bottom left).

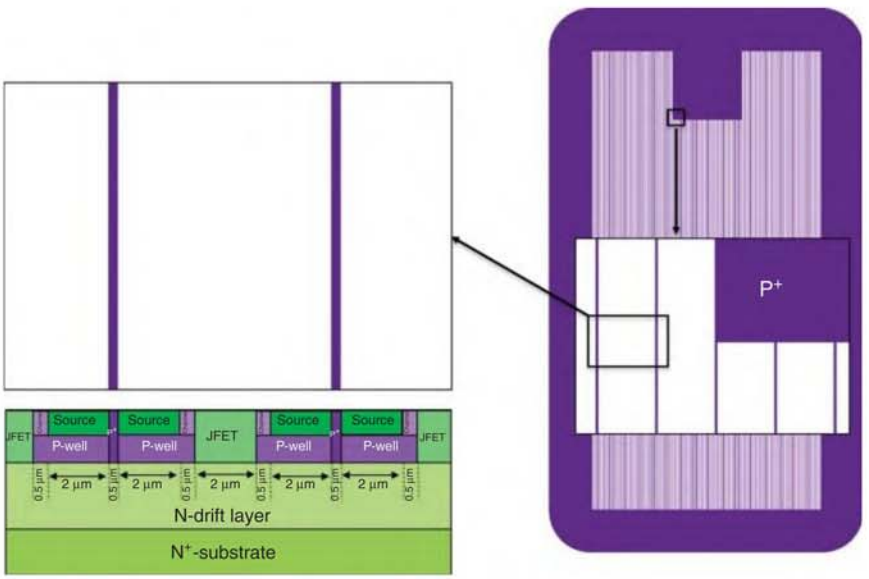


Figure 11.9 Mask #5: P^+ mask along with a cross-sectional view of the wafer (bottom left).

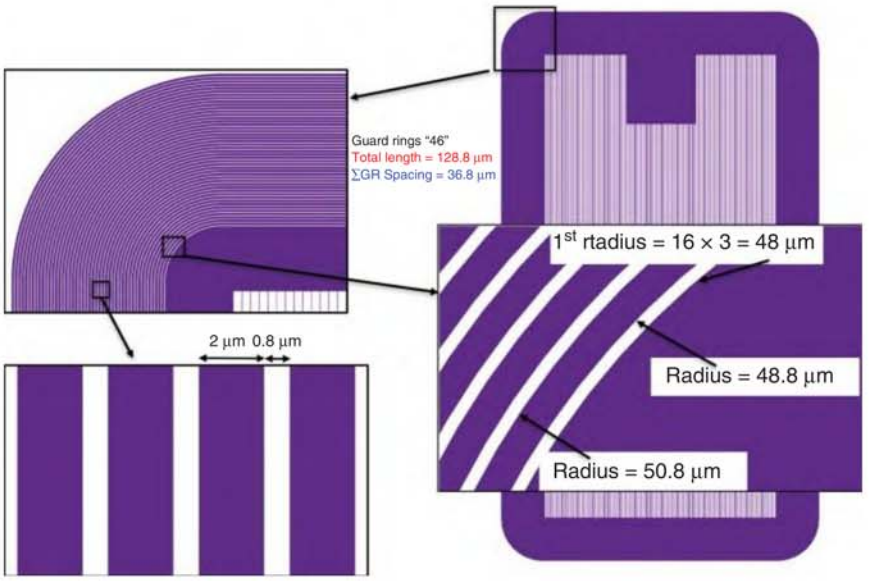


Figure 11.10 Guard rings in the Mask #5.

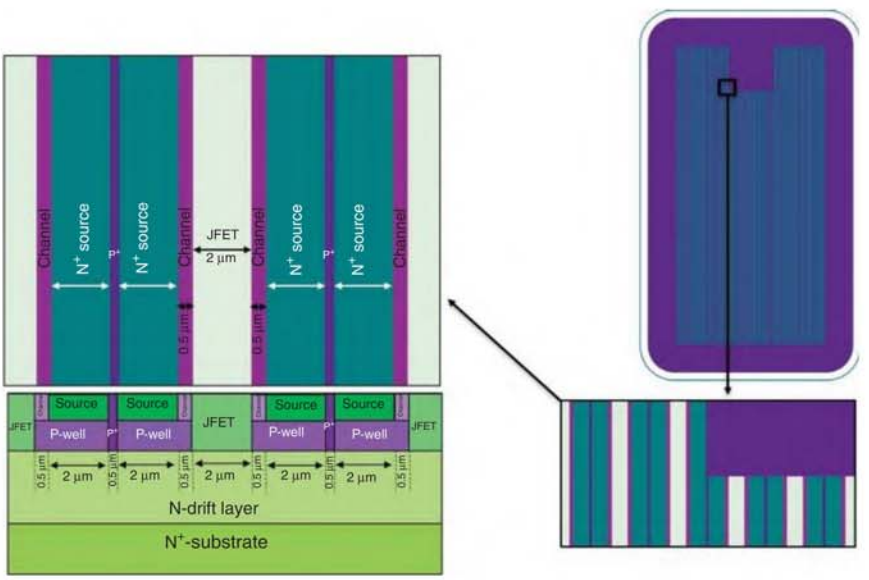


Figure 11.11 All masks #2 to #5 together for forming JFET, P-well, N^+ source, and P^+ in the drift layer by ion implantation.

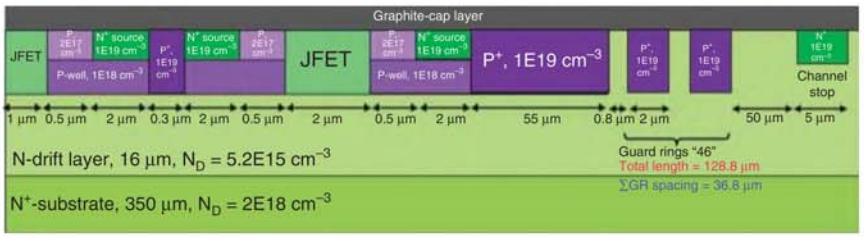


Figure 11.12 Formation of a graphite-cap layer used for activation anneal.

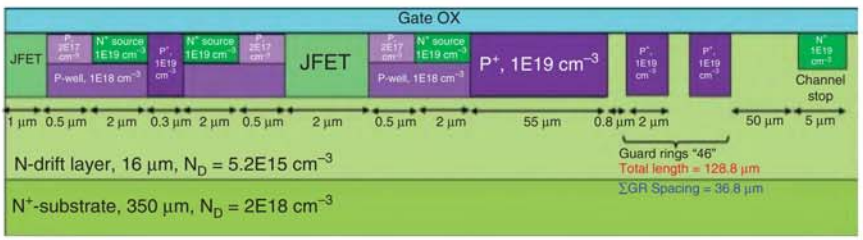


Figure 11.13 Gate oxide growing on the surface.

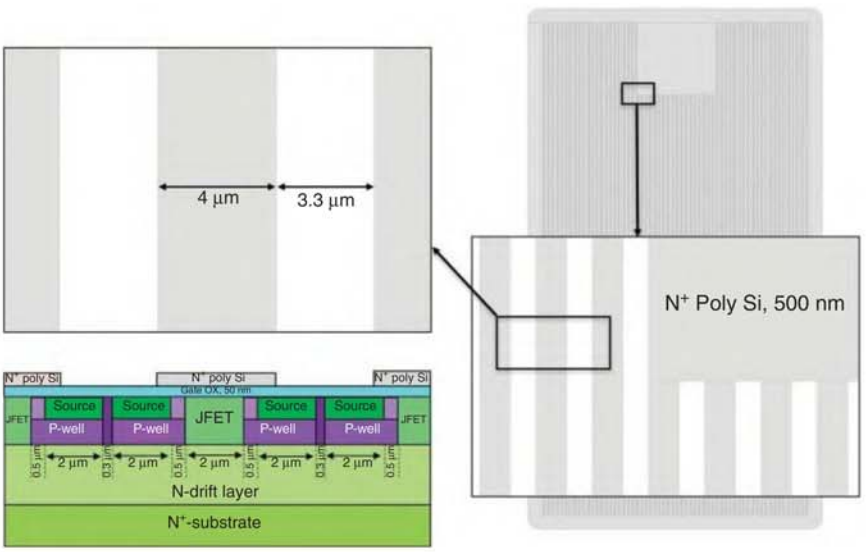


Figure 11.14 Mask #6: gate poly for forming the polysilicon on the gate oxide.

charges and interface state density are critical steps to achieving high channel mobility (see Figure 11.13).

A polysilicon layer (~500 nm) is deposited by low-pressure chemical vapor deposition (LPCVD). It is doped by phosphorus to obtain n-type polysilicon over the gate oxide. Then, Mask #6 Gate Poly is used to dry etch the polysilicon as shown in Figure 11.14.

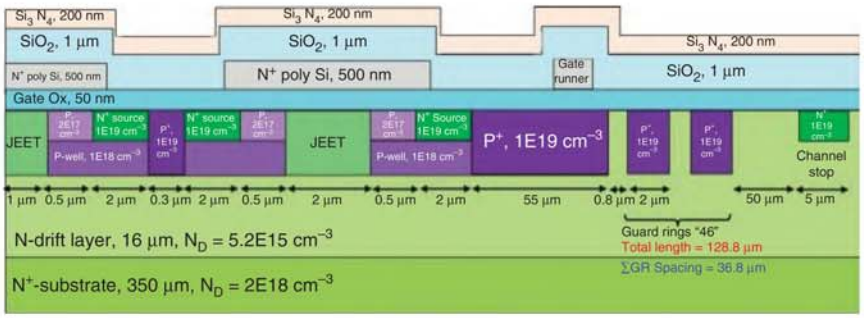


Figure 11.15 Stack of oxide and nitride layer deposition.

Stacked layers of SiO_2/Si_3N_4 are then deposited as passivation and moisture barriers (see Figure 11.15). The deposited SiO_2 layer is generally porous and should be densified by wet oxidation. Then, Mask #7 (Ohmic metal) is utilized to open windows over the N^+ source and P^+ by dry etching the passivation stack (see Figure 11.16). A 100-nm Ni deposition followed by first step anneal at a temperature of about 600 °C is performed in a rapid thermal anneal (RTA) equipment to make at least one phase of nickel silicide Ni_xSi_y [5]. The unreacted Ni over the oxide is then easily removed by wet etching with the Piranha solvent. Then, the second step RTA anneal at >950 °C for >1 minute in N_2 ambient is performed to form the low-resistivity ohmic contacts.

Figure 11.17 shows both Masks #6 and 7 Gate Poly and Ohmic Metal, respectively. It shows an overlap of the gate poly over the source determined by the photolithography resolution. The overlap is necessary to ensure that the gate poly can entirely cover the channel length. There is also a gap of 0.5 µm between gate poly and ohmic contact to n^+ source and p^+ body contact which ensures that there is no short between the gate and the source.

An ohmic metal is needed on the backside of the wafer for having a low resistivity contact to the drain. It can be done by Ni deposition on the backside. However, the native oxide on the backside should be removed by wet–dry etching before Ni deposition. Ni is deposited on the backside of the wafer followed by high-temperature annealing at 950 °C for one minutes in N_2 ambient to form the low-resistivity ohmic contact (see Figure 11.18).

Figure 11.19 shows Mask #8 Gate Runner used for oxide opening (via) by dry etching for the gate pad area and over the gate poly on the periphery of the device as shown in Figure 11.20. The gate runner at the periphery is made in order to have a uniform gate voltage distribution (a precondition for minimum switching losses) in the entire device. An overlayer metal is needed to connect the sources together and also provide a low resistance path on the gate runner. A thick layer (typically 3–5 µm) Al is sputtered on the wafer. Then, the overlayer metal over the source pad, gate pad, and the gate runner is formed by Al etching with Mask #9 as shown in Figure 11.21.

A thick layer (typically 5–10 µm) of polyimide is coated and formed utilizing Mask #10 on the wafer to provide insulation for high voltage areas for packaging as shown

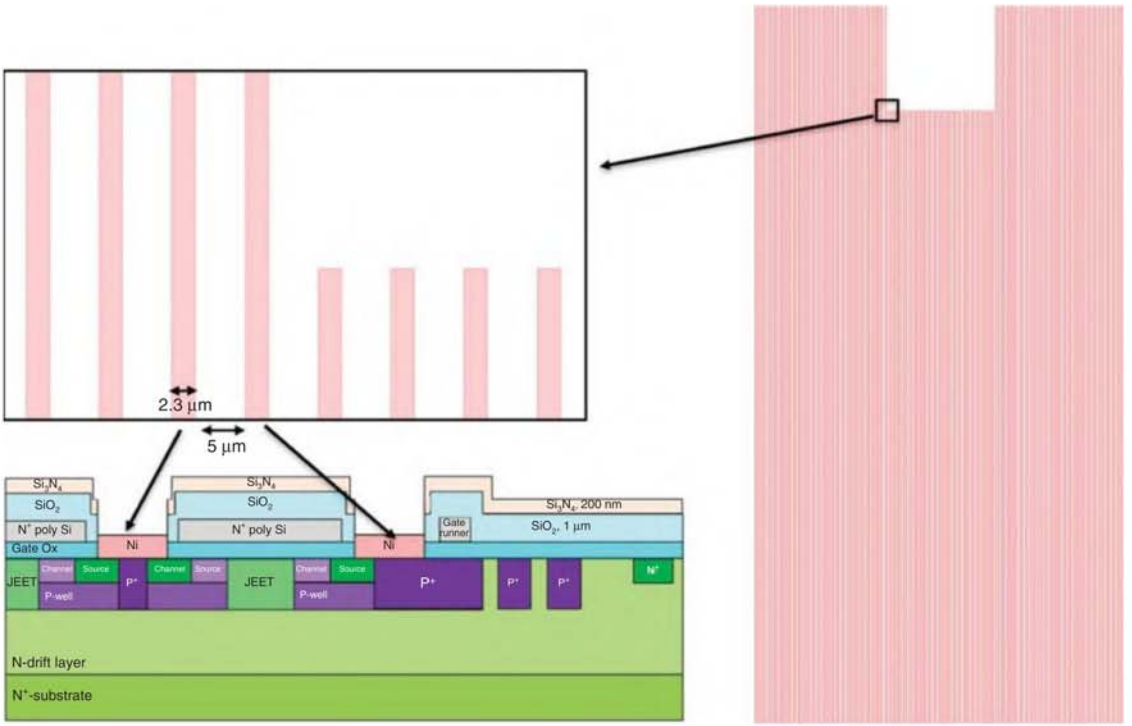


Figure 11.16 Mask #7: Ohmic Metal for forming the metal on the source.

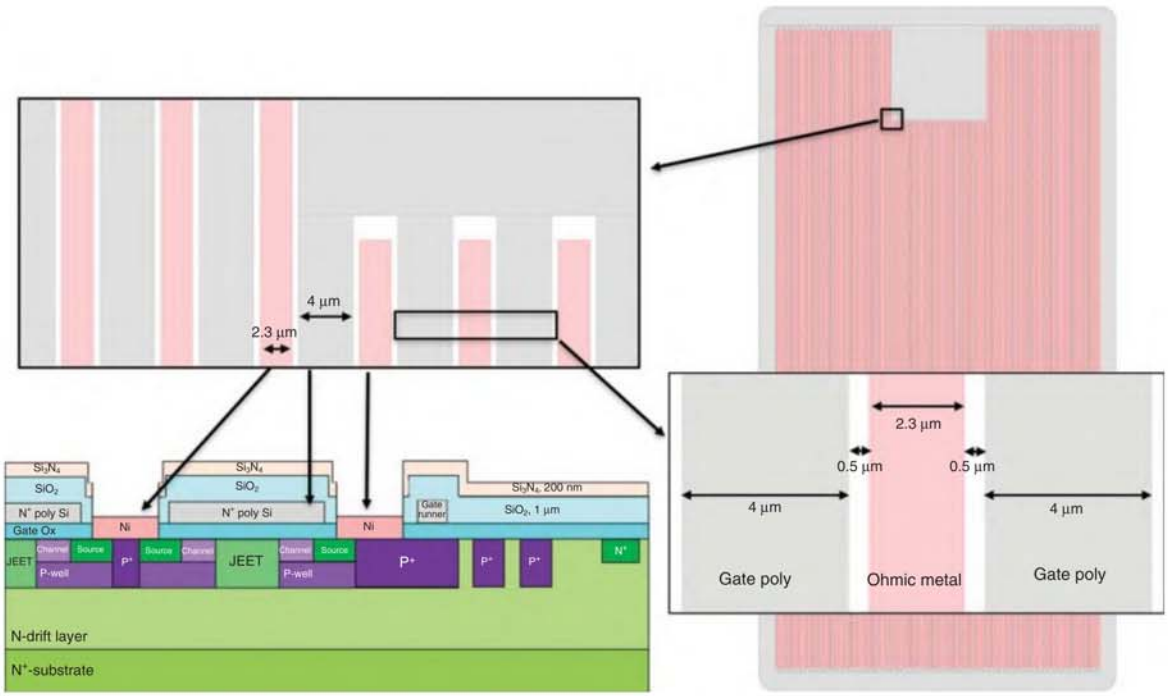


Figure 11.17 Mask #6 (Gate Poly) and #7 (Ohmic Metal).

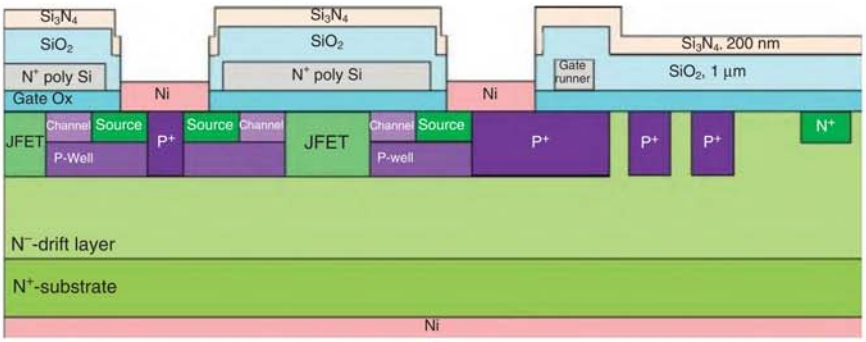


Figure 11.18 Backside ohmic metal deposition.

in Figure 11.22. Therefore, two vias are made over the source and gate pads while the rest of the die is covered by polyimide. It should be noted that the Al on the gate runner is connected to the gate pad not seen in Figure 11.22.

Finally, a stacked layer of metal is deposited on the backside (drain) of the wafer in order to have a better current distribution (see Figure 11.4) and solderability.

11.3.1 Lithography

Lithography is the cornerstone of fabrication process technology. G- or I-line steppers along with a suitable mask are normally utilized for fabricating power devices like DMOSFETs as shown in Figure 11.1. A minimum of 10 steps of lithography are needed to make this structure, i.e. Alignment marks, JFET implantation, P-well implantation, N^+ source implantation, P^+ implantation, Polysilicon gate, Ohmic metal, Gate Runner, Overlayer metallization, and Pad via. For example, to form the JFET region within the N^- drift layer by ion implantation, an oxide layer is utilized as a mask. However, this oxide layer needs to be formed by a lithography step following oxide dry etching. This lithography includes photoresist coating and exposing by ultra violet (UV) light through a mask. Generally, I-line lithography is used for SiC fabrication in existing 150–200 mm commercial foundries. The minimum line width and spacing are about 0.6–0.8 µm which are also process dependent and vary somewhat between various photolithography steppers. The typical alignment tolerance is 0.2 µm. Given these, the minimum pitch of a planar MOSFET cell is around 3.5–4 µm. Smaller pitch leads to better on-resistance since more width of MOSFET channel can be accommodated in a given active area of the chip.

11.3.2 SiC Etching

SiC etching can be done by wet or dry etching processes. SiC is an extremely inert material against chemical solvents, so the wet etch process is very difficult. Although SiC wet etching by molten KOH, NaOH, or Na_2O_2 at 450–600 °C and its mechanism has been reported [6], it results in some defects such as dislocation pits

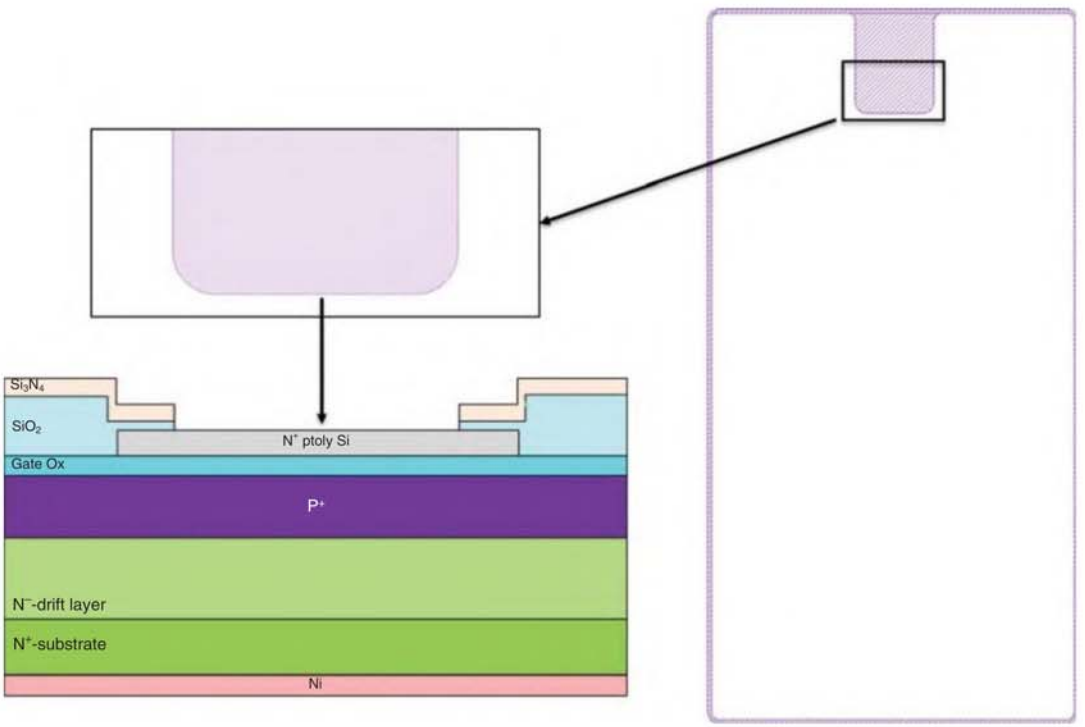


Figure 11.19 Mask #8: Gate Runner.

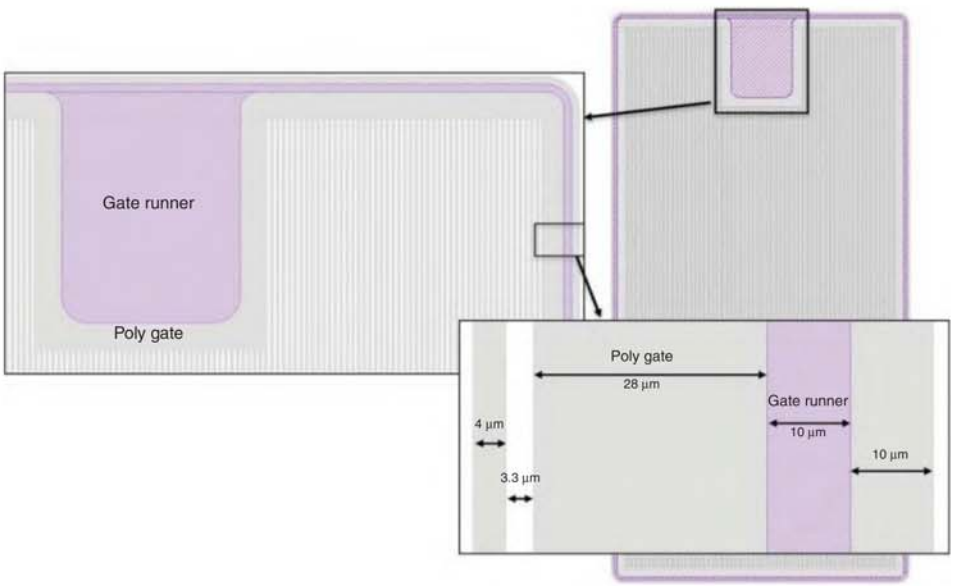


Figure 11.20 Mask #7 (Gate Poly) and #8 (Gate Runner) together.

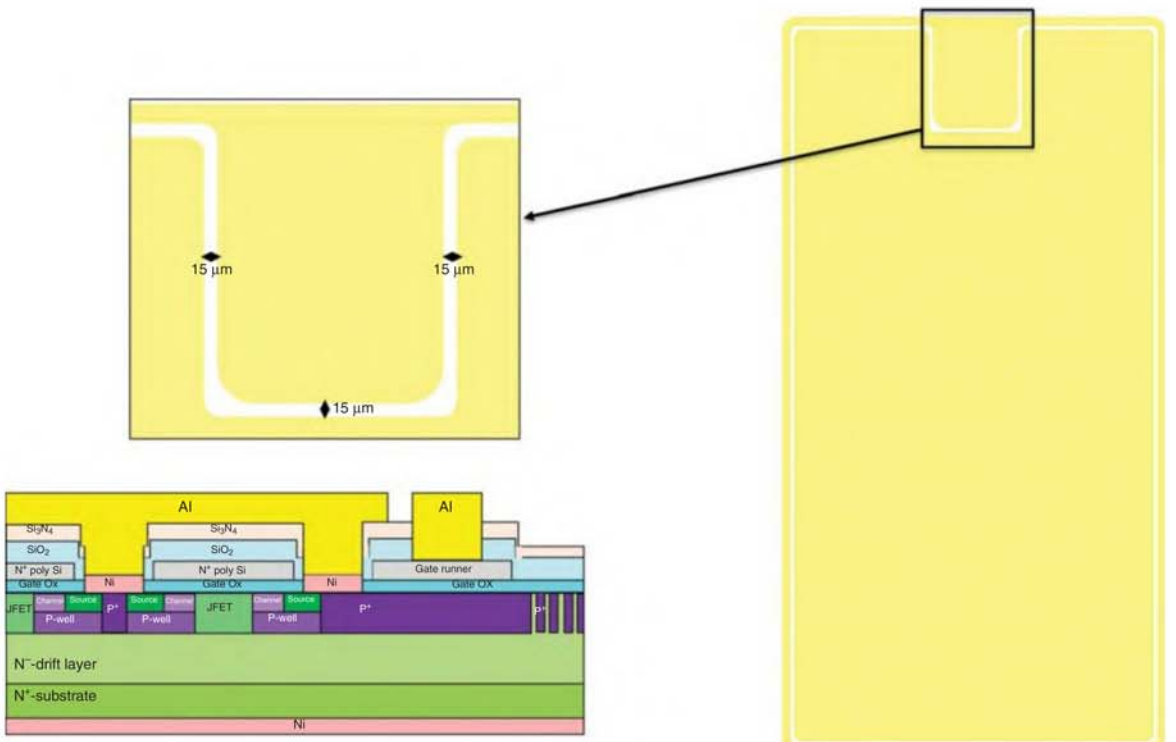


Figure 11.21 Mask #9: Overlayer Metal.

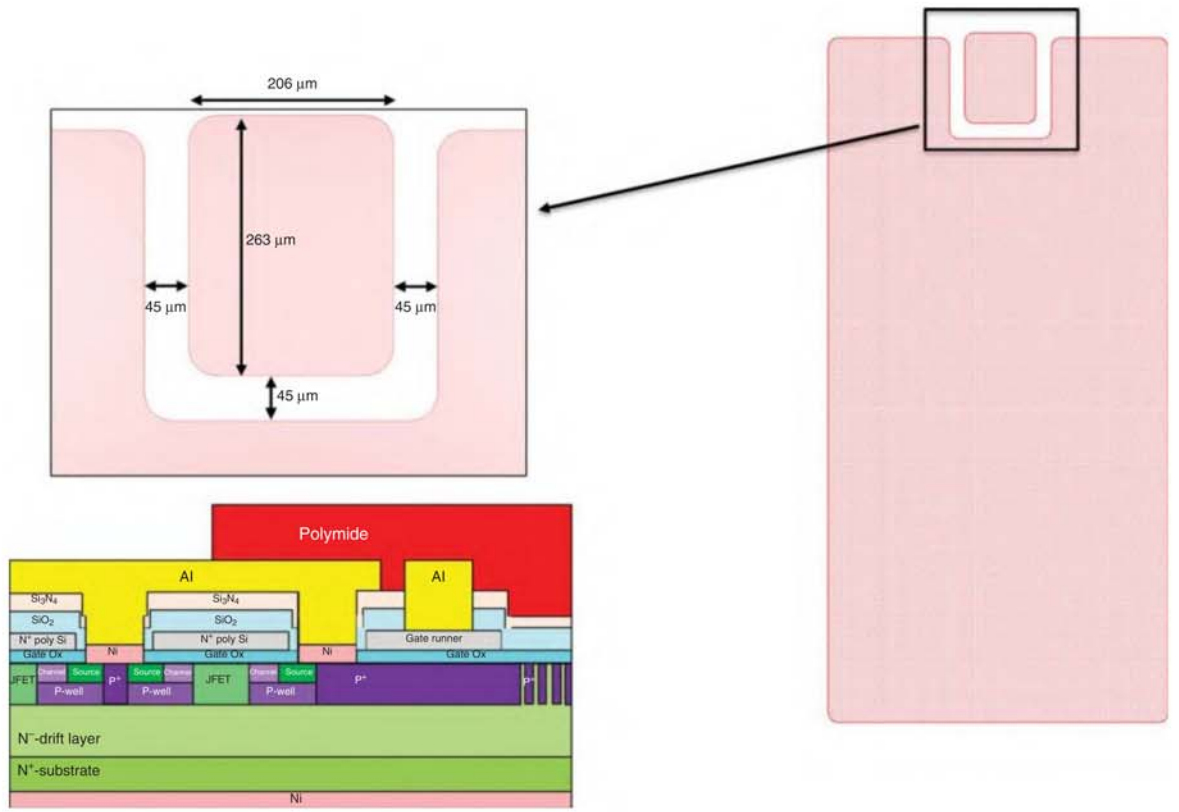


Figure 11.22 Mask #10 (Polyimide).

or hillocks on the surface [7]. Therefore, a dry etch process is generally utilized for SiC Technology [1–40].

The main difference between Si and SiC dry etching is how carbon is removed from SiC. In this process, generating positive ions and active radicals on plasma are accelerated toward the sample and induce physical and chemical etching, respectively. Three main etching gas systems are generally utilized for etching the SiC samples: fluorine-based (SF_6, CF_4, NF_3, BF_3, CHF_3), chlorine-based (Cl_2, $SiCl_4$, BCl_3), and bromine-based (Br_2, IBr) [7, 34]. Among these different gases, the fluorine-based ones make more volatile products thus resulting in higher etch rates. In order to increase the active species and enhance the etch rate one can add O_2 and Ar [13, 31]. In contrast, adding H_2 results in a lower etch rate [7] but may reduce micro-masking.

Inductively coupled plasma (ICP) and reactive ion etching (RIE) are widely employed for Si and SiC dry etching. RIE with a photoresist mask results in a faster process than ICP with a SiO_2 or metal mask. In an RIE, one can enhance the etch rates by increasing the direct current (DC) self-bias and plasma density. However, increasing the DC self-bias results in an increase of energy of ions which causes more surface damage. In addition, increasing the plasma density raises isotropic etching and can jeopardize the vertical sidewalls. Koutarou et al. reported that deep levels are also induced by the RIE process in both n- and p-type 4H-SiC [41]. Therefore, an ICP processing is preferred for SiC dry etching.

In ICP dry etching, by utilizing an radio-frequency (RF) power to an inductive coil, one can produce a high plasma density at low pressure with low ion energies. It results in a lower ion bombardment damage than the RIE [36]. It should also be noted that employing a mask oxide instead of metal in ICP prevents the trenching effect [37]. In order to improve the surface damage after dry etching, a sacrificial oxidation process needs to be utilized [35, 38].

An important challenge in dry etching is the selectivity when both sample and mask are etched at the same time. For example, when a photoresist is used as a mask, it shows a low selectivity and cannot be used for forming a deep mesa. It is a good candidate for a shallow etch. For etching in a medium-range, oxide films like SiO_2 and Si_3N_4 are utilized. A deep etching process utilizes a metal mask such as Ni, Al, and Cu. However, their nonvolatile by-products named micromasks are formed on the surface. These micromasks act as tiny masks and result in nanopillars on the surface during dry etching. This leads to a considerably rough surface (see Figure 11.23). Adding H_2 results in a lower etch rate [7] but may reduce micro-masking.

Micro-trenches or the trenching effect in which the area close to the sidewalls has a deeper depth than the bottom of the trench is another issue in the dry etching process (see Figure 11.24). This effect is strongly related to the DC self-bias. Utilizing a high DC-self bias increases the ion bombardment at the base of the sidewalls due to the deflection of ions impinging on the sidewall at low angles [12]. Therefore, all parameters such as DC-self bias, RF power, pressure, and gases flow should be comprehensively optimized in order to achieve an acceptable dry etch result.

Recently, Yu et al. reported an SiC deep dry etching of 184 μm utilizing a stacked layer of Ti/indium Ti oxide (ITO) with a ratio of 20 nm/2 μm as a hard mask to form a waffle structure on a SiC substrate (see Figure 11.25) [24]. ITO does not react with

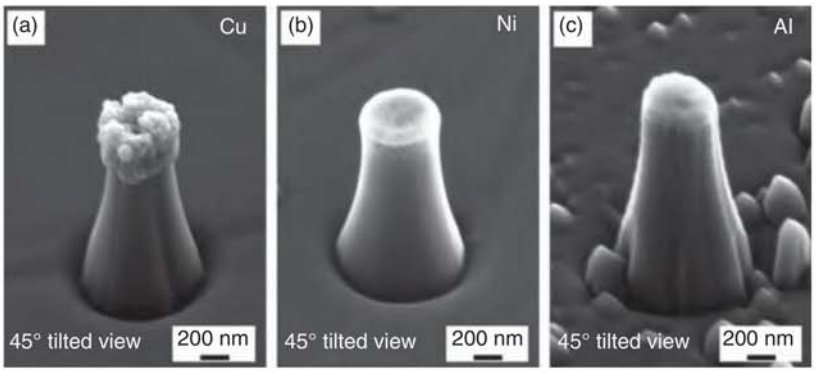


Figure 11.23 SEM images of nanopillars with (a) Cu, (b) Ni, and (c) Al metal mask (45° tilted view). Source: Choi et al. [13].

Figure 11.24 Micro-trenching side effect in a 4H-SiC dry etching. Source: Luna et al. [31].



fluorine ions and is stable under high energies. They reported a vertical sidewall with no micro-mask and micro-trenching in this work. Thinning a 4H-SiC substrate by chemical mechanical polishing (CMP) followed by forming a waffle structure could be used for lowering the on-resistance of the devices (up to 1200 V) by reducing the resistance of the substrate [39]. For a device with a voltage ≥1200 V, the main resistance component comes from the drift layer. Therefore, it is not worth performing this process on the substrate which raises the cost.

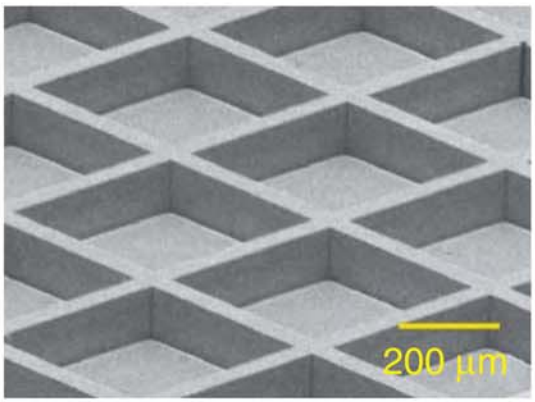


Figure 11.25 A waffle structure on a 4H-SiC substrate formed by dry etching. Source: Yu et al. [24].

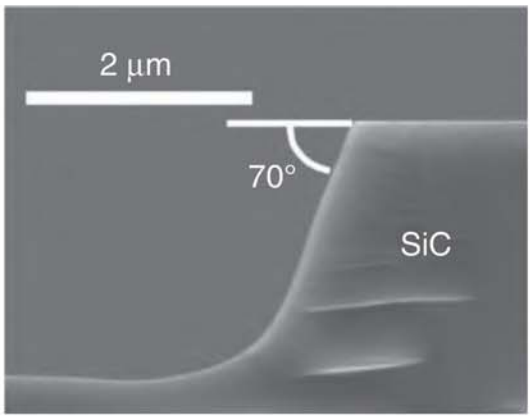


Figure 11.26 Improved bevel mesa formed with the optimized RIE condition. Source: Hiyoshi et al. [40].

When a rounded bottom is needed in a device (edge termination area as an example), one can form it by wet etching the SiO_2 mask followed by SiC dry etching (see Figure 11.26) [40].

Metal masks are generally avoided to reduce the contamination throughout the processing. A SiO_2 layer deposited by chemical vapor deposition (CVD) is a good candidate for a mask. By optimizing all etch parameters and adding O_2, one can increase the selectivity and form the trenches with a proposed angle.

One can conclude that, although the SiC dry etching has been developed in recent years, there are some issues such as vertical sidewalls, micro-trenching, micro-masking, and surface roughness that have not been fully optimized and need a comprehensive investigation. The process optimization of dry etching is very useful for trench MOSFETs.

11.3.3 Ion Implantation and Activation Annealing

Three different technologies generally can be utilized for the doping process in the semiconductor technology: diffusion processing, in situ doping during crystal and epitaxial growth, and ion implantation. Since SiC has wide bandgap energy and

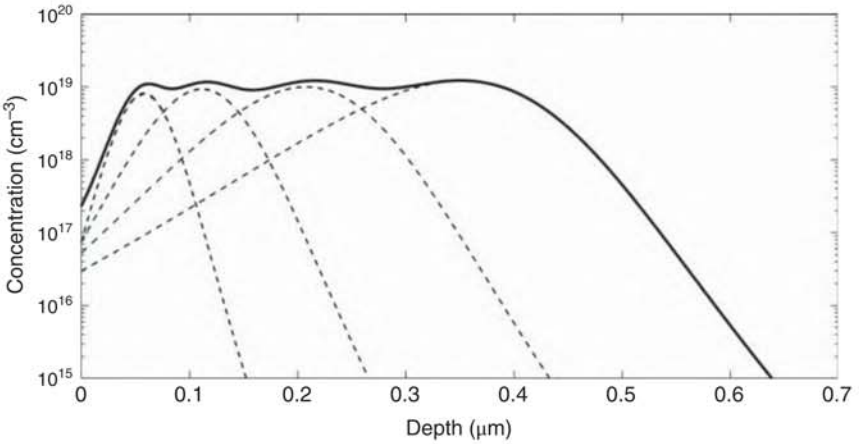


Figure 11.27 Simulation profile of N implantation for forming N^+ in 4H-SiC according to [42].

small interatomic distances, the main dopants have negligible diffusion coefficients even at high temperatures (>2000 °C). Diffusion processing in SiC is only available for small atoms such as H, He, Li, B, and Br [7, 34]. To predict the implant profiles by implanting various ions into different targets, Monte Carlo simulations, like SRIM (stopping and range of ions in the matter), are utilized.

Shielded DMOSFET results in a lower electric field peak in the JFET region and low saturation drain current at high drain voltages without compromising device on-resistance making this structure a preferred design to have a better short circuit capability [1]. This structure needs four ion implantation steps for forming the JFET region, P well, and P^+ shield under the P well (with one mask and process step), N^+ source, and P^+ into the N^- drift layer. In general, N and phosphorus are utilized for forming n-type regions, whereas Al and B are used for forming p-type regions. Figure 11.27 shows a simulation result of a nitrogen profile for forming an N^+ source with a doping concentration of 10^{19} cm^{-3} according to [42]. It consists of four implantation steps at room temperature with the energies of 35, 70, 140, and 260 keV and doses of 3.5×10^{13}, 7×10^{13}, 1.2×10^{14}, and 2×10^{14} cm^{-2}, respectively.

It should be noted for forming N^+ regions with a doping concentration greater than 10^{19} cm^{-3} (required for low ohmic contacts), phosphorous implantation results in a lower sheet resistance than an N implantation owing to its higher solid solubility limit [43, 44]. Therefore, P implantation at high temperatures is preferred for such a heavily doped N^+ region. Likewise, Al implantation results in lower sheet resistance than boron (B) implantation for forming P^+ regions with a doping concentration greater than 10^{19} cm^{-3}; thus, Al is preferred for heavily doped P^+ regions [7].

In recent years, there has been considerable interest in ion implantation study in SiC technology utilizing several ions [42–77]. Most of these works have studied the effect of ion implantation and its post-activation annealing in the SiC. The implantation energy needed to achieve a given depth in SiC is higher than Si due to the higher atomic density of SiC [7].

A valuable advantage of the ion implantation process is doping in the selected area by utilizing a mask and avoiding the wet or dry etching for forming the lateral structure. The type and thickness of the mask are related to the dose and energy of the ions. Photoresists, SiO_2, and some metals are utilized as a mask. It should be thick enough and robust at high temperature to stop the ions in the masked areas.

It should be noted that to prevent a highly damaged lattice in SiC, the implantation process should be done at elevated temperatures (300–800 °C), especially when the dose is higher than 10^{15} cm^{-2}. Otherwise, it results in an amorphous structure at the surface, and there is no guarantee to recover the lattice and obtain the original polytype of SiC with any high-temperature annealing [7]. However, room temperature implantation could be performed for lower doses ($<10^{15}$ cm^{-2}) [75]. Ion implantation generally causes some damages to the crystal lattice in which the ions can kick out the Si and C atoms from their lattice positions thus leaving vacant lattice sites [76]. It is worth noting that the C displacement rate is higher than the Si displacement. Thus, the implanted ions can occupy the interstitial lattice sites. They should be steered to substitutional lattice sites to be electrically active. Therefore, a post-high-temperature activation annealing (>1600 °C for SiC) is necessary to activate the dopants (>95%) even if the implantation has been done at elevated temperature [7]. In this process, the interstitial ions compete with interstitial Si and C atoms to take the vacancies in the crystal lattice and be electrically active. During the activation annealing, a capping layer like SiO_2, Si_3N_4, AlN, or graphite (carbon) should be deposited on the SiC surface to suppress the migration of surface atoms and Si desorption [7]. Negoro et al. reported that utilizing a carbon cap layer in an Ar ambient provides the most successful results [43]. Figure 11.28 shows atomic force microscopy (AFM) images of Al^+-implanted (with a total dose of 10^{16} cm^{-2}) off-axis 4H-SiC (0001) annealed at 1800 °C for five minutes with and without a carbon cap layer [7]. It shows utilizing a carbon cap layer results in better surface roughness.

As discussed above, the implanted ions make Si and C vacancies in the lattice. These vacancies become mobile during high-temperature annealing forming some

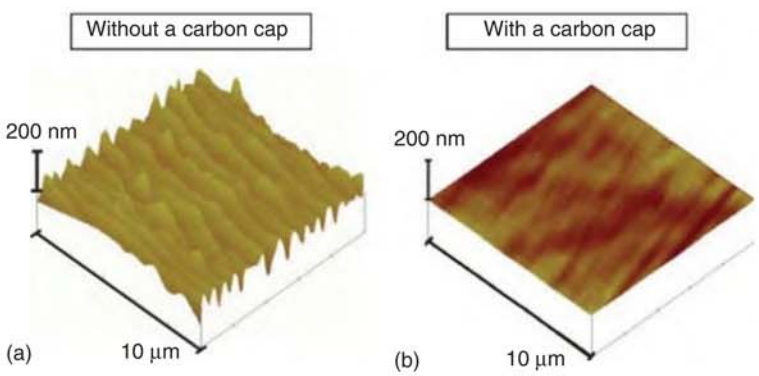


Figure 11.28 Atomic force microscopy (AFM) images of Al^+-implanted (with a total dose of 1016 cm^{-2}) off-axis 4H-SiC (0001) annealed at 1800 °C for five minutes with and without a carbon cap layer. Source: Kimoto and Cooper [7].

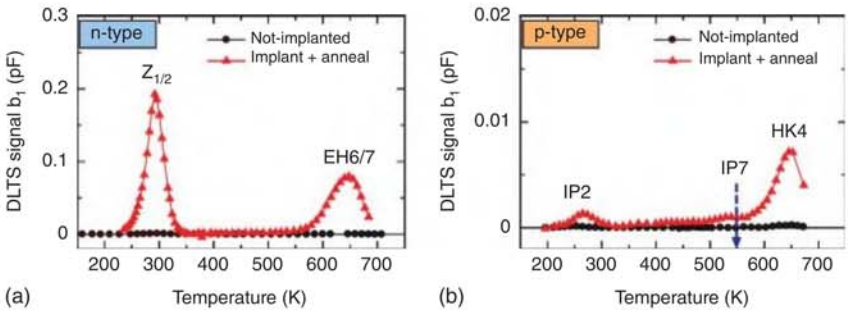


Figure 11.29 The DLTS spectra obtained from Al^+- room temperature implanted followed by annealing at 1700 °C for 20 minutes in (a) n-type and (b) p-type 4H-SiC epitaxial layers. Source: Based on Kawahara et al. [80].

defects such as vacancy clusters, interstitial clusters, and anti-site vacancy pairs [7]. These defects act as localized shallow- or deep levels in the bandgap thus affecting the on-state and off-state characteristics. For example, $Z_{1/2}$ ($E_C - 0.63$ eV) [77], $EH_{6/7}$ center ($E_C - 1.55$ eV) [78], and HK4 center ($E_V + 1.45$ eV) [79] are three major deep levels generated during this processing. $Z_{1/2}$ centers caused by C vacancies are one of the most important defects in SiC known as carrier lifetime killer which causes higher on-resistance, lower reversed recovery charges, and faster switching in pn junctions. Figure 11.29 shows the deep level transient spectroscopy (DLTS) spectra obtained from Al^+-room temperature implanting followed by annealing at 1700 °C for 20 minutes in (a) n-type and (b) p-type 4H-SiC epitaxial layers [80]. It shows how this process results in an increase of these defects.

Additionally, the ion implantation followed by high-temperature annealing can form basal plane dislocations (BPDs). This effect may be strongly dependent on the implant temperature, annealing temperature, the quality of the graphite cap, etc. This high-temperature processing results in stress within the SiC thus causing movement of pre-existing dislocations and even making new dislocations. The BPDs are reported to act as a source of expanding stacking faults (SFs) formation during the bipolar injection. These SFs induce energy levels in the SiC bandgap which act as recombination centers, decreasing the minority carrier lifetime in the drift layer. This may result in an increased forward voltage drop during the on-state mode, i.e. bipolar degradation [36, 81].

Today, there are various companies providing ion implantation for SiC technology processing with different doses, energies, temperature, and sources. Table 11.1 summarizes these companies available around the world.

11.3.4 Oxidation and Oxide

Both Si as an elemental semiconductor and SiC as the only compound semiconductor have a unique advantage over the other semiconductor materials of thermally grown SiO_2 on their surfaces. It is worth noting that Si_3N_4 is generally utilized as a moisture barrier in the Si and SiC technology. The SiO_2 layer can be employed

as a gate dielectric in MOSFETs. The main difference in the thermally grown SiO_2 layer on Si and SiC surfaces is the presence of C atoms in the SiC. The quality of the grown SiO_2 layer plays an important role in device reliability and on-state and off-state characteristics. This quality is related to the oxidation condition, surface roughness before deposition, semiconductor material, the device area, post-annealing condition, etc. The channel mobility is a good example showing how poor quality of the SiO_2 layer at the SiO_2/SiC interface lowers the mobility by an order of magnitude. Although the bulk electron mobility in an n-type 4H-SiC may reach to about 1000 cm^2/V-s, it degrades to about 10–30 cm^2/V-s in an n-channel of a MOSFET. This is due to the presence of a high-density interface states at the SiO_2/SiC interface especially close to the conduction band [82]. Dangling bonds at the SiO_2/SiC interface also contribute to the interface state density.

Moreover, the presence of the fixed charges in the gate oxide affects the threshold voltage and its stability. In addition, SiO_2/SiC has a lower barrier height than the SiO_2/Si interface. This results in higher tunneling current at the higher electric field and elevated temperature and affects the oxide reliability. As a result, the growth of gate oxide film, improving its quality, and its effects on device performance have been considerably studied in the last few years [82–120].

The thermal growth of SiO_2 on Si and SiC is performed by oxidation in dry (O_2) or wet (H_2O) oxidation in an oxidation furnace. The wet oxidation is faster than dry oxidation in SiC [34]. To enhance the oxidation growth rate of SiC, an elevated temperature (>1000 °C) is utilized. Figure 11.30 shows how oxide thickness is increased at elevated temperatures in dry thermal oxidation of the a-face of 4H-SiC [83].

In the oxidation process of SiC, the free C atoms escape from the surface through the formation of CO gas or remain at the surface and form C clusters at or near the SiO_2/SiC interface. These C clusters affect the electrical properties at the interface [34] such as channel mobility in the SiC MOSFETs. Although one can decrease

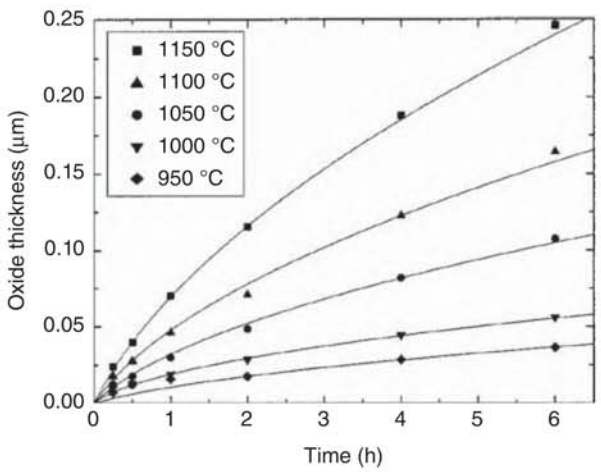


Figure 11.30 Oxide thickness as a function of time and temperature for dry thermal oxidation of the a-face of 4H-SiC. Source: Song et al. [83]. © 2004, AIP Publishing.

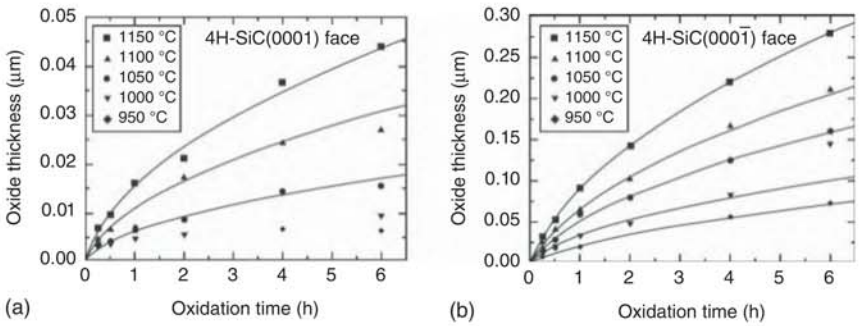


Figure 11.31 Oxide thickness of 4H-SiC for (a) Si-face and (b) C-face as a function of oxidation time at different temperatures. Source: Kimoto and Cooper [7]. John Wiley & Sons. © 2014, John Wiley & Sons.

these C clusters at the interface by depositing SiO_2 instead of the thermal growth process, the quality of the deposited layer is still under investigation [34].

The thermal oxidation growth rate of SiC is much lower than Si. The thermal oxidation of C face is about three to ten times faster than Si face in SiC [34]. The rate is related to the temperature of the oxidation process. Figure 11.31 shows the oxide thickness of 4H-SiC for Si-face and C-face as a function of oxidation time at different temperatures. Other faces like a-face and m-face have thermal oxidation rates between the Si- and C-faces (see Figures 11.30 and 11.31). This processing becomes important in trench shape structures like trench MOSFETs in which the side walls oxidize more than three times faster than the bottom of the trenches. It is also worth noting that the oxidation rates are increased for the implanted regions and decreased for the dry-etched regions [34].

Despite a lot of optimization and enhancement of the thermally grown oxide quality in SiC processing, the SiC/SiO_2 interface has a high density of interface state defects. It 'is about two orders of magnitude higher than for the Si/SiO_2 interface which affects the reliability and performance of the SiC power devices [117]. This topic is discussed in detail in the chapter written by Thomas Aichinger and Gregor Pobegen in this book.

Most of the interface states in the lower half of the SiC bandgap (near the valance band) are donor like [7]. They capture the holes in and do not release them at room temperature [118]. These holes act as positive fixed charges. It has been reported that wet oxidation results in better quality than the dry oxidation and lowers the density of these donors like states at the SiC/SiO_2 interface [118].

Likewise, most of the interface states in the upper half of the SiC bandgap (near the conduction band) are acceptor like. They capture electrons and do not release them at room temperature. These electrons act as negative fixed charges at the interface. It is worth noting that in an n-channel MOSFET, when an inversion layer is formed by a positive gate voltage, many electrons may be captured in these states. The captured electrons become immobile and act as Coulomb scattering centers thus lowering the effective n-channel mobility (5–8 cm^2/V s with no POA [7]). Most recent work at the time of proof reading this chapter was reported by Kobayashi et al. This work was

able to reduce the interface states in the upper half of the band gap to very low numbers equivalent to what is generally found in Si MOS structures by using hydrogen etching, oxidized silicon at 700 °C and POA with Nitrogen gas at >1400 °C. [Applied Physics Express 13, 091003 (2020)].

Afanas'ev et al. reported that the source of the donor-like interface states is carbon clusters, whereas the source of the acceptor-like interface states is near interface states [119, 120]. These states are located inside SiO_2 close to the interface and act as a trap for electrons.

11.3.5 Post Oxidation Annealing

POA is a good method to passivate dangling bonds at the interface and reduce fixed positive charge in the gate oxide films. In Si technology, a hydrogen-containing gas, like an H_2–N_2 mixture, at 400–500 °C is utilized to lower the interface state density (D_{it}) to about 10^9 eV^{-1} cm^{-2} [121]. Fukuda et al. reported that in SiC technology, hydrogen POA needs to be done at elevated temperatures (about 1000 °C) to reduce the D_{it} to about 10^{11} eV^{-1} cm^{-2} [122].

A popular way for reducing the fixed oxide charge and D_{it} in SiC processing is a POA in an inert gas such as Ar and N_2 at the same temperature of the oxidation (1100–1200 °C) [7]. In addition, it was reported that Ar POA results in an improvement in the dielectric properties and reliability of oxides [99]. Kato et al. reported that an Ar POA at high temperature (1300–1350 °C) after thermal oxidation followed by N_2O annealing results in diffusion of accumulated carbon atoms at the SiO_2/SiC interface. This process results in an improvement of the peak value of field-effect mobility from 19 to 33 cm^2/V-s [123].

As discussed in the previous section, wet oxidation generally has better quality than dry oxidation. It shows a significantly lower D_{it} near the valance band and slightly lower D_{it} near the conduction band. Therefore, it results in better hole mobility in a p-channel device. However, for improving the electron channel mobility in an n-channel device, one can utilize dry oxidation at a high temperature of about 1250–1300 °C. This can reduce the D_{it} near the conduction band [7]. However, when the oxide thickness exceeds 20 nm, the D_{it} is increased as shown in Figure 11.32 [124]. These results show the D_{it} and V_{fb} values as a function of oxide thickness with no POA process after dry oxidation. The positive flat band voltage (V_{fb}) shift shows an increase of the negative fixed charges in the oxide by increasing the oxide thickness.

In recent years, there has been a considerable interest to lower the D_{it} by post-oxidation nitridation in a nitrogen-containing gas such as nitric oxide (NO) [105, 110, 111, 125–135], nitrous oxide (N_2O) [136, 137], ammonia (NH_3) [138, 139], and in the presence of nitrogen radicals [140]. Figure 11.33 clearly shows how N_2O and NO POA results in a lower D_{it} over the entire range of energies within the bandgap [7]. This causes the dangling bonds to passivate and remove the interstitial carbon and carbon clusters left in the oxidation process [111]. It should be noted that two mechanisms compete during POA in NO or N_2O ambient, i.e. nitridation and oxidation. Figure 11.33 illustrates how NO POA results in lower D_{it} than N_2O POA.

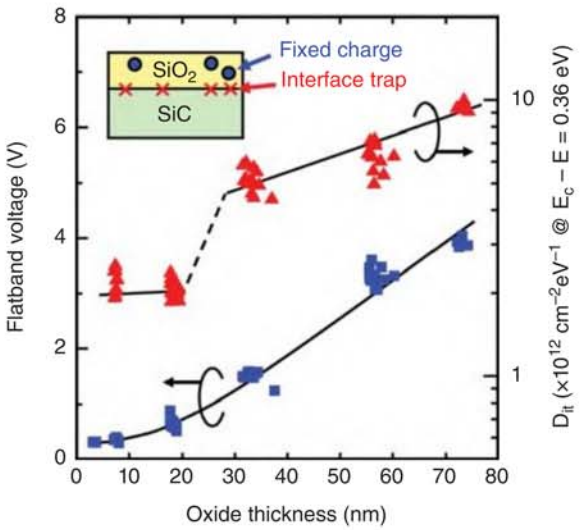


Figure 11.32 D_{it} and V_{fb} values as a function of oxide thickness with no POA process after dry oxidation [124].

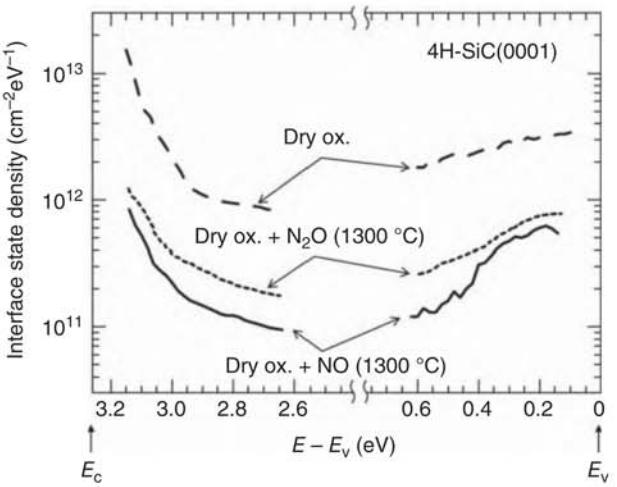


Figure 11.33 Reduction of the D_{it} over the entire range of energies within the SiC bandgap in 4H-SiC (0001) MOS capacitors utilizing N_2O and NO POA. Source: Kimoto and Cooper [7]. © 2014, John Wiley & Sons.

Decomposition of N_2O results in N_2, O_2, and NO. Figure 11.34 shows the percentage of NO is increased by increasing temperature. One can conclude that N_2O POA should be done at higher temperatures than the NO POA to increase the nitridation and decrease the oxidation.

Figure 11.35 shows the positive/negative bias threshold voltage instability (PBTI/NBTI) tests for five different commercially available 1200 V 4H-SiC MOSFETs. Due to the existence of these traps, when a positive DC bias is applied to the gate over a long period of time, the threshold value shifts in the positive direction due to the tunneling and capture of electrons by near interface traps. Conversely,

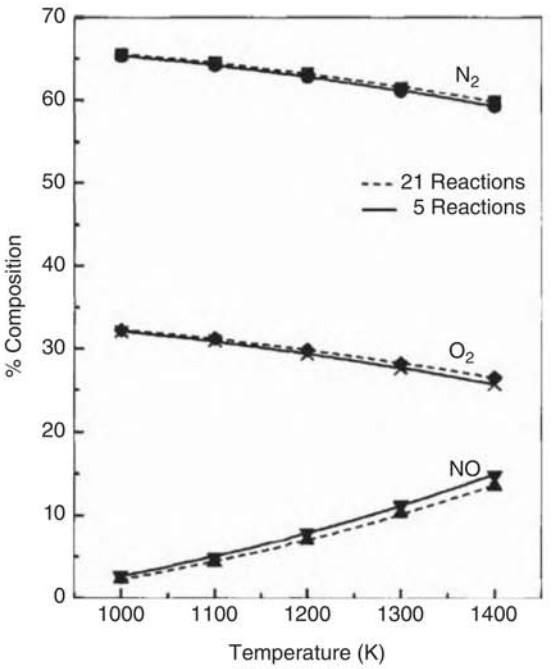


Figure 11.34 Gas composition in the decomposition of N_2O at various temperatures. Source: Gupta et al. [141]. © 1998, Elsevier.

when a negative bias is applied to the gate over a long period of time, the threshold voltage shifts in the negative direction resulting in a significant increase in leakage current in the off-state. Furthermore, a negative shift of threshold voltage can cause devices to turn on unexpectedly and lead to failures. We investigate this particular trap-induced device degradation on commercially available devices by applying positive voltage stress on the gate over a long period of time, with source and drain grounded. At the end of each stress, transfer characteristics (I_D–V_G) were measured to determine the threshold voltage shifts. The considerable variance between devices from different vendors was observed implying that while some vendors have been able to significantly reduce the near-interface traps in the gate oxide, the others may still need some development.

11.3.6 Poly-Si Deposition

Polysilicon is normally utilized as gate electrode material in metal–oxide–semiconductor (MOS) devices as shown in Figure 11.1. LPCVD is normally utilized for polysilicon deposition [143–150]. It can be undoped or doped with some elements such as N or P. The dopants can be incorporated in situ during the deposition or later by diffusion or ion implantation. Phosphorus doping of polysilicon is very popular in the Si industry as the phosphorus helps to getter the impurities in the gate oxide films during the soak at 800 °C. A higher final doping of the poly Si allows lower internal gate resistance and therefore more homogenous switching of the device in case of fast gate voltage transients.

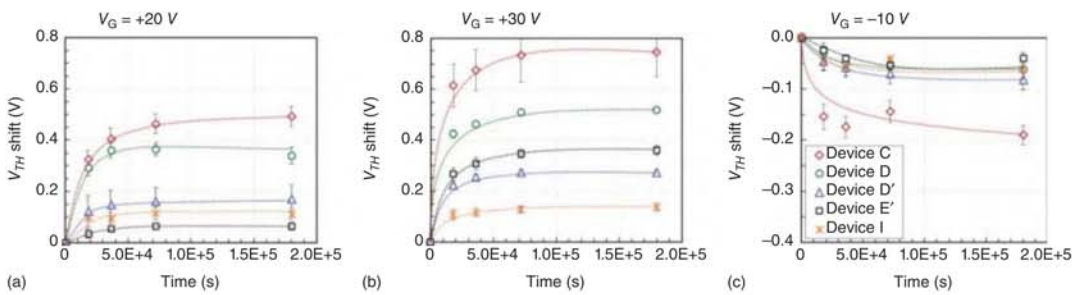


Figure 11.35 Time-dependent threshold voltage shifts for (a) positive bias-stress of +20 V, (b) +30 V, and (c) negative bias-stress of −10 V for 50 hours for different commercial available 1200 V 4H-SiC MOSFETs. Source and drain were grounded at room temperature. Source: Yu et al. [142]. © 2020, IEEE.

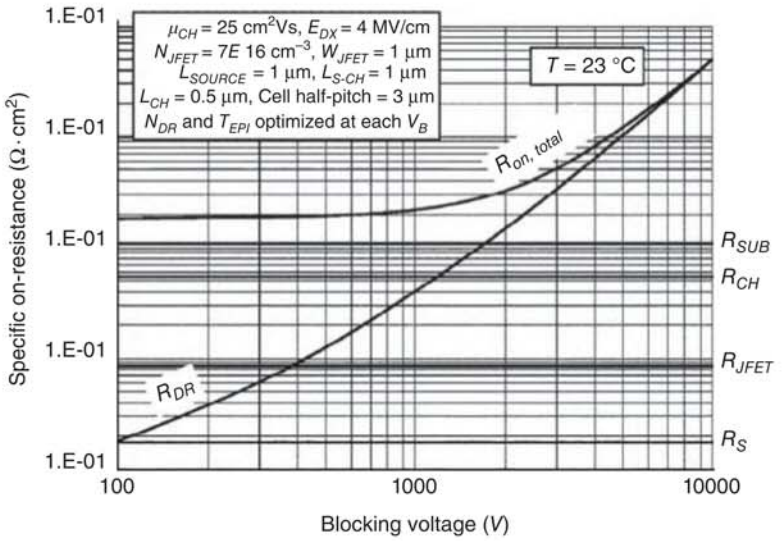


Figure 11.36 The internal resistance components state-of-the-arts SiC power MOSFETs as a function of blocking voltage. Source: Cooper [39].

11.3.7 Backside Thinning and Waffle Substrates

Specific on-resistance ($R_{on,sp}$) of a power DMOSFET has several internal resistance components such as source resistance, channel resistance, JFET resistance, drift resistance, and substrate resistance [39]. $R_{on,sp}$ plays a key role in power devices because the cost of a power DMOSFET scales as the square root of $R_{on,sp}$ at a given on- and off-state performance [39]. For example, if $R_{on,sp}$ decreases four times, the total cost might lower to about two times. Figure 11.36 shows the 4H-SiC substrate resistance is a dominant resistance below about 1700 V. This component is even more important for diodes since they do not have contributions from MOSFET channel. Therefore, lowering this component in the SiC devices below 1700 V could be considered for lowering the total cost. To date, two techniques have been reported for lowering the substrate resistance, i.e. wafer thinning and waffle structure.

Backside wafer thinning was reported by Rupp et al. [151]. This process includes wafer grinding at the last steps of the fabrication in which the substrate thickness is lowered from about 350 to <150 µm. This process results in better electrical and thermal behavior of the SiC devices. It is worth noting that one cannot reduce the thickness more than this range due to an increase in the probability of the wafer bowing and breaking. Cooper reported a technique named waffle substrates for thinning the substrate up to 50 µm [39]. In this technique, the substrate thickness is firstly lowered by backside wafer thinning as above. Then, the waffle structure is made by SiC dry etching utilizing a metal mask (see Figure 11.25). Finally, a suitable metal is deposited on the backside. It should be noted that since both of the above techniques are done at the last steps of the processing, one cannot utilize regular post metal annealing for creating a proper ohmic contact. However, a laser annealing

with a suitable spot area and energy could be utilized after the metallization on the backside of the wafer.

11.3.8 Ohmic Contacts and Metallization

Although some devices such as metal–semiconductor field-effect transistors (MESFETs) and Schottky diodes utilize a Schottky contact, a proper metallization with a good ohmic contact is needed for other devices because a large voltage drop in a poor ohmic contact leads to power loss. A sacrificial oxidation process after ion implantation and dry etching is often used before the metallization to remove damage in SiC.

Three different methods can be used for metal deposition on Si or SiC samples: evaporation, sputtering, and CVD. Evaporation should be performed in an ultra-clean vacuum system to achieve higher rates of deposition. However, poor adhesion of the metal to the sample can be a problem in this method. Sputtering is considered a fast and economical method with good adhesion; however, it might be problematic for lift-off patterning. Although Ni is mostly used as metal for n-type 4H-SiC, different compounds such as Ti [152], Al/Ti [153], Ti/Al [153, 154], Ni/Al [155, 156], Ni/Ti/Al [156, 157], and Ti/Ni/Al [157] have been reported for p-type 4H-SiC metallization.

A key factor for forming good ohmic contacts is post-metal annealing (PMA) in an oxygen-free ambient. It is worth noting that very high-temperature annealing may result in a rough contact surface morphology [156] and might be problematic for adhesion of over-layer metal, poor alignment accuracy in the photolithography process, and reliability of the contacts. Therefore, optimizing the annealing temperature is necessary to have good ohmic contact for all structures at lower temperatures. As Ni atoms can be mobile at about 450 °C, a temperature of 700 °C might be high enough to form the *Nickel-Silicide* for n-type ohmic contacts [36]. However, to achieve good ohmic contact with a high intensity of NiSi and $NiSi_2$ contacts, a temperature of about 960 °C is needed [158–160]. To have good ohmic contact for p-type 4H-SiC, a lower temperature (750–850 °C) is required [157]. It has been reported that among different intermetallic phases, Ti_3SiC and $NiSi_2$ show a significant effect in the formation of p-type ohmic contacts [161].

Although the self-aligned silicide process (Salicide) has been used in Si technology for many years, it has been recently reported in SiC technology [5, 162]. In this process, first, a SiO_2 layer is deposited and patterned on the SiC surface. Then a metal like Ni is deposited and first step annealing (FSA) is performed at lower temperatures (700–800 °C) as shown in Figure 11.37. This forms one phase of Ni silicide in the contact openings (VIAs). There is no reaction between Ni and SiO_2 and unreacted Ni can be easily removed by Piranha clean. One can increase the intensity of the Ni silicide by performing the second step annealing (SSA) at higher temperatures.

A *Nickel-Silicide* is also used for the backside metallization of the wafer for having a low resistivity contact for the 4H-SiC processing technology [36, 38, 163, 164]. It should be noted that the native oxide on the backside should be removed by wet–dry etching before Ni deposition as shown in Figure 11.18.

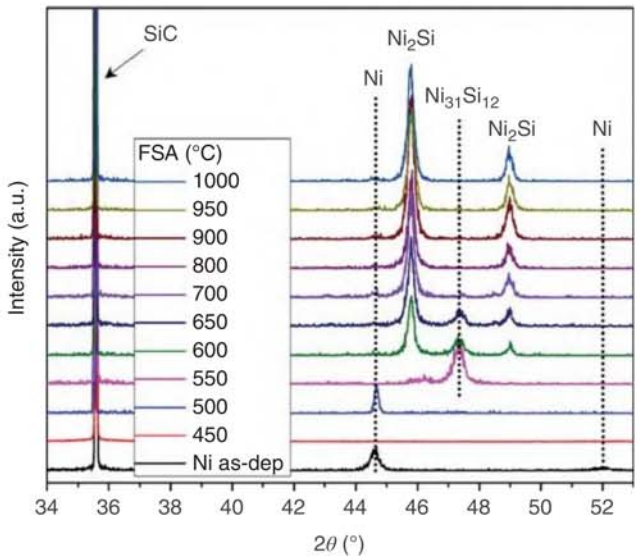


Figure 11.37 The X-ray diffraction (XRD) spectra of the Ni contact layer after the first step annealing (FSA) at different temperatures and removal of unreacted Ni. Source: Elahipanah et al. [5]. Licensed under CC BY 4.0.

An overlayer metal on the topside is utilized to connect the source cells together and also provide a low resistance path on the gate runner. A thick layer (typically 3–5 μm) Al is sputtered on the wafer. It also provides an appropriate surface for wire bonding in packaging. Similarly, an overlayer metal on the backside is needed to achieve a desired current distribution. A stacked-layer metal of Ni/Ti/Ag or Ni/Ti/Au is popular for the backside overlayer metal. It worth noting that the processed wafers need to be shipped in vacuum in the case of using Ag to prevent oxidation of silver.

11.3.9 Polyimide Deposition

The last step to process before dicing and wire bonding is a deposition of suitable passivation layer to achieve the electrical insulation of the components in high-voltage devices [145, 149]. Polyimide (PI) materials are considered as suitable candidates due to their excellent intrinsic properties such as high dielectric breakdown fields ($E_{BR} > 2$ MV/cm), thermal stability (weight losses <1% at 500 °C), relatively low losses, and thermomechanical matching with components [148, 150]. Commercial polyimides for microelectronic applications may be prepared as polyamic acid (PAA) solution [148]. This solution is typically spun onto the wafer. Then, a thermal curing process at high temperature (>300 °C) in N_2 ambient for an hour [165] is utilized to drive off the solvent and initiate polyimide ring closure which produces the insoluble polyimide [143]. An alternative deposition method is CVD which results in a better uniformity in thickness [143, 147].

11.4 Commercial Foundries for Si and SiC Devices

Although SiC devices have become commercially available in the market, they are still more expensive than the Si devices. Moreover, there are additional equipment and/or unit process steps needed for SiC technology when implemented in a commercial Si Foundry. SiC substrates are available in 150 mm diameter with 200 mm on the horizon. Most Si foundries are at 200 mm or higher and therefore compatibility with 150 mm SiC substrates at the present time is not ideal. There are a few 150 mm Si foundries in the world which may take advantage of the SiC technology to add a few more years to their useful life. Cost model and new equipment and processing requirements are discussed in this section.

11.4.1 Cost Model

11.4.1.1 Cost Roadmap for WBG Devices

A cost reduction roadmap based on cost models and the Fabless Foundry concept has been developed by Woongje Sung and shows the feasibility of achieving *PowerAmerica* Institute's wide-bandgap (WBG) price goals in three to five years [166].

Referring to Figure 11.38, a DMOSFET structure with a pitch of 5 μm has been modeled by Woongje Sung. It has p^+ contact regions placed orthogonally to the n^+ contacts. The structure was modeled for various voltage ranges.

The doping and drift layer thickness values are shown in Table 11.1 along with modeled values for specific on resistances. The average inversion layer mobility was assumed to be 20 $cm^2/V\,s$ and the substrate thickness 180 μm. The chip size was calculated for a maximum current rating of 20 A (junction temperature of 150 °C) assuming a gate pad size of 0.4 mm^2, dicing lane of 50 μm, and edge termination width of five times the drift-layer thickness.

Assuming the price of a 150 mm SiC substrate and epilayer, as shown in Table 11.1 (these costs are based on basic calculations using SiC powder cost, capital cost

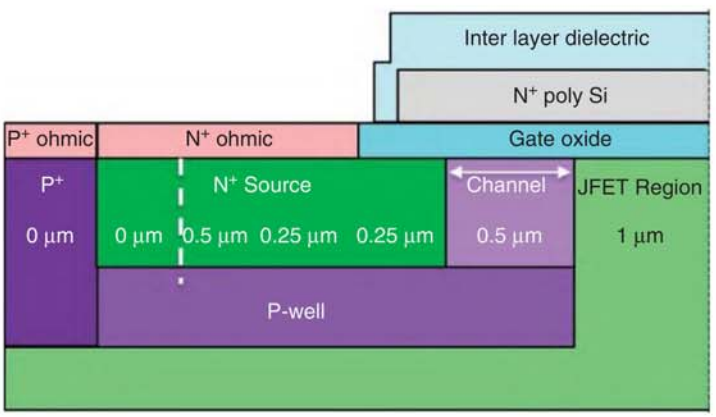


Figure 11.38 Cross-section of the MOSFET structure modeled.

of furnaces, and other equipment such as wafering and polish, manpower, and utility bills and adding in 25% profit margin by the supplier), a processing cost of $800/wafer (this can be reduced to $500/wafer in high volume), production in a commercial silicon foundry, and adding a gross margin of 50% (price = 2× the cost), the projected price of SiC chips is shown in Table 11.1. The overall yield is assumed to combine testing and manufacturing (breakage, miss-processing, etc.) yields. The price for a 1.2 kV, 20 A SiC chip is calculated to be 4.7 cents/A, significantly below the *PowerAmerica*'s target of 10 cents/A. The 15 kV SiC chip should be priced at $3/A assuming a yield of 50% and $3000 for the 150 mm substrate + epilayer.

If the industry can approach these numbers in three to five years (this seems to be very feasible given the demands of the automotive segment), then the device demand will grow exponentially across multiple applications. Furthermore, 200 mm SiC substrates, expected by 2020–2021, will further reduce the cost of SiC MOSFETs. Additionally, other devices such as JFETs are expected to cost significantly less due to their superior specific on-resistance.

This model applies to a fabless company manufacturing SiC power MOSFETs in a mixed Si/SiC foundry which buys 150 mm SiC substrates and epitaxial layers from vendors who have their own profit margins included in the price of the material. The sawing and testing cost is included in the foundry cost. What is not included is packaging yield (typically 95%) and packaging cost (typically 1–2 cent in large-volume packaging facility in TO-247 or equivalent package). High-voltage devices will require more sophisticated packages and modules which will cost much more.

Table 11.1 Calculation of potential price/Amp for 20 A max rated SiC chips at different voltages in a high volume commercial 150 mm mixed Si/SiC Foundry.

	1.2 kV	1.7 kV	3.3 kV	4.5 kV	6.5 kV	10 kV	15 kV
Drift layer doping (cm^{-3})	1×10^{16}	7×10^{15}	3×10^{15}	2×10^{15}	1.2×10^{15}	8×10^{14}	4×10^{14}
Drift layer thickness (μm)	10	15	30	40	60	95	145
$R_{on,sp}$ (mΩ-cm^2)	1.7	2.5	7.8	14.5	34.0	77.8	237.8
Chip area (mm^2)	3.7	4.5	8.0	11.0	17.3	28.0	50.9
Overall yield (%)	85	84	82	80	75	67	50
Packing factor	0.945	0.939	0.925	0.914	0.902	0.890	0.846
Price for 150 mm SiC + epilayer ($)	800	881	1126	1289	1615	2185	3000
Price per Amp ($/A) (50% Gross margin assumed)							
Price ($/A) for 20 A maximum	0.047	0.062	0.133	0.205	0.402	0.910	2.91

11.4.2 New Equipment and Processing Requirements

The requirements for additional equipment and/or unit process steps needed for SiC technology when implemented in a commercial Si Foundry are listed below:

1. *Dry etch*: Since SiC is relatively inert, it is not possible to use wet etching. Therefore, dry RIE equipment is needed to etch SiC such as alignment marks, backside etching of vias or thinning with a high etch rate, and trench etch for JFETs or trench MOSFETs. ICP etch systems are popular for etching SiC.
2. *Ion-implantation and post implantation anneal*: As mentioned earlier in this chapter, ion implantation above the amorphization dose of $10^{15}\,cm^{-2}$ is carried out at high temperature (350–650 °C). This requires implanters especially equipped with a hot wafer stage. Also, since annealing is carried out at approximately 1700 °C with a graphite cap layer, a special anneal equipment is needed for batch processing. The most important considerations are temperature ramp rates and temperature uniformity within the chamber across the substrate and from substrate to substrate in a stack of typically 10–24 substrates.
3. *Gate oxide furnace*: Gate oxidation is critical for SiC MOS devices. Presently, the high density of interface traps at the 4H-SiC/SiO_2 interface limits the effective inversion layer mobility in the 4H-SiC MOSFETs to typically 15–20 $cm^2/V\,s$. Even this low value is achieved by POA in NO gas at high temperatures. Therefore, specialized oxidation furnace (Quartz or poly SiC tubes), with dry oxidation capability, equipped with NO gas fittings and associated safety measures is required.
4. *Frontside ohmic contact rapid thermal anneal (RTA) furnace*: Typically, SiC ohmic contacts to the frontside are made with Ni (for n^{++} ohmics) and Ti/Al (for p^{++} ohmics) by evaporating 10–20 nm of metals and annealing them between 800 and 1050 °C for a few minutes. Separate RTA furnaces are recommended for SiC processing in a Si process line to avoid cross contamination.
5. *Backside ohmic contact and thinning systems*: It is important to thin the substrate to 100–150 μm from a standard thickness of 350 μm to reduce the substrate resistance from approximately 0.7 to 0.2–0.3 $m\Omega\,cm^2$. This is important in devices rated at 1200 V or below. This is completed as a last step in the process sequence by mounting the frontside of the processed wafer down on a lapping fixture and grinding the backside to the desired thickness. After this, the backside is cleaned while keeping the wafer mounted and a thin metal Ni layer is evaporated on the backside. The Ni is annealed by a raster scan of a laser beam. The wavelength of the laser beam is selected such that it is completely absorbed in a small depth of the SiC and the heat does not reach the frontside of the processed wafer. After this, suitable overlayer is sputtered on the backside and the substrate is released from the lapping plate. The suitable backside lapping and laser anneal systems are needed for this purpose. If the target device voltages are 1700 V or greater, then this step can be skipped.
6. *Transparent wafers*: SiC wafers are transparent to visible light. This may complicate photolithography as the focal plane is determined with the use of an optical microscope. Other tools may be needed (software/gain/hardware adjustments to

move to wavelengths where SiC is opaque) to process SiC wafers through steppers in a Si Fab.

7. *Steppers with long objective length*: Relative lack of flatness in SiC wafers can complicate photolithography and other processing particularly of high-voltage devices (thick drift epitaxial layers). High-temperature processes can further impact wafer flatness. For SiC power devices, "I-line" (365 nm) steppers are usually sufficient which can create 350 nm wide lines. Lense with a long objective length can help with focussing on warped wafers.

11.5 Dedicated Foundries vs. Commercial Foundries

SiC devices used to be fabricated in dedicated SiC foundries where the foundry is owned by one user. A good example is General Electric's 100 mm fab facility in Niskayuna, NY, and 150 mm fab at The New York Power Electronics Manufacturing Consortium (PEMC), led by SUNY Poly in Albany, NY. This model slowed down the development as many researchers and companies were left out since they could not afford to have their own Fabs. Building a dedicated Fab costs $100–200 M USD and takes a long time to become profitable because the fab has to be fully loaded. It should be noted that PEMC has closed its doors and is looking for industrial partners to be viable at the time of writing this chapter. However, the advantage of this approach is that the dedicated user has the full flexibility of changing the process as needed to improve the performance of SiC devices. This indeed has been proven since the GE devices have demonstrated the best performance and reliability.

PowerAmerica, in 2015, introduced the idea of a commercial Si Fab (XFAB in Lubbock, Texas) that can be equipped to handle a small volume of 150 mm SiC wafers along with a high volume of silicon wafers. This was accomplished by a small investment of less than $20 M shared equally by *PowerAmerica* and XFAB. These funds were used to buy SiC-specific equipment listed in the previous section. This enabled a lot of small companies to be fabless and yet utilize a well-functioning production facility with high yields where the major cost of running the fab is borne by high Si volume. This proved to be a highly successful model, and as a result, SiC design innovations and production increased rapidly by 25+ users, each with moderate volume. More players mean more innovations in the technology. A secondary benefit of this approach was that it provided a concept of adding 10–15 years to an otherwise obsolete Si foundry. This approach is now being used worldwide. However, XFAB evolved and grew with each user bringing its own process to the foundry. As a result, XFAB is having to manage many different process flows with minor differences between them. This makes it difficult to ramp up volume. Furthermore, small researchers and many small companies were left out of using XFAB as they did not bring enough volume to the fab. A big advantage of this approach has been to reduce the cost of SiC components very rapidly as the fab cost is lower by leveraging Si processes and equipment which are fully depreciated. The major cost of SiC fabrication is in starting material (substrates + epilayer) as seen in the discussion of cost earlier in this chapter. By combining volumes by many users, the foundry can get huge discounts on starting material.

The best approach would be to convert an existing commercial Si Fab to a mixed Si/SiC Fab, which can offer its own process flow and SiC-specific unit processes such that almost all users (small and moderately big) can use almost the same process with minor differences. This setup will allow users to bring their innovative design ideas to the market with a relatively small expense. The volume can be rapidly ramped up across 100+ users and cost can be further reduced. Having the same process means several projects can be combined on a single mask set so that the individual cost to each project can be further reduced along the lines of highly successful Si program called "MOSIS". Reducing the cost of innovation will prove to be a game changer in the future. As mentioned before, this can be done by investing $15–20 M USD by simply purchasing SiC-specific equipment listed in the previous section.

Another concept would be to build a fab dedicated to SiC manufacturing but run it as a prototyping or commercial foundry with one process flow and design rules. The number of users can again be ramped up easily. However, the initial capital cost of building an SiC-dedicated fab and ramping up the process over two to three years with small number of initial users may be a drawback of this approach. Clas-SiC foundry in Scotland has been fashioned after this model. As of writing this chapter, it has successfully developed the Schottky diode process and is engaged in developing a planar SiC MOSFET process. Once they are ready to offer the process and design kit to the users, it is expected that business will ramp up very quickly. Just getting there requires an investment of approximately 100 M USD. It may take five years to be profitable and fully load the foundry capacity.

As the volume goes up to 50–100 000 SiC wafers per month in the future, enabled by Electric Vehicles, and the 200 mm SiC substrates become the norm, many of the abovementioned foundry models will exist and will serve various needs of customers. It is absolutely certain that the fabless approach will bring about many innovations in this area.

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12

Unipolar Device in SiC: Diodes and MOSFETs

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12.1 Introduction

Power devices in 4H-silicon carbide (4H-SiC) show great performance advantages as compared to those made with other semiconductors. Compared to silicon, 4H-SiC has one order of magnitude higher breakdown electric field ($2–4 \times 10^6$ V/cm), while bulk electron mobility is only about 20% lower than that of silicon. The drift layer of a 4H-SiC power device may have one-tenth the thickness and one hundred times the doping concentration of the drift layer of a silicon power device with the same blocking capability, resulting in about a factor of 800 reduction in drift layer resistance for 4H-SiC power devices. Because of this advantage, high-voltage (>600 V) 4H-SiC power devices have significantly smaller die size compared to those of silicon power devices with comparable on-state resistance and blocking voltage.

The thinner and higher doped drift layers in 4H-SiC devices result in approximately a factor of 10 larger drift layer capacitances per unit area, which translates into 10× greater stored energy, often represented as $\frac{1}{2}CV^2$, per unit area, compared to silicon devices with the same blocking voltage. However, due to the much smaller device area of 4H-SiC devices for the same on-state resistance, total device capacitance and stored energy in 4H-SiC are expected to be up to a factor of 80 smaller than silicon devices with comparable blocking voltage and on-resistance. Because of the lower drift layer capacitance and stored energy, 4H-SiC power devices can offer operation at significantly higher switching frequencies, theoretically up to 80 times faster than what silicon devices can offer, while providing equal or better system efficiency.

4H-SiC is not the only wide bandgap semiconductor material available. However, 4H-SiC stands out because of the availability of high-quality commercial substrates, and it can be thermally oxidized to form high-quality gate oxide layers for metal-oxide-semiconductor (MOS) devices. In addition, fabrication processes for selective doping, for both p- and n-type, are well established in silicon carbide, which enables realization of most power devices structures, including Schottky and PiN diodes, bipolar junction transistors (BJTs), gate turn off (GTO) thyristors, metal oxide semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs).

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.
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In this chapter, basic physics of device operations for the unipolar diodes and power MOSFETs will be discussed. Recent experimental demonstrations and developments will be reviewed and presented.

12.2 Unipolar Diodes – 4H-SiC JBS Diodes

The band structure for the metal and the semiconductor, when they are electrically and physically isolated from each other, is shown in Figure 12.1. For simplicity, only n-type semiconductor material with Fermi level positioned above that of the metal is shown, which is the case for most of the n-type 4H-SiC and metal combinations in use today. The work function of the metal (Φ_m) is defined as the energy required to move an electron from the Fermi level (E_F) position in metal to a state at rest outside the surface of metal, which is called the vacuum level. The work function can also be defined similarly in semiconductors as the energy required to move an electron from the Fermi level in the semiconductor to a state at rest outside the surface of the semiconductor. It should be noted that the Fermi level in semiconductor is placed within the bandgap, where electrons cannot reside in equilibrium. Instead of work function, electron affinity (χ_s), defined as the energy required to move an electron from the bottom of the conduction band to the vacuum level, is more commonly used in semiconductors.

Figure 12.2 shows the energy band diagram when an intimate connection is made between the metal and the semiconductor. The vacuum level must be continuous across the interface between the metal and the semiconductor as shown. This forces formation of a barrier between the metal and the conduction band of the semiconductor, referred to as the Schottky barrier, with a barrier height (Φ_b) determined by the difference between the metal work function and semiconductor electron affinity. When the metal and the semiconductor are electrically connected, through power supplies or characterization systems, electrons are transferred from the semiconductor to the metal to establish thermal equilibrium. The energy band diagram after thermal equilibrium, where Fermi levels for both sides line up, is

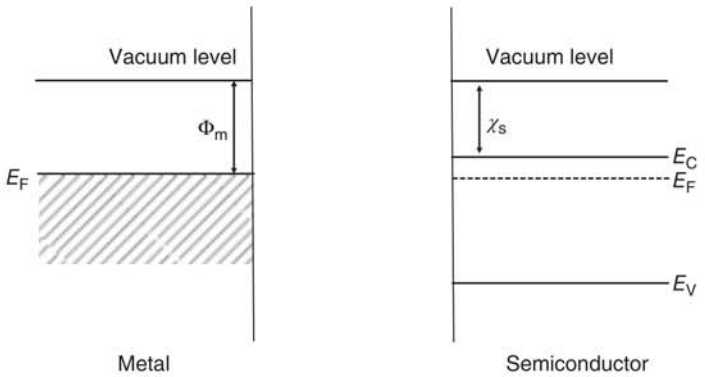


Figure 12.1 Energy band diagrams for a metal and a semiconductor.

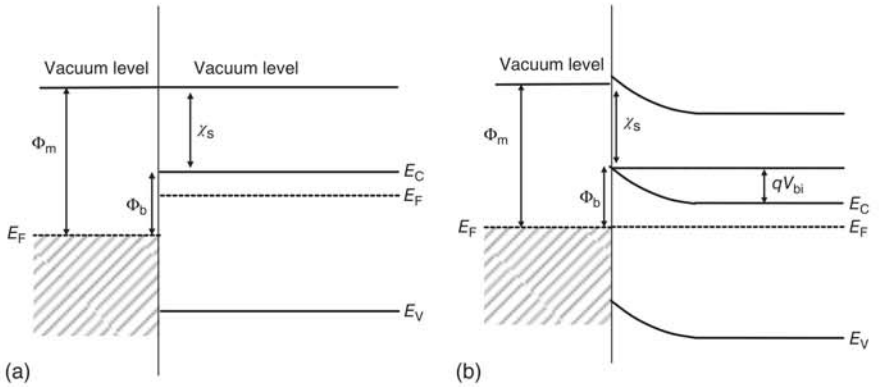


Figure 12.2 Energy band diagrams for a metal–semiconductor system. (a) After an intimate contact and (b) after thermal equilibrium.

shown in Figure 12.2. The transfer of electrons provides negative charge on the metal side, which is equal in magnitude to the positive charge in the depletion region at the surface of the semiconductor. The voltage formed across the depletion region at thermal equilibrium is referred to as the built-in voltage (V_{bi}).

When a negative bias is applied to the semiconductor side with respect to the metal side (forward bias), the height of barrier electrons in the semiconductor side that has to jump over to flow into the metal side reduces and electrons with sufficient energy can transport over the potential barrier into the metal. The current formed by this phenomenon is called thermionic emission current, which increases exponentially with the applied bias. For high-voltage (>600 V) power switching diodes in 4H-SiC, the structure is built with using an n-type semiconductor layer with relatively low doping concentration, typically 5×10^{16} cm^{-3} or lower, with a thickness of several microns (μm), which results in a series drift resistance. When a forward bias of greater than V_{bi} is applied, the current through the structure increases linearly with applied bias, with the slope defined by the series drift resistance.

When a positive bias is applied to the semiconductor side with respect to the metal side (reverse bias), the depletion region extends into the semiconductor and supports the voltage. The leakage current of the Schottky barrier diode (SBD) is dominated by the thermionic emission from the metal, which depends exponentially on the Schottky barrier height. It should be noted that the Schottky barrier height reduces with increasing E-field in reverse bias due to image force barrier lowering. Combination of those two effects results in reverse leakage current that increases with temperature and bias.

Junction barrier Schottky (JBS) diode structure [1–3], also referred to as merged PiN Schottky (MPS) diode structure [4], minimizes the impact of image force barrier lowering. Cross sections of a 4H-SiC JBS rectifier operating in the forward and reverse bias are shown in Figure 12.3. A JBS diode consists of interdigitated Schottky and p^+ areas, which are mostly formed by ion implantations in 4H-SiC. In forward bias, only the Schottky regions of the diode conduct provided that the voltage drop across the pn junction, formed at the p^+ region and the n^- drift layer,

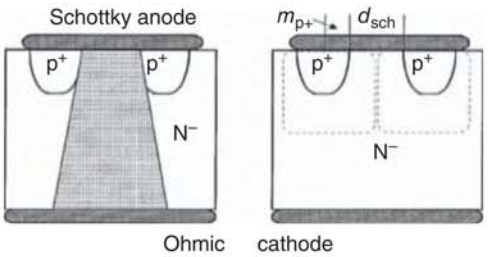


Figure 12.3 Junction barrier Schottky diode structures [4]. On-state current flows through the Schottky anode, while reverse leakage is limited by depletion from adjacent grids in a JBS diode. Source: Hefner et al. [4]. © 2001, IEEE.

is less than 3 V. In reverse bias, the p^+ areas provide shielding to the Schottky barrier formed at the metal–n^- SiC interface. As the reverse bias increases, the depletion regions from adjacent p^+ regions pinch-off the leakage current from the Schottky contacts of the device. The presence of the p^+ regions reduces the *E*-field at the metal–n^- SiC barrier because of two-dimensional charge sharing, where *E*-field lines originating from positively charged donors in the drift layer terminate in the negatively charged acceptors in the p^+ regions. This is a very important feature for devices in 4H-SiC, with very high breakdown *E*-field and high power density resulting in high junction temperatures. Most, if not all, of the commercially available 4H-SiC Schottky diodes are utilizing the JBS structure for superior blocking performances at elevated temperatures.

The biggest benefit of 4H-SiC JBS diodes is in the reverse recovery characteristics. Figure 12.4 compares the reverse recovery characteristics of a 1500 V 4H-SiC JBS diode and a 1000 V ultrafast silicon PiN diode [4]. The recovery of the 4H-SiC JBS diode is mostly capacitive in nature, and the amount of reverse recovery charge represents depletion capacitance of the drift layer. Hence, the reverse recovery waveforms show virtually no temperature dependence throughout the temperature range used for the measurements, as shown in Figure 12.4. On the other hand, silicon diode reverse recovery waveforms showed much larger amount of reverse recovery charge and time, which increased significantly with the temperature, as shown in Figure 12.4. This indicates that the excess charge storage is far greater than the junction depletion charge and can seriously impact the switching performance of the diode. A factor of 2 increase in reverse recovery time (50 ns at 25 °C, to 100 ns at 100 °C) and a factor of 4 increase in reverse in reverse recovery charge were measured, leading to an unfavorable positive feedback between switching losses and further temperature increase.

The benefits of reduced reverse recovery charge show up in the turn-on losses in the switches. Figure 12.5 shows the schematics of a constant current mode (CCM) active power factor correction (PFC) booster converter [5]. One of the most common applications for the 4H-SiC JBS diode is the use as a boost diode in the PFC circuit. Figure 12.6 shows the reverse recovery waveforms, both voltage and current, of a 4H-SiC JBS diode and a silicon PiN diode. It should be noted that voltage rise is almost immediately observed for the 4H-SiC JBS diode, but the voltage rise is delayed for the silicon PiN diode structure until the peak reverse recovery current has been reached [4]. This means the switch, shown as the MOSFET in Figure 12.5, experiences full load supply voltage at full current (load current plus the reverse recovery

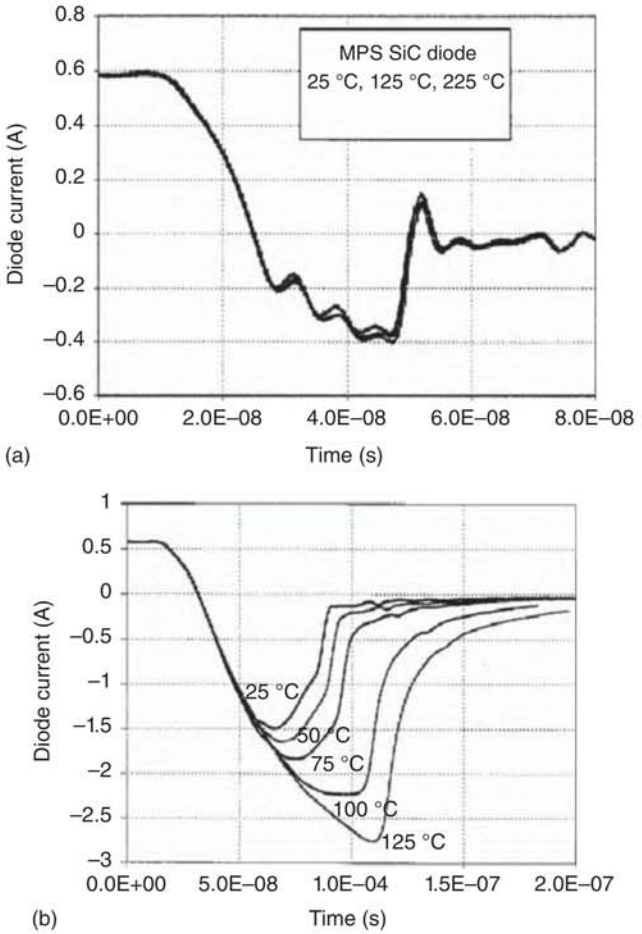


Figure 12.4 Measured temperature dependence of the reverse recovery characteristics for (a) a 1500 V, 0.5 A 4H-SiC MPS (JBS) diode [4], and (b) a 1000 V, 1 A ultrafast Si PiN diode (MUR1100). Source: Hefner et al. [4]. © 2001, IEEE.

current of the diode) during the turn-on transients until a peak reverse recovery current is reached, resulting in very high turn-on losses. The use of 4H-SiC JBS diode, instead of the silicon PiN diode, significantly reduces the stress on the switch due to reduced current requirement, as well as voltage stress since the switch voltage starts decreasing without delay. This feature allows system designers to use MOSFETs with significantly reduced current ratings, resulting in substantial cost savings, as well as clear improvements in system efficiency [5].

12.2.1 Optimization of 4H-SiC JBS Diodes

Commercial availability of high-performance 4H-SiC JBS diodes revolutionized the power industry. However, the adoption of 4H-SiC JBS diodes was limited to high-end switching power applications. The cost of silicon carbide devices was still very high.

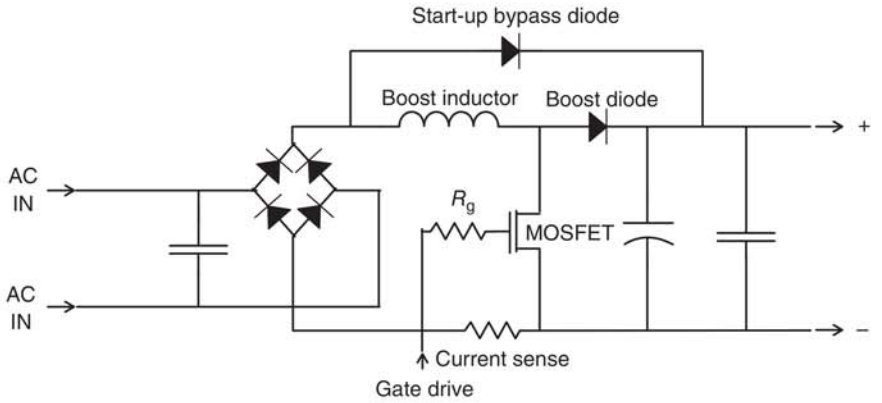


Figure 12.5 Active power factor correction boost converter. Source: Wolfspeed [5]. © 2012 Cree, Inc.

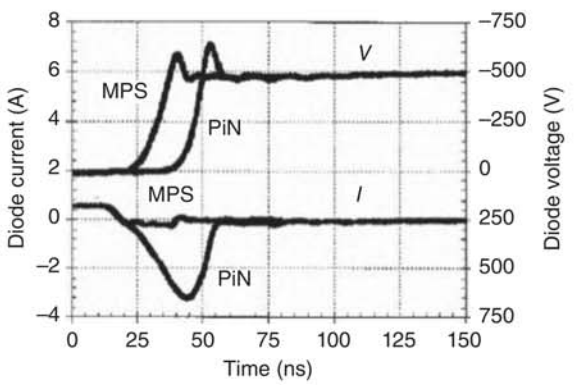


Figure 12.6 Comparison of the reverse recovery characteristics of the 4H-SiC MPS (JBS) and silicon PiN diode (MUR1100) at a d*i*/d*t* of 100 A/μs. Source: Hefner et al. [4]. © 2001, IEEE.

To win wider acceptance in a wide range of applications, further optimization of the 4H-SiC JBS diode structure was necessary. The following improvements were made to the 4H-SiC JBS diode structure to answer these challenges.

- Improvements in surge current capability.
- Further reduction in forward voltage drop.
- Increase in current conduction capability.

12.2.1.1 Injection from the p^+ Regions for Surge Operation

4H-SiC JBS diodes show typical characteristics of majority carrier devices. The forward resistance depends on the resistivity of the drift layer, which is determined by doping concentration and electron mobility in the layer. The electron mobility reduces with temperature due to lattice scattering, which results in an increase of drift resistance and the forward voltage drop (V_F) of the diode; hence, the positive temperature coefficient of V_F is achieved as shown in Figure 12.7, while a negative temperature coefficient of V_F is observed for silicon bipolar diodes. This is a great feature when paralleling multiple discrete power devices, when a suitably rated single device is not available. Paralleling can also help to simplify thermal management

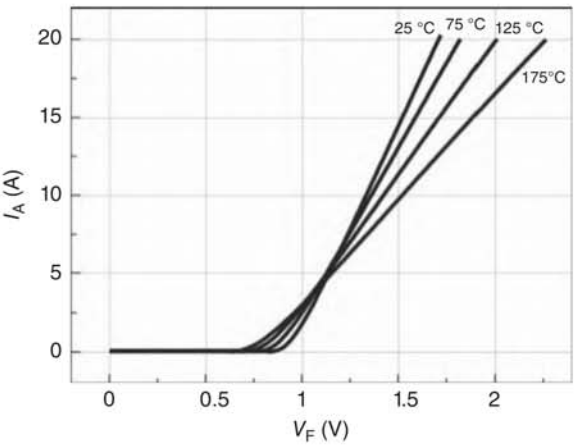


Figure 12.7 Forward bias curves of a 600 V 4H-SiC Schottky diode as a function of temperature.

by distributing power losses evenly to a larger area in a module [6]. The positive temperature coefficient of V_F helps to balance currents among paralleled devices. The device carrying more initial current experiences higher power dissipation and heats a little more than its neighbors. This results in an increase of V_F, which causes the current to decrease. A stable operating point is reached where currents through all the devices are balanced, though junction temperature of each device may be slightly different.

However, the positive temperature coefficient of V_F can cause a thermal runaway when the device is exposed to surge current stress [7]. One example of the surge current situation is start-up conditions, where output capacitance charges up to a steady state value, for which a silicon bipolar diode can be used as the start-up bypass diode, as shown in Figure 12.5 [5].

This weakness was addressed by optimizing p regions within the JBS diode with respect to emitter efficiency and conductivity, which can eliminate the needs for an additional surge current bypass diode [6, 7], as shown in Figure 12.8. During normal forward operation at typical operating currents, only the unipolar structure of the device is active with fast turn-off characteristics. However, under transient

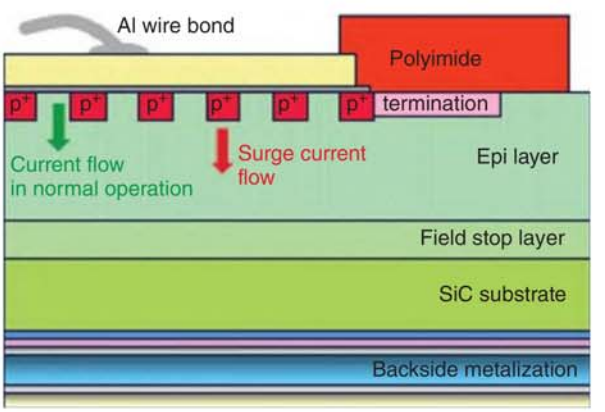


Figure 12.8 SiC diode with merged p-doped islands (MPS structure). Source: Rupp et al. [7]. © 2006, IEEE.

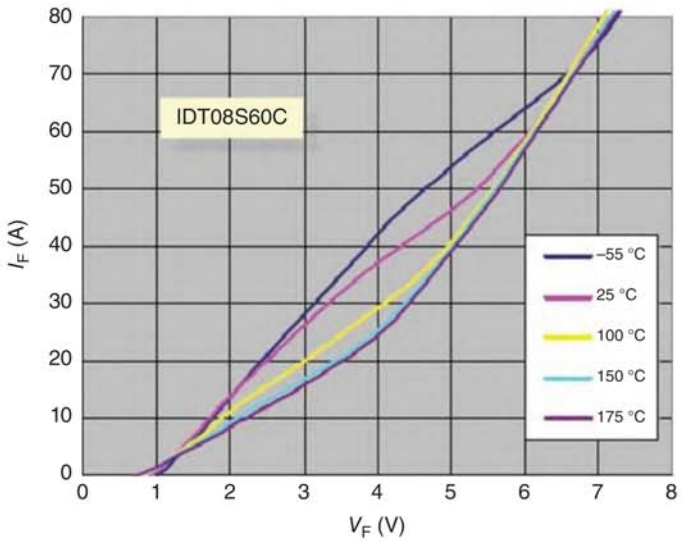


Figure 12.9 *I–V* characteristics for different temperatures of an 8 A/600 V MPS SiC diode. The various temperature curves all merge in one straight line corresponding to the nearly temperature independent substrate resistivity. Source: Rupp et al. [7]. © 2006, IEEE.

forward surge conditions, the embedded PiN diodes turn on, enabling the device to conduct the extreme surge current while maintaining low V_F, thus enabling it to survive a transient event that would otherwise cripple a pure unipolar diode [6]. *I–V* characteristics for different temperatures of an 8 A/600 V MPS SiC diode are shown in Figure 12.9 [7]. The onset of minority carrier injection reduces with temperature because of the reduced effectiveness of the shunt across the p^+n junction, caused by increased unipolar resistance in the n-region. In the minority carrier injection mode at high current density, the remaining drift layer resistance becomes negligible compared to the substrate resistance, which leads to temperature insensitive forward characteristics, as shown in Figure 12.9 [7].

12.2.1.2 Trench JBS Diodes

It was discussed in Section 12.2 that the JBS or MPS structure shields the Schottky interface from the high *E*-field, which in turn improves the reverse blocking performance. In 4H-SiC dopant, diffusivity is negligible. The junction depth of p^+n junction is limited by practical ion implantation energies and implant straggle and is fairly shallow, which limits the *E*-field protection at the Schottky interface. As a result, majority of leakage current comes from the Schottky contact area, which can be high at operating junction temperatures. The high leakage current makes it very challenging to develop large amperage Schottky diodes with a reasonable cost in 4H-SiC. In addition, further cost reduction by reducing the die size is extremely difficult unless the Schottky leakage current is significantly reduced.

Trench JBS diodes in 4H-SiC [8–11] were developed to alleviate this problem. To improve shielding of the Schottky interface, p^+ regions with deep junction depth

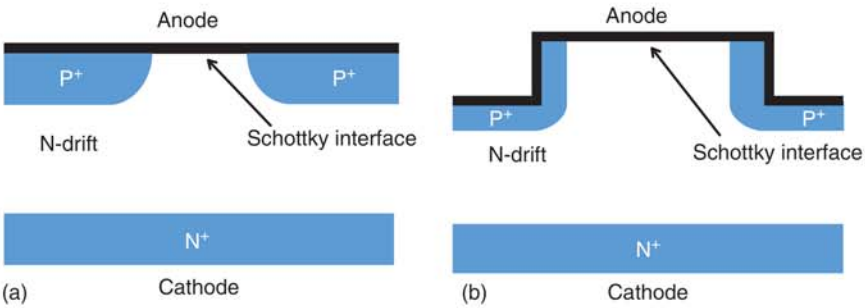


Figure 12.10 Cross-sectional views of (a) planar JBS and (b) trench JBS diodes.

and high aspect ratio are necessary. A comparison of planar JBS diode structure and trench JBS diode structure is given in Figure 12.10. In trench JBS diodes, the trenches are formed using dry etching, which include reactive ion etching (RIE), then the p-type impurities are implanted along the sidewall and bottom of the trenches. With the same ion implantation energy, the junction barrier can be largely extended below the Schottky interface and a substantial reduction in image force barrier lowering [8].

A comparison of blocking performance of 650 V, 10 A 4H-SiC planar and trench JBS diodes fabricated on the same wafer was reported [8]. The trench JBS diode clearly showed improvements in the blocking performance, showing an increase of approximately 150 V in blocking voltage. This suggests that for the same blocking voltage rating, the trench JBS diode structure allows drift layers with heavier doping concentration so that the differential specific on-resistance can be reduced, resulting in smaller chip sizes. Similar comparisons were made using 1200 V, 20 A diodes. In addition, the leakage current distribution for the trench structure becomes much tighter than that of the planar structure, indicating the lower E-field at the Schottky interface significantly reduced the role of imperfections of the wafer, such as doping and thickness variation of the drift layer and the effects of crystal defects [8].

12.2.1.3 Use of Low Work Function Metal for Anode Metal

Continuous efforts are being made to reduce forward voltage drop (V_F) of the 4H-SiC JBS diodes. Such reductions lead to smaller die size, which results in a reduction in cost, and a reduction in switching losses due to decreased device capacitances. One of the approaches to achieve this goal is to use heavier doped, thinner drift layer to reduce drift layer resistance, which results in lower differential on-resistance, discussed in Section 12.2.1.2. The other approach is to use lower barrier height metal for the Schottky interface, such as tantalum (Ta)- [12] and molybdenum (Mo)-based materials [13, 14], to reduce the knee voltage or threshold voltage of the diodes. The reduction in V_F was demonstrated using two Schottky interfaces, one with a barrier height of 1.31 eV, and the other with a barrier height of 0.85 eV [9]. The diodes had an active area of 3.05 mm^2 and used 5 μm thick drift layer with a doping concentration of 1.0×10^{16} cm^{-3}. The diode with lower barrier height utilized the trench JBS structure to minimize leakage current in the reverse bias. A trench JBS diode with

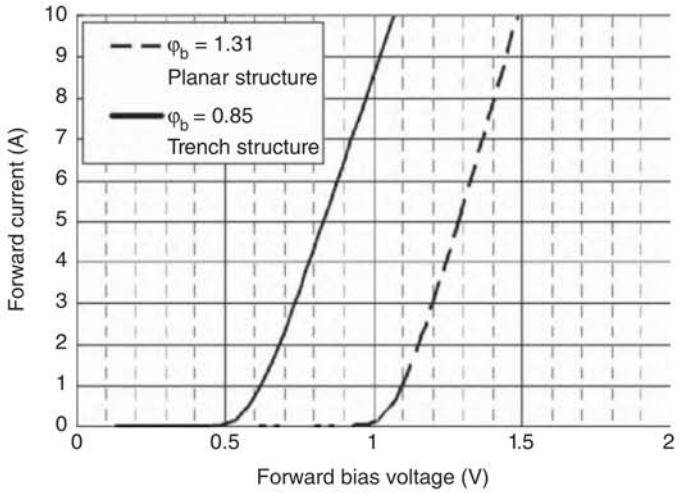


Figure 12.11 Forward *I–V* characteristics of the planar structure and the trench structure. The difference of threshold voltage is related to barrier height. Source: Nakamura et al. [9]. © 2011, IEEE.

a lower barrier height metal showed 0.48 V smaller threshold voltage compared to the planar structure, as shown in Figure 12.11. Figure 12.12 shows the *I–V* characteristics in the reverse bias. The trench structure has higher reverse leakage current at lower bias due to the lower barrier height Schottky interface. At higher biases, the leakage current of the trench structure is less than that of the planar structure due to more effective shielding of the Schottky interface.

It should be noted that the rate of increase in leakage current, as a function of temperature, is greater for low barrier height Schottky interface devices [14].

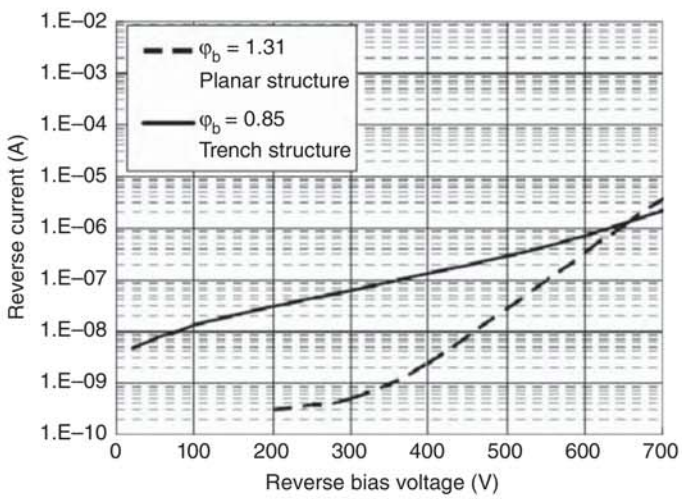


Figure 12.12 Reverse *I–V* characteristics of the planar structure and the trench structure. Source: Nakamura et al. [9]. © 2011, IEEE.

The increased leakage current leads to static power loss in the blocking state, which can impact system efficiency. When designing a JBS diode using low barrier height Schottky metal, proper shielding of the Schottky interface must be provided to keep the power losses due to reverse leakage current less than 1% of the nominal power losses [14].

12.3 Unipolar Switches: Power MOSFETs

A power MOSFET is an easy-to-drive device with high switching speeds, which makes it a very attractive option for power switching applications. The main advantage of the power MOSFET structure is the high impedance gate, which requires zero gate current in the steady state, and the gate drives are only required to provide relatively small amount of gate current to charge and discharge the capacitances. The current conduction in the power MOSFET structure occurs through transport of majority carriers in the drift region and does not involve minority carrier injection. Hence, there are no delays associated with storage or recombination of minority carriers in power MOSFETs. It is also easy to parallel multiple power MOSFETs because of the positive temperature coefficient of the forward voltage drop, due to the decrease in carrier mobility at elevated temperatures, which prevents current hogging and subsequent thermal runaways. In addition, the power MOSFETs do not go through second breakdown like bipolar junction transistors and offer excellent safe operating area.

On-resistance of a power MOSFET increases quite rapidly with blocking voltage of the device. For power MOSFETs in silicon, which is the most commonly used semiconductor material, the on-resistance of a power MOSFET can be very small if the design voltage of the device is 200 V or less [15]. Of course, power MOSFETs in silicon can be designed for voltages greater than 200 V. However, this results in unacceptably high on-resistance, large chip area, and significant increases in parasitic capacitances. Researchers in silicon power devices addressed this issue by placing an injecting junction at the drain side of the device, which reduced the drift layer resistance by minority carrier injection, or conductivity modulation of the drift layer [16, 17], resulting in the development of insulated gate bipolar transistors (IGBTs). The other approach used to reduce the on-resistance of silicon power MOSFETs is the use of superjunction (SJ) structure [18], which utilizes alternating n- and p-layers with relatively heavy doping concentrations. Excellent results have been achieved for devices with blocking voltages up to 900 V [19].

An IGBT provides significantly lower forward voltage drops compared to a conventional power MOSFET in higher blocking voltage (>600 V) rated devices by injecting minority carriers from the backside (collector) into the drift region during the forward conduction. However, this reduction in on-state forward voltage drop comes with some serious drawbacks listed below.

- The on-state forward voltage drop in IGBTs includes a voltage drop across a forward biased pn junction. At higher current levels, IGBTs have lower conduction losses than power MOSFETs due to lower forward voltage drop. However, at lower

current levels, where forward voltage drop of power MOSFETs can be lower than the voltage drop across a pn junction, IGBTs have higher conduction losses than power MOSFETs.

- The additional pn junction blocks reverse current flow. Unlike power MOSFETs, IGBTs cannot conduct currents in the reverse direction. In applications where reverse current flow is needed, an external anti-parallel diode is required, which results in increases in the chip count and the system cost, as well as a reduction in power density. Developments in reverse conducting IGBTs (RC-IGBTs) [20], which require significantly more complicated fabrication processes, can address this weakness.
- The minority carriers injected into the drift region requires significant delays during the turn-on and turn-off transients. The delay in the turn-on results in voltage overshoots, and the delay in the turn-off results in tail currents. This results in longer switching times and substantially higher switching losses, when compared to a power MOSFET.

Power devices in wide bandgap materials, such as silicon carbide (SiC), gallium nitride (GaN), and gallium oxide (Ga_2O_3), can address these issues. The wide bandgaps of these materials result in high breakdown E-fields, which allows thinner drift layer with significantly higher doping concentration. This allows designs of unipolar power devices with extremely low on-resistance, which addresses most of the issues discussed above. Fabrication processes, including techniques to form high-quality gate oxide films and selective doping methods, are well established in silicon carbide, which culminated in successful development and commercialization of silicon carbide power MOSFETs, while more developments are needed in other wide bandgap materials [21, 22].

Various semiconductor materials, including III–V compounds and ternary alloys, as well as silicon were considered for vertical power FET structures, and it was shown that the power handling capability of the devices increases as the third power of the energy bandgap, and linearly with increase in electron mobility [23]. A figure of merit was developed to compare semiconductor materials for uses in unipolar power switching devices [23–25]. The figure of merit can also be used to gauge the level of optimization of a power device by comparing its performance to a theoretical maximum performance determined by the material properties.

Figure 12.13 shows a simple blocking structure and E-field distribution used for the derivation of the figure of merit. The structure consists of a blocking pn junction, a drift layer with a uniform doping concentration of N_D and a thickness of D, and an N^+ layer which serves as the field-stop layer or backside contact. The maximum blocking voltage of this structure is achieved when the maximum E-field in the structure is equal to the critical field for avalanche voltage (E_C), at which point breakdown occurs. The E-field reduces linearly as x increases, and the drift layer thickness D is selected so that E-field reduces to zero when x equals D.

The peak E-field, or E_C, can be calculated using Gauss's law

$$E_C = \frac{qN_D D}{\varepsilon_s} \tag{12.1}$$

where ε_s is the dielectric constant of the semiconductor material.

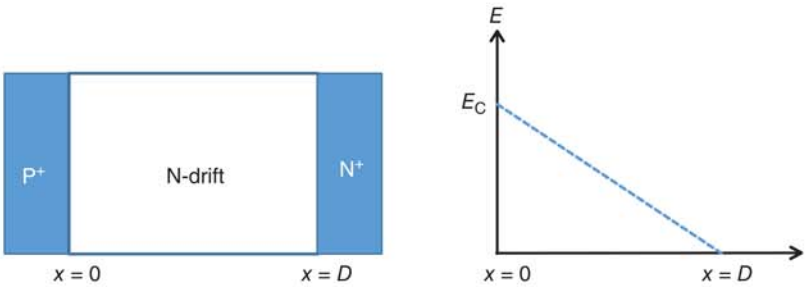


Figure 12.13 Simplified blocking structure represented as a PiN diode (a), and *E*-field profile in blocking mode (b).

The breakdown voltage (V_B) of the structure can be calculated using Poisson's equation

$$V_B = \frac{qN_D D^2}{2\varepsilon_s} \tag{12.2}$$

The area normalized resistance of the drift layer can be calculated as below

$$R_{on} \cdot A = R_{on,sp} = \frac{D}{q\mu_n N_D} \tag{12.3}$$

where μ_n is the bulk electron mobility of the semiconductor material.

From Eqs. (12.1) and (12.2), we can see that

$$D = \frac{2V_B}{E_C} \tag{12.4}$$

and

$$qN_D = \frac{\varepsilon_s E_C^2}{2V_B} \tag{12.5}$$

When we insert (12.4) and (12.5) into Eq. (12.3), we get

$$R_{on,sp} = \frac{D}{qN_D\mu_n} = \frac{2V_B}{E_C} \cdot \frac{2V_B}{\varepsilon_s E_C^2} \cdot \frac{1}{\mu_n} = \frac{4V_B^2}{\mu_n \varepsilon_s E_C^3} \tag{12.6}$$

Theoretical specific on-resistance ($R_{on,sp}$) values calculated using Eq. (12.6) are plotted in Figure 12.14 for silicon and 4H-SiC. Performance points of Wolfspeed (Cree) Power MOSFETs with blocking voltages ranging from 900 V to 15 kV are also shown on the plot. For devices with blocking voltages of 6.5 kV or higher, the performance points are close to the ideal silicon carbide 1-D limit, since the on-resistance of the devices is dominated by the drift resistance. For devices with blocking voltages of 3.3 kV or lower, the performance points deviate from the ideal 1-D limit due to other internal resistance components, such as MOS channel resistance and spreading resistance, to be discussed in Section 12.3.1.

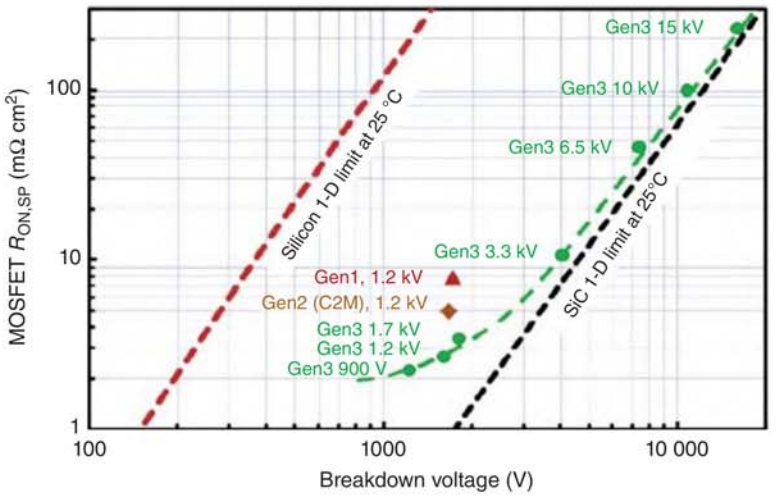


Figure 12.14 Specific R_{ds}, on as a function of breakdown voltage. Included are points describing performance points using the avalanche breakdown voltage, of Wolfspeed (Cree) power MOSFETs at room temperature. Source: Lichtenwalner et al. [26].

12.3.1 4H-SiC Power MOSFET Structures

12.3.1.1 DMOSFETs

Figure 12.15 shows a simplified cross section of a power double implanted MOSFET (DMOSFET) in silicon carbide. The n^+ sources and MOS channel regions are built on implanted p-wells. The n^+ source regions and the p-wells are tied together using common contacts to source, to keep the potential difference between the two regions at minimum. The device turns on when a positive bias exceeding the threshold voltage of the device is applied to the gate electrode. In the on-state, electrons flow from the n^+ source regions through the MOS channel formed in the p-well into the junction field-effect transistor (JFET) region. The length of the MOS channel is determined by the distance from the edges of the n^+ regions and the p-wells, and the JFET regions are defined as the n-type region formed between

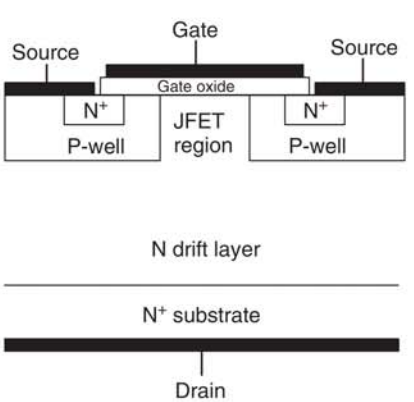


Figure 12.15 Simplified cross section of a 4H-SiC DMOSFET.

adjacent p-wells. The electrons then spread into the drift layer and then flow into the n^+ substrate and exit the structure through the drain electrode. In the off-state, a bias less than the threshold voltage of the device is applied to the gate electrode, which removes the inversion channel in the MOS region in the p-well and isolates the n^+ regions from the JFET regions. The device turns into a PiN diode structure, which can block the voltage when a positive bias is applied to the drain electrode and allow current to flow through when a negative bias is applied to the drain electrode. It should be noticed that the depletion regions from the p-wells merge and provide shielding to the gate oxide layers. The doping concentration and the width of the JFET region should be set carefully to provide sufficient shielding to the gate oxide in the off-state, as well as low resistance during the on-state operation of the device [27].

4H-SiC DMOSFET Resistance Components There are several resistance components in the DMOSFET structure. The main components include MOS channel resistance, JFET resistance, drift resistance, and spreading resistance. There are other resistance components, such as contact resistance and substrate resistance, but those will be ignored in this calculation for simplicity.

The channel resistance (R_{ch}) represents the resistance of the MOS inversion layer in the channel. In the on-state operation of the power DMOSFET, for low drain bias (V_{DS}) values structure, R_{ch} can be expressed as below.

$$R_{ch} = \frac{L \cdot P}{2 \cdot \mu_{n,ave} \cdot C_{ox} \cdot (V_g - V_{th})} \tag{12.7}$$

where L is the channel length and P is the device cell pitch, as shown in Figure 12.16. $\mu_{n,ave}$ is the average MOS inversion layer mobility, and C_{ox} is the oxide capacitance per unit area (ε_{ox}/t_{ox}), and V_{th} is the device threshold voltage.

The JFET resistance (R_{JFET}) represents the resistance through the narrow region between the p-wells. This resistance is determined by the doping concentration in the JFET region (N_D), the width of the region (W), and the depth of the p-well (d) and can be expressed as below.

$$R_{JFET} = \frac{d \cdot P}{q \cdot \mu_{n,bulk} \cdot N_D \cdot W} \tag{12.8}$$

where $\mu_{n,bulk}$ is the bulk electron mobility in the JFET region.

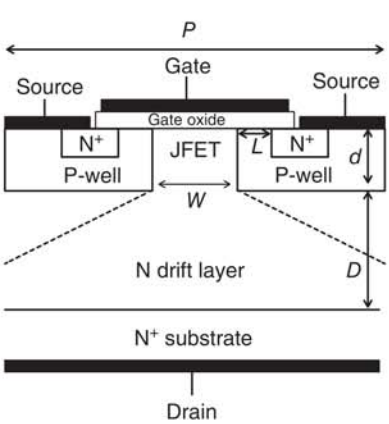


Figure 12.16 4H-SiC DMOSFET dimensions for on-resistance calculations.

Equation (12.8) ignores the impact of the depletion region formed at the metallurgical junction of the p-well and the n-drift layer, which becomes wider with a positive drain bias applied for normal on-state operation, increasing the JFET resistance. The JFET resistance reduces when a negative drain bias is applied, and as a result, the width of the depletion region reduces. This is the case when the power MOSFET is used as a synchronous rectifier.

The drift resistance (R_{drift}) represents the resistance through the drift layer. For this calculation, a parallel plate operation with uniform current density is assumed. This resistance can be expressed as below.

$$R_{\text{drift}} = \frac{D}{q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \tag{12.9}$$

where D is the drift layer thickness. This is identical to Eq. (12.3).

The spreading resistance (R_{spread}) represents the increase in on-resistance when electron flow exits the narrow JFET gap into a much wider drift layer, shown as the dotted line in Figure 12.16. Due to conductivity anisotropy in 4H-SiC [28, 29], electron mobility in the vertical direction is approximately 15% greater than the electron mobility in the lateral direction. The current spreads with a 41° angle, and the resistance in the cone depicted in Figure 12.16 can be calculated as below.

$$R = \frac{P}{q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \int_0^X \frac{1}{W + 1.74y}\,\text{d}y \tag{12.10}$$

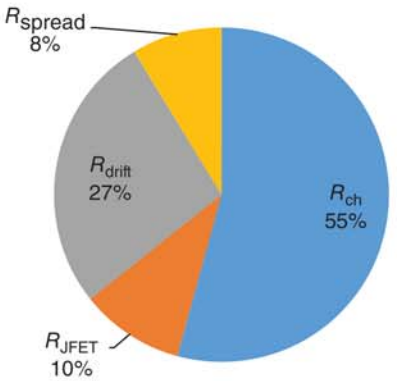
where y is the depth under the metallurgical junction and X is the depth at which the width of the cone equals the cell pitch P. With a spreading angle of 41° angle, it can be shown that X equals 0.575 ($P - W$). With this assumption, Eq. (12.10) simplifies to the following expression.

$$R = \frac{P}{1.74q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \ln\left(\frac{P}{W}\right) \tag{12.11}$$

Since the spreading resistance represents the increase in resistance due to current spreading, the ideal resistance of the resistance needs to be subtracted from Eq. (12.11). Hence, the spreading resistance can be expressed as below.

$$\begin{aligned} R_{\text{spread}} &= \frac{P}{1.74q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \ln\left(\frac{P}{W}\right) - \frac{P-W}{1.74q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \\ &= \frac{P}{1.74q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \left(\ln\left(\frac{P}{W}\right) - 1 + \frac{W}{P}\right) \end{aligned} \tag{12.12}$$

Assuming $\mu_{\text{n,ave}}$ of 12 $\text{cm}^2/\text{V s}$, $\mu_{\text{n,bulk}}$ of 700 $\text{cm}^2/\text{V s}$ at room temperature, a cell pitch (P) of 10 µm, a JFET gap (W) of 3 µm, a junction depth (d) of 1 µm, a drift layer thickness of 9 µm, a drift layer doping concentration (N_{D}) of 8×10^{15} cm^{-3}, a MOS channel length (L) of 0.5 µm, a V_{g}–V_{th} of 12 V, and a C_{ox} of 8.63×10^{-8} F/cm^2, we can estimate the values for the resistance components, normalized for the area, as given in Figure 12.17. Given thickness and doping concentration of the drift layer, we can deduce that this device has a rated voltage of about 1200 V. The drift resistance of this device accounts for only 27% of the total on-resistance. The on-resistance of the MOSFET is heavily influenced by other parasitic resistance components, and



Resistance component	Value
R_{ch}	2.01 mΩ-cm^2
R_{JFET}	0.371 mΩ-cm^2
R_{drift}	1.00 mΩ-cm^2
R_{spread}	0.323 mΩ-cm^2
Total	3.70 mΩ-cm^2

Figure 12.17 4H-SiC DMOSFET resistance components. Assumptions: $\mu_{n,ave}$ of 12 cm^2/V s, $\mu_{n,bulk}$ of 700 cm^2/V s, a cell pitch (P) of 10 μm, a JFET gap (W) of 3 μm, a junction depth (d) of 1 μm, a drift layer thickness of 9 μm, a drift layer doping concentration (N_D) of 8×10^{15} cm^{-3}, a MOS channel length (L) of 0.5 μm, a $V_g - V_{th}$ of 12 V, and a C_{ox} of 8.63×10^{-8} F/cm^2.

out of the parasitic resistance components, the MOS channel resistance is the most dominant factor, accounting for 55% of the total on-resistance.

4H-SiC DMOSFET Optimization For optimization of power DMOSFETs in 4H-SiC, it is very important to minimize the MOS channel resistance. First successful approach for reducing the MOS channel resistance was to utilize self-aligned ion implantation to reduce the MOS channel length [30]. This approach resulted in 2 kV power MOSFETs in 4H-SiC with a specific on-resistance of 10.3 mΩ-cm^2 and provided an important basis for the commercialization of power MOSFETs in silicon carbide.

Attempts were made to improve MOS interface properties by incorporating impurities other than nitrogen into the gate oxide to achieve greater MOS channel mobility than what can be obtained using NO or N_2O anneals. Doping of the oxide layers with phosphorus [31] and boron [32, 33] has been investigated. A MOS channel mobility of 98 cm^2/V s as achieved using phosphorus doping approach [30] and boron doping approach resulted in a MOS channel mobility of 102 cm^2/V s [32], and a 4.5 kV power DMOSFET was demonstrated [33]. Approximately a factor of 3 improvements in MOS channel mobility over nitridation using NO or N_2O was observed using this approach. However, it was determined that these approaches were not suitable for commercial 4H-SiC power MOSFETs since a reasonable threshold voltage stability could not be achieved (P. Godignon, private communications).

Usage of alkaline earth elements, such as strontium (Sr) and barium (Ba), as interface passivation materials for 4H-SiC MOSFETs was also investigated [34–36]. The passivation was performed by placing a very thin interlayer material directly on the 4H-SiC surface, followed by deposition of gate dielectric layer, typically SiO_2, which was annealed in O_2/N_2 ambient for densification [34]. Sr passivation of the MOS interface showed a very promising result, resulting in a MOS channel mobility of 40 cm^2/V s, which was comparable to the values achievable using an NO anneal [34]. Passivation using Ba turned out to be significantly more efficient, resulting in a

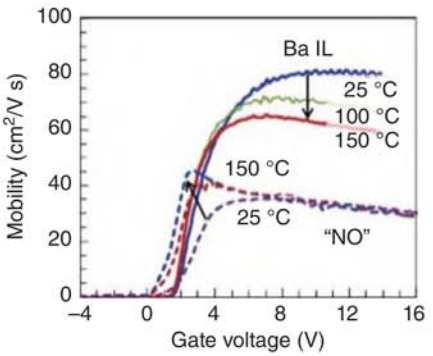


Figure 12.18 MOS channel mobility comparing samples with Ba interlayer to those with an NO anneal, as a function of temperature (25, 100, and 150 °C). Source: Lichtenwalner et al. [26].

MOS channel mobility of 85 $cm^2/V\,s$ at room temperature, which is approximately double the value from an NO annealed sample [34]. A comparison of MOS channel mobility at temperatures ranging from 25 to 150 °C is shown in Figure 12.18. A test lateral MOSFET with conventional NO anneal process and a device with Barium interlayer (Ba IL) passivation process were used for this comparison [34]. The samples were fabricated on $5 \times 10^{15}\,cm^{-3}$ doped p-type epilayers on 4H-SiC substrates. The MOS channel mobility of the Ba IL-passivated sample decreases with temperature, as expected due to phonon scattering effects. This is in contrast to the NO annealed sample, which showed an increase in MOS channel mobility with temperature due to the higher interface density near the conduction band. Figure 12.19 shows the interface state density (D_{it}) distributions from high to low capacitance-voltage (CV) measurement for the MOS capacitors formed on lightly doped n-type epilayers. Results were compared to capacitors with as-grown thermal oxide. Both the NO annealed capacitor and the Ba IL-passivated capacitor showed significantly lower D_{it}, with the Ba IL processed device showing the lowest D_{it}.

Vertical 4H-SiC DMOSFETs were fabricated using the Ba IL process [36]. The devices were stressed under a negative gate bias of −15 V at 150 °C. A threshold voltage shift of less than 0.2 V was observed after 150 hours, demonstrating very good stability of threshold voltage. MOS capacitors with an area of 4 mm^2, fabricated with Ba IL passivation process, were tested under ramped V_g sweep conditions

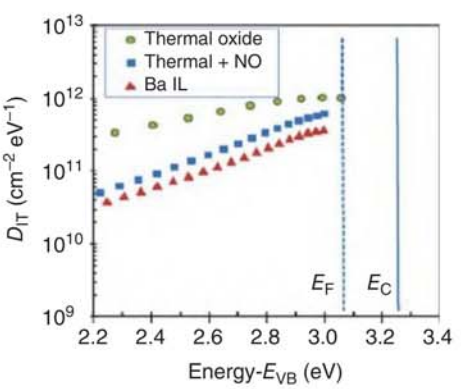


Figure 12.19 Interface state density extracted from the high-low $C-V$ measurements of NMOS capacitors, comparing samples with thermal oxidation only to those with NO anneal and Ba interlayer. Source: Lichtenwalner et al. [26].

(ramped time dependent dielectric breakdown [TDDB] measurements) [36]. More than 100 capacitors were measured for the breakdown statistics. The gate oxide formed with the Ba IL process with deposited oxide showed a reasonable maximum breakdown *E*-field, close to 10 MV/cm with a small temperature dependence from 25 to 150 °C. However, the breakdown field is lower than that of the thermal oxides with an NO anneal, and more extrinsic failures were noticed for the devices with the Ba IL process. At this time, it is not clear whether this is due to a fundamental weakness of the Ba IL process or due to a weakness of the deposited gate oxide process [36].

12.3.1.2 Trench MOSFETs

Trench MOSFET structureshown in Figure 12.20, can provide devices with very tight cell pitch because it places the MOS channel on the etched sidewalls. Additional real estate necessary for proper MOSFET operations, such as gate-to-source overlap and gate-to-ohmic metal gap, can also be placed on the sidewalls. Such design can result in a substantial increase in gate-to-source capacitance. This is actually highly desirable feature for high speed switching applications since it enhances immunity of the power MOSFET from erroneous turn-on during a high dv/dt turn-off event, provided that the increase in gate-to-drain capacitance could be avoided [37]. The first trench MOSFETs in silicon carbide, using 6H-polytype, were reported by Palmour et al. [38]. The first trench MOSFETs in 4H-SiC were also demonstrated by Palmour et al. [39].

It was also experimentally demonstrated that the MOS channel mobility can be significantly higher on the etched sidewall compared to the Si-face of 4H-SiC [40]. The simplified trench MOSFET structure shown in Figure 12.20 does not have a JFET region, which also helps reducing the on-resistance. It is expected that a well-optimized 4H-SiC trench MOSFET structure can offer significantly lower on-resistance compared to a 4H-SiC DMOSFET with the same voltage rating. However, it should be noted that one of the most important functions of the JFET region is to provide an adequate protection of the gate oxide from high *E*-field in the blocking mode, and the structure in Figure 12.20 does not have any protection for the oxide at the trench bottom, and this issue must be addressed before finalizing any 4H-SiC trench MOSFET designs.

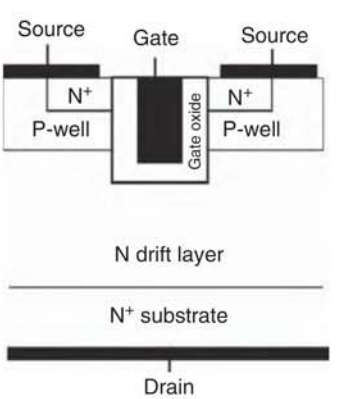


Figure 12.20 Simplified cross section of a 4H-SiC trench MOSFET.

4H-SiC Trench MOSFET Resistance Components Although trench MOSFETs have a different structure from DMOSFETs, many of the resistance components for the trench MOSFETs can be calculated the same way they were calculated for the DMOSFETs. The main components include MOS channel resistance, drift resistance, and spreading resistance. There is no JFET region in the simplified trench MOSFETs. As mentioned in Section 12.3.1.2, this simplified structure (Figure 12.20) does not have a mean to shield the gate oxide at the trench bottom. When a shielding structure is implemented to protect the trench bottom oxide, it can be represented as a JFET structure and a JFET resistance component can be added. However, this protection structure can take several forms and will not be included in this section. Other resistance components, such as contact resistance and substrate resistance, are ignored for trench MOSFET resistance component calculations, as was the case for the DMOSFETs.

The channel resistance (R_{ch}) represents the resistance of the MOS inversion layer in the channel. In the on-state operation of the power trench MOSFET, for low drain bias (V_{DS}) values structure, R_{ch} can be expressed as below.

$$R_{ch} = \frac{L \cdot P}{2 \cdot \mu_{n,ave} \cdot C_{ox} \cdot (V_g - V_{th})} \tag{12.13}$$

where L is the channel length and P is the device cell pitch, as shown in Figure 12.21. $\mu_{n,ave}$ is the average MOS inversion layer mobility, and C_{ox} is the oxide capacitance per unit area (ε_{ox}/t_{ox}), and V_{th} is the device threshold voltage.

The drift resistance (R_{drift}) represents the resistance through the drift layer. For this calculation, a parallel plate operation with uniform current density is assumed and can use the identical expression used for the DMOSFETs used in Section 12.3.1.1 (Eq. (12.9)).

The spreading resistance (R_{spread}) for the trench MOSFET can be derived the same way it was derived for the DMOSFET. The MOS gate trench width should be used for the trench MOSFETs in place of the JFET width in the DMOSFET. The spreading

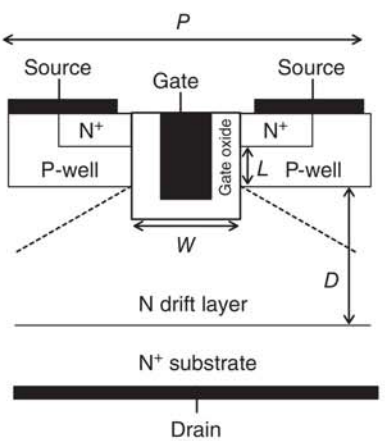


Figure 12.21 4H-SiC trench MOSFET dimensions for on-resistance calculations.

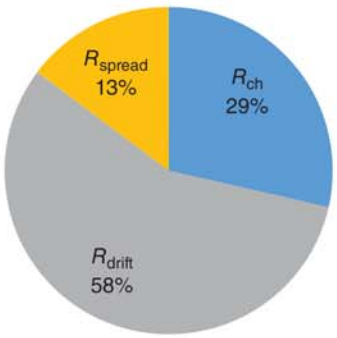
resistance can be expressed as below.

$$R_{\text{spread}} = \frac{P}{1.74q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \ln\left(\frac{P}{W}\right) - \frac{P-W}{1.74q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}}$$
$$= \frac{P}{1.74q \cdot \mu_{\text{n,bulk}} \cdot N_{\text{D}}} \left(\ln\left(\frac{P}{W}\right) - 1 + \frac{W}{P}\right) \quad (12.14)$$

where W is the MOS trench width, as shown in Figure 12.21.

The resistance values of the trench MOSFET, with the same drift layer as the DMOSFET discussed in Section 12.3.1.1 can be calculated with the following assumptions. $\mu_{\text{n,ave}}$ value increases to 24 $\text{cm}^2/\text{V s}$ (from 12 $\text{cm}^2/\text{V s}$ for DMOSFETs), and the cell pitch P decreases to 5 μm (from 10 μm for DMOSFETs), with a trench width W of 1 μm. All the other parameters stay the same: $\mu_{\text{n,bulk}}$ of 700 $\text{cm}^2/\text{V s}$ at room temperature, a drift layer thickness of 9 μm, a drift layer doping concentration (N_{D}) of 8×10^{15} cm^{-3}, a MOS channel length (L) of 0.5 μm, a $V_{\text{g}} - V_{\text{th}}$ of 12 V, and a C_{ox} of 8.63×10^{-8} F/cm^2. Using these values, we can get the values for the resistance components, normalized for the area as shown in Figure 12.22. The MOS channel resistance of this device accounts for only 29% of the total on-resistance. The trench MOSFET structure showed approximately 53% reduction in on-resistance compared to the DMOSFET using the same drift layer.

4H-SiC Trench MOSFET Optimization The simple trench MOSFET structure, discussed in Section 12.3.1.2, works very well in silicon, since the breakdown E-field for SiO_2 is 2 orders of magnitude greater than that of silicon; hence, oxide breakdown is not an issue in silicon devices. However, the breakdown E-field of 4H-SiC is approximately a factor of 3 lower than the theoretical breakdown E-field of SiO_2. The E-field increases further at the SiO_2/SiC interface by more than a factor of 2 due to the difference in dielectric constant between the two materials. This represents a huge reliability issue of 4H-SiC trench MOSFETs. For reliable operations, the gate oxide



Resistance component	Value
R_{ch}	0.504 mΩ-cm^2
R_{drift}	1.00 mΩ-cm^2
R_{spread}	0.260 mΩ-cm^2
Total	1.76 mΩ-cm^2

Figure 12.22 4H-SiC trench MOSFET resistance components. Assumptions: $\mu_{\text{n,ave}}$ of 24 $\text{cm}^2/\text{V s}$, $\mu_{\text{n,bulk}}$ of 700 $\text{cm}^2/\text{V s}$, a cell pitch (P) of 5 μm, a MOS trench width (W) of 1 μm, drift layer thickness of 9 μm, a drift layer doping concentration (N_{D}) of 8×10^{15} cm^{-3}, a MOS channel length (L) of 0.5 μm, a $V_{\text{g}} - V_{\text{th}}$ of 12 V, and a C_{ox} of 8.63×10^{-8} F/cm^2.

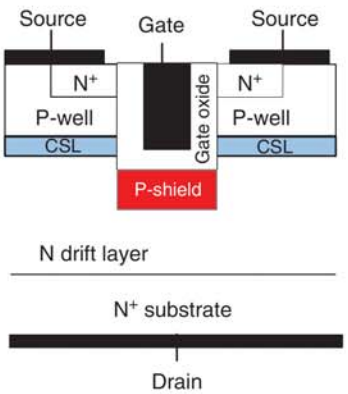


Figure 12.23 Cross section of the 4H-SiC trench MOSFET with trench bottom protection. The device includes a p-type implant in the bottom of the trench and an n-type current spreading epilayer (CSL) beneath the p-base. Sources: Tan et al. [41], Kyogoku et al. [42].

at the trench bottom must be properly shielded from the high voltage during the off-state.

Figure 12.23 shows a 4H-SiC trench MOSFET structure with a p-type implanted in the bottom of the gate trench. The p-shielding region was connected to the source region and provided excellent protection to the gate oxide at the bottom of the trench. It should be noted that this p-type protection layer and the p-base of the trench MOSFET can form a very narrow JFET region, which can add significant amount of JFET resistance, increasing the total on-resistance of the structure. This issue was addressed by placing a thin, heavier doped n-type current spreading layer (CSL) beneath the p-base layer [41]. The device used a 10 μm thick drift layer and demonstrated a blocking voltage of 1400 V and an on-resistance of 15.7 mΩ-cm^2. It should be noted that the gate-to-drain capacitance is very small, but switching losses will increase if the resistance between the protection p-region and source is very high. Layout must be optimized for this structure to achieve optimal on-state and switching performances [42].

Figure 12.24 shows a 4H-SiC trench MOSFET structure with double-trench protection approach [9]. The bottom of the gate trench was shielded by a deeper source trench, place approximately 2 μm away from the gate trench. The MOS channel mobility on the etched sidewall was 11 cm^2/V s, which was considerably lower than that expected for a trench MOSFET in 4H-SiC. With this structure, a specific on-resistance of 0.79 mΩ-cm^2 was achieved for a 630 V 4H-SiC trench MOSFET, and an on-resistance of 1.41 mΩ-cm^2 was achieved for a 1260 V trench MOSFET, respectively.

Figure 12.25 shows a 4H-SiC trench MOSFET structure with asymmetric protection implants. In this device, only one side of the trench sidewall is used as MOS channel, which is exactly aligned to the ⟨1120⟩ crystal plane [43]. The deep p-wells are used to limit the *E*-field in the gate oxide at the bottom and the corners of the trench. This cell structure has a small ratio of the Miller charge (Q_{GD}) to gate–source charge (Q_{GS}). It should be noted that this structure adds significant amount of JFET resistance. However, the added JFET regions resulted in reduced saturation currents, which improved the short circuit withstand time (t_{scwt}).

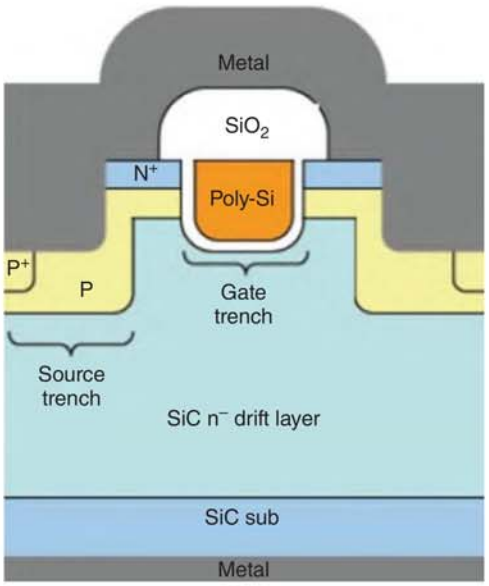


Figure 12.24 Cross section of the 4H-SiC trench MOSFET with double-trench protection. Source: Nakamura et al. [9]. © 2011, IEEE.

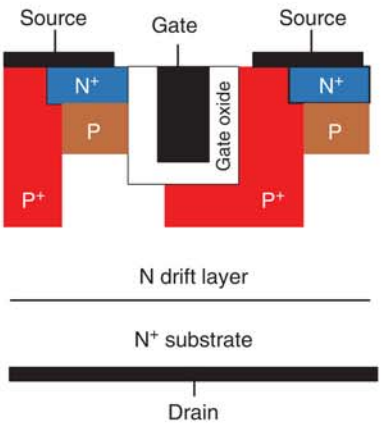


Figure 12.25 Cross section of the 4H-SiC trench MOSFET with asymmetric protection p-well implants. Source: Based on Peters et al. [43].

The a-face of 4H-SiC (sidewalls of trench MOSFET/UMOSFETs) has lower density of interface states (D_{it}) closer to the conduction band edge than the Si-face of 4H-SiC. However, the a-face has significantly more midgap states, which may not impact the MOS channel mobility, but result in significant sub-threshold hysteresis [44, 45]. A preconditioning routine is required to measure threshold voltage from 4H-SiC trench MOSFET. Although this may not impact the device reliability or stability [44], it is preferred to minimize the hysteresis for easier control of the devices. Further developments in MOS surface passivation techniques are recommended, to minimize the impact of midgap interface states.

12.3.2 Advanced Power MOSFET Structures in 4H-SiC

12.3.2.1 Superjunction MOSFETs in 4H-SiC

Superjunction (SJ) structure [18] overcomes the trade-off relationship between breakdown voltage and on-resistance of the conventional semiconductor devices by utilizing a number of alternatively stacked, p- and n-type thin semiconductor layers with heavy doping concentrations. By controlling the degree of doping and the thickness of these layers, low on-resistance and high breakdown voltage can be achieved.

A simplified cross section of a superjunction (SJ) drift layer is shown in Figure 12.26. It is assumed that the entire drift layer has the full SJ structure, and equal widths are used for both N- and P-pillars. In unipolar devices, on-state conduction happens only through the N-pillar. A perfect charge balance is assumed for the N- and P-pillars, and it is assumed that both layers are fully depleted at a relatively low value of drain bias. Once the full depletion is achieved, a rectangular *E*-field profile is achieved in the vertical direction as shown in Figure 12.27, instead of triangular or trapezoidal E-field profile observed in conventional power device structures. As for lateral *E*-field, center of each pillar should have zero field (for both P- and N-pillars) and peak *E*-field should be placed at the lateral metallurgical junction between adjacent P- and N-pillars, as shown in Figure 12.27.

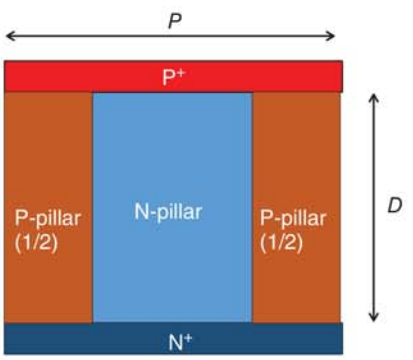


Figure 12.26 Simplified cross section of a superjunction drift layer.

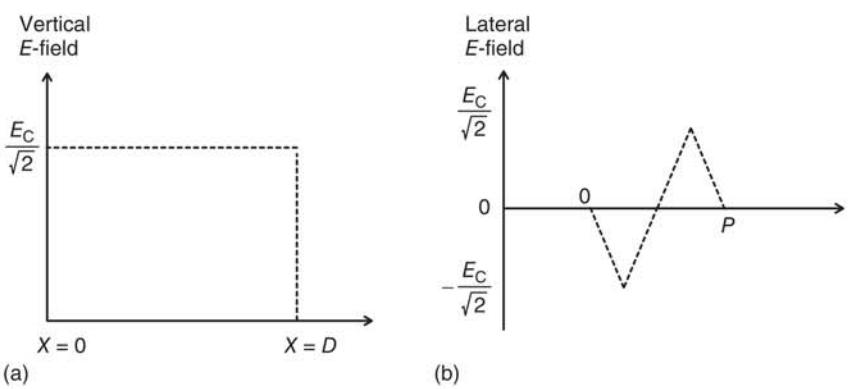


Figure 12.27 *E*-field profile of a superjunction structure in blocking mode. Vertical *E*-field profile (a), and lateral *E*-field profile (b).

For simplicity, peak E-field of $\frac{E_C}{\sqrt{2}}$ is assumed for both vertical E-field and lateral E-field to keep the peak E-field at E_C within the structure.

Doping concentration for the N- and P-pillars can be calculated below.

$$N_A = N_D = \frac{\varepsilon_s \cdot {}^{E_C}/\sqrt{2}}{q \cdot {}^{P}/4} = \frac{4\varepsilon_s \cdot E_C}{\sqrt{2} \cdot q \cdot P} \tag{12.15}$$

Blocking voltage of this structure is given below.

$$V_B = \frac{E_C \cdot D}{\sqrt{2}} \tag{12.16}$$

On-resistance can be calculated from the doping concentration and the dimensions of the structure, and can be expressed as below.

$$R_{on} = \frac{D \cdot P}{q \cdot N_D \cdot {}^{P}/2 \cdot \mu_n} = \frac{2D}{q \cdot N_D \cdot \mu_n} \tag{12.17}$$

From Eqs. (12.15) and (12.16)

$$q \cdot N_D = \frac{4\varepsilon_s \cdot E_C}{\sqrt{2} \cdot P} \quad \text{and} \quad D = \frac{\sqrt{2} \cdot V_B}{E_C} \tag{12.18}$$

Apply this to Eq. (12.17) we get

$$R_{on} = \frac{2V_B}{E_C} \cdot \frac{P}{4\varepsilon_s \cdot E_C \cdot \mu_n} \cdot 2 = \frac{V_B \cdot P}{\varepsilon_s \cdot E_C^2 \cdot \mu_n} \tag{12.19}$$

Theoretical specific on-resistance as a function of blocking voltage for conventional structure and SJ structures with pitch ranging from 2.5 to 20 µm in 4H-SiC is shown in Figure 12.28. Performance points of recent experimental results are also shown in the plot [46–48]. It is shown that the on-resistance can be further reduced by using tighter pitch SJ designs. Also, the on-resistance reduction over conventional structure is more significant for higher voltage devices. As discussed in Sections 12.3.1.1 and 12.3.1.2, 4H-SiC MOSFETs have significant parasitic on-resistance components, such as MOS channel resistance. It is expected that relatively small improvements in device performances will be observed for 4H-SiC SJ MOSFETs with blocking voltages of 1.2 kV or lower. More substantial impacts are expected for higher voltage devices, with blocking voltages of 6 kV or higher.

Superjunction MOSFETs in 4H-SiC, using multiple implants and epi regrowth steps, have been experimentally demonstrated [46, 47, 49, 50]. Dopant diffusion cannot be utilized in the fabrication of superjunction structures in 4H-SiC due to negligible diffusion coefficients in 4H-SiC [49]. Hence, for this type of approach, the superjunction drift layer requires several iterations of thin epigrowth and ion implantations. In Ref. [46], the each iteration of epigrowth was limited to 0.7 µm and 7 iterations of epigrowth and implantation steps were performed to form a drift layer for a 1200 V class device. A blocking voltage of 1170 V and an on-resistance of 0.63 mΩ-cm^2 were reported for this structure [46].

Performance of 4H-SiC superjunction MOSFETs and a conventional trench MOSFET was compared [47, 50]. 1200 V class 4H-SiC superjunction MOSFETs

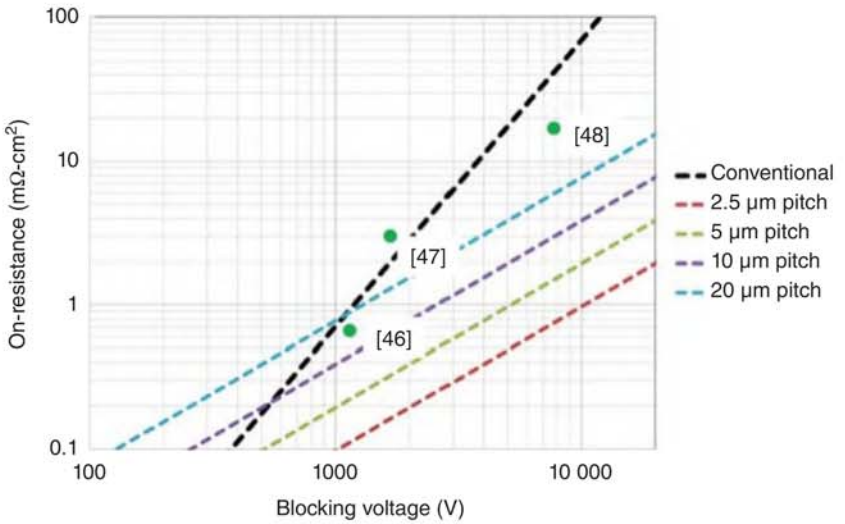


Figure 12.28 Specific on-resistance of a function of breakdown voltage calculated for conventional structure and superjunction structures, with pitch ranging from 2.5 to 20 μm. Includes performance of experimental results. Sources: Masuda et al. [46], Harada et al. [47], Kosugi et al. [48].

with 2.5 and 5 μm pitches were fabricated, as shown in Figure 12.29. The superjunction devices showed very little reduction of on-resistance and slower switching characteristics compared to the conventional devices at room temperature [47]. This was predicted above since the on-resistance of 4H-SiC power MOSFETs with lower blocking voltage is dominated by MOS channel resistance, and drift resistance accounts for a small fraction of the on-resistance. However, the superjunction devices showed measurable advantages in on-resistance at elevated temperatures, as shown in Figure 12.30, where the MOS channel resistance reduces due to a reduction on threshold voltage, and drift resistance increases due to a decrease in bulk mobility

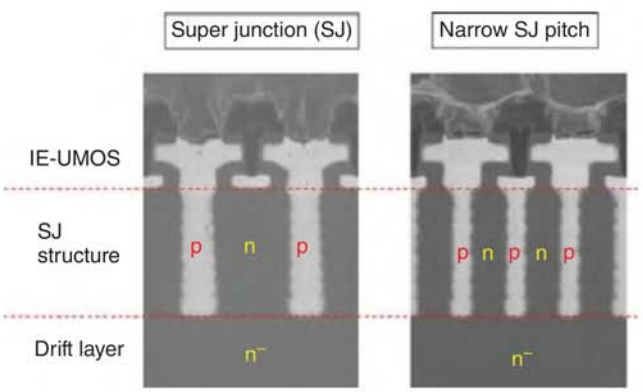


Figure 12.29 Scanning electron microscopy (SEM) images of 4H-SiC superjunction MOSFETs with different pitches. Source: Kobayashi et al. [50].

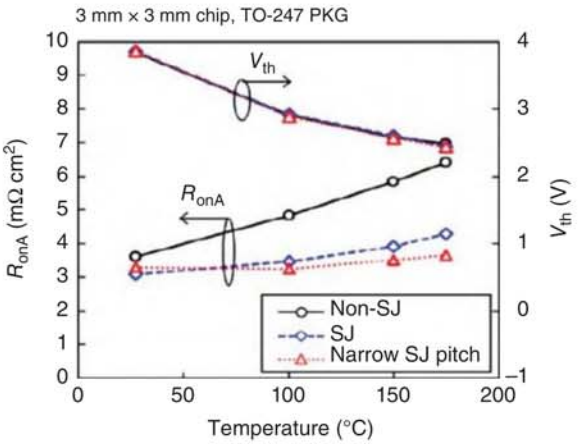


Figure 12.30
On-resistance and threshold voltage as a function of temperature for a conventional device and superjunction MOSFETs. Source: Kobayashi et al. [50]. © 2019, IEEE.

at elevated temperatures. Superjunction devices showed significantly smaller rate of increase in on-resistance over temperature compared to the conventional device. The superjunction device with tighter pitch and higher drift doping concentration showed smaller rate of increase compared to the SJ device with larger pitch.

As discussed above, the benefits of superjunction structure are greater for higher voltage (>6 kV) devices. It is technically possible to build devices using multiple regrowth approach, but such approach is not realistic due to manufacturing costs associated with the approach. For such thick superjunction structures, "trench etch and refill" approach is more reasonable. A 6.5 kV 4H-SiC MOSFET with partial superjunction structure, with 23 μm thick superjunction region and 41 μm thick, 2×10^{15} cm^{-3} doped drift region was experimentally demonstrated [48, 51]. A trench pitch of 5 μm was used. For proper epi-fill of the trenches, the trenches must be precisely aligned to $\langle 11\bar{2}0 \rangle$ direction. 4H-SiC power DMOSFET structure with a cell pitch of 10 μm was built on the superjunction drift layer to complete the fabrication of the device. The completed 4H-SiC partial SJ MOSFET showed an on-resistance of 17.8 mΩ-cm^2 with a blocking voltage of 7.8 kV. The on-resistance values measured from this device is significantly lower that the theoretical 1-D limit for 4H-SiC drift resistance.

12.3.2.2 Integrated JBS Diodes in 4H-SiC Power MOSFETs

4H-SiC power MOSFETs with integrated JBS diodes are being investigated to prevent the growth of stacking faults caused by basal plane dislocations, as well as improve the reverse recovery performance of the built-in body diode [52–56]. Schematic behaviors of a 4H-SiC MOSFET with integrated JBS diode and a conventional MOSFET with an external JBS diode are depicted in Figure 12.31. To suppress the pn junction from injecting minority carriers, the applied voltage across the pn junction should be less than its built-in potential. For 4H-SiC power MOSFETs with integrated JBS diodes, this is relatively easy since the only requirement is to keep the voltage drop across the Schottky contact and the JFET region below the Schottky contact to less than the pn junction built-in potential. When external JBS diodes are used, voltage drop of the entire structure and associated inductances must be

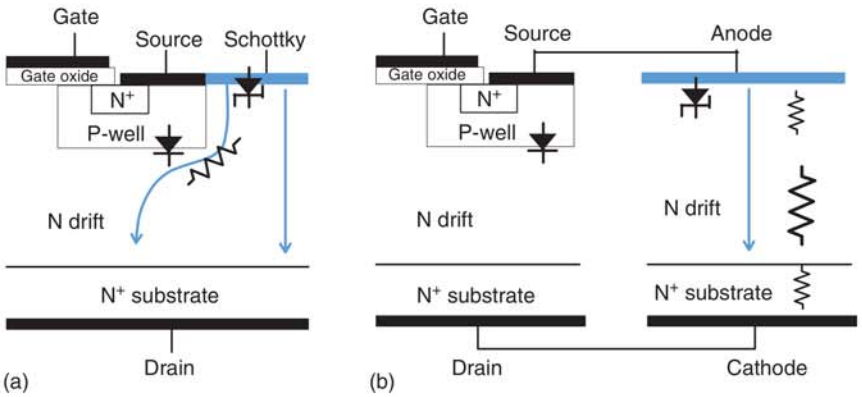


Figure 12.31 Cross section of (a) a MOSFET embedding SBD, (b) a conventional MOSFET coupled with an external SBD.

less than the built-in potential of the pn junction. Experimental demonstration of such structure was shown for the 4H-SiC planar MOSFETs [52, 53, 56] and 4H-SiC trench MOSFETs [54, 55]. 4H-SiC MOSFETs with integrated JBS diodes showed superior switching performances over the conventional option, which used external JBS diodes [53]. With savings in the chip size and performance advantages, 4H-SiC power MOSFETs with integrated JBS diodes were recommended for high speed switching applications [53]. However, a significant reduction in short-circuit withstand time (t_{scwt}) was reported for 4H-SiC power MOSFETs with integrated JBS diodes [55, 56]. At a short-circuit situation, the leakage current through the Schottky barrier increases due to high junction temperature and the increased Schottky leakage current further increases the junction temperature, which increases the Schottky leakage further, resulting in a destructive positive feedback loop between Schottky leakage current and junction temperature [55]. Usage of higher barrier height Schottky metal was suggested to alleviate this issue, which in turn reduces the effectiveness of the bypass capability of the integrated JBS diode.

12.4 Summary

We reviewed JBS diodes and power MOSFETs in 4H-SiC. In 4H-SiC JBS diodes, the focus has been on improving surge capability and overall power handling capability of the devices. Minority carrier injection from p^+ grid and conductivity modulation of the drift layer enhanced surge current capability of 4H-SiC JBS diodes. Use of trench shield structure, which allowed the use of more aggressively doped drift layer, resulted in significantly reduced conduction losses of the diodes. The conduction losses were further reduced by the use of lower barrier metals, such as Mo compounds, as Schottky barrier metal. It should be noted that an increase of leakage current was also observed with this approach, but the power losses due to this leakage was kept less than 1% of the conduction losses of the diodes.

4H-SiC DMOSFET and trench MOSFET structures were reviewed. In 4H-SiC DMOSFETs, devices with voltage ratings ranging from 900 V to 15 kV have been developed. Devices with blocking voltages of 6 kV or greater show performances very close to the 1-D ideal limit, but the devices with lower voltage ratings showed significantly higher on-resistance than the 1-D limit due to the parasitic resistance components. Surface passivation techniques using phosphorus, boron, and alkali metal elements like barium were attempted to produce higher MOS channel mobility over the current NO- and N_2O-based passivation techniques. Boron- and phosphorus-doped gate oxide devices showed higher MOS channel mobility, but failed to provide sufficient threshold stability. Ba IL passivation technique showed very encouraging results, demonstrating both high MOS channel mobility and good threshold voltage stability, but suffered from density of defects in the gate dielectric. At this point, it is not clear if this was due to a fundamental weakness of the Ba IL process or due to weaknesses in the gate oxide deposition technique used in conjunction with the Ba IL process. 4H-SiC trench MOSFETs have promises of lower on-resistance based on tighter gate packing density and higher MOS channel mobility on etched sidewalls of the gate trench. The challenges in the 4H-SiC trench MOSFET design are in the protection of the trench bottom gate oxide with minimum impact on the device on-resistance. Devices using trench bottom p-implants, double-trench protection, and asymmetric implant protection were developed with very good results. Another challenge in the 4H-SiC trench MOSFETs is the high density of midgap interface traps. The high D_{it} at midgap causes significant subthreshold hysteresis, and for proper threshold measurements, preconditioning steps are needed. Further developments in surface passivation are needed to overcome this issue.

Superjunction MOSFETs were demonstrated in 4H-SiC. 4H-SiC superjunction MOSFETs with lower blocking voltage (around 1.2 kV) used multi-epi growth approach to form the structure. Since the devices were limited by the performance of the 4H-SiC MOS channel, very little performance improvements were observed at room temperature. However, it was observed that the 4H-SiC superjunction MOSFETs have much lower rate of increase in on-resistance at elevated temperatures than conventional structure. Trench etch and epitaxial refill approach was used for a 6.5 kV 4H-SiC superjunction MOSFET. The device used partial superjunction structure, and superjunction drift layer covered only about 1/3 of the drift layer thickness, but still showed about 50% reduction in R_{ds}, on over state-of-the-art conventional 6.5 kV 4H-SiC power MOSFET.

4H-SiC power MOSFETs with integrated JBS diodes were also discussed. The structure provides a very effective way of bypassing the built-in pn junction diode, suppressing the growth of stacking faults and minimizing reverse recovery of the body diode. However, the integration of JBS diodes resulted in significant reduction in short-circuit withstand time.

Power devices in 4H-SiC have come a long way, and significant progress has been made in recent years. 4H-SiC power devices are being accepted in many applications, which include automotives and trains. Most of the development in 4H-SiC power device development, so far, was focused on improving device performance.

It is expected that future development work in 4H-SiC power device development will include more research in device ruggedness and reliability as well as performance enhancements, to enable faster adoption of 4H-SiC power devices in wider range of applications.

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