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Ultra-High-Voltage SiC Power Device

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13.1 Introduction

To reduce CO_2 emissions as a countermeasure against global warming and to meet the increasing energy demand caused by the information explosion and the shift to electric vehicles, large scale introduction of renewable energy and energy storage is necessary. At the same time, energy-saving technologies need to be improved to increase the efficiency of energy use. In addition, to control unstable renewable energy and improve energy resilience, there is a need to develop energy management technologies that combine the Internet of Things (IoT) and energy technologies to realize a power system for a safer and more secure society.

In these circumstances, the main transmission system is expected to increase inter-regional interconnections, including the enhancement of long-distance direct current (DC) transmission, and increases in the volume of large-scale offshore wind generation interconnected to the grid. In the load-supply system, large-scale commercial solar power and storage batteries are expected to be installed extensively. In addition, in the last one-mile distribution system, energy management businesses such as demand response (DR) and virtual power plants (VPPs) that utilize small- and medium-sized solar power generation and storage batteries including those for residential use, are expected to expand in order to provide electricity within the region. Given that these next-generation power networks are designed with the best mixture of DC and AC, power converters are a key component. These power electronics should be compact, highly efficient, highly reliable, and low cost. Therefore, the role of power electronics and power electronic equipment has become increasingly important in the energy value chain with the fusion of energy and information.

Power electronics and power devices are the two sides of the ongoing evolution in energy distribution and consumption. The recent power electronics evolution,

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

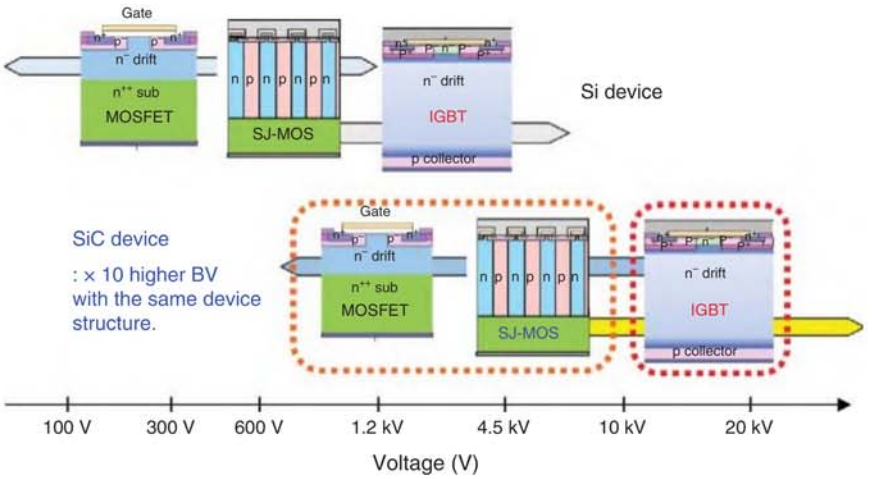

Figure 13.1 Comparison of advanced Si and SiC devices.

in particular, has been supported by the improvement of the trade-off between the reduction of conduction loss and switching loss in silicon (Si)-IGBT (Insulated Gate Bipolar Transistor). However, since the performance improvement of Si-IGBTs has reached a physical limit, expectations for wide band gap semiconductor devices are increasing. Silicon carbide (SiC) has a band gap three times larger than that of Si and a three times higher thermal conductivity. The breakdown electric field of SiC is 10 times higher than that of Si, allowing SiC devices to achieve 10 times higher breakdown voltages (BVs) than Si devices with the same structure, as shown in Figure 13.1, along with a high junction temperature. Therefore, by replacing 600 V–3.3 kV Si bipolar devices with unipolar SiC-MOSFETs (metal-oxide semiconductor field effect transistors) and SBDs, the size and cost of power electronics components are expected to be reduced significantly with low conduction loss and switching loss, thus social implementation has begun [1].

Another advantage of utilizing SiC-MOSFET body diodes is that the external SBD can be omitted. The use of a recombination enhancing layer and a built-in SBD structure suppresses forward degradation problems [2–4].

Conversely, the next generation SiC power devices, similar to the history of Si devices, the application of SJ (super junction) and IGBT structures are being considered to maximize the potential of SiC. By applying the SJ structure, a significant reduction of the drift layer on-resistance below the unipolar limit can be expected in the 1.2–6.5 kV range. Furthermore, if we apply the IGBT structure to SiC, over 10 kV MOS-controlled switching devices can be realized, which is difficult to attain with Si devices [5–9]. The application of high-voltage and ultra-high-voltage devices to high-voltage power electronics equipment used in next-generation power systems is expected to result in smaller size, higher efficiency, and lower cost.

In this chapter, elemental technologies related to ultra-high voltage SiC-PIN diodes and SiC-IGBTs are described, and static and dynamic characteristics such as BV and forward characteristics are explained based on simulation and experimental results (Figure 13.2).

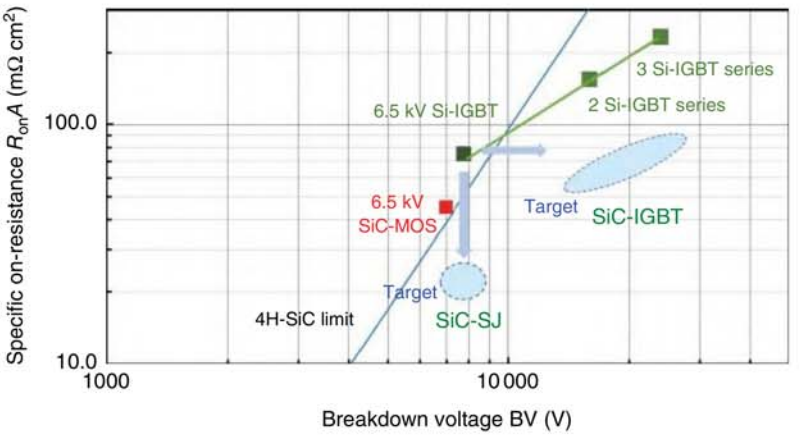

Figure 13.2 Specific on-resistance of SiC SJ-MOSFET and SiC-IGBT compared with Si-IGBT and normal SiC-MOS.

13.2 Ultra-high-voltage SiC PiN diode and SiC-IGBT

Structural comparison between a 1.2 kV class SiC MOSFET and an ultra-high-voltage bipolar device which operates at voltages > 10 kV is shown in Fig. 13.3. A 1.2 kV MOSFET has an n-layer thickness of approximately 10 µm, whereas an ultra-high-voltage device at 10 kV and higher requires an n-layer thickness which is 10 times higher and an impurity concentration of 5e 14 cm^{-3} or less. In a unipolar device where only electrons contribute to conduction, the on-resistance of the 100 µm n-layer is more than 100 mΩ cm^2 at elevated temperatures and the current

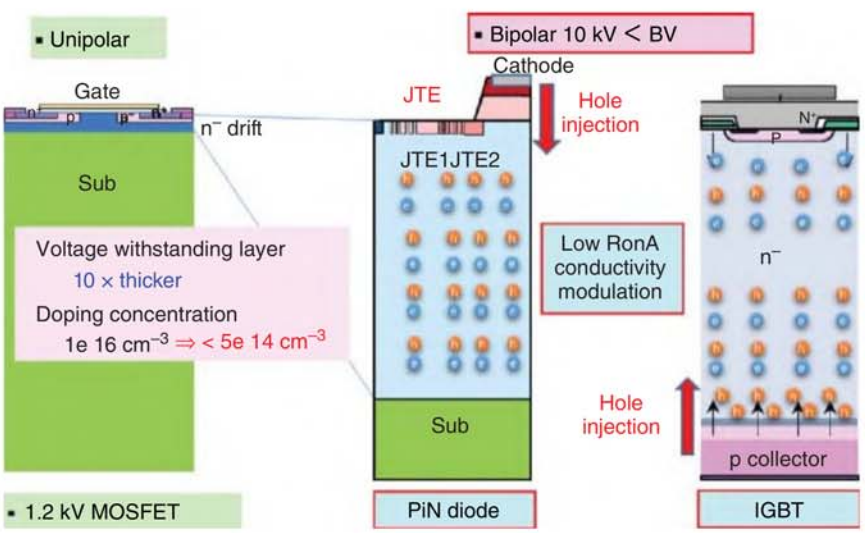

Figure 13.3 Structural comparison of unipolar 1.2 kV SiC-MOSFET and over 10 kV SiC-PiN and SiC-IGBT.

density cannot be increased. In contrast, in bipolar devices, the carrier density can be increased by conductivity modulation and the resistance can be greatly reduced by injecting holes into the n-layer. In a PiN diode, the hole is injected from the cathode at the top, whereas in an IGBT, the hole is injected from the collector at the back. In conductivity modulation, the lifetime carrier has a significant impact.

In the following chapters, the requirements for the n-layer thickness and concentration, edge termination voltage structure, and the carrier lifetime for sufficient conductivity modulation in ultra-high-voltage devices will be explained based on simulations and experimental results.

13.3 Reverse Characteristics of SiC Bipolar Device

13.3.1 Relationship Between Thickness and Density of Drift Layer and Breakdown Voltage

Compared with Si, SiC has an order of magnitude greater breakdown electric field. Therefore, the thickness of the drift layer can be lower, and the density of the drift layer can be higher. In this section, the relationships between the theoretical BV of pn junctions with $N_a \gg N_a$ and the thickness and doping concentration of the drift layer are presented.

Since the depletion layer can be considered to extend only into the n-type drift layer, the equation for the one-dimensional electrostatic field in the depletion layer can be expressed as

$$\frac{\mathrm{d}E(x)}{\mathrm{d}x} = \frac{\rho(x)}{\varepsilon_\mathrm{r}\varepsilon_0} = \frac{eN_\mathrm{d}}{\varepsilon_\mathrm{r}\varepsilon_0} = \text{const.} \tag{13.1}$$

$$-\frac{\mathrm{d}V(x)}{\mathrm{d}x} = E(x) \tag{13.2}$$

where ε_r and ε_0 denote the relative permittivity and permittivity of vacuum, respectively. Here, if the depletion layer width $D <$ the drift layer thickness W, $E(D) = 0$, and $V(0) = 0$, they can be arranged as

$$E(x) = \frac{eN_\mathrm{d}}{\varepsilon_\mathrm{r}\varepsilon_0}(x - D) \tag{13.3}$$

$$V(x) = \frac{eN_\mathrm{d}}{2\varepsilon_\mathrm{r}\varepsilon_0}(2D - x)x \tag{13.4}$$

Here, the electric field takes a negative maximum value $-E_\mathrm{max}$ at $x = 0$, and the voltage takes a maximum value of V_max at $x = D$. By using these conditions, and deleting D, these equations can be arranged as

$$V_\mathrm{max} = \frac{eN_\mathrm{d}}{2\varepsilon_\mathrm{r}\varepsilon_0}\left(\frac{\varepsilon_\mathrm{r}\varepsilon_0}{eN_\mathrm{d}}E_\mathrm{max}\right)^2 = \frac{\varepsilon_\mathrm{r}\varepsilon_0}{2eN_{\_}}E_\mathrm{max}^2. \tag{13.5}$$

Here, it is reported that the breakdown electric field E_B of 4H-SiC is given as a function of the doping density N_d by [10].

$$E_\mathrm{B} = \frac{2.49 \times 10^8}{1 - \frac{1}{4}\log\left(\frac{N_\mathrm{d}}{10^{22}}\right)}[\mathrm{V/m}]. \tag{13.6}$$

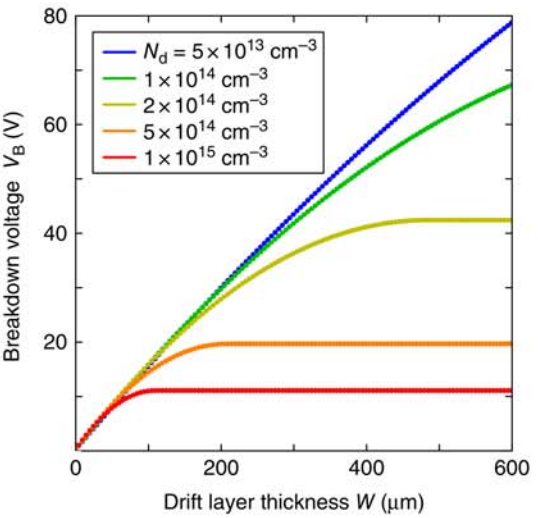

Figure 13.4 Theoretical breakdown voltage calculated from thickness and doping density of the drift layer.

Since $E_{max} = E_B$ at the breakdown, the breakdown voltage V_B can be expressed as

$$V_B = V_{max}(E_{max} = E_B) = \frac{\varepsilon_r \varepsilon_0}{2eN_d} E_B^2 \tag{13.7}$$

Next, if the depletion layer width $D >$ the drift layer thickness W, VB can be similarly expressed as

$$V_B = V(W) = W\left(E_B - \frac{eN_d W}{2\varepsilon_r \varepsilon_0}\right) = W\left[\frac{2.49\times10^8}{1 - \frac{1}{4}\log\left(\frac{N_d}{10^{22}}\right)} - \frac{eN_d W}{2\varepsilon_r \varepsilon_0}\right] \tag{13.8}$$

Figure 13.4 shows the theoretical BV calculated from the drift layer thickness and drift layer density. It is seen that 4H-SiC has a high BV. Nevertheless, BV is highly dependent on the termination structure; therefore, optimization of the termination structure will continue to be important in the future. Then, the termination structure has to be evaluated by comparing with the theoretical and experimental BV, and it is also important to verify the high breakdown electric field of SiC by approximating the measured value to the theoretical value.

13.3.2 Termination Structure of SiC Bipolar Devices

As discussed above, SiC has a very high theoretical BV value. However, it is difficult to achieve the theoretical BV because the high-voltage SiC PiN diodes have to form a mesa to separate the devices, and the electric field concentrates at the bottom edge of the mesa, causing breakdown. A JTE (Junction Termination Extention) structure, called the mesa-JTE, is formed around the mesa, as shown in Figure 13.5 [11]. A single-zone JTE formed with a single concentration has a BV of 19.5 kV (65% of the theoretical BV) [11]. It has been reported that a two-zone JTE with a JTE divided into two zones, with the outer concentration lower than the inner concentration and the maximum electric field value of the JTE reduced, is able to hold a

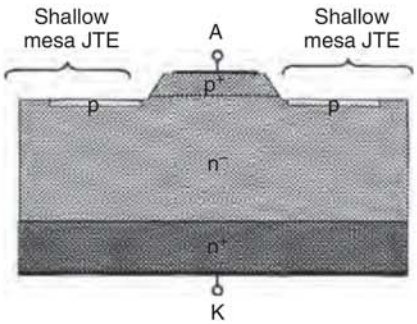

Figure 13.5 Cross-sectional structure of PiN diodes with mesa-JTE structure. Source: Sugawara et al. [11]. © 2001, IEEE.

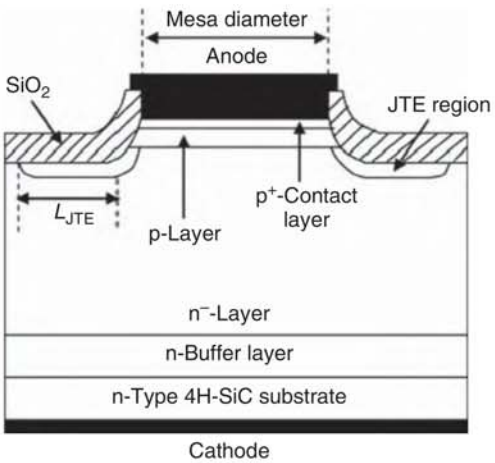

Figure 13.6 Cross-sectional structure of PiN diodes with inclined mesa structure. Source: Hiyoshi et al. [13]. © 2008, IEEE.

voltage of up to 20 kV (72% of the theoretical BV) [12]. It is also reported that a BV of 10.2 kV (73% of the theoretical BV) can be achieved even in a single zone when the mesa end is gently inclined as shown in Figure 13.6 [13]. Making the JTE multi-zone improves the BV but increases the number of ion implantations. Therefore, as shown in Figure 13.7, the concentration of the JTE is changed by adjusting the width of the mask for ion implantation and the JTE is multi-zoned with one ion implantation. It has been reported that a BV of 6.4 kV (90% of the theoretical BV) could be achieved using this method [14]. Furthermore, a BV of 21.7 kV (81% of the theoretical BV) has been achieved by introducing guard rings with gradually varying widths and spacing into the JTE, called as space-modulated JTE, as shown in Figure 13.8 [15]. By comparing the BV with the theoretical BV, it is possible to evaluate the JTE structure and demonstrate the high breakdown electric field strength of SiC.

13.4 Carrier Lifetime Dependence on the Characteristics of Bipolar Device

Power electronics devices such as inverters must be evaluated for their suitability in terms of power loss, expressed as the sum of the on-state and switching losses.

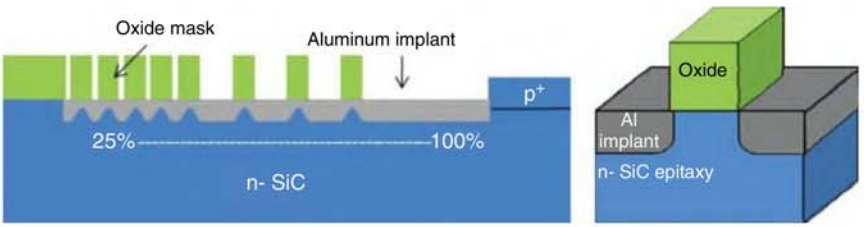

Figure 13.7 Cross-sectional structure of PiN diodes with multi-zone JTE structure with adjusted mask width. Source: Snook et al. [14]. © 2012, Trans Tech Publications Ltd.

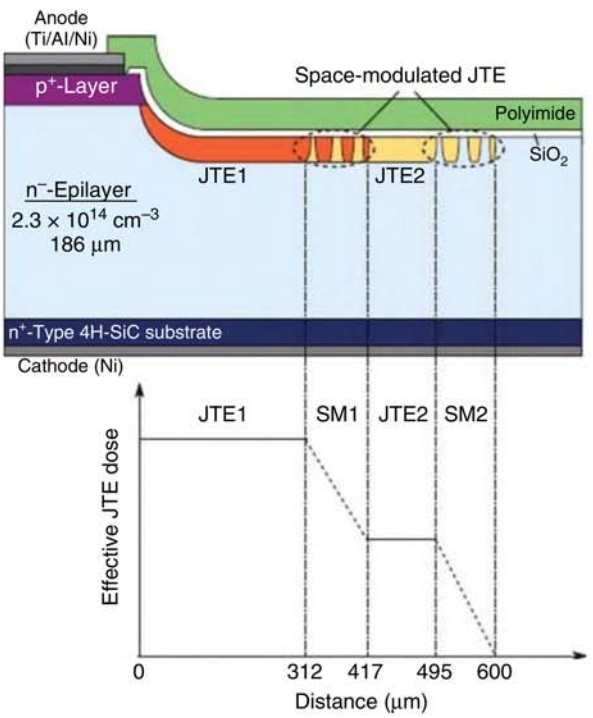

Figure 13.8 Cross-sectional structure of a PiN diode with a space-modulated JTE structure. Source: Niwa et al. [15]. © 2012, The Japan Society of Applied Physics.

In the case of diodes, the on-state loss is determined by the forward current–voltage characteristic and the switching loss is determined by the reverse recovery characteristic. For a bipolar device, such as PiN diode and IGBT, as shown in Figure 13.9, the forward voltage decreases and the reverse recovery loss increases, as the temperature increases. Improving this trade-off will be a key development. Since the carrier lifetime is important for devices such as 4H-SiC pn diodes with pn structure, it is necessary to evaluate the carrier lifetime in real devices. Therefore, a technology is required for evaluating the carrier lifetime by using electrical characteristics.

In this section, the static characteristics, dynamic characteristics, and their evaluation techniques are described.

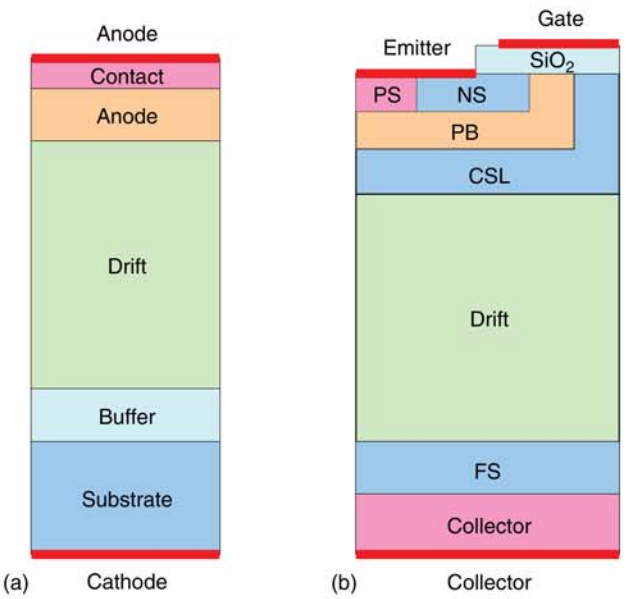

Figure 13.9 Relationship between the carrier life and the current density of the SiC PiN diode. (a) PiN diode and (b) IGBT.

13.4.1 Forward Characteristics of pn Diode

13.4.1.1 Analysis of Characteristics Under Low-Level Injection

Due to the wider band gap of SiC, the formation and recombination of carriers in the depletion layer cannot be ignored. Therefore, the static electrical characteristics of SiC pn diodes deviate from the ideal characteristics. The forward current density J_f of the pn diode at the forward bias is expressed as the sum of the diffusion current and recombination current, and it can be shown that [16]

$$J_f = e\left(\frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a}\right) n_i^2 \exp\left(\frac{eV}{kT}\right) + \frac{eW}{2} s v N_t n_i \exp\left(\frac{eV}{2kT}\right) \tag{13.9}$$

where e is the charge of the electron, D_p and L_p are the diffusion coefficient and diffusion length of the hole, respectively, D_n and L_n are the diffusion coefficient and diffusion length of the electron, respectively, N_a is the acceptor density of the p layer, N_d is the donor density of the n layer, n_i is the intrinsic carrier density, V is the applied voltage, k is the Boltzmann constant, T denotes the temperature, W is the depletion layer thickness, s and v are the carrier capture cross section and thermal velocity, and N_t is the trap density.

Here, the diffusion coefficient can be expressed as

$$L_p = \sqrt{D_p \tau_p} \tag{13.10}$$

$$L_n = \sqrt{D_n \tau_n} \tag{13.11}$$

In addition, from the SRH model [17], the carrier lifetime τ can be expressed as

$$\tau = \frac{1}{svN_t} \tag{13.12}$$

The recombination current equation can be shown that

$$J_f = e\left(\frac{1}{N_d}\sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_a}\sqrt{\frac{D_n}{\tau_n}}\right) n_i^2 \exp\left(\frac{eV}{kT}\right) + \frac{eWn_i}{2\tau}\exp\left(\frac{eV}{2kT}\right) \tag{13.13}$$

Assuming that the carrier lifetime is short and the term of the diffusion current in the recombination current is negligible, it can be shown that

$$J_f = \frac{eWn_i}{2\tau}\exp\left(\frac{eV}{2kT}\right) \tag{13.14}$$

The current density at the same voltage is inversely proportional to the carrier lifetime (τ), independent of the thickness of the drift layer. Figure 13.10 shows the relationship between the carrier life and the current density of the SiC PiN diode calculated by TCAD. It can be seen that the current density at 2.0 V is inversely proportional to the carrier lifetime. In contrast, the current density at 2.5 V is nearly inversely proportional to the 1/2 power of the carrier life. This suggests that the recombination current dominates at 2.0 V and the effect of the diffusion current does not become negligible at 2.5 V. 4H-SiC has a large band gap and a small intrinsic carrier density near room temperature (RT), thus the second term in the recombination current equation dominates. In addition, by using Eq. (13.5), the forward current J_f of the pn diode can be expressed as

$$J_f \propto \exp\left(\frac{eV}{nkT}\right) \tag{13.15}$$

where n is an ideal factor. In general, the forward current of a PN diode is dominated by the diffusion current in the equation when n is 1. When n is 2, the recombination current in equation is dominated.

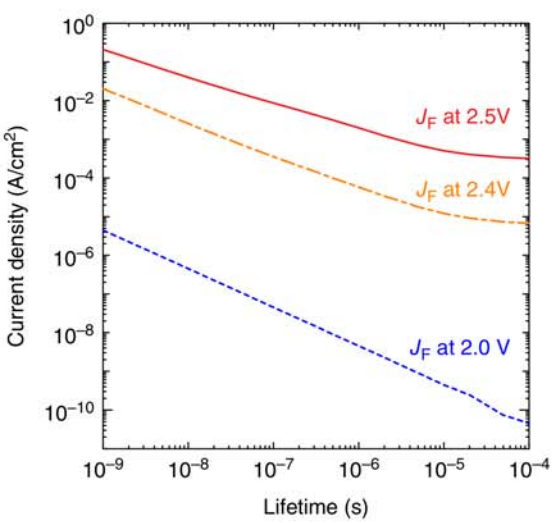

Figure 13.10 Relationship between the carrier life and the current density of the SiC PiN diode.

13.4.1.2 Analysis of Carriers in the Drift Layer Under High-Level Injection

First, we analyze the carrier distribution of the drift layer under high-level injection [18]. Under high-level injection, assuming that the carrier lifetimes of electrons and holes are equal, the continuity equation of the electron and hole, can be expressed as

$$\frac{\partial n}{\partial t} - = \frac{n}{\tau} + \mu_{\mathrm{n}} \frac{\partial (nF)}{\partial x} + D_{\mathrm{n}} \frac{\partial^2 n}{\partial x} \tag{13.16}$$

$$\frac{\partial n}{\partial t} - = \frac{n}{\tau} + \mu_{\mathrm{n}} \frac{\partial (nF)}{\partial x} + D_{\mathrm{n}} \frac{\partial^2 n}{\partial x} \tag{13.17}$$

From the charge–neutral condition, by assuming that p = n holds under high-level injection, by removing $\partial(nF)/\partial x$, it can be shown that

$$(\mu_{\mathrm{n}} + \mu_{\mathrm{p}}) \frac{\partial n}{\partial t} = -(\mu_{\mathrm{n}} + \mu_{\mathrm{p}}) \frac{n}{\tau} + (\mu_{\mathrm{p}} D_{\mathrm{n}} + \mu_{\mathrm{n}} D_{\mathrm{p}}) \frac{\partial^2 n}{\partial x^2}. \tag{13.18}$$

By arranging Eq. (13.18), it can be shown that

$$\frac{\partial n}{\partial t} - = \frac{n}{\tau} + \frac{\mu_{\mathrm{p}} D_{\mathrm{n}} + \mu_{\mathrm{n}} D_{\mathrm{p}}}{\mu_{\mathrm{n}} + \mu_{\mathrm{p}}} \frac{\partial^2 n}{\partial x^2} \tag{13.19}$$

Here, Einstein's relation can be expressed as

$$\frac{D_{\mathrm{n}}}{\mu_{\mathrm{n}}} = \frac{D_{\mathrm{p}}}{\mu_{\mathrm{p}}} = \frac{kT}{e} \tag{13.20}$$

By using Eq. (13.20), Eq. (13.19) can be arranged as

$$\frac{\partial n(x,t)}{\partial t} = -\frac{n(x,t)}{\tau} + D_a \frac{\partial^2 n(x,t)}{\partial x^2} \tag{13.21}$$

This equation is called as diffusion equation. D_{a} is defined as the ambipolar diffusion coefficient, which can be expressed as

$$D_{\mathrm{a}} = \frac{\mu_{\mathrm{p}} D_{\mathrm{n}} + \mu_{\mathrm{n}} D_{\mathrm{p}}}{\mu_{\mathrm{n}} + \mu_{\mathrm{p}}} = \frac{2 D_{\mathrm{n}} D_{\mathrm{p}}}{D_{\mathrm{n}} + D_{\mathrm{p}}} = \frac{2 \mu_{\mathrm{n}} \mu_{\mathrm{p}}}{\mu_{\mathrm{n}} + \mu_{\mathrm{p}}} \frac{kT}{e} \tag{13.22}$$

Under the steady-state condition, it can be written as

$$\frac{\partial n}{\partial t} = 0 \tag{13.23}$$

Equation (13.21) can be fixed by

$$\frac{\partial^2 n}{\partial x^2} - \frac{n}{D_{\mathrm{a}} \tau} = \frac{n}{L_{\mathrm{a}}^2} \tag{13.24}$$

where L_{a} is the ambipolar diffusion length, which can be expressed as

$$L_{\mathrm{a}} = \sqrt{D_{\mathrm{a}} \tau} \tag{13.25}$$

Here, the electron and hole current density (J_{n} and J_{p}) can be expressed as

$$J_{\mathrm{n}} = en\mu_{\mathrm{n}} F + eD_{\mathrm{n}} \frac{\partial n}{\partial x} \tag{13.26}$$

$$J_{\mathrm{p}} = ep\mu_{\mathrm{p}} F - eD_{\mathrm{p}} \frac{\partial p}{\partial x} \tag{13.27}$$

where F denotes the electric field and μ_n and μ_p denote the mobility of electron and hole, respectively. The boundary conditions can be assumed as

$$J_n(0) = 0, \quad J_p(0) = J_a \tag{13.28}$$

$$J_n(d) = J_a, \quad J_p(d) = 0 \tag{13.29}$$

where J_a denotes the total current density. By using these equations, the electron density can be expressed as

$$n(x) = \frac{\tau J_a}{eL_a} \cdot \frac{\frac{\mu_n}{\mu_p}\cosh\left(\frac{x-d}{L_a}\right) + \cosh\left(\frac{x}{L_a}\right)}{\left(\frac{\mu_n}{\mu_p}+1\right)\sinh\left(\frac{d}{L_a}\right)}, \tag{13.30}$$

where d denotes the drift layer thickness.

Here, the stored charge Q in the drift layer can be expressed as

$$Q = \int_0^d eSn(x)\,\mathrm{d}x = S\tau J_a \tag{13.31}$$

The stored charge is independent of the thickness of the drift layer and the mobility but depends on the current and carrier lifetime.

13.4.1.3 Relationship Between Carrier Life, Drift Layer Thickness, and Drift Layer Voltage Drop

By using Eqs. (13.26) and (13.27), and the charge–neutral condition p = n, it can be shown that

$$J_a = J_n + J_p = e(\mu_n + \mu_p)nF + e(D_n - D_p)\frac{\partial n}{\partial x} \tag{13.32}$$

By assuming that the carrier lifetime is sufficiently long, and x, $d = L_a$, it can be shown that

$$n = \overline{n} = \frac{Q}{edS} = \frac{\tau J_a}{ed} \tag{13.33}$$

$$\frac{\partial n}{\partial x} = 0 \tag{13.34}$$

$$F = \frac{V_{drift}}{d} \tag{13.35}$$

By using Eq. (13.32), it can be shown that

$$J_a = (\mu_n + \mu_p)\frac{\tau J_a}{d^2}V_{drift} \tag{13.36}$$

where V_{drift} denotes the voltage drop of the drift layer, which can be expressed as

$$V_{drift} = \frac{d^2}{(\mu_n + \mu_p)\tau} \tag{13.37}$$

The voltage drop of the drift layer at high-level injection is proportional to the square of the drift layer thickness d and inversely proportional to the carrier lifetime. The mobility of electrons and holes at 300 K is set at 950 $cm^2/V\,s$ and 125 $cm^2/V\,s$,

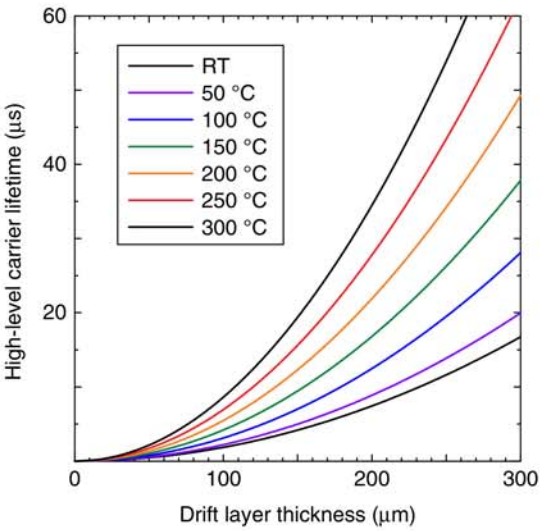

Figure 13.11 Dependence of carrier lifetime on drift layer thickness at each temperature.

respectively, and the temperature coefficient of the mobility of electrons and holes is set at 2.40 and 2.15, respectively [19], and the voltage drop of the drift layer is set at 0.05 V. The drift layer thickness dependence of the carrier lifetime at each temperature is shown in Figure 13.11. If the drift layer thickness is 250 μm, the carrier lifetime would require 12 μs at RT and 44 μs at 250 °C.

On the other hand, the voltage drop in the drift layer increases as the carrier lifetime is shortened. Therefore, the lifetime can be evaluated by measuring the on-voltage and differential on-resistance under high-level injection. In an actual device, $x, d = L_a$ does not hold and Eqs. (13.33)–(13.35) may not hold. Figure 13.12 shows the results of the carrier lifetime dependence of the forward voltage at 100 A/cm^2 using TCAD. As a result, V_F is larger than that of Eq. (13.37).

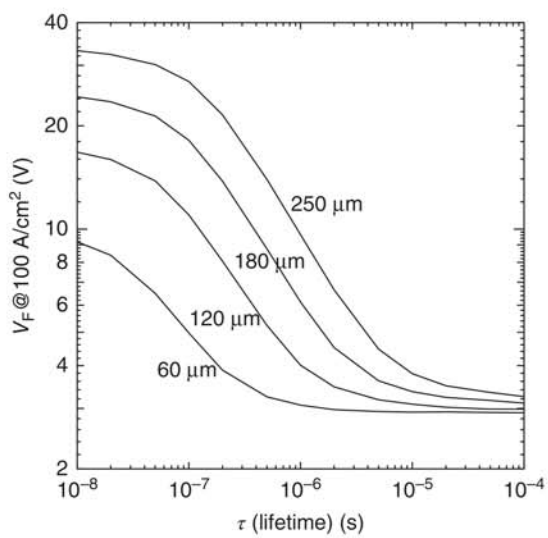

Figure 13.12 Carrier lifetime dependence of forward voltage at 100 A/cm^2 calculated by TCAD.

13.4.2 Reverse Characteristics of pn Diode

13.4.2.1 Reverse Leakage Current Characteristics

The reverse current density J_r of the pn diode is expressed as the sum of the diffusion current and the generated current, and can be expressed as [7]

$$J_r = e\left(\frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a}\right) n_i^2 + \frac{e n_i W}{\tau_e}$$
$$= \sqrt{ekT}\left(\frac{1}{N_d}\sqrt{\frac{\mu_p}{\tau_p}} + \frac{1}{N_a}\sqrt{\frac{\mu_n}{\tau_n}}\right) n_i^2 + \frac{e n_i W}{\tau_e} \tag{13.38}$$

where τ_e denotes the electron–hole pair generation time and Einstein's relationship (13.20) is used. The first term is approximately 1.6×10^{-49} A/cm^2, and the second term is 1.1×10^{-23} A/cm^2, where $T = 300$ K, $N_d = 1 \times 10^{14}$ cm^{-3}, $N_a = 5 \times 10^{18}$ cm^{-3}, $\mu_n = 950$ cm^2/V s, $\mu_p = 125$ cm^2/V s, $\tau_n = 1$ s, $\tau_p = 0.3$ s, $n_i = 5.5 \times 10^{-9}$ cm^{-3}, $W = 120$ μm, and $\tau_e = 1$ s. Since the 4H-SiC has a large band gap and a small intrinsic carrier density near RT, the generated current (second term) dominates. The reverse current of a real 4H-SiC pn diode is measured to be on the order of 10^{-9} A/cm^2. This is thought to be because of the current flowing around the mesa, through the JTE and the surface. In addition, depending on the rise rate of voltage during reverse characterization, a charging current flows into the depletion layer of the PN junction. Since this can be on the order of 10^{-9} A/cm^2, it is necessary to take measures such as decreasing the charging current by increasing the rising time.

13.4.3 Dynamic Characteristics of pn Diode

13.4.3.1 Reverse and Forward Recovery of Characteristics

The dynamic characteristics of PiN diodes include reverse recovery, forward recovery, and OCVD (open-circuit voltage decay). These are these methods for calculating the carrier lifetime.

In the reverse recovery characteristics, the carriers stored during the forward conduction are considered to be equal to the carriers extracted by the reverse recovery current and the analysis is performed. The carrier lifetime τ_{rr} calculated from the reverse recovery characteristics can be expressed as

$$Q = I_f \tau_{rr} = \int i_{rr} dt = \frac{1}{2} I_{rm} t_{rr} \tag{13.39}$$

By using this equation, it can be expressed as [20]

$$\tau_{rr} = \frac{I_{rm} t_{rr}}{2 I_f} \tag{13.40}$$

where Q is the charge stored in the drift layer during forward conduction, I_f is the forward current, i_{rr} is the current under reverse recovery, I_{rm} is the peak reverse recovery current, and t_{rr} is the reverse recovery time.

In the forward recovery characteristics, the carriers injected from the electrodes under forward recovery are considered to be equal to the carriers stored during

forward conduction. The carrier life τ_{fr} calculated from the forward recovery characteristics can be expressed as

$$Q = I_f \tau_{fr} = \int i_{fr} dt = I_f t_{fr} \tag{13.41}$$

By using this equation, it can be shown that [21]

$$\tau_{fr} = t_{fr} \tag{13.42}$$

where i_{fr} is the current under forward recovery and t_{fr} is the forward recovery time.

13.4.3.2 Open-Circuit Voltage Decay

In OCVD, the decrease in voltage after opening the circuit is related to the decrease in carrier density due to the dissipation of carriers; thus, the analysis is performed [22]. A PiN diode with a $p^+/n^-/n^+$ structure is considered as a device, and it is assumed to be in a high-level injection under forward conduction. For zero current, the electric field at the n^- layer, i.e. the voltage drop at the n^- layer, can be ignored, and the voltage between terminals is applied at the p^+/n^- and n^-/n^+ interfaces. Further, we calculate the voltages applied to the p^+/n^- and n^-/n^+ interfaces. The voltage difference at the p^+/n^- interface was determined by using the electric field F, it can be expressed as

$$V_{b1} - V_{j1} = -\int F \, dx \tag{13.43}$$

where V_{b1} is the diffusion voltage at the p^+/n^- interface and V_{j1} is the applied voltage at the p^+/n^- interface. Next, the hole current flowing through the p^+/n^- interface can be expressed as

$$J_p = ep\mu_p F - eD_p \frac{dp}{dx} \tag{13.44}$$

In OCVD, the current is zero, therefore, the electric field F can be expressed as

$$F = \frac{D_p}{\mu_p} \cdot \frac{1}{p} \cdot \frac{dp}{dx} = \frac{kT}{e} \cdot \frac{1}{p} \cdot \frac{dp}{dx} \tag{13.45}$$

where Einstein's relationship is used. By using Eq. (13.45), Eq. (13.43) can be arranged as

$$V_{b1} - V_{j1} = -\int F \, dx = -\frac{kT}{e}(\ln p_n - \ln p_0^+) \tag{13.46}$$

where $p_0{}^+$ is the equilibrium hole density in the p^+ layer and p_n is the hole density on the n^- layer side of the p^+/n^- interface.

Next, the n^-/n^+ interface can be similarly expressed as

$$V_{b2} - V_{j2} = -\int F \, dx = \frac{kT}{e}(\ln n_0^+ - \ln n_n) \tag{13.47}$$

where V_{b2} is the diffusion voltage at the n^-/n^+ interface, V_{j2} is the applied voltage at the n^-/n^+ interface, n_0^+ is the equilibrium electron density at the n^+ layer, and n_n is the electron density on the n^- layer side of the n^-/n^+ interface.

The sum of the diffusion voltage at the junction, $V_{b1} + V_{b2}$, was obtained by using the true carrier density n_i, and can expressed as

$$p_0^+ n_0^+ = n_i^2 \exp\left\{\frac{e}{kT}(V_{b1} + V_{b2})\right\} \tag{13.48}$$

And it can be arranged as

$$V_{b1} + V_{b2} = \frac{kT}{e}\{\ln p_0^+ + \ln n_0^+ - 2\ln n_i\} \tag{13.49}$$

By using Eqs. (13.46), (13.47), and (13.49), the sum of the voltage applied at the p^+/n^- interface and the n^-/n^+ interface can be expressed as

$$V_{j1} + V_{j2} = \frac{kT}{e}\{\ln p_n + \ln n_n - 2\ln n_i\} \tag{13.50}$$

In the case of high-level injection, ignoring the recombination at the interface, the carrier lifetime τ_{HL}, can be expressed as

$$-\frac{dp_n}{dt} = \frac{p_n}{\tau_{HL}} \tag{13.51}$$

$$-\frac{dn_n}{dt} = \frac{n_n}{\tau_{HL}} \tag{13.52}$$

And they can be arranged as

$$\frac{1}{\tau_{HL}} = -\frac{d(\ln p_n)}{dt} \tag{13.53}$$

$$\frac{1}{\tau_{HL}} = -\frac{d(\ln n_n)}{dt} \tag{13.54}$$

Then, the time differentiation of $V_{j1} + V_{j2}$ results in

$$\frac{d(V_{j1} + V_{j2})}{dt} = -\frac{kT}{e} \cdot \frac{2}{\tau_{HL}} \tag{13.55}$$

And it can be arranged as

$$\tau_{HL} = -\frac{2kT}{e} \Big/ \frac{dV_T}{dt} \tag{13.56}$$

where $V_T = V_{j1} + V_{j2}$ is the voltage between the diode terminals, and dV_T/dt is the rate of reduction of the voltage between the terminals.

In the case of low-level injection, the carrier lifetime τ_{LL}, ignoring the recombination at the interface, can be expressed as

$$-\frac{dp_n}{dt} = \frac{p_n}{\tau_{LL}} \tag{13.57}$$

And they can be arranged as

$$\frac{1}{\tau_{LL}} = -\frac{d(\ln p_n)}{dt} \tag{13.58}$$

Then, the time differentiation of $V_{j1} + V_{j2}$ results in

$$\frac{d(V_{j1} + V_{j2})}{dt} = -\frac{kT}{e} \cdot \frac{1}{\tau_{LL}} \tag{13.59}$$

And it can be arranged as

$$\tau_{LL} = -\frac{kT}{e} \Big/ \frac{dV_T}{dt} \tag{13.60}$$

13.4.3.3 Comparison of Reverse and Forward Recovery Characteristics and OCVD

In the reverse recovery characteristic, the carriers taken out by the reverse recovery current become smaller than the stored carriers due to recombination at the pn junction and other effects. With the same idea, the externally injected carriers by the forward recovery current become greater than the stored carriers. Therefore, it is expected that there is a relationship $\tau_{RR} < \tau_{OCVD} < \tau_{FR}$ in the carrier lifetime calculated from each characteristic. In this section, the relationship between the calculated carrier lifetimes and the SRH carrier lifetimes is calculated by using TCAD simulations.

Figure 13.13 shows the relationship of the SRH carrier lifetimes with the carrier lifetimes calculated from the reverse recovery characteristics, forward recovery characteristics, and OCVD using the simulation. Here, we plot the effective electron carrier lifetimes $\tau_{e,dop}$ as the SRH carrier lifetimes, which are calculated from

$$\tau_{e,dop} = \frac{\tau_e}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^{\gamma}} \tag{13.61}$$

$$\tau_{h,dop} = \frac{\tau_h}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^{\gamma}} \tag{13.62}$$

$$\frac{\tau_e}{\tau_h} = 3 \tag{13.63}$$

The red dotted line indicates that the calculated carrier lifetime is the same as the SRH carrier lifetime. The carrier lifetime calculated from OCVD increases with an increase in the SRH carrier lifetime. When the SRH carrier lifetime is small, the relationship $\tau_{RR} < \tau_{OCVD} < \tau_{FR}$ holds. However, when the SRH carrier lifetime

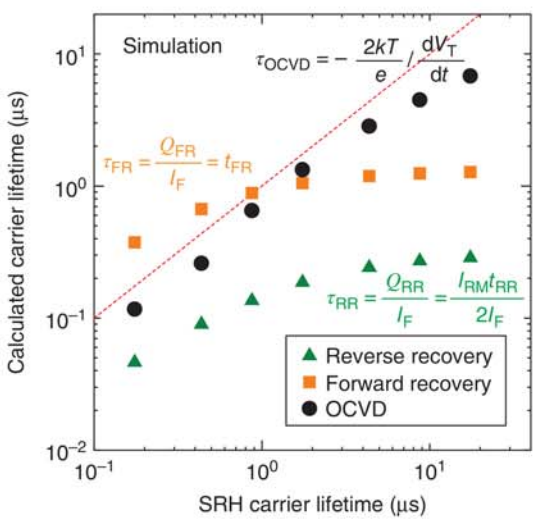

Figure 13.13 Relationship between the carrier lifetimes calculated from the reverse and forward recovery characteristics and OCVD, and the SRH carrier lifetimes: SRH carrier lifetimes are plotted on the effective electron carrier lifetimes $\tau_{e,dop}$.

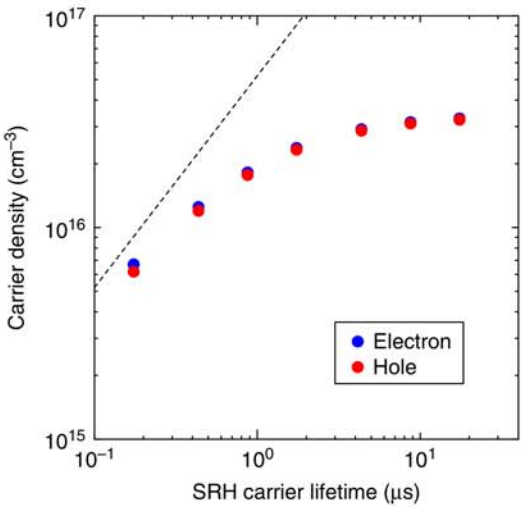

Figure 13.14 Dependence of the averaged density of electrons and holes in the drift layer at 100 A/cm^2 on the SRH carrier lifetime in the simulation: the dotted line plots the relationship between the SRH carrier lifetime, and the carrier density calculated from Eq. (13.33).

increases, the carrier lifetime calculated from the reverse and forward recovery characteristics gradually becomes saturated, which can be shown as $\tau_{RR} < \tau_{FR} < \tau_{OCVD}$.

We first investigated the charge stored in the drift layer at 100 A/cm^2. Figure 13.14 shows the dependence of the averaged electron and hole densities in the drift layer at 100 A/cm^2 on the SRH carrier lifetime. The dotted line plots the relationship between the SRH carrier lifetime and the carrier density calculated from (13.33). The averaged electron and hole densities in the drift layer deviate from Eq. (13.33) and tend to be saturated as well as the carrier lifetime calculated from the reverse and forward recovery characteristics. Figure 13.15 shows the carrier density distribution calculated from the TCAD simulation. This figure shows that the

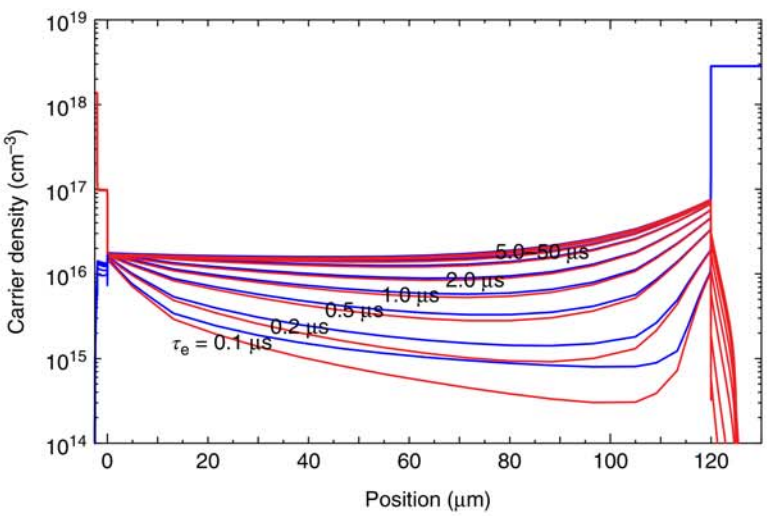

Figure 13.15 Dependence of the distribution of electron and hole densities in the drift layer at 100 A/cm^2 on the SRH carrier lifetime in the TCAD simulation.

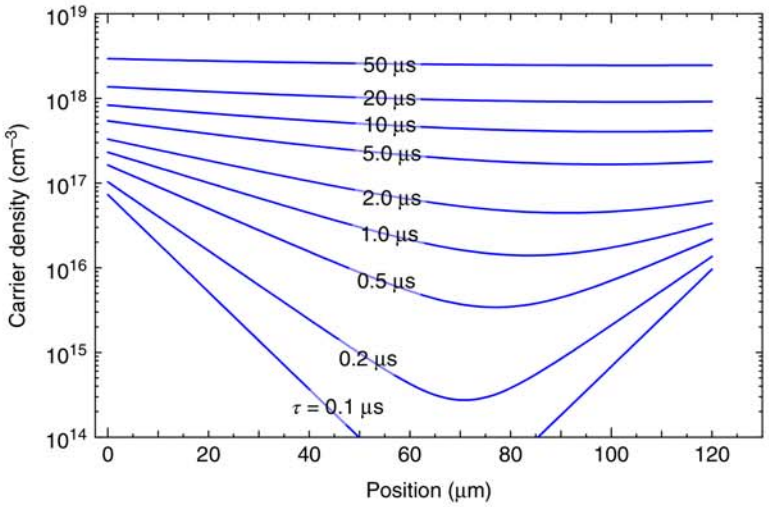

Figure 13.16 The distribution of carrier density calculated from Eq. (13.30): the mobility of electrons and holes is set to $\mu_n = 950\ cm^2/V\,s$ and $\mu_p = 125\ cm^2/V\,s$, respectively.

distribution of carrier densities does not change as the SRH carrier lifetime increases more than 5 μs. In Eq. (13.30), the electron and hole mobilities are set to $\mu_n = 950\,cm^2/V\,s$ and $\mu_p = 125\,cm^2/V\,s$, respectively, and the distribution of carrier density is shown in Figure 13.16. The carrier densities calculated from device simulations (Figure 13.15), show that the carrier density on the n^- drift layer side of the p^+/n^- interface saturates at around 1.5 to $1.7\times10^{16}\,cm^{-3}$, and that on the n^- drift layer side of the n^-/n^+ interface saturates at around 6.5 to $7.0\times10^{16}\,cm^{-3}$. On the other hand, as shown in Figure 13.16, the carrier density on the n^- drift layer side of the p^+/n^- interface increases from 7×10^{16} to $3\times10^{18}\,cm^{-3}$. Therefore, it can be concluded that the charge stored in the drift layer does not increase even though the carrier lifetime increases because the voltage and current are increased without sufficient carriers being injected into the drift layer due to the voltage drop at the interface. As shown in Figure 13.13, as the carrier lifetime increases, the carrier lifetimes calculated from the reverse and forward recovery characteristics become saturated, whereas those calculated from OCVD do not saturate as the SRH carrier lifetime increases. Therefore, OCVD is suitable as a method to estimate the carrier lifetime accurately from the dynamic characteristics.

13.5 Design and Device Performance of Bipolar Device

Bipolar devices in an inverter consist of IGBTs for switching and diodes for regurgitation. In this section, we describe the characteristics of these two devices.

In order to reduce the conduction losses in 4H-SiC bipolar devices, it is necessary to reduce the on-voltage by increasing the carrier lifetime and causing sufficient conductivity modulation throughout the drift layer. Although 4H-SiC is an indirect

transition type semiconductor, its carrier lifetime is very short, only a few μs. Particularly, 4H-SiC bipolar devices with high voltages of over 10 kV require an improvement in the carrier lifetime due to the thick drift layer. The main factor limiting the carrier lifetime of 4H-SiC is the point defect $Z_{1/2}$ center, which traps electrons and acts as a hole trap. The $Z_{1/2}$ centers are caused by carbon vacancies and are introduced by thermal equilibrium conditions during epitaxial growth, so it is difficult to realize long carrier lifetimes. In order to reduce the $Z_{1/2}$ center density, two methods are proposed to reduce the carbon vacancies by supplying interstitial carbon to 4H-SiC, taking advantage of the high diffusion coefficient of interstitial carbon in 4H-SiC. One method is the thermal oxidation of the 4H-SiC surface, wherein the excess carbon generated by the thermal oxidation is diffused into the 4H-SiC as interstitial carbon. The other method is the ion implantation of carbon atoms on the surface of 4H-SiC, and the implanted carbon is diffused into 4H-SiC as interstitial carbon by annealing. Both methods give a carrier lifetime of 20 μs for the bulk, excluding the effect of surface recombination. However, there are few reports on the electrical properties of 4H-SiC bipolar devices with thick drift layers, which are required for a longer carrier lifetime and high voltages. In this section, the electrical characteristics of 4H-SiC bipolar devices with extended carrier lifetime are investigated by device simulations.

In addition, the total loss of an IGBT or PiN diode is expressed as the sum of the on-state and switching losses. Therefore, the evaluation of IGBTs and PiN diodes is important not only for the on-state losses but also for the switching losses. In this section, we also investigate the on-state and switching losses of IGBT and PiN diodes with different BVs for different carrier lifetimes of the drift layer.

13.5.1 Carrier lifetime dependence

The hole density distributions in the drift layers of PiN diodes and IGBTs are shown in Figure 13.17. The blue and red lines indicate that the ambipolar carrier life (τ_a) is 1 and 10 μs, respectively. Both carrier distributions exhibit a concave shape and approach a flat shape as the carrier lifetime τ_a increases. A longer carrier lifetime leads to conductivity modulation and an increase in the hole density. In addition, the carrier densities of both the p-anode side of the PiN diode and the p-collector side of the IGBT are similar because the density of the p-layer, as well as the hole injection from the p-layer, is comparable. On the other hand, the electron density on the emitter side of the IGBT is significantly lower than that on the n-cathode side of the PiN diode because the injected electrons on the n-cathode side of the PiN diode and the emitter side of the IGBT are very different.

The forward characteristics of the PiN diodes and the on-state characteristics of the IGBTs are shown in Figure 13.18. As the carrier lifetime increases, the forward voltage and the on-state voltage decrease.

The electron and hole currents in the drift layer are dominated by the drift current, and ignoring the diffusion current, the total current can be expressed as

$$J_a = J_n + J_p = e(n\mu_n + p\mu_p)F = en(\mu_n + \mu_p)F \tag{13.64}$$

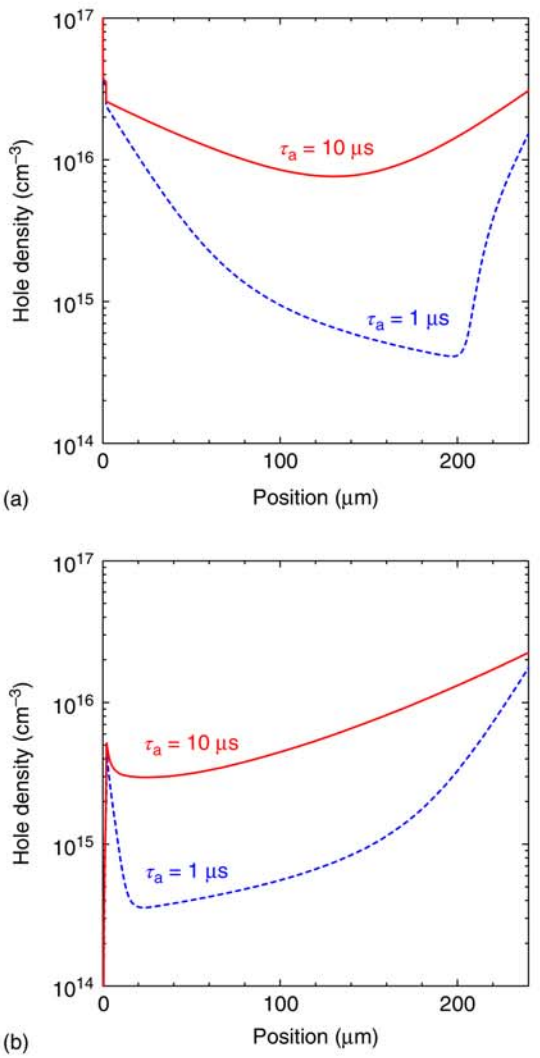

Figure 13.17 Hole density distribution of (a) PiN diode and (b) IGBT.

where n = p from the charge neutral condition. Then, the voltage drop in the drift layer can be expressed as

$$V_{\text{drift}} = \int F\,\mathrm{d}x = \int \frac{J_{\text{a}}}{en(\mu_{\text{n}} + \mu_{\text{p}})}\mathrm{d}x = \frac{J_{\text{a}}}{e(\mu_{\text{n}} + \mu_{\text{p}})}\int \frac{\mathrm{d}x}{n} \tag{13.65}$$

As the carrier density n increases, the voltage drop of the drift layer V_{drift} decreases. From Eq. (13.31), as the carrier lifetime increases, the carrier density in the drift layer increases and the forward voltage of the PiN diode and the on-voltage of the IGBT decrease, as shown in Figure 13.18. In addition, since the carrier density on the n-cathode side of the PiN diode is greater than that on the emitter side of the IGBT, the forward voltage of the PiN diode is smaller than the on-voltage of the IGBT.

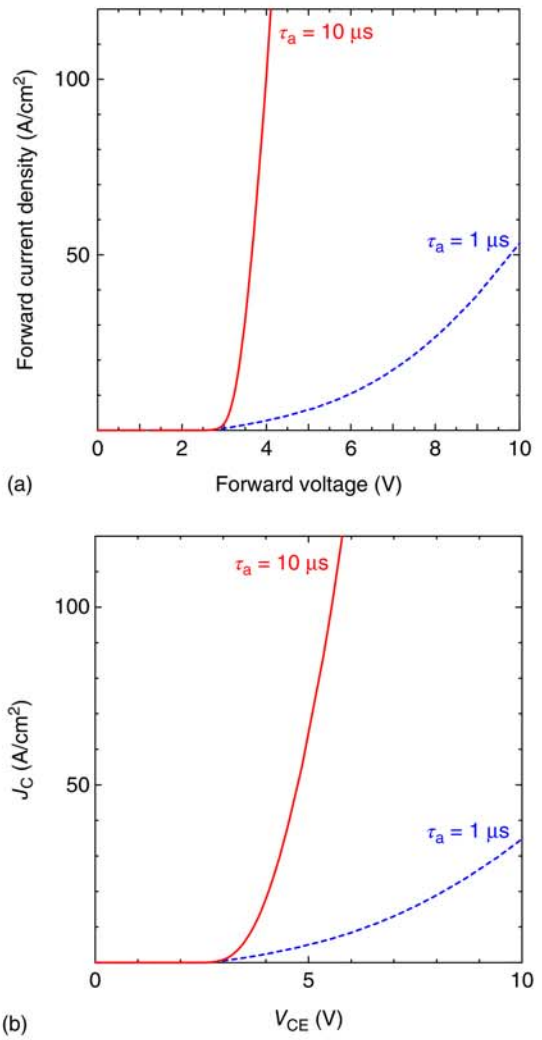

Figure 13.18 Forward characteristics of (a) PiN diode and (b) IGBT.

Therefore, it is important to reduce the on-voltage of the IGBT by increasing the carrier density on the emitter side of the IGBT and increasing the carrier lifetime.

13.5.2 Loss Estimation of Bipolar Device

The total loss of an IGBT or PiN diode is expressed as the sum of the on-state loss and switching loss. Therefore, the evaluation of IGBTs and PiN diodes is important for both the on-state losses and switching losses. In this section, the on-state and switching losses of IGBT and PiN diodes with different BVs are investigated for different carrier lifetimes of the drift layer.

As an application, a three-phase DC–AC PWM inverter is taken as an example and the total losses of IGBTs and PiNs with different BVs are compared. Figure 13.19 shows the relationship between the phase-to-neutral voltage and the phase-to-phase

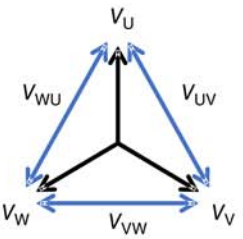

Figure 13.19 Vector diagram of 3-phase AC.

V_U, V_V, V_W : Phase-to-neutral RMS voltage
V_{UV}, V_{VW}, V_{WU} : Phase-to-phase RMS voltage

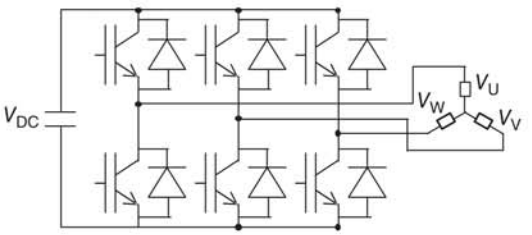

Figure 13.20 Circuit diagram of 3-phase DC-AC PWM inverter.

voltage, which can be given by

$$V_{UV} = V_{VW} = V_{WU} = \sqrt{3}V_U = \sqrt{3}V_V = \sqrt{3}V_W \tag{13.66}$$

Figure 13.20 shows the circuit diagram of the three-phase DC–AC PWM inverter. The DC and AC voltages can be expressed as

$$M \times \frac{V_{DC}}{2} = \sqrt{2}V_U = \sqrt{2}V_V = \sqrt{2}V_W \tag{13.67}$$

where M is the modulation ratio. In the case of connecting to a nominal voltage of 6.6 kV, each voltage of the 3-phase DC–AC PWM inverter is as shown in Table 13.1. For a 100 kV A class 6.6 kV 3-phase DC–AC PWM inverter, the RMS value of the phase current can be expressed as

$$I_{RMS} = \frac{100\,\text{kV A}}{\sqrt{3} \times 6.6\,\text{kV}} = 8.75\,\text{A} \tag{13.68}$$

Then, the maximum peak value of the phase current can be expressed as

$$I_p = \sqrt{2} \times 8.75\,\text{A} = 12.4\,\text{A} \tag{13.69}$$

In the following calculations, the DC supply voltage is assumed to be 13.5 kV and the peak value of the phase current is 12.4 A.

Table 13.1 AC and DC Voltages of the 3-phase DC–AC PWM inverter in the case of connecting to a nominal voltage of 6.6 kV.

AC phase-to-phase (line-to-line)		AC phase-to-neutral		DC voltage
Nominal voltage (RMS voltage)	**Peak voltage**	**RMS voltage**	**Peak Voltage**	***M* = 0.8**
6.6 kV	9.33 kV	3.81 kV	5.39 kV	13.5 kV

The loss of IGBT and PiN diodes in PWM inverters can be expressed as [23]

$$P_{\text{onIGBT}} = \frac{1}{2\pi}\int_0^{\pi} I_{\text{p}} \sin x \times V_{\text{on}} \sin x \times \frac{1 + D\sin(x+\theta)}{2} \mathrm{d}x$$
$$= I_{\text{p}} V_{\text{on}} \left(\frac{1}{8} + \frac{D}{3\pi}\cos\theta\right) \tag{13.70}$$

$$P_{\text{swIGST}} = \frac{1}{2\pi}\int_0^{\pi} \frac{E\text{sw}\ \sin\ x}{T_{\text{c}}}$$
$$= \frac{f_{\text{c}} E_{\text{sw}}}{\pi} \tag{13.71}$$

$$P_{\text{onPiN}} = \frac{1}{2\pi}\int_{\pi}^{2\pi} (-I_{\text{p}} \sin x) \times (-V_{\text{F}} \sin x) \times \frac{1 + D\sin(x+\theta)}{2} \mathrm{d}x$$
$$= I_{\text{p}} V_{\text{F}} \left(\frac{1}{8} - \frac{D}{3\pi}\cos\theta\right) \tag{13.72}$$

$$P_{\text{swPiN}} = \frac{1}{2\pi}\int_0^{\pi} \frac{E_{\text{rr}}}{T_{\text{c}}} \mathrm{d}x$$

$$= \frac{f_{\text{c}} E_{\text{rr}}}{2} = \frac{f_{\text{c}} I_{\text{RM}} V_{\text{DC}} t_{\text{rr}}}{8} = \frac{f_{\text{c}} V_{\text{DC}} Q_{\text{rr}}}{4} \tag{13.73}$$

Here, the on-state characteristics of the IGBT and PiN diodes are assumed to be linear, the switching loss of IGBT is assumed to be proportional to the current, and the reverse recovery loss of the PiN diodes is assumed to be constant regardless of the current. In this loss calculation, the switching losses of IGBT and PiN diodes are calculated only as turn-off losses and reverse recovery losses, respectively, because the turn-on losses are more dependent on the characteristics of the PiN diode than on the characteristics of the IGBT and therefore cannot be evaluated for losses derived from the IGBT. It is assumed that the turn-off loss of the IGBT is proportional to the DC voltage and turn-off current, and the reverse recovery loss of the PiN diode is proportional to the DC voltage.

Figures 13.21 and 13.22 show the trade-off between the on-voltage and switching loss of PiN diodes and IGBTs, respectively. For the estimation of losses, the carrier frequency f_{c} was set at 1 kHz, the modulation factor D was set at 0.8, and the power factor $\cos\theta$ was set at 0.95. The red, green, and blue dotted lines in the figure represent the combination of on-voltage and switching losses that takes the minimum total loss for each voltage class. The black dotted line represents the combination of on-voltage and switching loss where the on-voltage is equal to the switching loss. For both IGBTs and PiN diodes, as the carrier life increases, the on-state voltage decreases, but the switching loss increases. The calculated total losses are minimized when the carrier life is longer than 10 μs for IGBT and 2 μs for PiN.

Table 13.2 shows the results of the calculation of the total loss per arm for a 100 kVA class 6.6 kV 3-phase DC–AC PWM inverter. The losses with 24 kV devices were reduced by about 36% compared with those with 6.5 kV devices. Because the switching losses of 24 kV devices are greater than those of 6.5 kV devices, the difference between the 1 series of 24 kV devices and the 4 series of 6.5 kV devices

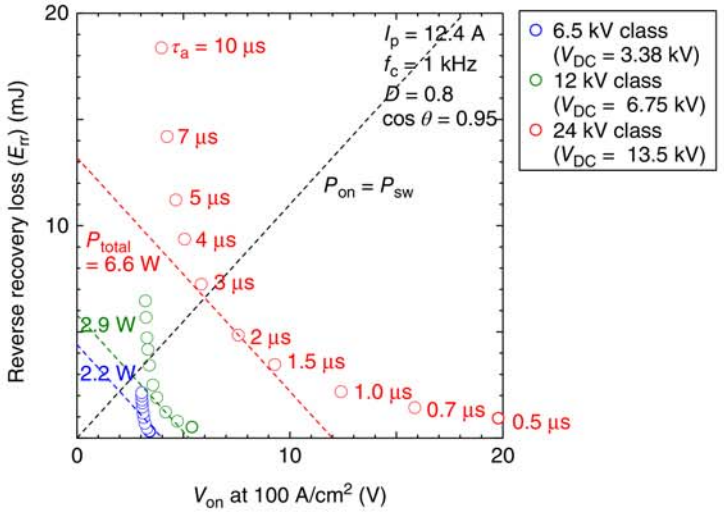

Figure 13.21 Trade-off between on-state voltage and switching loss in PiN diodes.

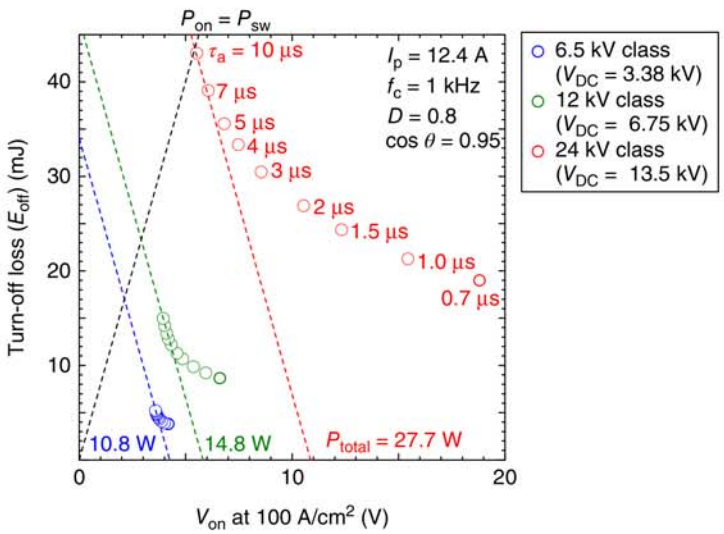

Figure 13.22 Trade-off between on-state voltage and switching loss in IGBTs.

may be reduced and reversed when the carrier frequency is increased. However, an increase in the number of series is still a problem due to the installation of snubber capacitors and the complexity of the control circuit, and a smaller number of series is still better, so 24 kV-class devices are more advantageous. Moreover, if the gate resistance is made small (51 Ω), the switching loss is reduced by an order of magnitude. In this case, it is expected that the losses of 24 kV-class devices will be small, even at high carrier frequencies.

Table 13.2 Results of the calculation of the total loss per arm for a 100 kVA class 6.6 kV 3-phase DC–AC PWM inverter.

BV class		6.5 kV	12 kV	24 kV
Series number		4	2	1
IGBT 10 μs	On-state	36.8	20.2	14.1
	Switching loss	6.5	9.4	13.6
	Total loss	43.3	29.7	27.7
PND 2 μs	On-state loss	6.9	3.9	4.2
	Switching loss	2.3	2.5	2.4
	Total loss	9.2	6.4	6.6
Sum		52.5	36.1	34.3
Ratio to 6.5 kV		1.00	0.69	0.65

13.6 Current Status of SiC Bipolar Device

In this chapter, we report on the current status of ultra-high-voltage bipolar devices and on other challenges.

In Figure 13.23, the characteristics of PiN diodes and IGBTs reported so far are plotted with the BV on the horizontal axis and the characteristic on-resistance at 100 A/cm^2 on the vertical axis, showing a comparison between the limit curve of SiC and the series of Si-IGBTs. With respect to the BVs, the voltage range of 4.5–29.6 kV was reported for PiN diodes and 6.5–27 kV was reported for IGBTs [6–9, 15, 24, 25]. Regarding the specific on-resistance, PiN diodes have been made to have low on-resistance as described before, but IGBTs have not yet been made

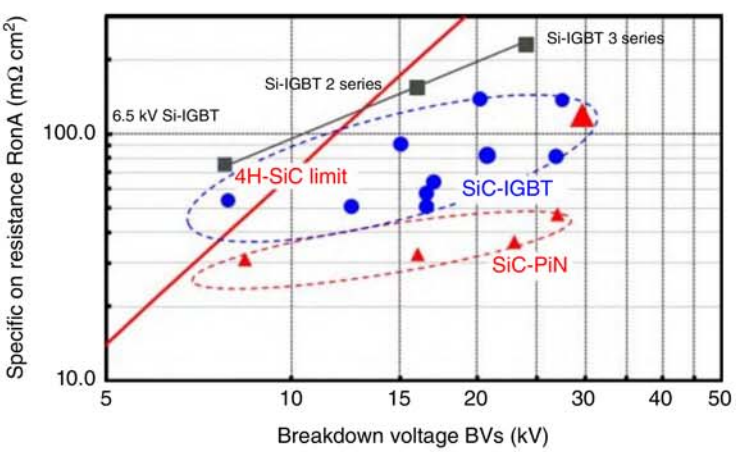

Figure 13.23 Reported Break down voltage vs. on-resistance at 100 A/cm^2 of IGBTs and PiN diodes.

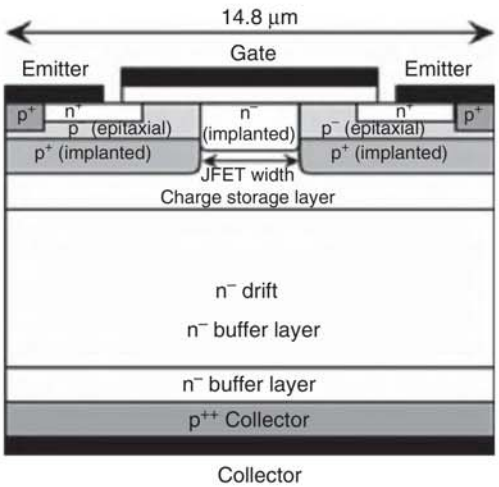

Figure 13.24 Cross-sectional view of the SiC-IGBT.

to have a sufficiently low on-resistance. In the following section, the 16 and 20 kV class SiC-IGBTs are introduced.

13.6.1 Device Performance of 16 kV Class SiC-IGBT

Figure 13.24 is a schematic cross-sectional view of a SiC-IGBT. Since the BV layer at 16 kV is as thin as 150 μm, a flip-type epitaxial wafer with a thick p^{++} epitaxial layer was used as a collector side substrate to pass through the device process. The flip-type wafer fabrication method is as follows. First, an n-type layer with a thickness > 170 μm and a field stop layer were grown on the Si surface n^{++} substrate. A p^+ current collector layer was formed. Subsequently, a p^{++} layer (2×10^{19} cm^{-3}) was grown to a achieve thickness of > 200 μm. Then, the substrate was turned over, the n^{++} substrate was removed, and the surface was polished with chemical mechanical polishing (CMP). After the edge treatment, a charge accumulation layer (CSL) was employed to enhance the charge accumulation effect [8] (Figure 13.25).

The device structure was optimized by TCAD simulation. In particular, the blocking voltage and the JFET width dependence of V_f were investigated to obtain the optimal structure for the ultra-high-voltage SiC-IGBT. In device fabrication, implantation and epitaxial (IE) MOSFET structure was employed [26]. On the CSL layer, p^+-based aluminum ions (Al^+) were selectively implanted to form the base of the p-well. A 0.5 μm thick p-epitaxial layer was then grown as the topmost p-layer. The JFET region was formed by selective implantation of nitrogen ions (N^+) into the p-layer. The fabricated device has a striped unit cell with a pitch of 14.8 μm. A two-zone (JTE) structure was used for the termination.

Figure 13.26 shows the image of the 16 kV SiC-IGBT (8 mm × 8 mm) and the blocking voltage [8].

The pulsed on-state I–V characteristics of the 16 kV SiC-IGBT are shown in Figure 13.27, where an on-state current of 20 A was obtained at a low on-state voltage (V_{on}) of 4.8 V and 60 A at V_{on} = 7.2 V. Further, $R_{onAdiff}$ was 14 Ω cm^2

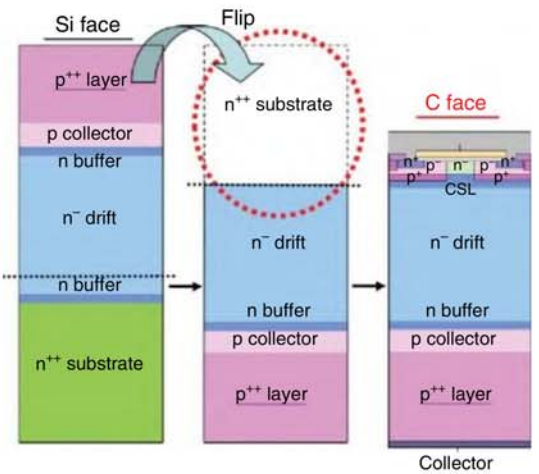

Figure 13.25 Trade-off between on-state voltage and switching loss in IGBTs.

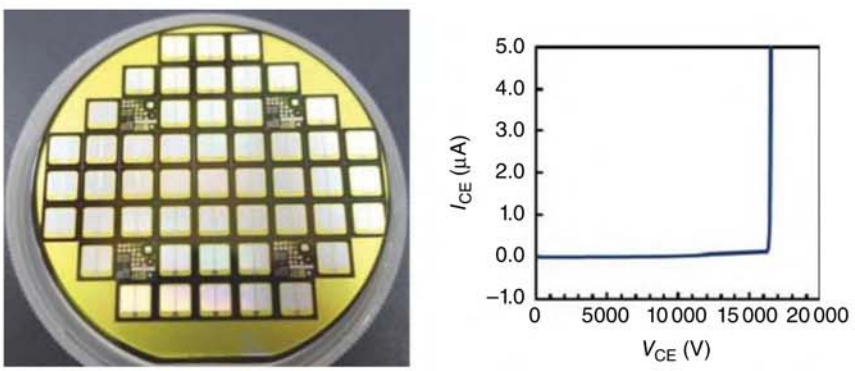

Figure 13.26 16 kV SiC-IGBT (8 mm × 8 mm) and reverse BV characteristics.

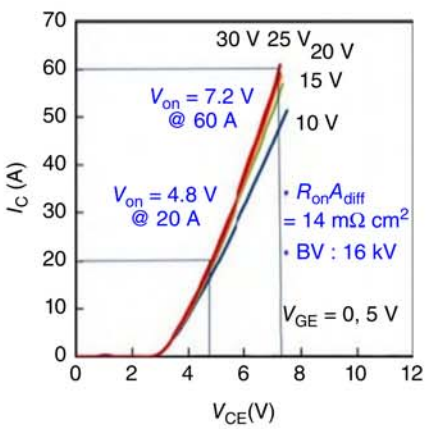

Figure 13.27 Pulsed on-state *I-V* characteristics of the 16 kV SiC-IGBT.

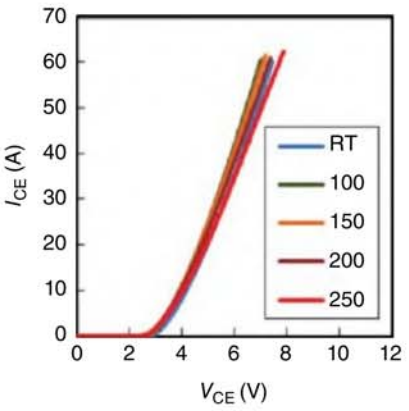

Figure 13.28 Temperature dependence of forward characteristics at $V_{GE} = 30\,V$.

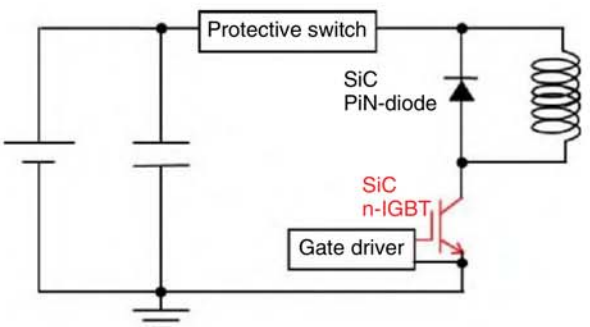

Figure 13.29 Circuit configurations for switching measurements.

at 100 A/cm^2 ($V_{GE} = +30\,V$). Figure 13.28 shows the forward characteristics of IE-IGBT from RT to 250 °C.

As for the dynamic characteristics, an ultra-high-voltage power module was assembled to evaluate the switching characteristics of the 16 kV SiC-IGBT. The power module consists of a tungsten base plate and a direct bonding copper (DBC) base using Si_3N_4, and a copper electrode, and the DBC base and the power device are molded with resin and housed in a module case. The module case is designed to maintain a sufficient distance between the electrodes to prevent creeping discharge.

The chopper circuit configuration used to evaluate the switching characteristics of the IE-IGBT is shown in Figure 13.29. A separate SiC PiN diode (5.3 mm × 5.3 mm) module was used as a freewheel diode in the circuit. A 300 Ω gate resistor was used for both turn-on and turn-off switching, and a VCE of up to kV was applied.

$V_{GEoff} = -10\,V$ and $V_{GEon} = +25\,V$ were applied as gate voltages, and the turn-off switching temperature was set from RT to 250 °C.

The turn-off switching waveforms of an 8 mm × 8 mm n-channel 16 kV SiC-IGBT are shown in Figure 13.30 in the temperature range from RT to 250 °C. A smooth turn-off waveform was obtained with VCE = 6.5 kV and ICE = 60 A. The turn-off energy was 36 mJ/pulse at RT, but increased to 199 mJ/pulse at 250 °C. The increase

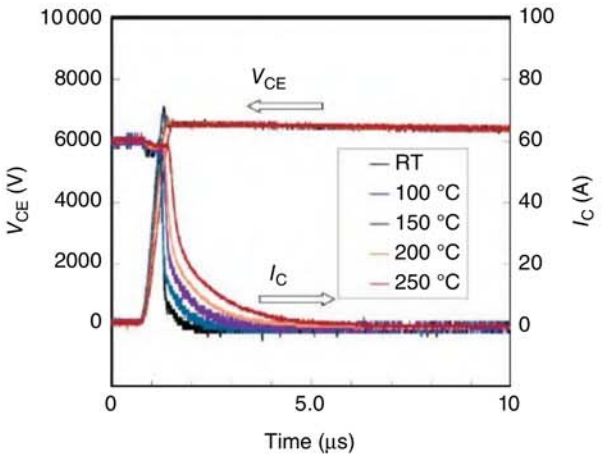

Figure 13.30 Turn-off switching waveforms of an 8 mm × 8 mm n-channel 16 kV SiC-IGBT.

in the tail current is mainly due to the prolongation of the carrier lifetime and the injection of holes increased with increasing temperature, which resulting in a higher carrier density in the voltage withstanding layer.

To demonstrate high power switching, we fabricated 1 in 1 module including four 16 kV SiC-IGBT (5.3 mm × 5.3 mm) chips connected in parallel and one PiN diode. The turn-off waveforms having a voltage of 10 kV are shown in these figures with current and temperature dependence. As shown in Figure 13.30. We successfully obtained a 10 kV, 100 A (1 MW) switching waveform. The slight change in the (dV/dt) of the collector voltage (V_{CE}) transients at about 1.2–1.5 ms, corresponds to the punch-through of the voltage-blocking layer (Figure 13.31).

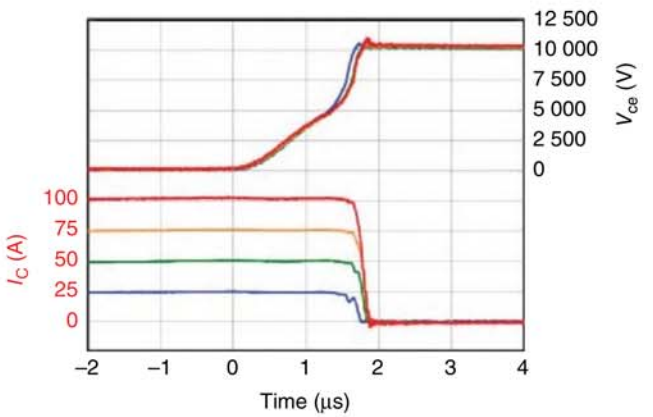

Figure 13.31 High power switching waveform of 4 16 kV SiC-IGBTs and PiN diode.

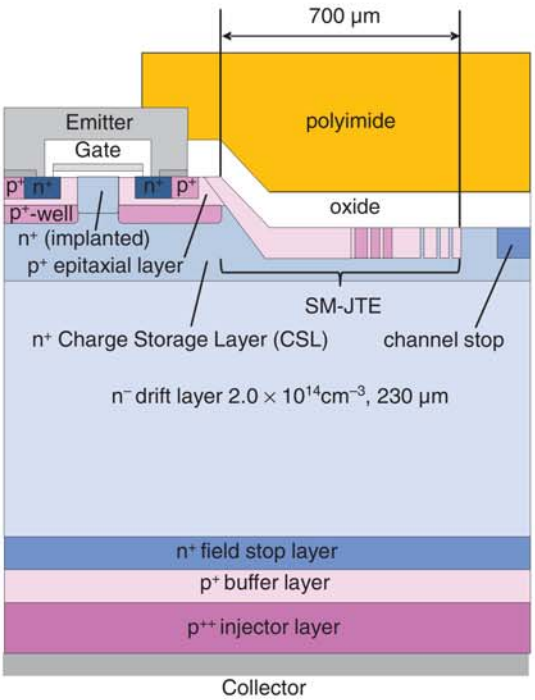

Figure 13.32 Cross-sectional image of over 20 kV class SiC-IGBT.

13.6.2 Device Characteristics of higher-than-20 kV Class SiC-IGBT

In this section, the prototype of a higher-than-20 kV class SiC-IGBT is introduced. A withstand voltage layer of 20 kV requires a thickness of 200 μm or higher. However, unlike the 16 kV class, the device process can be performed with a freestanding epitaxial layer, if the thickness is more than 200 μm. Figure 13.32 shows a cross-sectional view of the 20 kV class SiC-IGBT. The actual method of fabricating a freestanding epitaxial substrate was as follows.

First, a BPD/TED conversion layer was formed, and then an n-layer with a nitrogen concentration of 2e 14 cm^{-3} and a thickness of 270 μm was formed on the silicon surface (Si surface), which is conductive to obtain low nitrogen concentration. After adjusting the withstanding layer to about 250 μm, to achieve sufficient conductivity modulation for the purpose of low conduction loss as described above, carbon ion implantation and post annealing were carried out at 1650 °C [27]. The lifetime was enhanced by up to 9.6 μs, as measured by μ-PCD. After removing the n^{++} substrate by grinding, CMP was performed and an n^{+} field stop layer was deposited on the carbon face. In addition, a p^{++} layer was formed as a collector layer. Subsequently, the Si surface was further ground and subject to CMP, and the thickness of the voltage withstand layer was 230 μm, and 1.5e 16 cm^{-3} was formed as the CSL layer. Then, the active region of device was created with an IE structure.

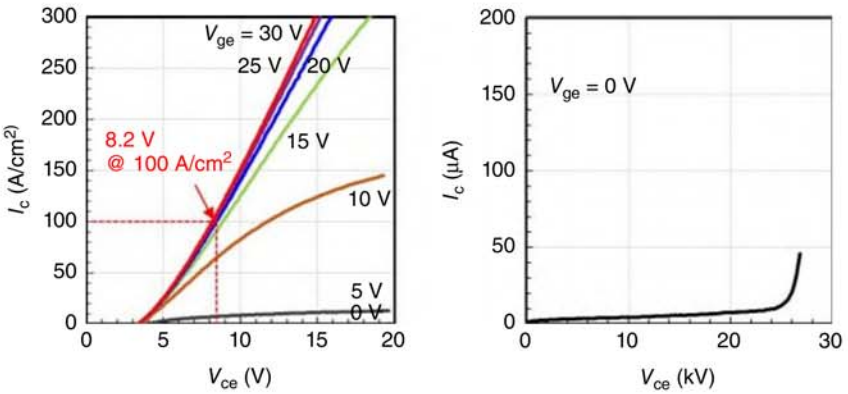

Figure 13.33 Forward and reverse characteristics of higher-than-20 kV class SiC-IGBT.

A space-modulated JTE was used as the peripheral withstand voltage structure [25]. The edge length was set to 700 μm.

Figure 13.33 shows the forward and reverse BV characteristics of the 20 kV SiC-IGBT obtained. A withstand voltage of 26.8 kV could be obtained, an on-voltage of V_{on} = 8.6 V at 100 A/cm^2, and a differential on-resistance of 36.9 mΩ cm^2 were obtained at RT [28].

13.6.3 Other Bipolar Devices Issues

The 16 and 20 kV SiC-IGBTs were introduced as ultra-high-voltage bipolar devices. In both cases, the withstanding voltage was secured and a specific (yet low) low conduction loss was obtained. However, the turn-off switching loss has high-temperature dependence and needs further improvement. To achieve low-conduction and low-switching losses at turn-off, it is necessary to make the conductivity modulation electron-dominant. To achieve this, as in the case of Si, it is necessary to apply an injection-enhancement effect structure with a long carrier lifetime, and to limit the hole injection from the collector side.

To fully exploit the performance of ultra-high-voltage IGBTs, it is necessary to develop not only the device design but also the peripheral technology, especially the heat extraction technology. Figure 13.34 compares the IV characteristics of an ideal 16 and 20 kV SiC-IGBT with SiC-MOSFETs and Si-IGBTs of the 16 kV equivalent series. The dotted lines show the cooling capacity curves. Normally, 2–300 W/cm^2 is the limit for air cooling, and 800 W/cm^2 and 800 W/cm^2 for double-sided cooled power cards. If there is a cooling method that exceeds 1000 W/cm^2, the potential of SiC-IGBTs can be maximized.

We hope that these ultra-high-voltage SiC bipolar devices will be used in the high-voltage power electronics for next-generation electricity network, and will contribute to the realization of a low-carbon and safer society.

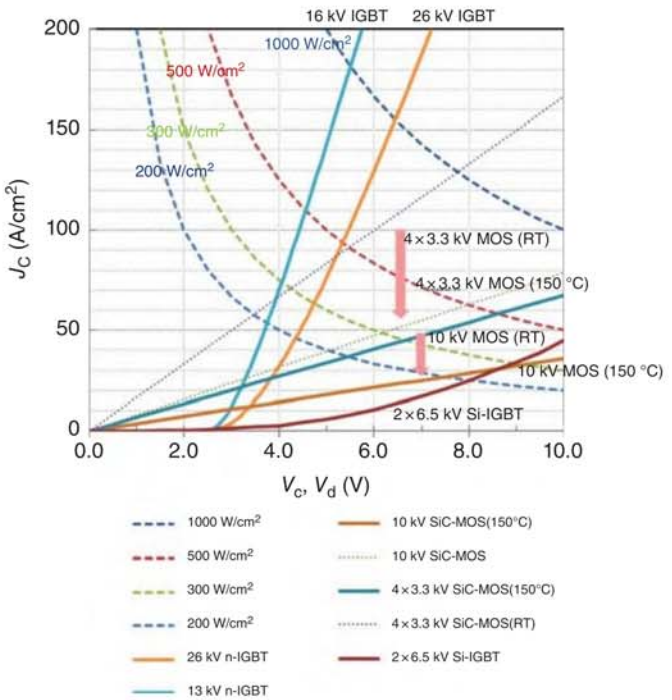

Figure 13.34 *I–V* curve comparison of ideal SiC-IGBT, series of equivalent BV of 16 kV SiC-MOSFET and Si-IGBTs with cooling capability curves.

References

1 Kimoto, T. and Cooper, J.A. (2014). *Fundamentals of Silicon Carbide Technology*. Singapore: Wiley.

2 Tawara, T., Miyazawa, T., Ryo, M., Miyazato M. et al. (2016). Short minority carrier lifetimes in highly nitrogen-doped 4H-SiC epilayers for suppression of the stacking fault formation in PiN diodes. *J. Appl. Phys.* 120: 115101.

3 Kawahara, K. et al. (2017). 6.5 kV schottky-barrier-diode-embedded SiC-MOSFET for compact full-unipolar module. *Proc. Int. Symp. Power Semiconductor Devices & ICs*: 41.

4 Kobayashi, Y. et al. (2017). Body PiN diode inactivation with low on-resistance achieved by a 1.2 kV-class 4H-SiC SWITCH-MOS. *IEEE International Electron Devices Meeting (IEDM)*: 9–1.

5 Wang, X. and Cooper, J.A. (2010). High-voltage n-channel IGBTs on free-standing 4H-SiC epi layers. *IEEE Trans. Electron Devices* 57 (2): 511–515.

6 Ryu, S. et al. (2012). Development of 15 kV 4H-SiC IGBTs. *Mater. Sci. Forum.* 717–720: 1135.

7 Yonezawa, Y. et al. (2013). Low V_f and highly reliable 16 kV ultrahigh voltage SiC flip-type n-channel implantation and epitaxial IGBT. *IEEE International Electron Devices Meeting (IEDM)*: 6.6.1–6.6.4.

8 Yonezawa, Y. et al. (2015). Device performance and switching characteristics of 16 kV ultrahigh-voltage SiC flip-type n-channel IE-IGBTs. *Mater. Sci. Forum* 821–823: 842–846.

9 van Brunt, E. et al. (2015). 27 kV, 20 A 4H-SiC IGBTs. *Mater. Sci. Forum* 821: 847–850.

10 Konstantinov, A.O., Wahab Q., Nordell N., and Lindefelt (1998). Study of Avalanche Breakdown and Impact Ionization in 4H Silicon Carbide. *J. Electron Mater.* 27: 335.

11 Sugawara, Y., Takayama, D., Asano, K. et al. (2001). 12–19 kV 4H-SiC PiN diodes with low power loss. *Proc. 13th Int. Symp. Power Semiconductor Devices & ICs*: 27–30.

12 Das, M.K., Sumakeris, J.J., Krishnaswami, S. et al. (2003). Latest advances in high voltage, drift free, 4H-SiC PiN diodes. *International Semiconductor Device Research Symposium*: 364–365.

13 Hiyoshi, T., Hori, T., Suda, J., and Kimot, T. (2008). Simulation and experimental study on the junction termination structure for high-voltage 4H-SiC PiN diodes. *IEEE Trans. Electron Devices* 55 (8): 1841–1846.

14 Snook, M., McNutt, T., Kirby, C. et al. (2012). Single photolithography/implantation 120-zone junction termination extension for high-voltage SiC devices. *Mater. Sci. Forum* 717–720: 977–980.

15 Niwa, H., Suda, J., and Kimoto, T. (2012). 21.7 kV 4H-SiC PiN diode with a space-modulated junction termination extension. *App. Phys. Express* 5: 064001.

16 Matsunami, H. (1999). *Handotai-kogaku*, 124–127. Tokyo: Shokodo [in Japanese].

17 Shockley, W. and Read, W.T. Jr., (1952). Statistics of the Recombinations of Holes and Electrons. *Phys. Rev.* 87: 835.

18 Baliga, B.J. (2010). *Advanced Power Rectifier Concepts*, Springer, p. 152.

19 Ayalew, T. (2004). SiC semiconductor devices, technology, modeling, and simulation. PhDthesis. Technishen Universiaet Wien, Austria.

20 Baliga, B.J. (1987). *Modern Power Devices*, vol. 411. New York: Wiley.

21 Kassakian, J.G., Schlecht, M.F., and Verghese, G.C. (1991). *Principles of power electronics*. Addison-Wesley, p. 486.

22 Schlangenotto, H. and Gerlach, W. (1972). On the post-injection voltage decay of p-s-n rectifiers at high injection levels. *Solid-State Electron.* 15: 393.

23 Yamagata, T. (2004). Transistor Gijutsu Special 85, 87–91. Tokyo: CQ Publishing Co., Ltd. [in Japanese].

24 Kaji, N. et al. (2015). Ultrahigh-voltage SiC PiN diodes with improved forward characteristics. *IEEE Trans. Electron Devices.* 62 (2): 374–381.

25 Nakayama, K. et al. (2018). 27.5 kV 4H-SiC PiN diode with space-modulated JTE and carrier injection control. *Proceedings of ISPSD*: 395–398.

26 Harada, S. et al. (2006). *Technical Digest of IEDM*, p. 903.

27 Storasta, L. and Tsuchida, H. (2007). Reduction of traps and improvement of carrier lifetime in 4 H-Si C epilayers by ion implantation. *Applied Physics Letters* 90 (6): 062116.

28 Koyama, A. et al. (2020). 20 kV-class ultra-high voltage 4H-SiC n-IE-IGBTs. *Materials Science Forum*, vol. 1004, pp. 899–904. Trans Tech Publications Ltd, 2020.

14

SiC Reliability Aspects

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14.1 Ruggedness and Overload Events

14.1.1 Short-circuit Ruggedness of SiC MOSFETs

Today, only a small number of manufacturers state a short-circuit capability in the datasheet of their respective SiC metal–oxide–semiconductor field-effect transistors (MOSFETs). One reason is the small intrinsic short-circuit capability compared to state-of-the-art insulated gate bipolar transistors (IGBTs). The root cause can be found in the unfavorable temperature distribution during and after a short-circuit event.

In the case of an SiC MOSFET, almost the entire short-circuit energy is generated and dissipated in the first some micrometers below the frontside chip surface. For a 1200 V SiC MOSFET, the "active" base width is just in the range of 10 µm.

In this region, most of the short-circuit power loss is generated. This leads to a high temperature at the frontside chip region which will stress especially the power metal, gate oxides, and other frontside topologies, see Figure 14.1 and [1, 2], respectively. Due to the strong temperature gradient in the SiC substrate, the backside of the chip remains almost at starting temperature. The IGBT distributes the temperature more homogenously across the total chip thickness and has, defined by the electric field distribution, the temperature maximum in the range of two-thirds from the frontside in the total chip thickness, see Figure 14.1. Therefore, to improve the short-circuit ruggedness of an SiC MOSFET, especially the frontside with its interconnections must be thermally optimized.

However, chip-internal characteristics can be adjusted as well. There are typical $R_{DS,ON}$ vs. short-circuit time trade-offs also known from the common silicon MOSFET structure. The most popular ones are the channel-width trade-off, the $V_{GS,TH}$ trade-off, and the gate-bias trade-off. Additionally, it is also possible to adjust the *n*-source resistance, as mentioned in [3]. In general, any short-circuit time can be achieved at the expense of $R_{DS,ON}$.

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

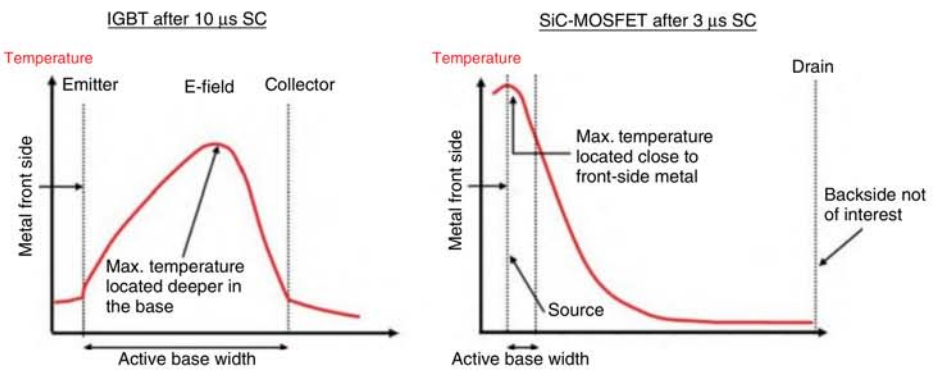


Figure 14.1 Schematic temperature distribution after short-circuit event of an IGBT (left) and an SiC MOSFET (right).

If the standard equation for the saturation regime of an MOSFET is used [4]

$$I_{D,\mathrm{sat}} = \frac{k}{2}(V_{\mathrm{GS}} - V_{\mathrm{GS,TH}})^2 \tag{14.1}$$

with channel conductivity (W, channel width, C_{OX}, oxide capacitance, μ_{n}, electron-channel mobility)

$$k = \frac{W \cdot C_{\mathrm{OX}} \cdot \mu_{\mathrm{n}}}{L}, \tag{14.2}$$

then the standard trade-offs for increasing the short-circuit withstand time which is proportional to the saturation current can directly be derived. On the other side, the trade-offs have also a consequence on the channel resistance R_{CH} with

$$R_{\mathrm{CH}} = \frac{1}{\frac{W}{L} \cdot C_{\mathrm{OX}} \cdot \mu_{\mathrm{n}} \cdot (V_{\mathrm{GS}} - V_{\mathrm{GS,TH}})}. \tag{14.3}$$

If the channel width is reduced, the saturation current is directly lowered. For increase of threshold voltage, $I_{\mathrm{D,sat}}$ is lowered. A gate-bias reduction also leads to a reduced saturation current. The gate-bias control method is already applied for SiC MOSFET short-circuit protection, where V_{GS} is instantly lowered, if a short-circuit event is detected [5, 6]. Some of the abovementioned trade-offs were simulated using TCAD in Figure 14.2, where $R_{\mathrm{DS,ON}}$ vs. the short-circuit withstand time is plotted for a high-voltage SiC MOSFET, similar to [3]. It has to be mentioned that a low $R_{\mathrm{DS,ON}}$ at the cost of short-circuit time is only possible to some amount since, e.g. sufficient field-shielding structures or minimal gate-oxide thicknesses for achieving high gate-oxide reliability are limiting. Furthermore, the trade-offs are strongly dependent on the cell design and voltage class. Figure 14.2 shows a schematic dependency.

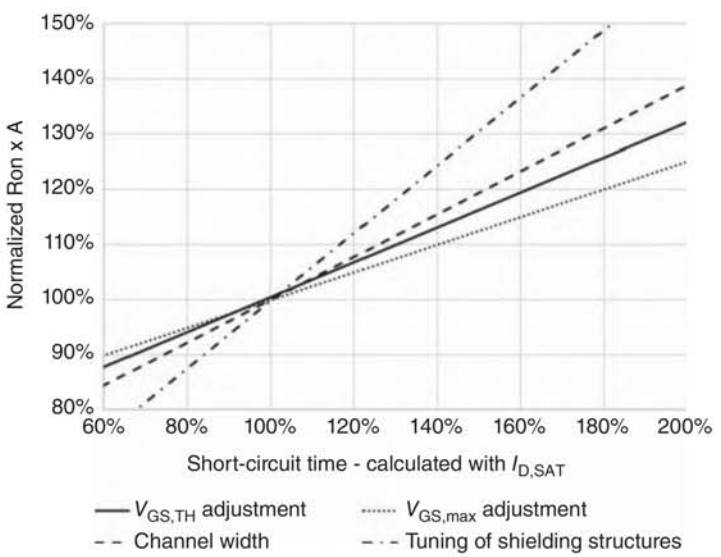


Figure 14.2 Simulated $R_{\mathrm{DS,ON}}$ vs. short-circuit time trade-offs, base for simulation is a high-voltage SiC MOSFET.

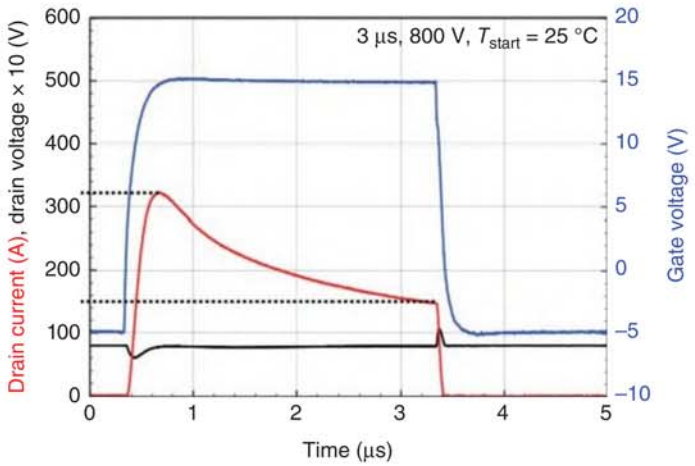


Figure 14.3 Typical short-circuit type 1 waveform of SiC trench MOSFET.

In comparison to the IGBT [7], the short-circuit type 1 waveform looks significantly different, see Figure 14.3. After a high short-circuit current peak at the beginning of the event the saturation current drops strongly to the half of the peak value after 3 µs. The reduction can be explained by a decrease in the channel mobility with temperature, see Eq. (14.1), and even more by the known junction gate field-effect transistor (JFET)-driven current-limiting effect, see [8]. The JFET is constructed by the shielding p-regions in the different SiC MOSFET structures and is used to protect the gate oxides from high electric fields. This JFET region can also be used to adjust the short-circuit ruggedness, see Figure 14.2. To achieve a low $R_{DS,ON}$ with high channel width, the relation "saturation current vs. application-near nominal current" is typically higher for the SiC MOSFET than for an IGBT in the same voltage class. For example, SiC MOSFETs show $I_{D,sat}/I_{nom}$ relations in the range of 10–15. For 10 µs short-circuit rugged IGBTs, the relation is more 3–5, which helps to keep the overall short-circuit energy dissipation low.

Additionally, the saturation current is strongly voltage dependent. The reason can be found in the typically pronounced drain-induced-barrier lowering (DIBL) effect which is directly connected with the use of short *n*-channels in SiC MOSFETs, see Figures 14.4 and 14.5 as well as [9]. If the drain-source voltage is increased, the electric field/space-charge region approaches closer to the channel region and shortens the channel effectively. Thus, $V_{GS,TH}$ is lowered and $I_{D,sat}$ rises with the drain-source voltage, see Eq. (14.1). This is important when the short-circuit detection levels at the gate drivers are implemented, especially when a current detection is used. The DIBL can be expressed by the following relation:

$$\text{DIBL} = \frac{\Delta V_{GS,TH}}{\Delta V_{DS}} \left[\frac{\text{mV}}{\text{V}}\right]. \tag{14.4}$$

For the 1200 V SiC MOSFET shown in Figure 14.4, the DIBL is, e.g. 1.63 mV/V demonstrating that from $V_{DS} = V_{GS}$ (pinch-off point) condition to $V_{DS} = 800$ V the threshold voltage is lowered by 1.3 V. The DIBL may vary between different MOS

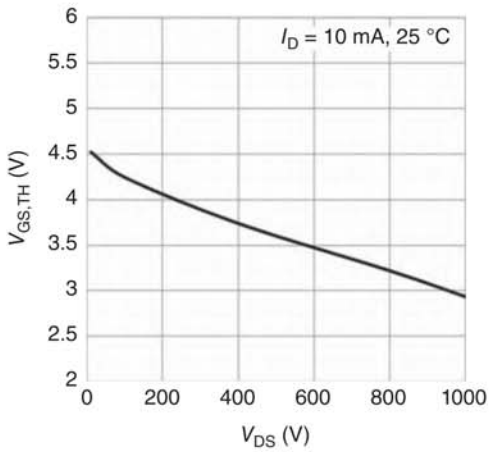


Figure 14.4 DIBL effect, $V_{GS,TH}$ is lowered with higher drain-source voltage.

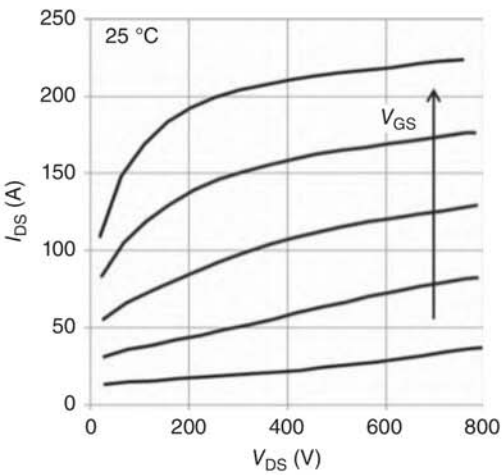


Figure 14.5 Rising saturation currents $I_{D,sat}$ with increased drain-source voltage.

cell structures and p-shielding regions [9]. In general, this effect is also known for silicon low-voltage MOSFETs [10].

For SiC MOSFETs, different short-circuit destruction modes are known [11]. One mode is the gate-source fail after turning off an event which has lasted too long, see Figure 14.6 left and [12]. Reasons can be found in the high thermomechanical stress from the power metal on the interlayer dielectrics which can lead to cracks and finally to a hard gate-source short, compare [12, 13] and Figure 14.7. With hard gate short, the device is in off-state and may prevent a hard DC link short in the power circuit. Precondition, however, is that the damage is concentrated to the gate structure. Other gate failures can be explained by a damage of the thin gate oxide. First evaluations connect high gate-source leakage currents and gate oxide pre-damages with a Schottky emission from the gate poly into the SiC bulk [14]. Fowler–Nordheim tunneling as a main driver for high leakage currents was excluded since the electric fields are assumed to be too low; furthermore, this tunneling effect is not much temperature dependent.

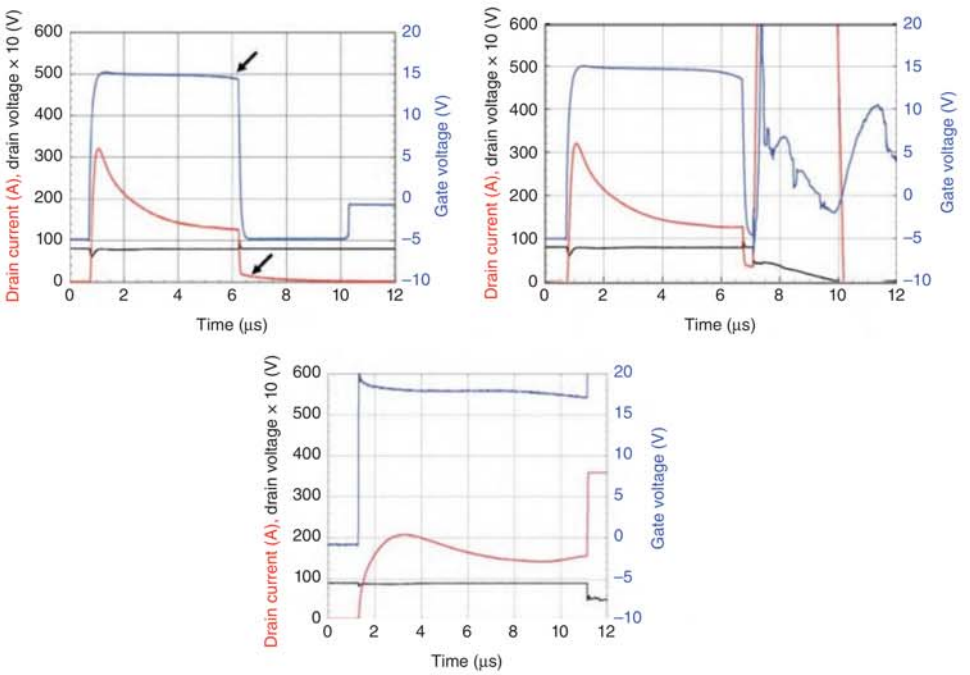


Figure 14.6 SiC MOSFET: different kinds of short-circuit destruction; Left: gate-source fail after withstanding the short circuit, Right: hard destruction at turn-off, Center: thermal runaway during the short-circuit event.

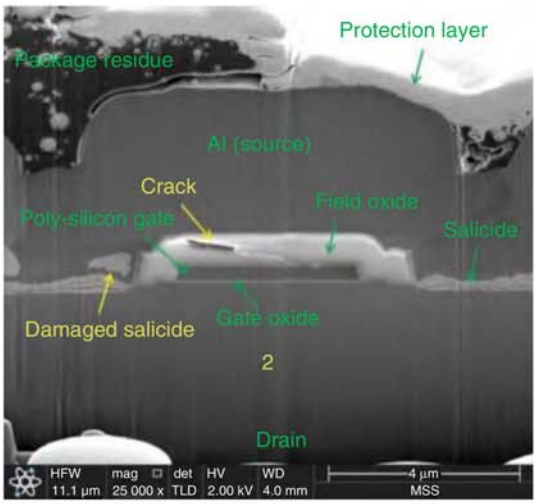


Figure 14.7 Possible failure picture with gate-source short after a long-lasting short-circuit pulse. The interlayer dielectric between the gate electrode and the power metal was cracked. Source: Picture from Reigosa et al. [13].

In general, dips in the gate voltage during the short-circuit event and upcoming "tail" currents are signs of heavy stress (arrows in Figure 14.6 left), which may also lead to early damage and go hand in hand with parameter drifts of, e.g. $V_{GS,TH}$. It is important to stay away from these early warnings. The drain tail current is connected with the parasitic npn-transistor part at the above mentioned high temperatures in the range of 1000 °C. Electrons are injected directly from the n^+-source into the device which cause a high drain-source leakage current, although the gate voltage is set to zero or even a negative value. Additionally, failures during turn-off or during the pulse may appear under different conditions (stray inductance, DC-link voltage, short-circuit time, etc.), see [11] und Figure 14.6 center and right.

Since the SiC MOSFET has the ability to turn on very fast, the package may also improve the short-circuit withstand capability as shown in Figure 14.8. If the device is turned-on without common-source inductance (with sense source) like in a TO-247 4-pin housing, the peak of the short-circuit current can be much higher compared to a package with a higher common-source inductance like the 3-pin version of the TO-247. The reason can be found in the missing self-heating effect at the beginning of the event for a 4-pin housing. For the 3-pin device, di/dt is lowered by the feedback of a source inductance on the gate loop. Therefore, the device has more time to heat up which lowers the peak current due to the reduction of the electron mobility. At the end of the short-circuit event, both housings show similar saturation current levels. However, since the 3-pin device dissipates less energy during the whole event, the overall robustness in this package is a little higher. A similar effect can be achieved when using a higher gate-turn-on resistor; however, this will increase also the switching losses in general. A higher common-source inductance is the better choice.

Another effect which is very special for SiC MOSFETs is the $V_{GS,TH}$ hysteresis [15, 16]. For lower off-gate-source voltages, the $V_{GS,TH}$ is lower when turning on into a short circuit. This results in a significantly increased peak current from 280 A

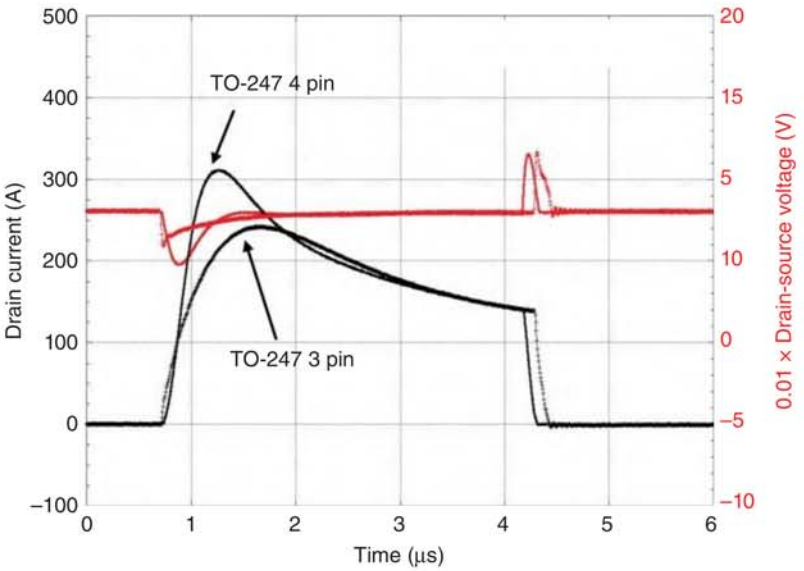


Figure 14.8 Short-circuit waveforms in different packages, $V_{DC} = 800\,V$, $V_{GS} = -5/15\,V$.

at 0 V $V_{GS,off}$ to 325 A at −10 V $V_{GS,off}$, see Figure 14.9. If SiC MOSFETs are used in parallel connections, this effect has to be considered in particular.

To overcome the hard trade-off between $R_{DS,ON}$ and short-circuit withstand capability, intelligent gate driver schemes are proposed from different manufacturers and institutes, see [5, 6, 17].

To verify a high short-circuit ruggedness, it may also be useful to check some repetitive short-circuit events. Parameters like $V_{GS,TH}$ and leakage currents have to be stable after e.g. 10–20 short-circuit events. Just to rely on a low short-circuit time alone may be critical, since the top-side structure is exposed to a very high temperature swing with possible crack initiation, see Figure 14.7.

14.1.2 Surge-current Ruggedness

During converter operation, the power semiconductor devices can be imposed to high over currents with a duration in the millisecond range, defined as surge currents. To withstand these currents, devices like diodes and thyristors are rated for the case of surge current. Typically, a maximum allowed (non-repetitive) peak current during a 10 ms sine half-wave is given in the datasheet (I_{FSM}). This standard pulse is related to grid errors with a 50 Hz grid frequency. In addition to this specific current, an i^2t-value is often given in the datasheet. In the past, different publications already explained the behavior of silicon bipolar devices in general during high overcurrents, see, e.g. [18]. A schematic waveform of a silicon pin-diode is given in Figure 14.10 left. The corresponding I–V curve, which can be used for a more detailed analysis, is shown in Figure 14.10 right. In principle, two cases can occur in the I–V diagram: positive or negative differential resistance behavior.

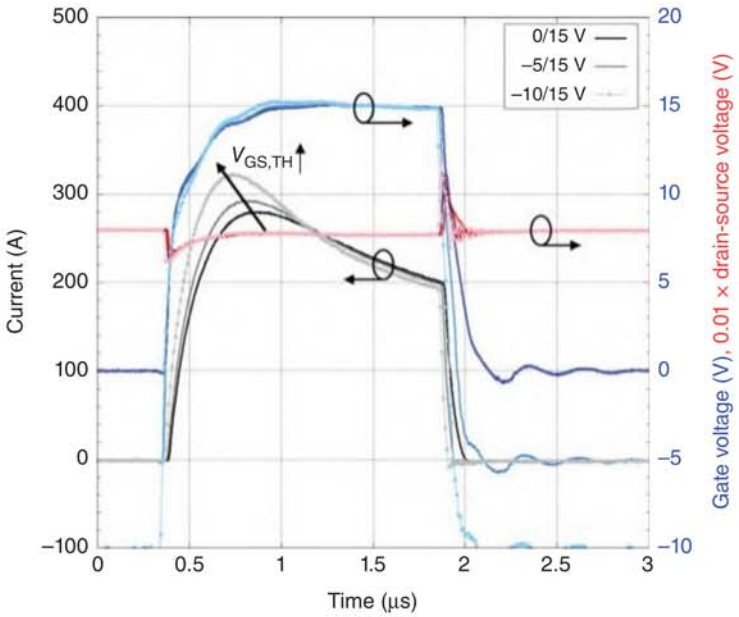


Figure 14.9 Impact of $V_{GS,TH}$ hysteresis on short-circuit.

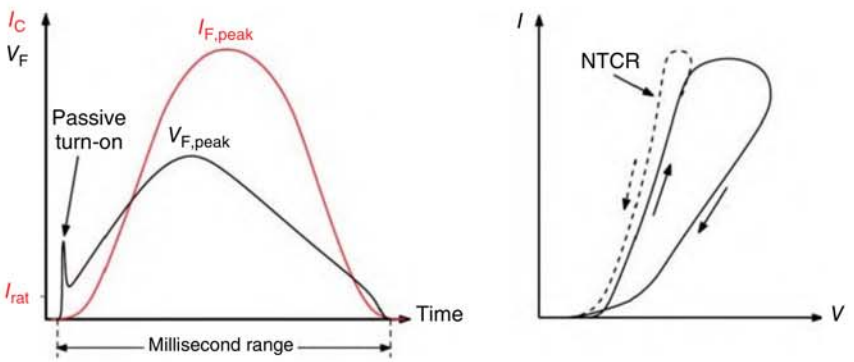


Figure 14.10 Schematic surge-current event (left) and corresponding *I*–*V* curve (right). NTCR means negative temperature coefficient resistance.

This depends also on the specific temperature characteristic of the device. For the negative case, inhomogeneous current distribution may occur. Regarding the parallel connection of single chips, the second case can be more critical.

For SiC MPS (Merged–PN–Schottky) diodes, a crossing point between the falling and rising branch occurs at higher currents due to the onset of hole injection of the p-regions, see Figure 14.11 and [19]. The highly pronounced incomplete ionization of SiC p-doped regions (e.g. Al doping) at room temperature also leads to a better p-emitter efficiency at higher temperatures which amplifies the effect of a negative differential resistance.

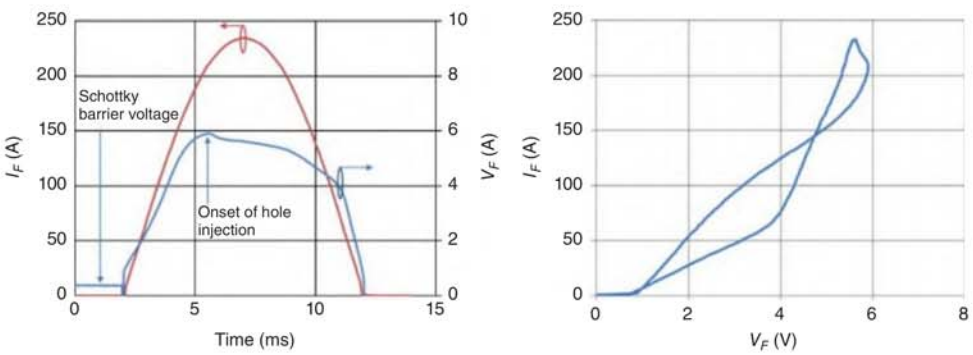


Figure 14.11 Surge-current event at 1200 V/20 A rated SiC MPS diode (left) and corresponding *I*–*V* curve (right).

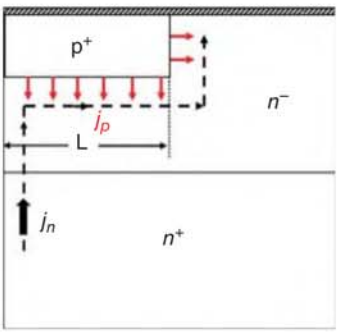


Figure 14.12 MPS diode: schematic way of electrons around p-island.

Often, these diodes are used in boost-converter/PFC topologies and they are exposed to high currents e.g. if the DC-link capacitor has to be re-charged quickly after a grid-voltage drop.

In [20], the on-set voltage of the hole injection was approximated by integrating along the way of the electrons around the p-islands as shown in Figure 14.12 and Eq. (14.5).

$$V_{\mathrm{p}} = \int_0^L R \cdot j_{\mathrm{n}} \cdot x \, \mathrm{d}x = \frac{1}{2} \cdot R \cdot j_{\mathrm{n}} \cdot L^2 \tag{14.5}$$

Here, R is the resistivity in Ω/□ and L is the dimension of the pn-region, where R can be approximated by ρ/d for the thin epi-layer thickness d. The p-region will inject as soon V_{p} is equal to the difference of built-in voltage of the pn-junction and the threshold voltage of the Schottky junction. Finally, the necessary electron current density can be expressed with

$$j_{\mathrm{n}} = \frac{2 \cdot (V_{\mathrm{bi\_pin}} - V_{\mathrm{Schottky}})}{R \cdot L^2}. \tag{14.6}$$

Failure patterns during surge currents are typically found in the modification of the frontside metallization and bond-wire aging/destruction. Reason is the high temperature rise of the frontsidenear layers, described also in [21]. Temperatures up to 500 °C and more are reached easily during an event close to the destruction limit, see Figure 14.13 and 14.14.

Additionally, the surge-current ruggedness of the internal body diode of SiC MOSFETs is put more into the focus [22, 23]. Since this diode is used as a free-wheeling diode, it must be able to withstand surge-currents generated in special failure cases and to carry, e.g. the failure current of a motor load. A typical surge-current event at the body diode is shown in Figure 14.15.

A similar failure pattern like for SiC MPS diodes is observed during the surge-current event of the body diode under different pulse lengths. The prominent failure mechanism at very high surge-current pulses is molten source metallization which also might shorten the gate-source path at the gate runners/fingers, see Figure 14.16. However, the thermal limitation of the body diode is similar to the SiC MPS diode, if applied in the same housing (here TO-247).

Since the diode characteristic can be controlled via the gate potential of the MOSFET, it is also possible to start the surge-current event with a positive V_{GS} as shown in

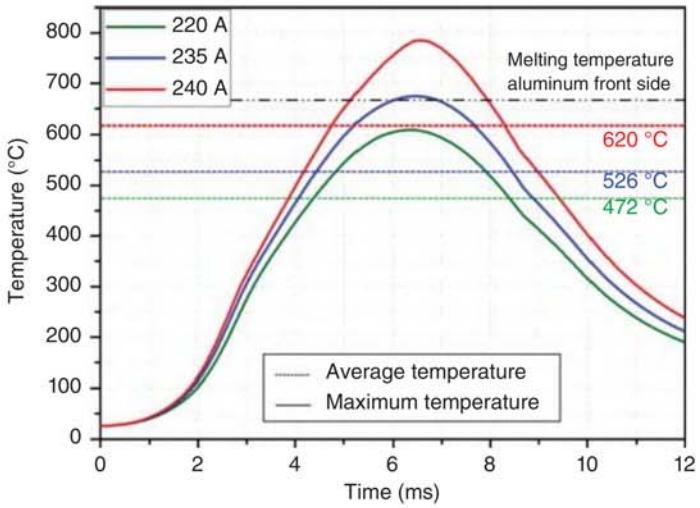


Figure 14.13 Simulated temperatures during a 10 ms surge-current event with different peak currents for a 1200 V/20 A MPS diode. For simulation, an ANSYS model was used taking into account metallization, bond wires and the thermal properties (solder, etc.) until the lead frame. Source: Palanisamy et al. [21].

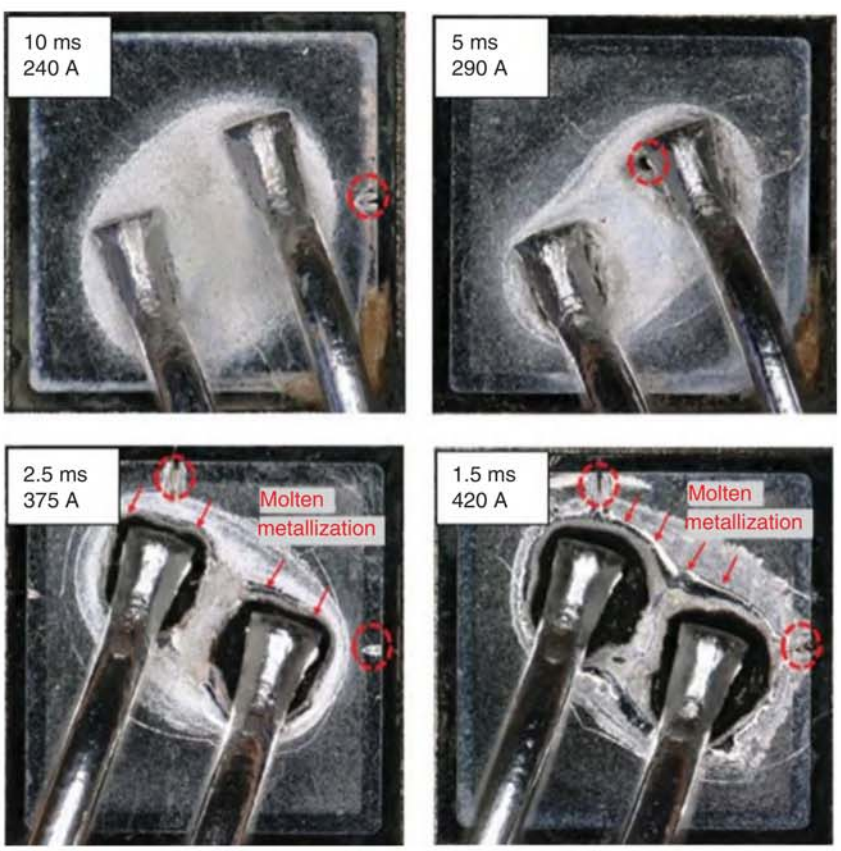


Figure 14.14 Failure pictures after single-event destructive surge-current pulses with a 1200 V/20 A SiC MPS diode.

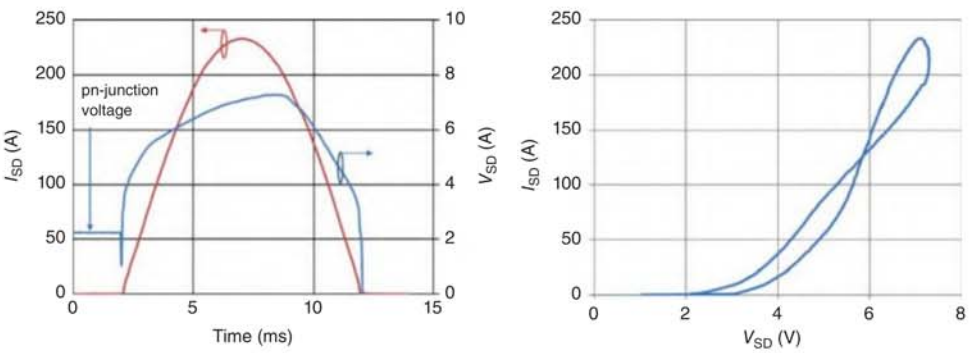


Figure 14.15 Last pass surge-current waveform of a 1200 V/20 A SiC MOSFET body diode at $V_{GS} = -5$ V.

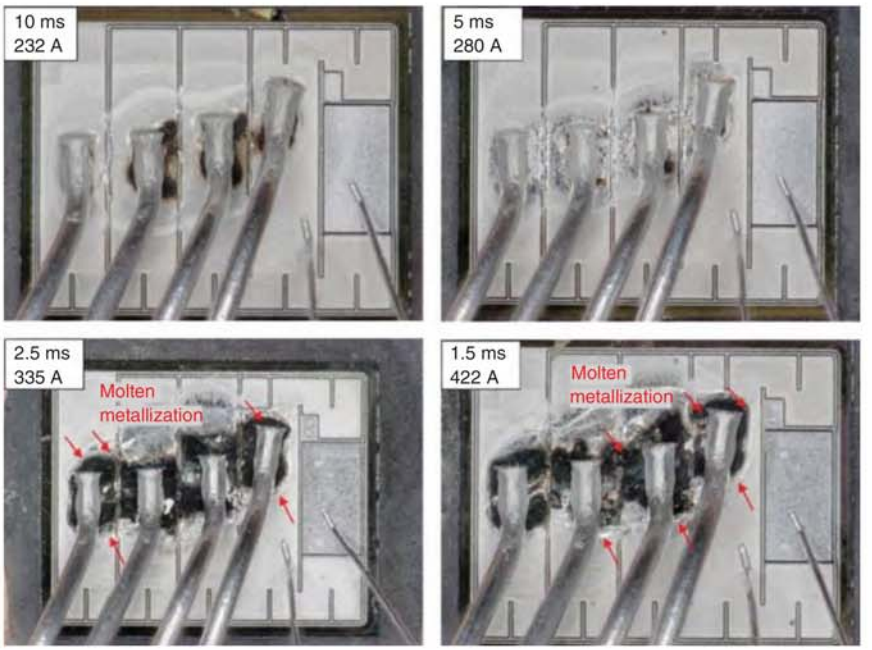


Figure 14.16 Surge-current destruction behavior of 40 mΩ class, 1200 V SiC MOSFET under different pulse lengths. Surge current applied to body diode (third quadrant) with $V_{GS} = -9$ V.

Figure 14.17 at $V_{GS} = 15$ V. The most distinct difference is the missing pn-junction voltage at the beginning of the event and the visible p-region injection start, similar to the SiC MPS diode in Figure 14.11. In the 1200 V class, no huge difference between opened/closed channel operation and the maximal possible surge currents was found [9]. For higher voltage classes, it is possible that an opened *n*-channel hinders the p-regions from injecting holes more effectively due to the higher voltage drop across the drift region, leading to a reduced ruggedness. It has to be taken into account that for body diodes a new failure mode is added, which can be found in a damage of the gate-source path [22]. Therefore, after every surge-current pulse, the blocking capability of the drain-source path and the gate-source path has to be checked.

Especially, if SiC MPS diodes are used in booster topologies, repetitive over/surge currents may be possible. It was found that SiC MPS diodes could withstand a high number of high-energy surge-current pulses [24]. The main final failure mechanism is a thermomechanical destruction at the bond-wire feet which may also lead to a loss of the blocking capability, see Figure 14.18. Additionally, in some cases also cracks in the SiC substrate were found, compare Figure 14.19. A very high temperature swing in connection with different coefficients of thermal expansion (e.g. backside solder, SiC substrate, lead frame) is the root cause. Similar failures were also reported for silicon diodes exposed to high surge currents. In practice, the current peak and

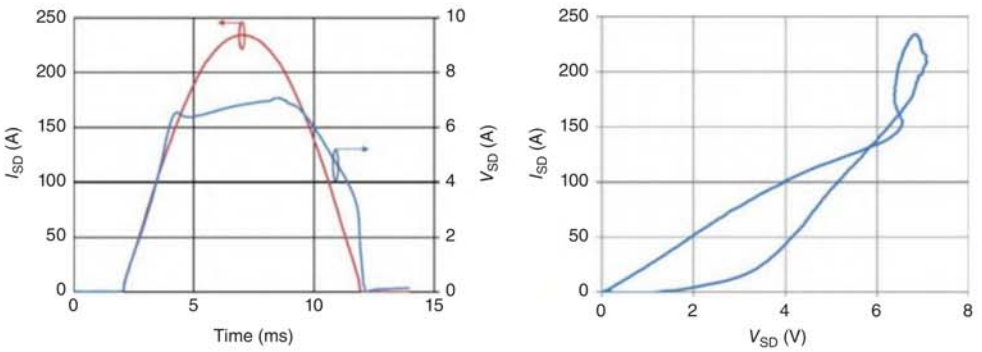


Figure 14.17 Last pass surge waveform of a 1200 V/20 A SiC MOSFET in the third quadrant $V_{GS} = 15$ V. The body diode part of the device starts to conduct current at c. 4 ms.

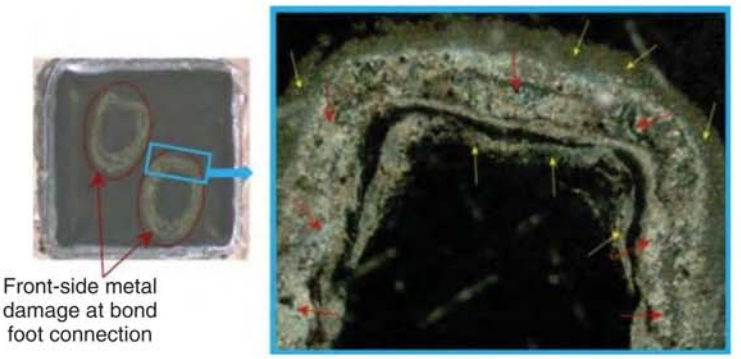


Figure 14.18 Optical microscope image from chip backside (after removal of backside metal) after doing 533 pulses with 240 A peak current at a 20 A/1200 V SiC MPS diode.

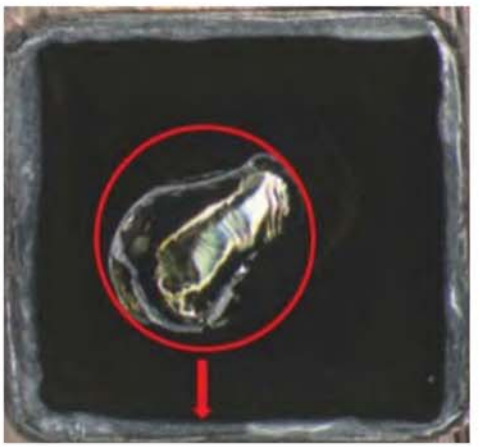


Figure 14.19 Shell-like crack at backside of the chip after doing 2570 pulses with 220 A/10 ms at a 20 A/1200 V SiC MPS diode.

thus the temperature for repetitive surge currents will be smaller to stay within the datasheet limits. Therefore, a high number of possible repetitive over-current events is expected. For future optimization, a thicker frontside high-melting metallization, e.g. copper, would be an improvement. An improved chip-backside connection to a lead frame or DCB also helps to increase the maximum possible surge-current energy, at least for pulses in the millisecond range. Sintering or diffusion soldering would be an adequate option.

It was reported that for very high repetitive surge currents in the bipolar regime, the growth of stacking faults is somehow unavoidable [24]. A countermeasure could be a very thick but expensive buffer region. Fortunately, compared to the normal operation condition, a surge-current event is rather seldom. Figure 14.20 shows the I/V curves of a 20 A/1200 V SiC MPS diode under a very high repetitive surge-current stress. An increased leakage current was found after the test and a shift of the forward voltage drop in the unipolar and bipolar region was observed as well. However, it is hard to distinguish between thermomechanical and bipolar degradation just from

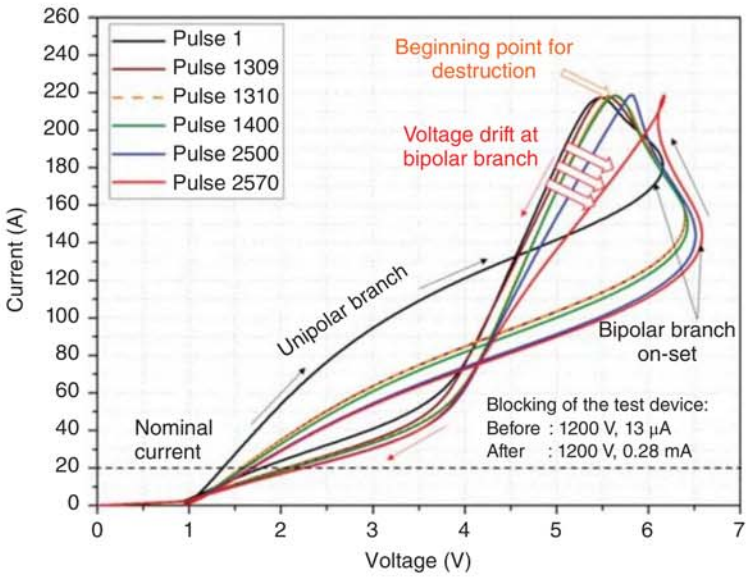


Figure 14.20 *I/V* curves of 220 A peak/10 ms sine-shape repetitive surge currents at 20 A/1200 V SiC MPS diode. An increase in leakage current and V_F shift in unipolar and bipolar regime was observed. Source: Palanisamy et al. [24].

the I/V curves. Only a detailed failure analysis, including an electroluminescence investigation of the forward-current flow, can give further insights.

Repetitive surge-current tests with SiC MOSFETs have been carried out in [25]. The applied current was higher than 10 times the channel's rated current for a time of 10 µs. No substantial electric characteristic degradation could be observed in the devices that survived 1000 repetitive 10 µs surge-current pulses with subsequent 80% rated reverse voltage applied as soon as the current pulse is extinguished. Three suppliers were tested. This result confirms that SiC devices are quite rugged in surge-current conditions.

14.1.3 Avalanche Capability

The avalanche capability of a device can be a big advantage for the application and for the self-protection against overvoltages which might be too high. With regard to silicon devices, MOSFETs are typically rated for avalanche in the datasheet. For higher voltage classes above 650 V, IGBTs or silicon pin-diodes are used, where no avalanche capability is rated. At most, some manufacturers allow to drive the device with some milliampere into the breakdown. However, this is not comparable with a hard avalanche rating, where the device is able to withstand more than the nominal current at the breakdown branch.

SiC devices are predestined to allow avalanche clamping also for high voltage classes above 1200 V and up to high currents. First 3.3 kV SiC MOSFETs have already been avalanche rated [26]. Due to the high critical field strength in SiC, the drift-zone

doping N_D can be adjusted to very high values. In the 1200 V class, base dopings in the range of $1 \times 10^{16}\,\mathrm{cm}^{-3}$ are found. In avalanche, holes p_{av} and electrons n_{av} are generated. Holes are flowing to the source, respectively anode, and electrons to the drain, respectively cathode [27]. Within the space-charge region, the generated carriers p_{av} and n_{av} can be included in the basic Poisson equation according to their polarity, in a one-dimensional expression as

$$\frac{dE}{dx} = \frac{q}{\varepsilon_0 \cdot \varepsilon_r}(N_D + p_{av} - n_{av}). \tag{14.7}$$

At the source (anode) side border of the space-charge region, no electrons arrive and the reverse/avalanche current is carried by holes only. The small contribution of diffusion current and recombination center-induced leakage current will be neglected. Then at this position holds

$$p_{av} = \frac{j_R}{q \cdot v_{sat}(p)} \tag{14.8}$$

where j_R denotes the reverse/avalanche current and $v_{sat}(p)$ denotes the saturation velocity of holes at the given high electric field. At the drain (cathode) side border, the arriving reverse current is a pure electron current. The density of generated electrons is

$$n_{av} = \frac{j_R}{q \cdot v_{sat}(n)} \tag{14.9}$$

with $v_{sat}(n)$ of 2×10^7 cm/s for SiC at $T = 300$ K. This results in a current density of 32 kA/cm^2 required to have the same amount of electrons as the background doping, which is the condition for possible branches with a negative differential resistance (NDR) [27]. This is about 60 times the rated current density (e.g. 500 A/cm^2). MOSFETs and MPS diodes can be designed to have the avalanche breakdown in the volume. Even with local current crowding due to the NDR effect, such values will hardly be achieved. Therefore, SiC devices show stable I/V curves at the breakdown branch up to very high current density values. In the MOSFET, the turn-on of the parasitic npn-transistor has to be considered as well. However, due to the short channel length, this requires also extreme high current densities.

Practically, taking the overall high power dissipation during an avalanche event into account, it was found that for a microsecond time under avalanche, 1200 V SiC MPS diodes could withstand more than 10 times the nominal current without destruction [28].

A second prerequisite for a high avalanche ruggedness, besides a high drift-zone doping, is to have the location of the avalanche breakdown within the active area of a chip. The junction termination is not able to carry high currents. This is fulfilled for most of the SiC devices. Due to the necessity of shielding Schottky junctions or gate oxides with deep p-regions, the initial breakdown point can be typically found in the active area for MPS diodes and SiC MOSFETs, see Figure 14.21.

If the electroluminescence picture of the chip is recorded at the breakdown event (Figure 14.22, [29]), it can be seen that it is not completely uniform over the chip. An anisotropy in the ionization rates leads to a preferred starting region [30, 31]. With

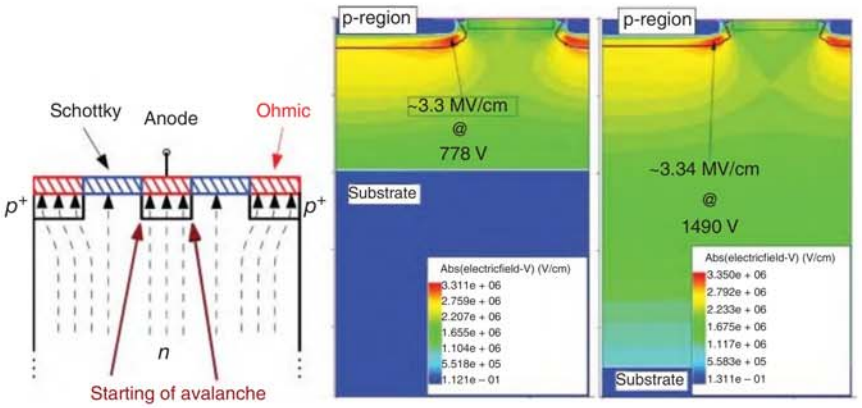


Figure 14.21 Left: onset of avalanche breakdown in the active area of a SiC MPS diode due to deep p-regions, right: TCAD simulation at breakdown condition with electric field strength, 650 V vs. 1200 V SiC MPS diode. Source: Rupp et al. [29]. © 2014, IEEE.

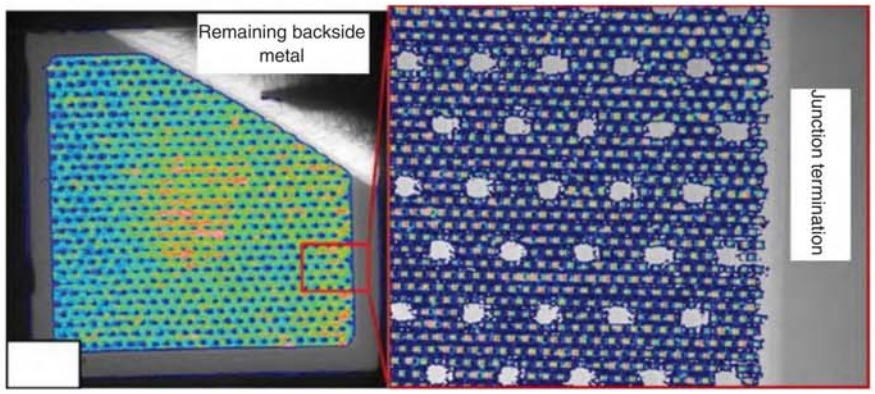


Figure 14.22 Electroluminescence picture at breakdown of SiC MPS diode. Slightly higher rate of impact ionization at the right side of the chip. Source: Rupp et al. [29]. © 2014, IEEE.

increased temperature during avalanche, the region changes by changed (increased) impact ionization rates and distributes the dissipated energy more homogenously.

Since diodes cannot be actively switched into an unclamped-inductive switching mode, an auxiliary switch, e.g. a high-voltage IGBT, can be used to trigger the avalanche, see circuit in Figure 14.23.

A typical unclamped-inductive switching event with an 8 A/1200 V SiC MPS diode is shown in Figure 14.24. With the help of the temperature dependence of the breakdown voltage, it is possible to estimate the temperature during a clamping event (Figure 14.24 right), which is in the range of 230 °C. However, this value is just an average value since a homogenous temperature and current distribution are assumed. Compared to silicon power devices, a much lower temperature

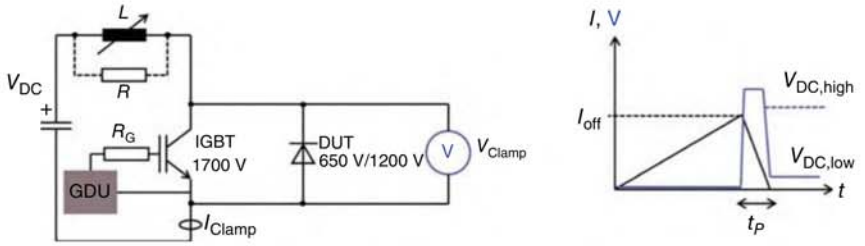


Figure 14.23 Unclamped-inductive switching test circuit for diodes and schematic clamping waveform.

dependency of the breakdown voltage is found (e.g. 1.2 V/K vs. 0.33 V/K in the 1200 V class), which is quite favorable for avalanche condition. The voltage during a clamping event will stay more stable.

Another positive effect of SiC devices is the very low intrinsic carrier density. This makes it possible to block, e.g. a high DC-link voltage after withstanding an unclamped-inductive switching event, see Figure 14.25. The temperature rise during the clamping event is not high enough to raise the intrinsic carrier density n_i to values where the leakage current level will lead to thermal runaway. Even though the saturation current term j_s is dependent on n_i^2 as given in the overall leakage current density j_r of a pn-junction (Schottky contact contribution neglected) [32]:

$$j_r = j_s + j_{SCR} = q \cdot \left(n_i^2 \cdot \frac{D_p}{L_p \cdot N_D} + n_i \cdot \frac{w_{SCR}}{\tau_{SCR}} \right) \tag{14.10}$$

with q is elementary charge, D_p is diffusion constant of holes, L_p is diffusion length of holes, N_D is base doping, w_{SCR} is space-charge region, τ_{SCR} is generation lifetime in the space charge region.

For silicon devices, unclamped-inductive switching may lead to thermal runaway more early, caused by too high leakage currents afterward.

To be able to evaluate the avalanche performance over a wider current and pulse range, a test series with different inductances can be recorded, see Figure 14.26. The failed chips of the study show a burn mark within the active area and not in the junction termination, compare Figure 14.26 right. For small inductance values, the current in avalanche can be very high and trigger further destructive failure modes, e.g. turn-on/latch-up of the parasitic npn-transistor in the case of MOSFET devices [33]. The energy during such a pulse can be calculated with

$$E_{AV} = \frac{1}{2} \cdot L \cdot I_{off}^2 \cdot \frac{V_{Clamp}}{V_{Clamp} - V_{DC}}. \tag{14.11}$$

For MPS diodes, the maximum energy during clamping was found to be reduced at medium inductances [28]. At these clamping times and currents, following the Z_{th} characteristic, the frontside metal is stressed most which can also be seen in the failure pattern for 400 µs. For even higher inductances and lower currents, deeper

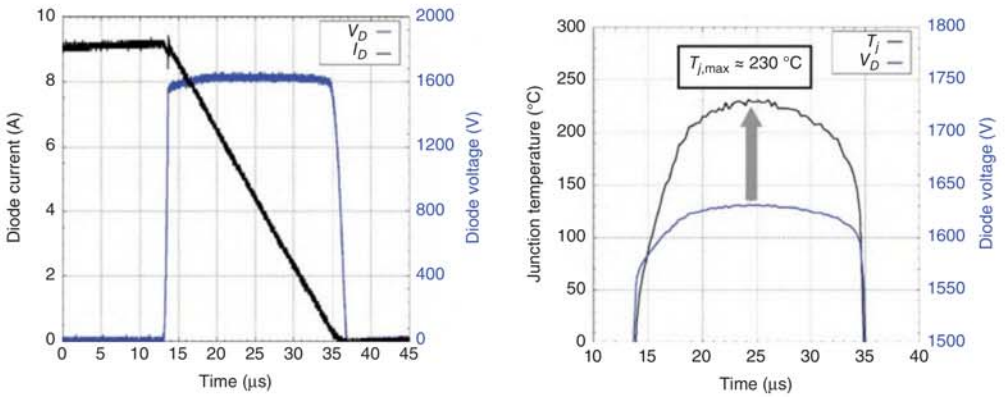


Figure 14.24 Left: lastpass unclamped-inductive switching pulse of an 8 A/1200 V SiC MPS diode with $L = 3.8$ mH, Right: temperature estimation with the help of temperature-dependent breakdown voltage 0.33 V/K measured before. Source: Basler et al. [28].

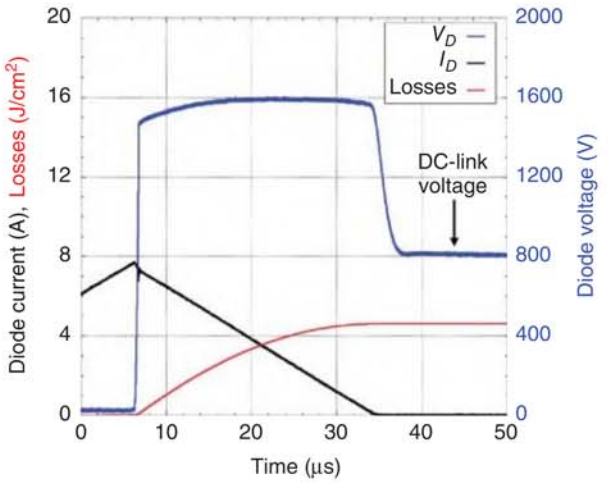


Figure 14.25 Unclamped-inductive switching event of an 8 A/1200 V SiC MPS diode with blocking the DC-link voltage of 800 V after the clamping event, $L = 3$ mH. Source: Basler et al. [28].

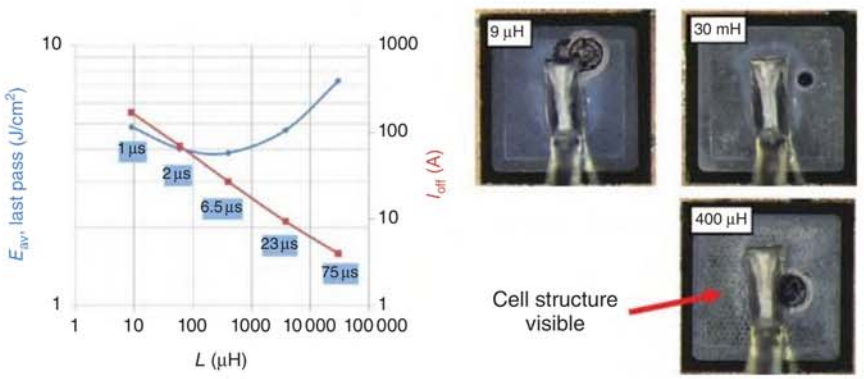


Figure 14.26 Left: last-pass energy and currents of an 8 A/1200 V SiC MPS diode under unclamped-inductive switching. Right: different failure patterns. Source: Basler et al. [28].

layers of the complete assembly are used (SiC substrate, lead frame) and the energy is increased again.

A similar $E = f(L)$ plot for a 40 mΩ SiC MOSFET is shown in Figure 14.27 and single waveforms in Figure 14.28. This device is able to resist clamping currents above 100 A without destruction. In principle, the SiC MOSFET shows a comparable avalanche robustness as the MPS diodes. This holds for planar and trench concepts, shown, e.g. in [34]. A latch-up for a SiC MOSFET is more unlikely since the built-in voltage of the n^+-source/p-body junction is very high (≈2.7 V at 25 °C) compared to silicon and needs to be exceeded during an unclamped-inductive switching

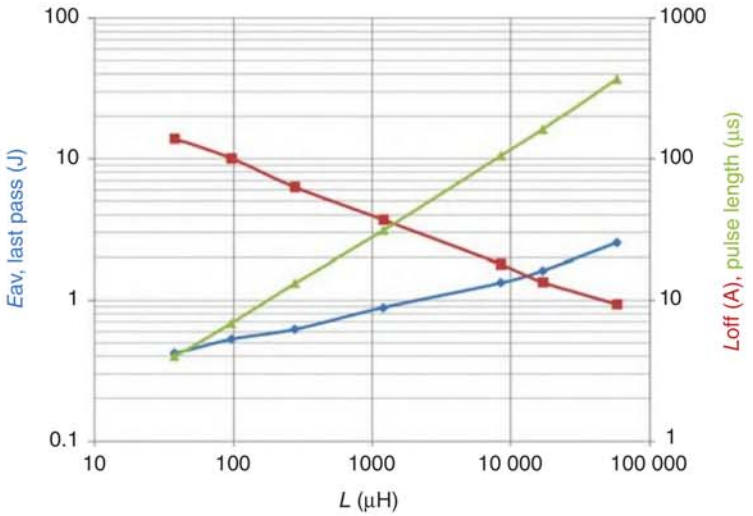


Figure 14.27 Unclamped-inductive switching with last-pass energy of a 40 mΩ/1200 V SiC MOSFET.

event. After performing a high-energy clamping event, the leakage currents should be checked, especially the gate-source leakage path of an SiC MOSFET.

Since SiC devices have a proven high single-event avalanche capability, a next step would be to also define a repetitive/periodic avalanche energy. First studies [28, 35, 36] already show a high performance. For SiC MPS diodes, it was proven that the high-energy repetitive avalanche is very stable, showing no bipolar degradation. Only thermomechanical fails, such as modifications of the bond-wire connection or frontside metal were observed, see Figure 14.29 [36], caused by the strong temperature swing, similar to a high-current short-pulse power cycling. Due to the modifications, the Schottky barrier height or threshold voltage $V_{GS,TH}$ may change as well, as shown in Figure 14.29 right.

Still, more studies have to be conducted to also verify the gate oxide and general parameter stability of SiC MOSFETs under a repetitive avalanche condition. For silicon low-voltage MOSFETs, it was shown that especially shielded-gate technologies are susceptible to parameter change. The main reason is the change of the charge characteristic at the trench oxide due to, e.g. hot carriers (holes). As a consequence, the breakdown voltage or gate-threshold voltage may change [37]. Since the shielding structures of SiC MOSFETs are setting the point of the avalanche breakdown deeper into the device and keep it away from the gate oxides, it is expected that these types of MOSFETs behave more stable. First results already confirm this [35]. Furthermore, the avalanche current does not directly flow at the channel region.

However, material defects (e.g. crystal defects) have to be minimized to achieve a high avalanche robustness in general [38]. Wafer-level unclamped-inductive switching tests may be helpful as shown in [39].

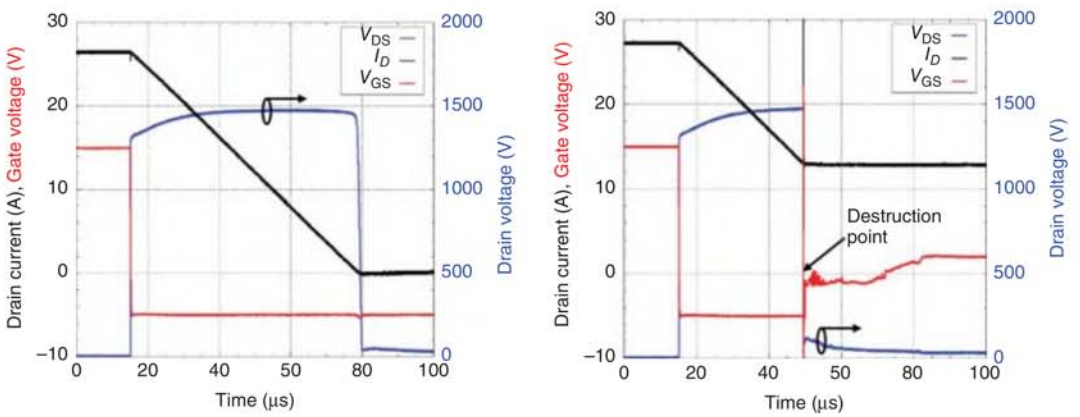


Figure 14.28 Unclamped-inductive switching event of 40 mΩ/1200 V SiC MOSFET, $L = 3.5$ mH, Left: last-pass event, Right: destruction event.

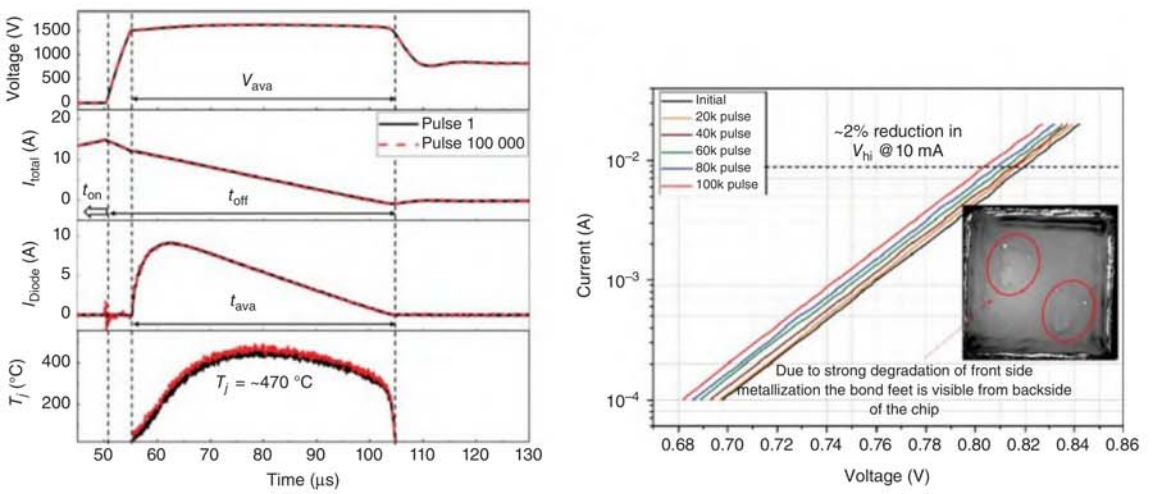


Figure 14.29 Left: Repetitive unclamped-inductive switching event of 1200 V SiC MPS diode, $L = 3.1$ mH, $V_{DC} = 820$ V, $t_{interval} = 1$ second, $T_{case} = 25$ °C, Right: Degradation of the Schottky barrier and degradation pattern (modification of bond wire connection – red circles) of chip after the test is shown from the back side. Source: Palanisamy et al. [36].

14.2 Cosmic-Ray Stability

Cosmic-ray stability is an important reliability criterion. SiC is discussed to be "radiation-hard" in applications for semiconductor detectors working in harsh environments like nuclear, space and particle physics [40]. For SiC, where the carrier concentration is very low, the change of the leakage current with radiation dose was observed to be minimal. Sometimes, statements such as "radiation hard" are made for SiC power devices. However, this cannot be applied for the radiation tolerance of power devices against cosmic ray effects. These effects are quite different. The most important cosmic ray failure mechanism for power devices is the "single event burnout" (SEB) [41] or also named "single event effect" (SEE) [42] which is a complete different phenomenon. In recent work, SiC devices have been evaluated to show high total ionizing dose (TID) tolerance, but low SEE tolerance [42].

Cosmic ray faults not only occur in space but also on the earth surface. High-energy primary cosmic ray particles from deep space collide with atmospheric particles and generate a variety of secondary high-energy particles. Neutrons are most relevant for generating device damage on the earth surface. The neutron flux density is in the range of $20\,cm^{-2}/h$ at sea level [43] and increases strongly with altitude. At 12.2 km (40 000 ft, the upper flight level of civil airplanes), there is a neutron flux density of $7200\,cm^{-2}/h$ for a latitude of 45° [44]. The maximum neutron flux density is found at an altitude of 18 km. Further relevant parts are high-energy protons, which contribute to the total cosmic radiation with 20% to 30% at sea level and 50% at 12.2 km altitude. Creation and absorption compete in the showers in the higher atmosphere. Regarding space application, the majority of energetic particle flux at low earth orbit consists of proton flux [45]. Protons as charged particles can be shielded; however, aluminum shielding of 2.5 mm thickness is no proper protection against proton flux, since a large fraction of proton flux exhibits a high energy above the 100 MeV range [45].

To evaluate cosmic ray failure rates, tests with a large number of devices at high DC voltage were carried out. First, tests at high altitudes were arranged, since the terrestrial cosmic particle flux increases with altitude above sea level. In parallel, tests with particle accelerators were carried out and neutron sources emitting neutron beams with atmospheric-like spectrum are used as well. Such sources can be found at the Research Center for Nuclear Physics RCNP (Osaka University, Japan), or at the Los Alamos Neutron Science Center (LANSCE, United States). Nowadays, cosmic ray stability is mostly evaluated by using particle accelerators or neutron sources, since this delivers relevant results in a short amount of time.

The cosmic ray failure (SEB, SEE) occurs in a device while it is exposed to a high voltage and consequently a high internal electric field strength. The impact of particles colliding with a lattice atom creates, at high electric fields, an electron–hole plasma. Impact ionization is enhancing the effect, in detail different for Si and SiC.

For high-voltage Si devices, the space charge is wide, e.g. in the range of 100 µm for a 1200 V device. After impact and resulting plasma, an extreme high gradient density of charge density emerges at the borders between the plasma and the space

charge, leading to very high and steep field peaks. If the electric field exceeds a certain threshold value, impact ionization creates enhanced carrier density. One field peak runs to the anode, the other to the cathode. A so-called "streamer" is formed in analogy to a discharge in a gas. The device is flooded locally with free carriers within some hundred picoseconds; hence, a local current tube occurs. Still, the time in the range of 200 ps [46] is too short for a temperature increase that would lead to destruction. However, arriving at the pn- and nn^+ junction, the streamer shortens both sides of the device and is, at the first moment, combined with an avalanche generation at both sides. For an abrupt nn^+ junction, the cathode-side injection delivers the main part of the generated current. It is assumed that this or other type regenerative mechanism is finally responsible for the destruction of the device. Details are described in [47].

For SiC, the width of the space charge is 1 order of magnitude lower. The initially generated plasma already shortens the space charge [48].

The failure pattern shows, if the device is protected by a fuse, a narrow pinhole in Si as well as in SiC. An example for a SiC MPS diode is shown in Figure 14.30 [49]. In simulations of cosmic ray failures in SiC MPS diodes by Shoji, similar effects like in Si diodes were found [49]. The SEB current produced by impact ionization at the nn^+ interface is common to both Si and SiC power diodes. It corresponds to the destruction caused by an Egawa-type field with a field peak on both sides [50]. The effect is denoted as dynamic avalanche of the third degree in [47]. In [49], the same effect is denominated as "local second breakdown."

Experiments were carried out to compare SiC devices with Si devices. For 1200 V Si IGBTs, a sharp increase of cosmic ray failures is found above a threshold voltage of 70% of V_{rated} [51], in accordance with [52]. At 85% of V_{rated} for 1200 V SiC MOSFETs, first failures were detected [53]. However, 1200 V Si diodes with a threshold above

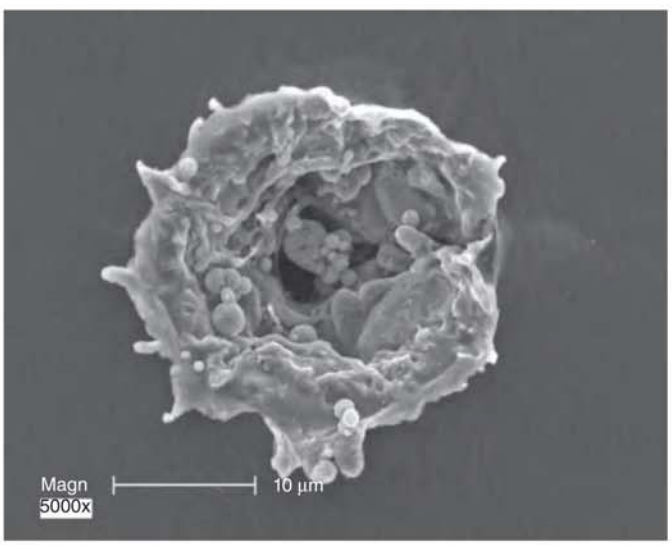


Figure 14.30 Cosmic-ray failure of a SiC MPS diode. Source: Figure from Shoji et al. [49].

100% of the rated blocking voltage are found [51]. The specific design is of strong influence.

A detailed comparison is reported in [54]. The devices are compared not only for the rated voltage but also for the measured breakdown voltage. This is a reasonable method since many SiC devices are rated for lower voltage than the breakdown voltage given by the volume of the device. The rated voltage compared to the measured breakdown voltage V_{BD} for the investigated 1200 V Si IGBTs was found to be 88% to 89%, for the 1200 V SiC MOSFET it is 73%. For 1700 V, the Si IGBT used 79% of the breakdown voltage as rated voltage, while the SiC MOSFET used 64%. This shows that the high critical field strength of SiC is only partially exploited in the investigated SiC designs. The results analyzed in dependence of V_{DC}/V_{BD}, meaning normalized to applied DC voltage V_{DC} compared to the measured breakdown voltage V_{BD}, are as follows: for 1200 V devices, a small advantage for the SiC MOSFET was found, see Figure 14.31a. For 1700 V devices, the failure rate becomes significant at similar V_{DC}/V_{BD} (Figure 14.31b).

For Si, the different devices were fitted by [55] with the empirical equation

$$r = C_3 \cdot e^{\frac{C_2}{C_1 - V_{bat}}} \tag{14.12}$$

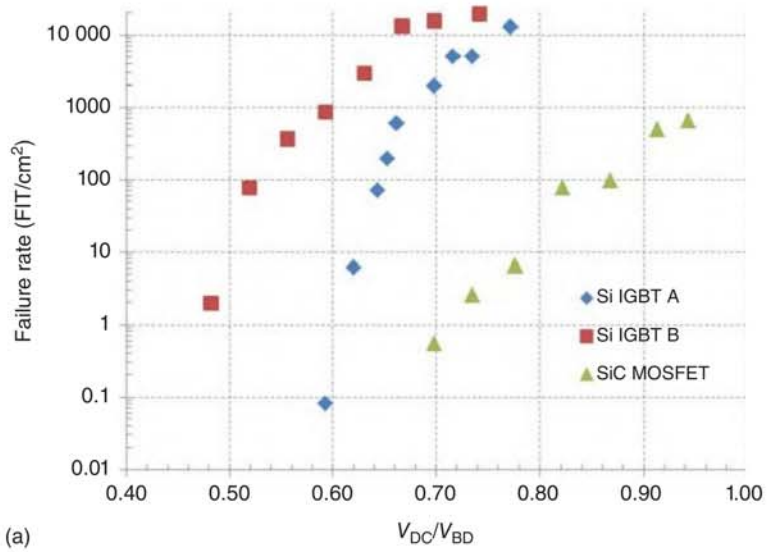
where C_1, C_2, and C_3 are empirical constants. The function has a pole at the voltage C_1 in Eq. (14.12). Below C_1 the model is not valid, and the failure rate is zero. All recent experiments with Si [49, 51, 52] can be well described with a function of type Eq.(14.12). For SiC, the pole C_1 is not visible in the same way. If given, it occurs at lower V_{DC}/V_{BD}. Up to now, the models do not explain this difference, and further research is needed. However, the effect has to considered for SiC in aircraft applications where the cosmic ray particle flux is several decades higher.

The physics of cosmic ray failures seems to be very similar for Si and SiC. However, with the perspective of increased crystal quality in the future, for SiC the full potential of the material will also be used. More data for SiC and for Si are of high interest. For the same rated current, there is a lower device area for SiC. Therefore, it may remain a small advantage for SiC at terrestrial levels.

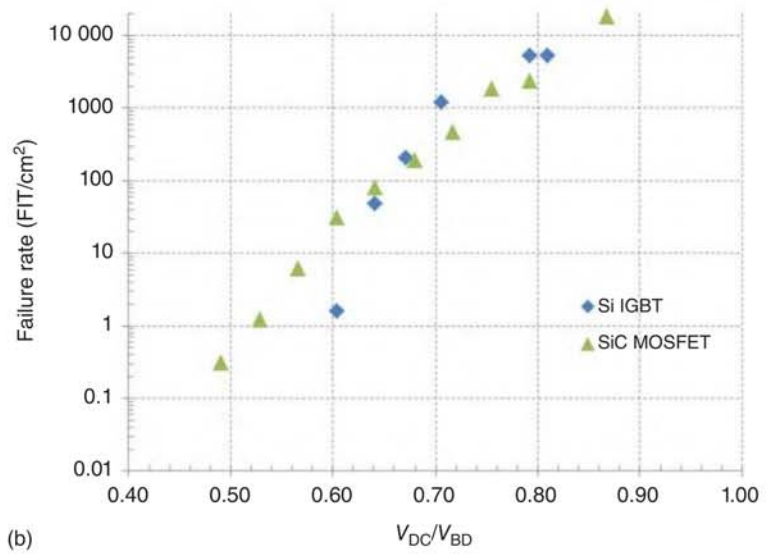
14.3 Thermomechanical Reliability

The thermomechanical reliability of a device is determined by its packaging technology. The challenges for SiC packages are significantly higher than that for Si. This is due to these factors:

- The capability of fast switching requires a very low internal inductivity; therefore, the package has to be compact and internal leads/bond-wire loops have to be short. Additionally, a very symmetrical arrangement of internal connectors at paralleling of devices is required. This holds for the main terminals as well as for the gate wiring.
- For the same current, SiC devices are smaller. This means a higher current density, which is combined with a higher power-loss density.



(a)



(b)

Figure 14.31 Comparison of Cosmic ray failure rates for Si IGBTs and SiC MOSFETs normalized to applied DC voltage V_{DC} compared to the measured breakdown voltage V_{BD}. (a) 1200 V rated devices and (b) 1700 V rated devices. Source: Figures according to data from Felgemacher et al. [54].

Table 14.1 Thermomechanical material data.

	Si	4H-SiC	GaN
Thermal conductivity (W/mmK)	0.13	0.37	0.13[a)]
Specific heat [J/(kg*K)]	700	690	490
CTE (ppm/K)	2.6	4.3	3.17
Young's modulus E (GPa)	162	501	181

a) on Si substrate.

- SiC is a very stiff material exposing every interface to higher stress under conditions of mismatch of coefficients of thermal expansion and temperature swings.

A comparison of the thermomechanical characteristics is given in Table 14.1.

In SiC, both the thermal conductivity and Young's modulus are in fact anisotropic, but this fact is usually neglected. The thermal conductivity of SiC is about three times higher. However, also the Young's modulus describing mechanical stiffness is more than three times larger than it is for Si. Thermal–mechanical simulations in [56] of a chip soldered on a DCB substrate showed that the mechanical energy, determined by the stress–strain integral ΔW, is more than three times higher at the corner of a SiC device than for a Si device for the same geometry and the same temperature swing. Since ΔW represents the force driving the initiation and propagation of a crack in a solder layer, the crack propagation rate in SiC is expected to be faster by the same factor.

14.3.1 Temperature-sensitive Electrical Parameters

The power-cycling test is the main test to determine the lifetime of a device when exposed to load cycles in the application. The power chips are actively heated by the losses generated in the power devices themselves in a power-cycling test. It is therefore necessary to measure the temperature. Usually, the devices are packaged. The surface temperature of the housing will deviate strongly from the temperature of the semiconductor die, especially for short electric load pulses. Therefore, a temperature-sensitive electrical parameter (TSEP) is necessary. For Si devices, the established method is the determination of the junction voltage of a pn-junction $V_j(T)$ which decreases strongly with increasing temperature due to the increasing intrinsic-carrier density in semiconductors [47]. The pn-junction of a diode or the base-emitter junction of a bipolar transistor is used [57]. This method has been established since the beginning of power device development. The so-called determined temperature is called virtual junction temperature T_{vj}. The measurement has to be executed in the range of 1/1000 rated current. The thermal resistance in data sheets of European manufacturers is initially determined with the $V_j(T)$ method. It is reinvestigated in detail for Si IGBTs in [58].

Note that in fact a device has a significant vertical and lateral temperature profile and every location has a different temperature, especially for large chips with an area

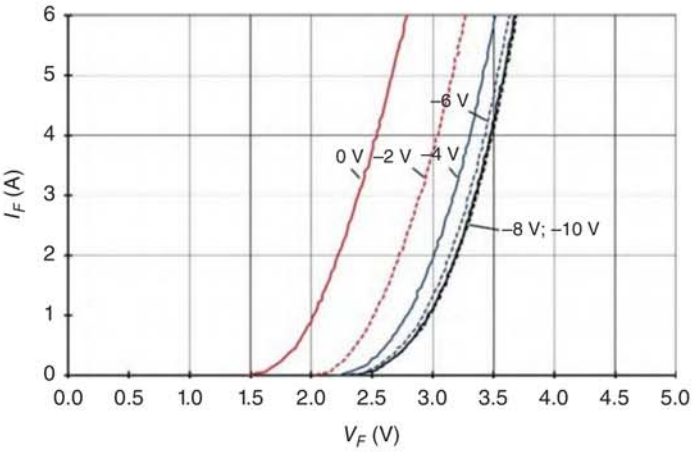


Figure 14.32 Forward characteristics of the inverse diode of the SiC MOSFET IMW120R045M1 (Infineon) for different gate voltages, $T = 145\,°C$.

$>0.5\,cm^2$. T_{vj} determined with the $V_j(T)$ method was found to be close to the area average calculated from the measurements with infrared camera at the surface of an opened device.

For the SiC MOSFET, the voltage drop of the inverse diode $V_{SD}(T)$ at a low measurement current can be used as TSEP, which is recommended in [59]. However, the gate-channel of the SiC-MOSFET is not completely off at $V_{GS} = 0\,V$ and a voltage in conduction direction of the inverse diode The voltage drop up to the built-in voltage of the pn-junction opens the channel partially and enables a part of the current to pass the slightly inverted channel. The current–voltage characteristic of the inverse diode depending on the gate voltage is shown in Figure 14.32. It indicates that only for the gate voltage of −6 V and lower the characteristics of the diode do not change anymore and the junction voltage $V_j(T)$ can be measured.

Since the current through the MOS channel will depend on the threshold voltage, it has to be ensured that the channel is turned off even if there is a drift of $V_{GS,TH}$. Therefore, a negative gate voltage below −6 V is recommended. Figure 14.33 shows $V_j(T)$ for a SiC MOSFET measured with $V_{GS} = -8\,V$.

There are also other possible temperature-sensitive electrical parameters. The gate threshold voltage $V_{GS,TH}$ is strongly temperature dependent, but it is affected by a trapping phenomenon: after a power cycle with positive V_{GS} over several seconds, it was found that SiC MOSFETs might need up to seconds to recover to the initial $V_{GS,TH}$ value. Point defect states are negatively charged during a positive V_{GS}, neutralized at the inversion to a negative V_{GS}. Turning on from a negative V_{GS} will lead to the measurement value $V_{TH,up}$, after turn-off from a positive V_{GS}, the value $V_{TH,down}$ will occur [60]. This $V_{GS,TH}$ hysteresis $\Delta V_{TH,HYST}$ displayed in Figure 14.34 is reversible as shown in [61]. $V_{GS,TH}$ measurements have to be performed in a predefined procedure (e.g. $-5\,V \rightarrow +15\,V$, comparable is only $V_{TH,UP}$ with $V_{TH,UP}$ or $V_{TH,DOWN}$ with $V_{TH,DOWN}$).

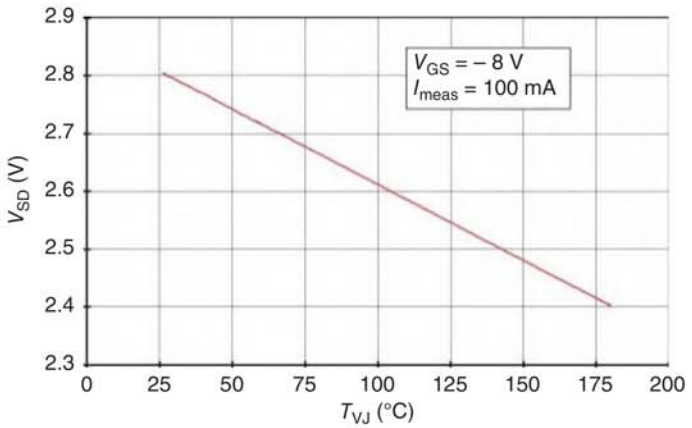


Figure 14.33 Calibration function V_j (T) for the 1200 V SiC MOSFET IMW120R045M1 (Infineon) at $V_{GS} = -8$ V.

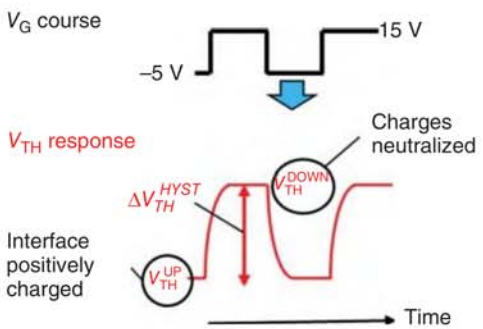


Figure 14.34 Threshold voltage hysteresis depending on V_{GS} before measurement.

However, there is also an irreversible $\Delta V_{GS,TH,BTI}$ drift which is called bias temperature instability – BTI. Observed is a positive drift PBTI and negative drift NBTI. It is shown in Figure 14.35.

This drift remains in the range of +25% resp. −25% even at long times and it differs from manufacturer to manufacturer. It is predictable for application. However, because of this effect, the $V_{GS,TH}$ is not suitable as TSEP.

During power cycling, $R_{DS,ON}$ will be affected by a bond-wire lift-off and the by gate-threshold voltage $V_{GS,TH}$ drift. $R_{DS,ON}$ is already included in the V_{DS} determination. The on-state resistance $R_{DS,ON}(T)$ is not suitable since it will increase at bond wire failures, and the separation of degradation effects will be complex. Furthermore, V_{GS}–$V_{GS,TH}$, which defines $R_{DS,ON}$ according to Eqs. (14.13) and (14.3), is influenced by a gate-threshold voltage $V_{GS,TH}$ drift.

The measured $R_{DS,ON}$ consists of

$$R_{DS,ON} = R_{pack} + R_{epi} + R_{CH} + R_A + R^* \tag{14.13}$$

where R_{pack} is the resistance due to bond wires, metallization, etc., R_{epi} is the resistance of the base layer, R_{CH} is the channel resistance, R_A is the resistance of the

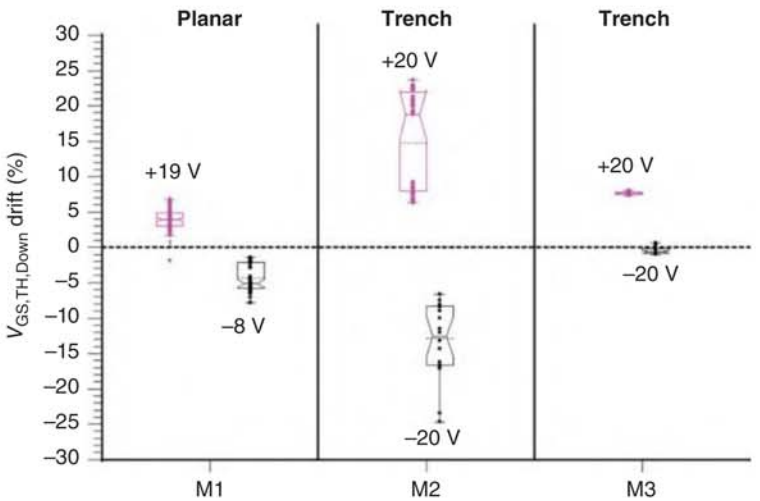


Figure 14.35 Bias temperature instability test of different manufacturers. 500 hours at 150 °C, 200 pieces per type. $V_{GS,TH}$ readout at $V_{TH,}$DOWN point. Source: Aichinger et al. [61]. © 2018 Elsevier.

accumulation layer, and R^* summarizes the other components, e.g. the substrate. If there is a $R_{DS,ON}$ increase, it might be due to R_{pack} which is a typical power-cycling ageing effect, or due to an R_{epi} increase caused by stacking faults [62] or due to a $V_{GS,TH}$ increase which modifies R_{CH}, see Eq. (14.3) [47].

Increased $V_{GS,TH}$ will lead to a higher $R_{DS,ON}$ and thus also to a higher power loss. This in turn actively influences the temperature swing and thus the lifetime of the packaging technology. Since different effects contribute to it, $R_{DS,ON}$ is unsuited as TSEP. An investigation on parameters showing a drift, which makes them unsuitable as a reliable temperature indicator, is given in [63].

14.3.2 Execution of Power-cycling Tests

During power-cycling tests, the device under test is mounted on a heat sink as in a real application. A load current is conducted by the power chips, and the power losses heat up the chip. During each cycle, considerable temperature gradients are generated inside the module. While in a temperature cycling test, all layers in the test object have the same temperature; in a power-cycling test, different layers will have a different temperature and a different thermal expansion. Therefore, different failure mechanisms can be triggered.

Figure 14.36 shows the schematic and the control pattern for SiC MOSFETs [59]. The power losses are created in the forward mode which has a positive temperature coefficient, $R_{DS,ON}$ is increasing with T, while the body diode has a negative temperature coefficient. $V_j(T)$ is measured in reverse diode mode. Figure 14.36a shows the setup for one device under test (DUT), there may be several devices arranged in a series connection. In series with the current source for I_{sense} are some diodes for protection, the amount of diodes must be sufficient so that their sum of forward

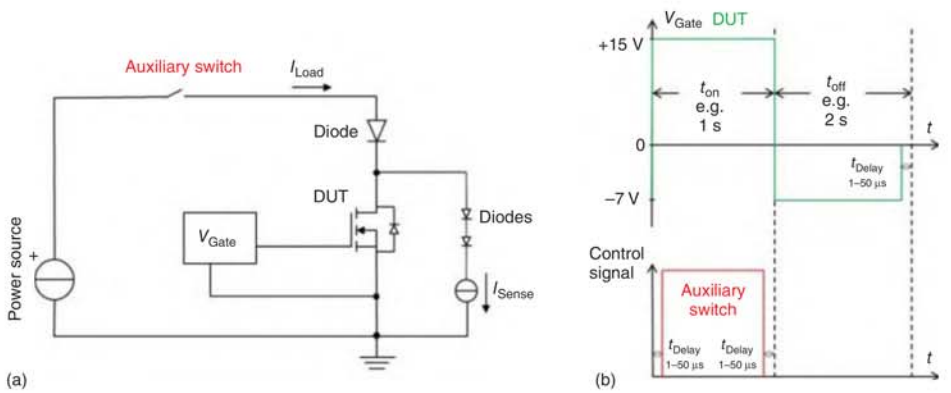


Figure 14.36 Power-cycling setup for SiC MOSFET with V_{SD}-method (a) schematic (b) control pattern. Source: Based on Herold et al. [59].

knee voltages is larger than the voltage drop across the DUT. Figure 14.36b shows the course of the control signals. First, V_{GS} is set on with the specified voltage $V_{GS,use}$ of the manufacturer. Next, the auxiliary switch is closed. Now the load current flows. The auxiliary switch is turned off. After a short delay, 1–50 µs, a negative voltage is applied, e.g. −7 V for the temperature measurement via $V_j(T)$ of the body diode of the MOSFET.

Meanwhile, the setup in Figure 14.36 has been used by different groups, e.g. in [64] and [65].

For SiC Schottky and MPS diodes, the junction voltage of the Schottky junction can be used as TSEP. The setup is then identical to the setup for IGBTs and Si diodes. It is recommended to control the junction voltage after the test, since a drift at the barrier at high repetitive load is not excluded.

14.3.3 Evaluation of SiC Power-cycling Tests

For measuring $V_j(T)$, there is again a delay time t_d between turning off of the load current and the moment of measurement. The cooling down during t_d is higher for SiC devices as compared to Si devices. For SiC power modules, it was found in the range of 4–5 K, even up to 6 K for a t_d of 1 ms, due to the higher power densities in SiC [66]. This is significant now, especially if packages with SiC and Si are compared. A correction of this measurement error is possible with the square-root-t method [67].

$$T_{vj(t)} - T_{vj(0)} = \frac{2 \cdot P_v}{(\rho \cdot \pi \cdot \lambda \cdot c_{spec})^{\frac{1}{2}} \cdot A} \cdot t^{\frac{1}{2}} \tag{14.14}$$

Equation (14.14) holds under boundary condition of a planar heat source at the surface of a semi-infinitely thick cylinder assuming a one-dimensional heat flow. Since the heat source in SiC devices is in a narrow region close to the device surface, Eq. (14.14) is found to hold for SiC devices with good accuracy [66]. It has to be mentioned that for Si IGBTs the use of Eq. (14.14) leads to a significant error, since the heat generation is across the whole thickness of the device.

For an exact evaluation of power cycling with SiC devices, the used delay time t_d between load current and T_{vj} measurement has to be added in documentation, if the measured values have been corrected with the square-root-t method or with a Z_{TH}-model or another method which is applicable. And, to be fair comparing Si and SiC, the higher t_d-caused error has to be considered as well.

To be compliant with the European standard AQG 324, two parameters have to be supervised and monitored in the test documentation: V_{DS} determined at T_{low} to indicate aging of electrical interconnections, and the virtual junction temperature, respectively, thermal resistance indicating the integrity of the thermal path.

However, V_{DS} in the MOSFET is given by $R_{DS,ON}$*I_D, and it is important to take care of some SiC-related semiconductor effects according to Eqs. (14.13) and (14.3):

- The term R_{epi} can increase due to bipolar degradation.
- The term R_{CH} can be modified by V_{TH} drift. In power-cycling tests, on-time t_{on} and off-time t_{off} are in the range of one to some seconds, and positive V_{GS} resp. negative V_{GS} is applied at the device accordingly. If there is a long-term drift, a $V_{GS,TH}$ increase will lead to a V_{DS} cold increase, and a $V_{GS,TH}$ decrease will lead to a V_{DS} cold decrease. Therefore, $V_{GS,TH}$ is to be controlled at intermediate measurements and the resulting effect to be considered in the evaluation.

Finally, an effect of bipolar degradation on the T_{vj} determination can occur for special devices. For T_{vj} measurements, the body diode is exposed to a negative V_{GS}. A measurement current I_{sense} of 100 mA for a typical small size SiC chip in a TO-housing is already in the range of 1 A/cm^2. In [68], an increase of the junction voltage V_j at low temperature was found for one of several high-voltage (3.3 kV) SiC devices. This means that T_{vjmin} will be measured as low. However, this is the only test having noticed this up to now. High-voltage SiC devices are more sensitive to bipolar degradation [62]. Just a small amount of tests of high-voltage SiC MOSFETs are reported up to now. Nevertheless, it is recommended to control the inverse diode characteristics before and after test. V_{SD} of the inverse diode should be controlled at $V_{GS} = -8$ V to -10 V and at rated current to consider this effect in the evaluation.

14.4 New Power-module Technologies with Sufficient Reliability

When using established power-module technology as soldering and wire bonding, the power-cycling capability is reduced to approximately 1/3, if Si devices are replaced by SiC devices [69]. This is explained by the higher Young's modulus of SiC, see Table 14.1, and it is confirmed by other groups, e.g. [65, 70]. Improved technologies are necessary to achieve high power-cycling lifetime with SiC devices.

14.4.1 Improved Die-attach Technologies

The Ag-sinter technology to replace solder layers is executed by densification of Ag powder layers with micro- or nanoparticles. It forms a porous rigid interconnection layer of high reliability [71]. The properties of this interconnection layer are superior to solder interfaces in all parameters. The specific thermal conductivity of the sinter layer can be as high as 220 Wm^{-1}/K and is therefore almost a factor of 4 times higher than that of a conventional SnAg3.5 solder layer. Together with a characteristic layer thickness of <20 µm, the sinter technology exhibits a reduced thermal resistance between the chip and the substrate compared to conventional solder layers of typically >50 µm thickness. The electrical conductivity is also improved due to the low specific electrical resistance of silver [47]. For Si applications, it was shown that this is increasing the lifetime by a factor of 20 and more [72]. In [64], this technology was applied to a power module with SiC MOSFETs, where on the top side

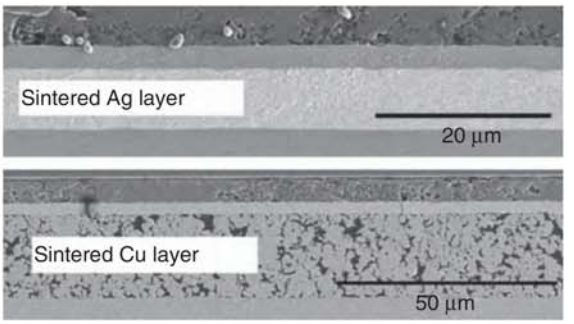


Figure 14.37 Sintered Ag-layer and sintered Cu-layer. Source: Figure from Konno et al. [73].

125 µm aluminum bond wires were applied. An excellent power-cycling capability was achieved.

Instead of Ag-sintering, Cu-sintering is also applied. Cu has a reduced CTE, an increased yield stress, and increased melting point, compared to Ag. It is more difficult to prepare a low-porosity interconnection layer; a comparison is shown in Figure 14.37 [73].

From Figure 14.37, it can be seen that the layers are different, the sintered Ag-layer of the test sample was without visible pores, and the sintered Cu-layer includes pores (12%). Nevertheless, the Cu-layer achieved a more than 4 times larger temperature cycling capability (−40 to 200 °C) than Ag. The Cu-sintered layer including pores showed a higher durability than a fine Ag-sintered layer. The higher yield strength and lower CTE of Cu make these results plausible.

Cu-sintering is used in [65, 70]. Results are shown in Figure 14.38. Si is compared with SiC for different technologies. For soldering, the reduced power-cycling capability of SiC is confirmed. For Cu-sintering, the lifetime is significantly increased and Si and SiC become comparable. The lifetime limit is now the bond wiring on the top side by applying a hard film over the bond wires it was further improved. Both Ag- and Cu-sintering improve the power-cycling capability significantly. For both technologies it was shown that the sinter layer is no longer a lifetime limiting factor.

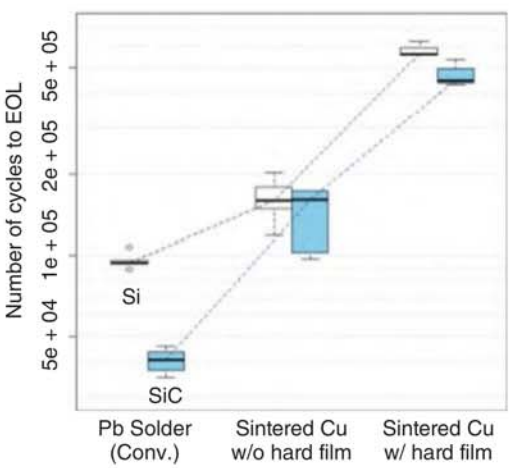


Figure 14.38 Progress in power-cycling capability, comparison of Si and SiC. Test conditions $T_{j,max} = 175\,°C$, $\Delta T = 125\,K$, t_{on} 1–2 seconds. Source: Figure from Yasui et al. [65]. © 2018, IEEE.

14.4.2 Improved Top-Side Interconnections

In the Semikron DPD (direct pressed die) technology, both the bottom-side and the top-side interconnections are executed with silver sintering. On the top side, there is a flexible foil. This allows a narrow distance between the + and − path of the current in a module, and the parasitic inductance can be set very low. In [74], a module inductance of 1.4 nH was achieved. For a complete system including the DC link, the inductance is about 4.5 nH. This compact integration technology facilitates the use of the fast switching capability of SiC devices. The power cycling capability shows a clear progress.

Infineon has introduced Cu bond wires on a top-side Cu metallization of the device. Together with Ag-sintering, it is named ".XT technology." Results of this technology are shown in Figure 14.39.

The power-cycling test in Figure 14.39 was finished because of the test time which took too long. No signs of end of life are visible. The V_F increase remained smaller than 1%.

Cu bond wires require higher ultrasonic power and pressure at the wire-bond process; they cannot be executed on a usual Al metallization layer. To allow Cu wire bonding on devices with Al metallization, a technology to plate the Al with a noble metal and silver sintering to a thin Cu foil was introduced [75], which is named "Danfoss bond buffer (DBB)" or "die top system (DTS)". Cu bond wires are applied on the Cu foil. The technology leads to a significant power-cycling capability. As failure mechanism, cracks in the to-side Al metallization were identified, as shown in Figure 14.40.

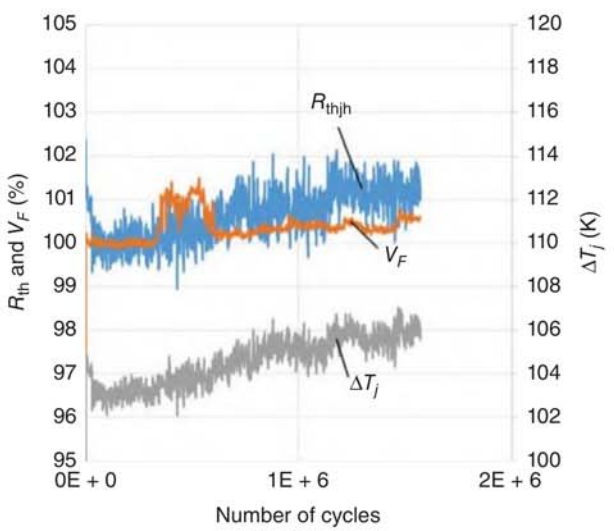


Figure 14.39 Power cycling of SiC Schottky diodes packaged with ".XT technology" – Cu Bonds, Ag-sintering, EasyPACK housing. $T_{j,max} = 150\,°C$, t_{on} 1.5 seconds. Test executed by C. Herold at TU Chemnitz.

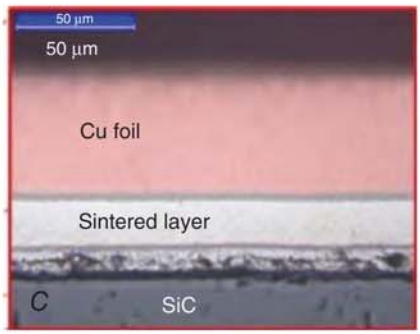
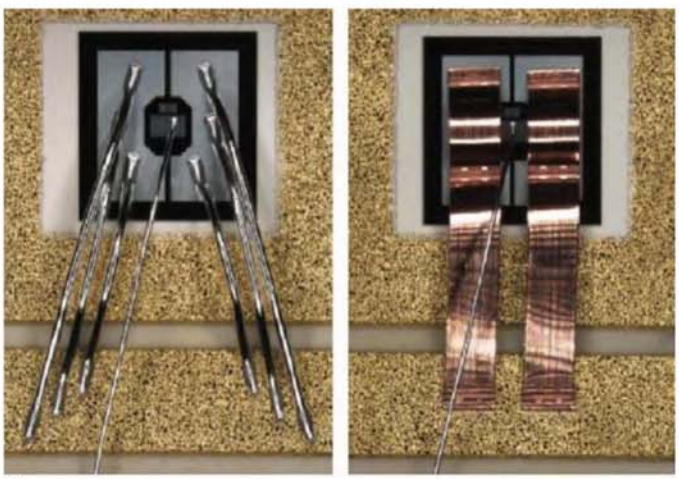


Figure 14.40 Sintered Cu-foil on top of a SiC device. Source: Figure from Streibel et al. [75].



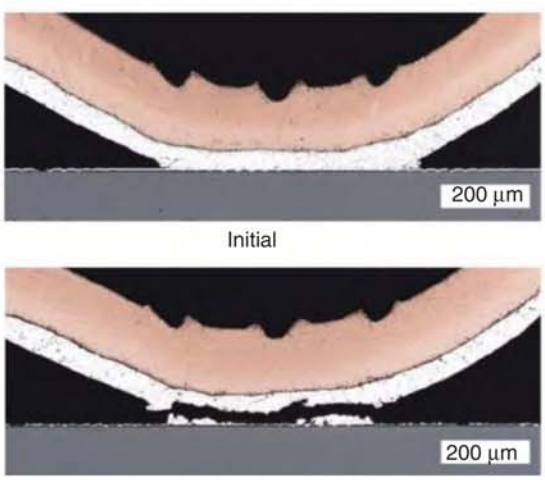


Figure 14.41 AlCu ribbons for possible replacement of Al wires. (a) top view and (b) cross section, showing the lifetime limiting cracks. Source: Figure from Clausner et al. [78].

Cu and SiC show very different CTEs; therefore, work on a 100 µm molybdenum top plate instead of the 50 µm Cu foil is reported in [76]. Molybdenum exhibits a low CTE which is well adapted to the CTE of Si as well as SiC.

Al-cladded Cu bond wires are also possible [77]. A further interesting alternative could be the use of AlCu ribbons [78], where the electrical parameters are dominated by Cu, and the bond process is executed as Al to Al process. Figure 14.41 shows this technology.

For both Al-cladded Cu bond wires and AlCu ribbons, no noble metal surface is necessary and established packaging tools can be used. Power-cycling results for both are only available for Si devices up to now. In both cases, an increase of a factor of 6–10, depending on the conditions, can be achieved compared to the Al bond wire.

In summary, SiC is more challenging regarding packaging technologies. For reliability, similar or higher compared to Si, new packaging technologies are necessary. However, modules with new technologies can achieve a very high power-cycling reliability. The final solutions on the market will be a trade-off between a high lifetime and the production effort/costs.

Acknowledgments

The presented material in the above paragraph, including pictures, was widely supported by several researchers from Infineon and Chemnitz University of Technology, namely, Caspar Leendertz, Rudolf Elpelt, Roland Rupp, Shanmuganathan Palanisamy, Christian Herold, Peter Seidel, and Maximilian Goller.

References

1 Wang, Z., Shi, X., Tolbert, L.M. et al. (2016). Temperature-dependent short-circuit capability of silicon carbide power MOSFETs. *IEEE Transactions on Power Electronics* 31 (2): 1555–1566.

2 Pappis, D., de Menezes, L., and Zacharias, P. (2017). Comparison of the short circuit capability of planar and trench SiC MOSFETs. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, PCIM Europe, 1–9.

3 Bolotnikov, A., Losee, P.A., Ghandi, R. et al. (2019). Optimization of 1700 V SiC MOSFET for short circuit ruggedness. In: *Silicon Carbide and Related Materials*.

4 Lutz, J., Schlangenotto, H., Scheuermann, U., and De Doncker, R. (2018). Semiconductor power devices: physics, characteristics, reliability. In: *MOS Transistors*. Springer.

5 Hofstetter, P., Hain, S., and Bakran, M. (2018). Applying the 2D-short circuit detection method to SiC MOSFETs including an advanced soft turn off. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, PCIM Europe, 1–7.

6 Soltau, N., Thal, E., and Matsuoka, T. (2019). The next generations of SiC power modules. *Bodo's Power Systems*. ISSN: 1863-5598

7 Letor, R. and Aniceto, G.C. (1995). Short circuit behavior of IGBTs correlated to the intrinsic device structure and on the application circuit. *IEEE Transactions on Industry Applications* 31 (3): 234–239.

8 Kampitsis, G., Batzelis, E., Gati, E. et al. (2015). Electro-thermal characterization of 1.2 kV normally-on SiC JFETs under hard switch fault. *2015 17th European Conference on Power Electronics and Applications* (*EPE'15 ECCE-Europe*), 1–9, https://doi.org/10.1109/EPE.2015.7309054.

9 Basler, T., Heer, D., Peters, D. et al. (2018). Practical aspects and body diode robustness of a 1200 V SiC trench MOSFET. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, PCIM Europe, 1–7.

10 Troutman, R.R. (1979). VLSI limitations from drain-induced barrier lowering. *IEEE Journal of Solid-State Circuits* 14 (4): 383–391.

11 Chen, C., Labrousse, D., Lefebvre, S. et al. (2015). Study of short-circuit robustness of SiC MOSFETs, analysis of the failure modes and comparison with BJTs. *Microelectronics Reliability* 55: 5.

12 Fayyaz, A., Boige, F., Borghese, A. et al. (2019). Aging and failure mechanisms of SiC Power MOSFETs under repetitive shortcircuit pulses of different duration. *International Conference on Silicon Carbide and Related Materials*. September 2019, Kyoto, Japan.

13 Reigosa, P. D., Iannuzzo, F., and Ceccarelli, L. (2018). Failure analysis of a degraded 1.2 kV SiC MOSFET after short circuit at high temperature. *2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits* (*IPFA*), 1–5. https://doi.org/10.1109/IPFA.2018.8452575.

14 Boige, F., Trémouilles, D., and Richardeau, F. (2019). Physical origin of the gate current surge during short-circuit operation of SiC MOSFET. *IEEE Electron Device Letters* 40 (5): 666–669.

15 Asllani, B., Morel, H., and Planson, D. et al. (2018). SiC power MOSFETs threshold-voltage hysteresis and its impact on short circuit operation. *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference* (*ESARS-ITEC*), 1–7. https://doi.org/10.1109/ESARS-ITEC.2018.8607547.

16 Peters, D., Aichinger, T., Basler, T. et al. (2018). Investigation of threshold voltage stability of SiC MOSFETs. *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD*), 40–43. https://doi.org/10.1109/ISPSD.2018.8393597.

17 Sadik, D., Colmenares, J., Tolstoy, G. et al. (2016). Short-circuit protection circuits for silicon-carbide power transistors. *IEEE Transactions on Industrial Electronics* 63 (4): 1995–2004.

18 Silber, D. and Robertson, M.J. (1973). Thermal effects on the forward characteristics of silicon p-i-n diodes at high pulse currents. *Solid-State Electronics* 16: 1337–1346.

19 Fichtner, S., Lutz, J., Basler, T. et al. (2014). Electro-thermal simulations and experimental Results on the Surge Current Capability of 1200 V SiC MPS Diodes. *8th International Conference on Integrated Power Electronics Systems*, CIPS 2014.

20 Palanisamy, S., Fichtner, S., Lutz, J. et al. (2016). Various structures of 1200 V SiC MPS diode models and their simulated surge current behavior in comparison to measurement. *28th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD*).

21 Palanisamy, S., Vishwamitra Yoganath, G., Zeng, G. et al. (2019). Temperature determination of SiC MPS diodes during surge current event with measurement and simulation. *Proceedings of the EPE*.

22 Hofstetter, P. and Bakran, M.-M. (2018). Comparison of the surge current ruggedness between the body diode of SiC MOSFETs and Si diodes for IGBT. *CIPS*.

23 Li, H., Wang, J., Ren, N. et al. (2019). Investigation of 1200 V SiC MOSFETs' surge reliability. *Micromachines* 10 (7): 485.

24 Palanisamy, S., Kowalsky, J., Lutz, J. et al. (2018). Repetitive surge current test of SiC MPS diode with load in bipolar regime. *IEEE 30th International Symposium on Power Semiconductor Devices and ICs* (*ISPSD*).

25 Soeiro, T. B., Mengotti, E., Bianda, E., and Ortiz, G. (2019). Performance evaluation of the body-diode of SiC MOSFETs under repetitive surge current operation. *IECON 2019 – 45th Annual Conference of the IEEE Industrial Electronics Society*.

26 GeneSiC datasheet. (2019). GR40MT33N, Rev 1.0.

27 Lutz, J., Schlangenotto, H., Scheuermann, U., and De Doncker, R. (2018). Semiconductor power devices: physics, characteristics, reliability. In: *Destructive Mechanisms in Power Devices*. Springer.

28 Basler, T., Rupp, R., Gerlach, R. et al. (2016). Avalanche robustness of SiC MPS diodes. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, PCIM Europe.

29 Rupp, R., Gerlach, R., Kabakow, A. et al. (2014). Avalanche behaviour and its temperature dependence of commercial SiC MPS diodes: influence of design and voltage class. *IEEE 26th International Symposium on Power Semiconductor Devices IC's* (*ISPSD*).

30 Hatakeyama, T., Watanabe, T., Shinohe, T. et al. (2004). Impact ionization coefficients of 4H silicon carbide. *Applied Physics Letters* 85: 1380–1382.

31 Konstantinov, A., Jinman, S., Young, S. et al. (2015). Silicon carbide Schottky–Barrier diode rectifiers with high Avalanche robustness. *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*.

32 Lutz, J., Schlangenotto, H., Scheuermann, U., and De Doncker, R. (2018). pn-Junctions. In: *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer.

33 Pawel, I., Siemieniec, R., Rösch, M. et al. (2006). Simulating the Avalanche behavior of trench power MOSFETs. *Proceedings of the 8th International Seminar On Power Semiconductors* (*ISPS*).

34 Deng, X., Zhu,H., Li, X. et al. (2019). Avalanche ruggedness assessment of 1.2 kV 45 mΩ asymmetric trench SiC MOSFETs. *Proceedings of ICSCRM*.

35 Wei, J., Liu, S., Li, S. et al. (2019). Comprehensive investigations on degradations of dynamic characteristics for SiC power MOSFETs under repetitive Avalanche shocks. *IEEE Transactions on Power Electronics* 34 (3): 2748–2757.

36 Palanisamy, S., Ahmmed, M.K., Kowalsky, J. et al. (2019). Investigation of the avalanche ruggedness of SiC MPS diodes under repetitive unclamped-inductive-switching stress. *Microelectronics Reliability*: 113435.

37 Berry, A. and Lawson, W. (2019). Defining the ruggedness of power MOSFETs used in repetitive Avalanche for automotive applications. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, PCIM Europe.

38 Konstantinov, A.O., Wahab, Q., Nordell, N., and Lindefelt, U. (1998). Study of avalanche breakdown and impact ionization in 4H silicon carbide. *Journal of Electronic Materials* 27: 335–341.

39 Lee, K., Domeij, M., Franchi, J. et al. (2018). Avalanche rugged low on-resistance 1200 V SiC MOSFETs with long-term stability. *PCIM Europe 2018, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*.

40 Rahman, M. et al. (2004). Super-radiation hard detector technologies: 3-D and widegap detectors. *IEEE Transactions on Nuclear Science* 51 (5): 2256–2261.

41 Albadri, A.M., Schrimpf, R.D., Walker, D.G., and Mahajan, S.V. (2005). Coupled electro-thermal simulations of single event burnout in power diodes. *IEEE Trans. Nucl. Sci.* 52: 2194–2199.

42 Lauenstein, J.M. et al. (2015). Single-event effects in silicon carbide power devices. *NASA Electronic Parts and Packaging Program Electronics Technology Workshop*, https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20150017740.pdf.

43 Normand, E. (2001). Correlation of in-flight neutron dosimeter and SEU measurements with atmospheric neutron model. *Trans. Nucl. Sci.* 48: 1996–2003.

44 Process management for avionics – Atmospheric radiation effects – Part 1: Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment. E DIN EN 62396-1:2010-11 (IEC 107/129/DTS:2010).

45 Dashdondog, E., Harada, S., Shiba, Y. et al. (2017). The failure rate calculation method for high power devices in low earth orbit. *Int. Symp. Space Technology and Science*, 1–5, Matsuyama City, Japan.

46 Weiß, C. (2015). Höhenstrahlungsresistenz von Silizium-Hochleistungsbauelementen. Ph.D. thesis, Munich.

47 Lutz, J., Schlangenotto, H., Scheuermann, U., and De Doncker, R. (2018). Physics, characteristics, reliability. In: *Semiconductor Power Devices*, 2e, Berlin: Springer.

48 Huang, Y., Lechner, B., and Wachutka, G. (2019). Comparative numerical analysis of the robustness of Si and SiC PiN diodes against cosmic radiation-induced failure. *Proceedings of ICSCRM 2019*, Kyoto.

49 Shoji, T., Nishidas, S., Hamada, K., and Tadano, H. (2014). Cosmic ray induced single-event burnout in power devices. In: *Proceedings ISPS*, 5–14. Prague: IEEE.

50 Egawa, H. (1966). Avalanche characteristics and failure mechanism of high voltage diodes. *IEEE Trans. Electr. Dev.* ED-13 (11): 754–758.

51 Scheuermann, U. and Schilling, U. (2015). Cosmic ray failures in power modules – the diode makes the difference. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. PCIM Europe.

52 Felgemacher, C., Vasconcelos, S. A., Nöding, C., and Zacharias, P. (2016). Benefits of increased cosmic radiation robustness of SiC semiconductors in large power-converters. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015. PCIM Europe.

53 Consentino, G. (2015). Are SiC HV power MOSFETs more robust of standard silicon devices when subjected to terrestrial Neutrons? *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. PCIM Europe.

54 Felgemacher, C., Araújo, S.V., Zacharias, P. et al. (2016). Cosmic radiation ruggedness of Si and SiC power semiconductors. In: *Proceedings of the 28st ISPSD*, 235–238. Prague: IEEE.

55 Kaminski, N. (2004). Failure rates of HiPak modules due to cosmic rays. ABB Application Note 5SYA 2042-02.

56 Poller, T. and Lutz, J. (2010). Comparison of the mechanical load in solder joints using SiC and Si Chips. *Proceedings of ISPS*, Prague: IEEE.

57 Oettinger, F.F. and Gladhill, R.L. (1973). Thermal response measurements for semiconductor device die attachment evaluation. *International Electron Devices Meeting* 19: 47–50.

58 Scheuermann, U. and Schmidt, R. (2009). Investigation on the $V_{CE}(T)$-method to determine the junction temperature by using the chip itself as sensor. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. PCIM Europe.

59 Herold, C., Sun, J., Seidel, P. et al. (2017). Power cycling methods for SiC MOSFETs. In: *Proceedings of ISPSD*, 367–370.

60 Unger, C. and Pfost, M. (2019). Determination of the transient threshold voltage hysteresis in SiC MOSFETs after positive and negative gate bias. In: *Proceedings ISPSD 2019*, 195–198. Shanghai: IEEE.

61 Aichinger, T., Rescher, G., and Pobegen, G. (2018). Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs. *Microelectronics Reliability* 80: 68–78.

62 Kimoto, T. et al. (2017). *Understanding and Reduction of Degradation Phenomena in SiC Power Devices*. Piscataway, NJ: Proceedings of IRPS.

63 Ibrahim, A., Ousten, J., Lallemand, R., and Khatir, Z. (2016). Power cycling issues and challenges of SiC-MOSFET power modules in high temperature conditions. *Microelectronics Reliability* 58: 204–210.

64 Schmidt, R., Werner, R., Casady, J., and Hull, B. (2017). Power cycle testing of sintered SiC-MOSFETs. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. PCIM Europe.

65 Yasui, K. et al. (2018). Improvement of power cycling reliability of 3.3 kV full-SiC power modules with sintered copper technology for $T_{j,max} = 175\,°C$. In: *Proceedings ISPSD*, 455–458. Chicago.

66 Herold, C., Franke, J., Bhojani, R. et al. (2016). Requirements in power cycling for precise lifetime estimation. *Microelectronics Reliability* 58: 82–89. https://doi.org/10.1016/j.microrel.2015.12.035.

67 Blackburn, D.L. and Oettinger, F.F. Transient thermal response measurements of power transistors. *IEEE Trans. Ind. Electr. and Control Instrumentation* IECI-22 (2): 134–141.

68 Hoffmann, F., Soler, V., Mihaila, A., and Kaminski, N. (2019). Power cycling test on 3.3 kV SiC MOSFETs and the effects of bipolar degradation on the temperature estimation by VSD-method. In: *Proceedings ISPSD*, 259–262. Shanghai.

69 Herold, C., Schäfer, M., Sauerland, F. et al. (2014). Power cycling capability of modules with SiC-diodes. *CIPS 2014 International Conference on Integrated Power Electronics Systems*, VDE.

70 Yasui, K. et al. (2019). A 3.3 kV 1000 a high power density SiC power module with sintered copper die attach technology. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. PCIM Europe.

71 Mertens, C. and Sittig, R. (2002). Low temperature joining technique for improved reliability. In: *Proceedings of CIPS*, 95–100. Nuremberg: VDE.

72 Amro, R., Lutz, J., Rudzki, J. et al. (2006). Power Cycling at High Temperature Swings of Modules with Low Temperature Joining Technique. In: *Proceedings of ISPSD*. Naples: ISPSD.

73 Konno, A., Andou, T., Morita, T. et al. (2018). Reliability evaluation of sintered metal bonding. *Micro Electronics Symposium 2018*, Japan: Japan Institute of Electronics Packaging.

74 Kasko, I. et al. (2017). High efficient approach to utilize SiC MOSFET potential in power modules. *Proceedings 29th ISPSD*, Sapporo: IEEE.

75 Streibel, A. et al. (2019). Reliability of SiC MOSFET with danfoss bond buffer technology in automotive traction power modules. *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. PCIM Europe.

76 Schuderer, J. et al. (2019). High-power SiC and Si module platform for automotive traction inverter, *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. PCIM Europe.

77 Schmidt, R., Scheuermann, U., and Milke, E. (2012). Al-Clad Cu wire bonds multiply power cycling lifetime of advanced power modules. In: *Proceedings of PCIM Europe*, 776–783. Nuremberg.

78 Clausner, S., Jiang, N., Thomas, S. et al. (2018). Power cycling capability of AlCu ribbons. *Proceedings of the ISPS*, Prague: IEEE.

15

Industrial Systems Using SiC Power Devices

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15.1 Introduction

Based on its unique properties, SiC offers unparalleled opportunities for industrial electronics just the way it does for most medium- and high-power applications. However, individual applications profit in individual ways, and some still existing drawbacks of SiC prevent its advantages from being fully exploited. In other words, the appraisal of potential benefits from SiC devices is necessarily a case-to-case judgement. Nevertheless, the exploitation of the SiC advantages goes along the same few lines for all applications, though to an individual extent. In Figure 15.1, the main lines of benefit are sketched.

15.1.1 Benefits of SiC Devices

Due to the stronger bonds between the atoms in the SiC single crystal, more energy is required to excite electrons from the valence band to the conduction band. That is what has been modelled as the eponymous "wide bandgap."

On the one hand, this means more heat is required to achieve the same intrinsic carrier concentration like in silicon. In SiC, about 600 °C equals room temperature in silicon. Thus, SiC devices inherently have an excellent high temperature capability – at least theoretically. Today, standard packaging materials still prevent true high-temperature applications in the mainstream, while the SiC devices utilised for high-end applications come at a significant premium on the packaging cost. Furthermore, the power cycling capability of SiC devices is lower compared to silicon for the same temperature swing because SiC is much stiffer. This limits the utilisation of higher temperatures because in operation a high peak temperature usually goes together with high temperature swings, which lead to a correspondingly higher level of thermomechanical stress [1]. The same argument limits the reduction of the cooling effort, i.e. simpler or smaller, in any case cheaper coolers, because the reduced cooling would lead to higher temperature swings for the same loss level. Therefore,

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

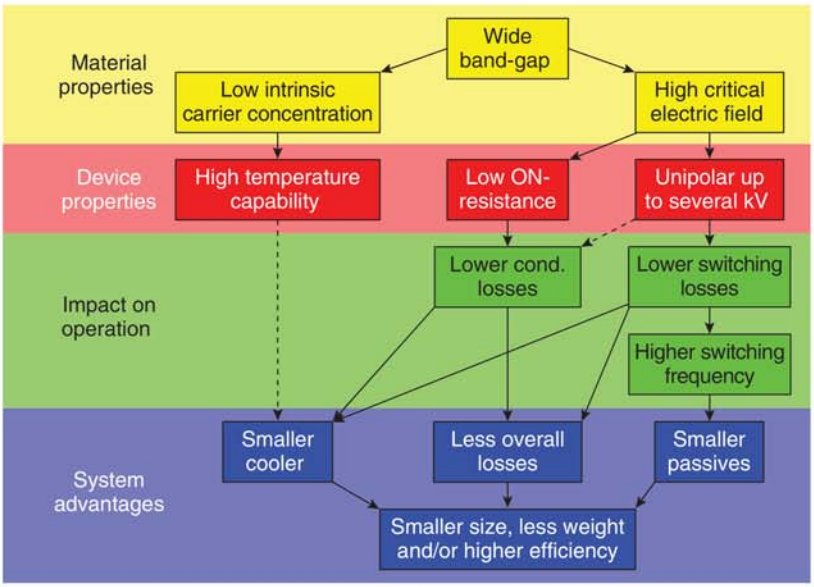

Figure 15.1 Impact of the SiC properties on the system.

the link between high temperature capability and smaller cooler is sketched only as dotted line in Figure 15.1.

On the other hand, a higher electric field is required to accelerate electrons such that they can kick other electrons out of their bonds. The critical electric field, at which this so-called impact ionisation occurs, is in SiC about 10 times higher than in silicon and allows for about 100 times higher doping levels as well as 10 times thinner active layers for a given blocking voltage. Both effects together reduce the series resistance of the active layer in Schottky diodes and metal oxide semiconductor field-effect transistors (MOSFETs) by a factor of roughly 500 at a given breakdown voltage or increase the blocking capability at a given on-resistance by a factor of about 12. Therefore, SiC devices with blocking capabilities exceeding 1 kV can still be unipolar, while in silicon, this is clearly the realm of devices like pin diodes or insulated gate bipolar transistors (IGBTs), which are flooded in on-state with electron–hole–plasma (conductivity modulation) to reduce the series resistance.

While the plasma is an advantage during conduction, its dynamics establish a massive drawback at turn-off. The additional charge causes substantial switching losses when extracted from the device, and the plasma's "inertia" limits the switching speed significantly. From unipolar SiC devices, only the doping charge or "capacitive" charge has to be extracted and the switching speed is no longer limited by the device, but by the surrounding circuitry. Thus, the time at high voltage and high current can be reduced to the nanosecond scale and the switching losses can be factors lower than with the plasma-modulated silicon devices. However, there is a lower barrier for the switching losses of the unipolar MOSFET, which results from the energy stored in the output capacitance. This amount of energy is lost when the MOSFET is turned on again, i.e. once in every cycle.

Furthermore, the injection of electron–hole–plasma requires a forward-biased junction that shows up in pin diodes and IGBTs as a threshold of the well-known 0.7 V before significant current can flow through the device. Of course, this causes additional conduction losses. The SiC MOSFET does not show this issue and has at least at low current density, i.e. under partial load conditions, an additional advantage. Again, the line towards lower conduction losses in Figure 15.1 is dotted because in MOSFETs the advantage is usually compensated by the series resistance towards higher current density and because SiC Schottky diodes do not show this advantage (Schottky barrier) at all. Furthermore, the advantage transforms into a disadvantage for very high-voltage SiC devices. Beyond 10 kV blocking capability, the series resistance in unipolar SiC devices increases to such high values that a plasma flooding is required too. Due to the wide bandgap (WBG), the junction voltage is now about 3 V instead of the 0.7 V [2]. This is the reason why the plasma flooding in SiC makes sense at very high blocking voltages only and has not yet gained any ground in commercial devices. Of course, the bipolar degradation is yet another argument.

Both the lower conduction losses and the lower switching losses have a positive impact on the cooling requirements. Simpler coolers, e.g. air instead of water coolers, or just smaller coolers can be utilised and significant system advantages can be achieved beyond the higher system efficiency. System advantages are anyway a major argument to justify the use of SiC devices.

Due to the more complex manufacturing process, SiC wafers will remain more expensive per area than silicon or GaN on silicon. To a certain degree, this can be compensated by smaller chip sizes sacrificing the on-resistance, but loss density and the necessity to get the current into the chip are limiting the shrinking. Usually, a similar power density will be the guideline for dimensioning, and, thus, for the foreseeable future, SiC chips will remain more expensive per ampere than silicon ones. Consequently, the deployment of SiC devices has to gain system advantages to prevail.

In this context, the low switching losses of SiC devices can help because the switching frequency can be much higher without running directly into a temperature or efficiency problem. At higher switching frequency, the energy, which capacitors and inductors have to store during the shorter cycle, can be proportionally smaller and so can be the volume of those passive components – at least their active volume. Doubling the frequency would reduce the energy storage to half of its original value, size, and hopefully also its cost. Unfortunately and due to e.g. windings, the volume is going down in reality more like with the square root of the frequency [3] not even considering other system constraints. Nevertheless, a substantial system advantage can be achieved.

However, as the switching losses are not zero and anyway limited towards lower values by the capacitive charge that is lost in every cycle, the “affordable” frequency is certainly a trade-off between conduction losses and switching losses. Figure 15.2 gives an idea about the achievable frequencies. The data points show IGBTs and SiC MOSFETs of the different voltage classes. For each data point, the frequency is calculated such that the (hard) switching losses at nominal current and typical direct

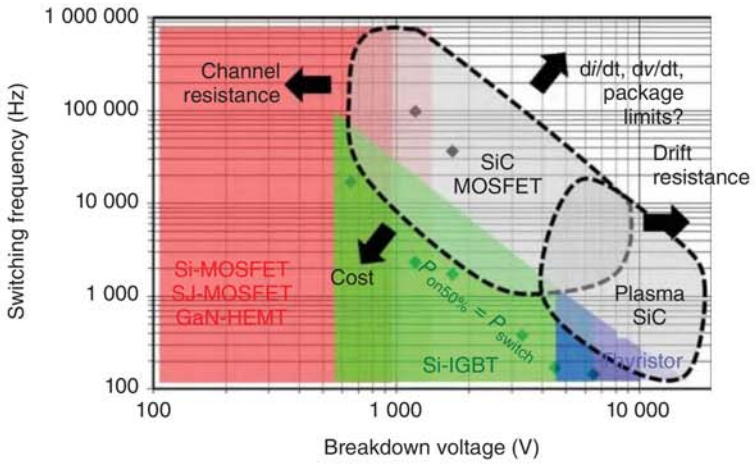

Figure 15.2 Application ranges for SiC devices. Data points are calculated to be the points of equal switching and conduction losses.

current (DC)-link voltage are equal to the conduction losses at nominal current and 50% duty cycle. The shaded area ends where switching losses reach 10 times the conduction losses. In this simple estimation, 1200 V IGBTs can go to 20 kHz, while 1200 V SiC MOSFETs can go all the way up to 1 MHz. However, IGBTs can be optimised for low conduction losses and high switching losses (high plasma concentration for low-frequency applications) or high conduction losses and low switching losses (low plasma concentration for high-frequency applications). Of course, this would change the figure significantly. Furthermore, soft or resonant switching is another factor that changes the loss balance substantially and is not reflected in the figure. After all, the appraisal of potential benefits from SiC devices is indeed a case-to-case judgement.

15.1.2 Competition by Other Technologies

Figure 15.2 also indicates potential limitations or rather competition of the SiC devices. Towards lower frequency, the SiC MOSFET cannot exploit its low switching losses and the silicon IGBT can prevail due to its cost advantage. Towards lower blocking capability, the still high channel resistance of SiC MOSFETs, mainly resulting from the low channel mobility, becomes dominant and limits the overall resistance downwards to about $1\,\mathrm{m\Omega\,cm^2}$ such that devices like the silicon super junction (SJ) MOSFET (currently about $8\,\mathrm{m\Omega\,cm^2}$ at 600 V with prospective $4\,\mathrm{m\Omega\,cm^2}$) or the GaN high electron mobility transistor (HEMT, prospectively $\ll 1\,\mathrm{m\Omega\,cm^2}$) have an edge over the SiC MOSFET in those voltage classes [2]. At really low voltages, even the simple silicon MOSFET is better! Towards higher blocking capability, the series resistance of the SiC MOSFET's drift zone gets too high, so that plasma flooding is beneficial even for SiC and given the junction voltage of 3 V, which has to be overcompensated by less series resistance, before an advantage is achieved. Finally, towards higher frequency, the SiC MOSFET faces

several limitations by the packaging and the surrounding circuitry [1]. All kinds of stray inductances and stray capacitances limit the switching speed, either directly by slowing down the switching process at some point or indirectly by causing oscillations, critical electromagnetic interference (EMI), or instabilities, which can only be controlled by slower switching, i.e. smoother switching transients. In fact, these kinds of package-induced problems are already an issue for silicon devices, and switching slopes beyond 50 or 100 $V\,ns^{-1}$ require better packages than just normal surface-mounted device (SMD) ones. Furthermore, components outside the SiC device might degrade from such high-voltage slopes, with the insulation of the windings of electrical machines being an extreme example.

Thus, the decision to utilise SiC devices is quite complex and can be summarised in Murphy's law for WBG devices: anything that can be made from silicon will be made from silicon, in the most reliable and cost-efficient way. The competition is nicely sketched in Figure 15.3, which locates the various applications in a voltage class vs. power-level diagram (a voltage vs. current diagram would give a similar message). SiC devices will serve the >1000 V and >10 kW applications, and the main competitor in that range is the silicon IGBT. Towards lower voltage and lower power, GaN competes with silicon field-effect transistors (FETs), and as long as the channel resistance is high in SiC MOSFETs, they will face problems there, although the market of 650 V SiC MOSFETs is growing rapidly, with Tesla alone generating a nine-digit Euro revenue with their Model 3 using 650 V SiC MOSFETs. Only the SiC Schottky diodes prevail in this market due to their unipolarity and high-frequency capability, but in some applications, they are already replaced by FETs used as synchronous rectifiers to avoid the diodes' threshold.

The following sections will provide an overview of how SiC can serve different applications and their respective requirements and in which cases competing technologies might offer a better solution. Of course, this work can only outline some general trends. For a wider overview and more details, refer to e.g. [5] and [6].

15.2 DC/DC Converters

It might sound contradictory to consider DC/DC converters as high-frequency systems, but it is absolutely not. In many other systems, the switching frequency is given or at least strongly influenced by the system frequency, while in DC/DC systems, the frequency is a free parameter and is ideally not even detectable outside the DC/DC converter. As discussed in the introduction already, a higher switching frequency increases the switching losses, but it also reduces the required size of the passives, i.e. inductors, capacitors, and filters significantly and might be also beneficial with respect to EMI issues. This way, the system cost can be reduced substantially and the overall system cost can be smaller compared to a silicon-based solution even though the SiC devices are still more expensive. This was already the business case for the first commercial SiC device, the 600-V Schottky diode. In an early application example [7], the cost of a classical boost converter used as the power factor correction (PFC) stage of a switched-mode power supply (SMPS)

Figure 15.3 Application ranges for SiC devices in competition with silicon IGBTs, silicon FETs, and GaN devices. Source: Kinzer and Oliver [4]. © 2016, IEEE.

could be reduced by 9% by going up from 140 to 500 kHz, although the SiC Schottky diode was 2.5 times (5 times per ampere) more expensive than the silicon diode and required a more expensive silicon SJ MOSFET to reach the high switching frequency. This business case paved the way for generations of SiC devices and started the race to make the switching frequency of DC/DC converters as high as affordable, reaching values into the megahertz range. However, in the meantime, the switching frequencies are rather coming down again to values well below 100 kHz. Other improvements, especially on the coils and the control scheme, allow for size reduction such that the extremely high switching frequency is no longer required and can be reduced for the sake of lower switching losses.

In any case, switching frequency of an individual device is not a value by itself but increases the switching losses and might compromise the overall efficiency. Here, the topology the devices are operating in and its control scheme have a massive impact. As an example, Figure 15.4 shows the trends in PFC stages [8], the circuit that allows to draw sinusoidal currents from the grid to avoid harmonic distortion. Today, such circuits are legally required for switch mode power supplies beyond 75 W and for lighting applications beyond 18 W already. One trend is integrating the rectifier bridge into the boost converter ("bridge-less") to reduce the number of diodes in the current path and, thus, to avoid diode on-state losses. Another trend is replacing diodes by switches to avoid the higher losses due to the diodes' threshold voltage. Ironically, this leads to PFC stages without any of the Schottky diodes that started the SiC market [9]. Furthermore, this opens up options on the control scheme. However, the details about continuous conduction mode (CCM), triangular current mode (TCM), boundary current mode (BCM), etc. go beyond the scope of this chapter but have clearly an impact on the performance of the converter and the requirements for the "ideal switch." In fact, the latest topologies use different switches for defining the current path (low on-state required, low switching frequency) and for doing the actual boosting (low switching losses required, high switching frequency) and the frequencies range from a few 100 kHz up to about a megahertz.

As indicated in Figure 15.4, the optimum device for the bridge-less PFC is not necessarily an SiC MOSFET. In the 600-V class, several other device options are available: GaN HEMTs, silicon SJ MOSFETs, or, in some cases, even silicon IGBTs. With respect to the technology, the 600-V class is, thus, the most competitive market. In this application range, the device properties have to perfectly fit the requirements of the topology, and a little drawback in one parameter might make the competing device better suited already – and prevailing. An overview of the latest devices and the applications they are best suited for is given in Figure 15.5. Depending on the specific application, different figures of merit (FoM) are decisive and the overall cost is anyway giving a strong bias towards silicon solutions. Thus, 600 V is a difficult battle ground for SiC, and only a few applications are clearly suitable.

One of those suitable applications is the DC/DC converter with galvanic insulation, which is usually the main stage behind the PFC in an SMPS. The galvanic insulation is provided by a transformer, and on the primary side, one or more switches generate a high frequency input, while on the secondary side a

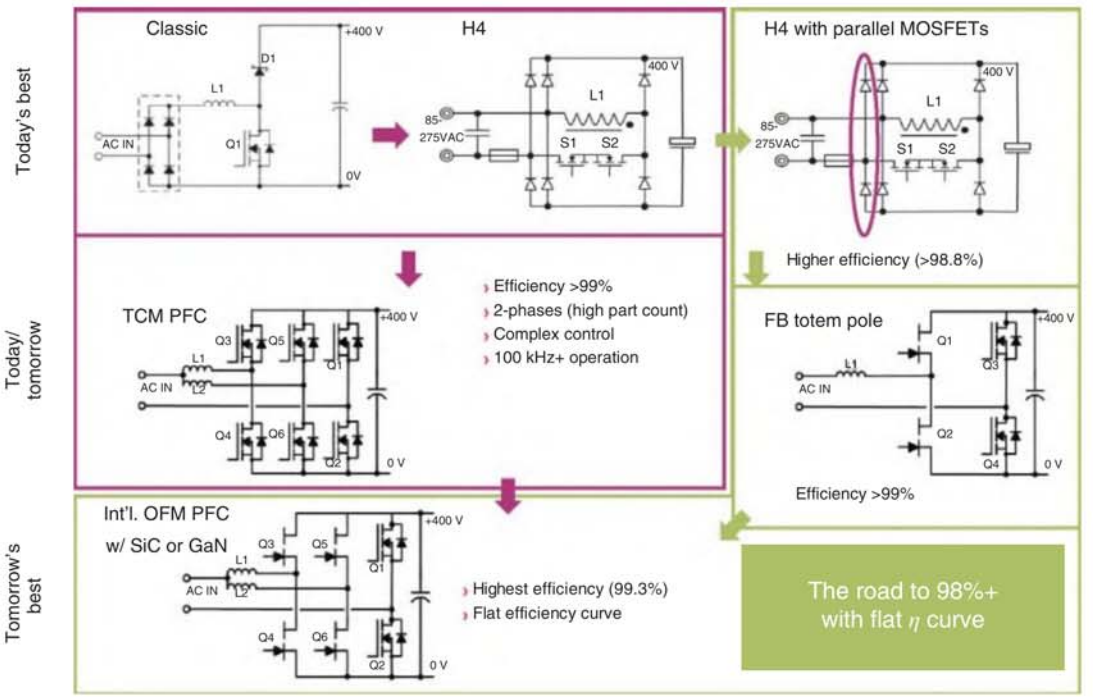

Figure 15.4 Trends in bridge-less power factor correction (PFC) stages. Source: Deboy et al. [8]. © 2016, IEEE.

Device	$V_{(BR)DSS}$ (V)	$R_{DS(on)}$*Q_{rr} (mΩ * µC)	$R_{DS(on)}$*E_{oss} (mΩ * µJ)	$R_{DS(on)}$*Q_g (mΩ * nC)	$R_{DS(on)}$*Q_{os} (mΩ * µC)
CoolMOS™ 7	600	100%	100%	100%	100%
CoolMOS™ 7–fast diode	600	10%	104%	108%	104%
CoolGaN™ Gen 1	600	0%	84%	6%	13%
CoolSiC™ Gen 1	650	2%	133%	41%	21%

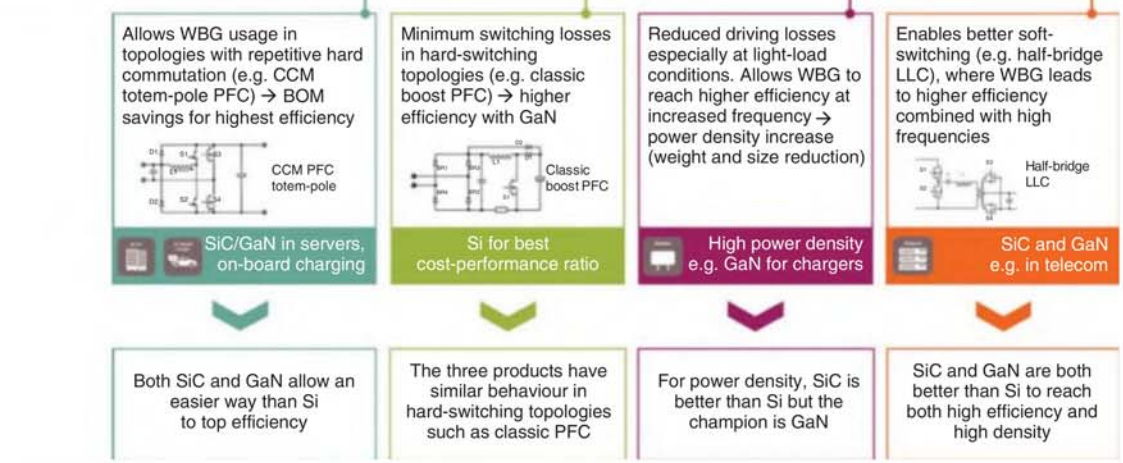

Figure 15.5 Technology comparison between silicon, SiC, and GaN devices. Source: Courtesy of Infineon.

rectification is provided. For low power, flyback converters as the simplest variant with only one switch, recently preferably extended to resonant mode, or forward converters as the more efficient variant were utilised for insulated DC/DC conversion. For higher power, the main stream is feeding the transformer by a half-bridge or a full-bridge topology [9, 10], which generate the high-frequency input. Again, the higher the frequency is, the smaller the transformer can be. To be even more efficient, the primary side can be extended by an inductor and a capacitor to form a resonant system and to operate in soft switching mode. This is then called the LLC topology and is the main stream for highest efficiency. On the secondary side, the rectifier can be a simple diode bridge or an active half or full bridge. The active bridges are more efficient and offer more functionality, in particular energy can also be fed back to the primary side. Of course, active bridges are also more expensive. A schematic is shown in Figure 15.6 as the inner part (between the capacitors) of a power electronic traction transformer (PETT) cell.

Such LLCs operate at frequencies from a few 10 kHz to beyond a megahertz [13], and they are suited for a wide range of applications. At the 600-V class, GaN constitutes a strong competition, but as soon as the voltage or power level increases, SiC has an advantage. Examples are the auxiliary power supply in trains [14], with 99% efficiency (96% for the entire AC/AC system) at 50 kHz and 1200 V MOSFETs or 6.6 kW electric vehicle (EV) chargers [13], with 98% efficiency at 625 kHz and 650 V MOSFETs. However, it becomes really exceptional, when 10-kV SiC MOSFETs are used to supply 25 kW to 400 V (e.g. data centres) directly from a 7-kV DC source [15]. The converter operates at 48 kHz and has a measured efficiency of 99% with 99.2% easily achievable by using different SiC devices on the secondary side. In such applications, admittedly a niche yet, no other technology can rival SiC performance – except from the good old transformer and its unbeatable reliability, which is pivotal in data centres, no matter if that comes at the price of lower efficiency. After all, there are several DC/DC applications in which SiC can excel, and the market perspective looks great over the entire range of voltage classes.

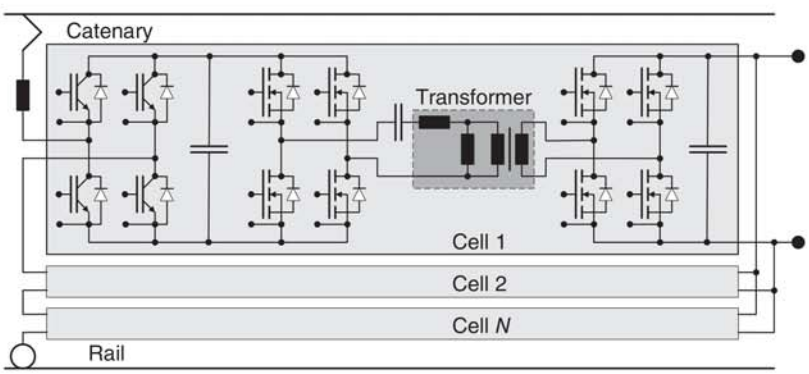

Figure 15.6 PETT topology according to [11, 12], with the primary-side low-frequency AC/DC converter equipped with an IGBT full bridge and the high-frequency DC/DC converter equipped with SiC MOSFET full bridges.

15.3 Solid-State Transformer (SST)

The basic idea of the solid-state transformer (SST) dates back to the late 1960s and is all about replacing a bulky, inefficient low-frequency transformer by a smaller, lighter, and more efficient transformer operating at significantly higher frequency [16]. Obviously, those advantages come at the extra effort to generate a higher frequency input for the transformer from the low-frequency supply. The extra effort on the secondary side depends a lot on the load to be supplied and might be even smaller in case it is just a rectification. After all, the SST is a kind of a high-power variant of the SMPS and the variety of topologies has become similarly diverse.

The main differences between the topologies occur on the primary side and concern the way of how the higher frequency is generated. The original way is direct conversion by chopping the low-frequency AC such that a higher frequency AC results. This is a single-stage process with low losses but causes a lot of harmonics. The alternative way is to rectify the low-frequency AC first and then generate the higher frequency AC from the resulting DC-link. Although this is a two-stage process with respective losses and requires a DC-link, the design freedom in the second stage due to the decoupling by the DC-link is dominant and allows for a much better system.

To reduce the switching losses, resonant or soft switching can be applied instead of the hard-switching mode. The semiconductors switch at a moment without a voltage drop across them or without a current flow through them and, thus, the switching losses disappear – at least under ideal conditions. In fact, the control of the current waveform is usually even more sophisticated [11] and opens the path to even higher frequency without the disadvantage of reduced efficiency and is, thus, widely deployed.

The third difference is how the high voltage is applied to the primary side. Is the full voltage applied to a single transformer, or is a series connection of lower voltage SSTs connected to the high-voltage mains and then connected in parallel on the secondary low-voltage side? A third, yet rarely used alternative is deploying a modular multi-level converter (MMC or M^2LC, cf. Section 15.8.1) on the primary side, which resembles a distributed DC-link.

SSTs are a combination of these three properties, and it depends a lot on the particular application, i.e. voltage level and frequency of the mains, which variant is best suited. The fields of traction and smart grids will be discussed in the following sections.

15.3.1 Traction

Maybe the most obvious application for an SST and the first one realised is replacing the bulky low-frequency main transformer of a train. This is particularly valuable in Germany, Switzerland, Austria and parts of Scandinavia, where the AC voltage of the catenary is 15 kV at a frequency as low as 16.7 Hz. In those cases, the SST can reduce volume and weight substantially and can go under floor or on top of the roof of the train to free up space for passengers. Furthermore, a substantial efficiency

improvement can be achieved and functionalities are available that go far beyond a simple transformer.

An example of such an SST for traction applications is shown in [9] under the name of PETT. Whereas the early SSTs for traction were based on thyristors and increased the frequency to only 400 Hz, the PETT used 6.5-kV IGBTs and the transformer frequency went up to 1.75 kHz (thermally limited). To cope with the peak voltage of $15\,\text{kV}\cdot\sqrt{2} = 21.2\,\text{kV}$ (plus fluctuation margin), the PETT used an input series output-parallel (ISOP) topology with 9 SSTs (one for redundancy) of 150 kVA each, giving a total power of 1.2 MVA. The topology also used soft switching to reduce switching losses with zero voltage at turn-on and low current at turn-off. In total, the efficiency of the prototype achieved 96% (98% for the DC/DC converter part), which is 2–4% better than with the traditional solution, while the power density went up as well as the weight went down by a factor of more than two.

Although this is quite a progress over the traditional technology already, SiC can further improve the PETT. This potential step forward is documented, e.g. in [11] on a PETT designed for 25 kV and 50 Hz (catenary in western and eastern Europe). It has quite a similar topology based on soft switching like the previous PETT but uses 3.3-kV SiC MOSFETs and has a much higher transformer frequency. In fact, the ideal frequency is no longer determined by the semiconductors and their losses but by the transformer properties and the exact control scheme. For the DC/DC "converter part", efficiencies of well above 99% at frequencies between 10 and 20 kHz have been achieved.

Obviously, the PETT is a promising field of application for SiC devices and an attractive market. However, the reliability of the bulky and lossy low-frequency transformer is unbeatable and, given the worldwide efforts to improve dependability of the train service, the train operators will not accept higher failure rates due to the PETT. Thus, a special focus has to be on the PETT's reliability, if necessary by means of redundancy as demonstrated in the early PETTs already.

15.3.2 Power Grid

Although in both cases the grid frequency is low, the situation of an SST in the power grid is obviously different from the PETT. While high efficiency and reliability are extremely relevant for both applications, volume and weight are of less concern for a grid transformer and a conventional high-power transformer can already reach an efficiency of 99% and above [17]. Here, it is more the additional functionality or controllability that makes the SST superior to the conventional transformer. Typical examples are phase shift, voltage regulation, or control of reactive power as it is required, e.g. in grids with a strong feed-in of renewable energy. Thus, the SST is usually quoted together with the smart grid, and the goal is a smart transformer without sacrificing efficiency too much. However, some of the control features like the voltage regulation can be achieved by mechanical tap-changers or power electronics processing only a smaller fraction of the power [17]. Furthermore, the SST is not a drop-in replacement for conventional transformers because the protection schemes are incompatibly different. Thus, the grid concept has to be reconsidered

anyway, and in the future, some of the controllability features might be taken over by the increasing number of feed-in inverters themselves. Thus, the SST in power grids does not look like an attractive market for any kind of semiconductors, though SiC would bring the technology closer to the efficiency benchmark set by the conventional transformer. However, the situation looks better if the SST is not connecting two AC grids (of the same frequency) but is feeding a DC grid from an AC grid (cf. Section 15.7), i.e. there is no secondary inverter, while the conventional transformer would require the rectification step.

15.4 Wireless Charging

Due to the air gap of a few centimetres or even beyond 10 cm required for practicability, the vast majority of wireless charging systems, especially in the high-power range relevant for the application of SiC devices, is based on inductive coupling and, thus, is usually called inductive power transfer (IPT) [18, 19]. Such a system can be considered a galvanic insulated DC/DC converter or SST using a high-frequency transformer, which can be split in two parts such that the primary and the secondary side of the system can be separated. Indeed, creating the transformer from two independent and in-field service not necessarily well-aligned coils introduces a number of restrictions for the charging system, concerning the design of the coils and the core, the material selection, EMC regulations, and particularly safety [20]. It is getting even more challenging if the secondary side is moving while charging like in case of trains [21, 22] or cars [23] or if harsh conditions like snow or (even ferromagnetic) debris compromises the transmission [24]. But even if the EV is at rest in its protected garage or the tram has a stop at a clean station, the charging system has to cope with varying system properties, i.e. changing coupling, parasitics and resonances, which requires an adaptive or resonant network or an even smarter control. Consequently, most of the specific work has been done on the coils and the control, which goes clearly beyond the scope of this chapter.

The rest of the IPT system, in particular its topology, is pretty much the same as an SST, though the IPT has sometimes a three-phase design [22]. However, there is some impact on the rest of the system as well and the most striking is the still much lower efficiency than the 99% achieved in galvanic insulated DC/DC stages or the only slightly lower values of a complete SST. A silicon equipped 1 MW system feeding in to a 2.8-kV busbar of a high-speed train shows 82.7% efficiency at a frequency of 61.5 kHz [21] and the 50-kW system feeding into the 800-V busbar of a tram shows 88% efficiency at only 25 kHz [24]. Because the coil system is the main issue, moving to SiC is indeed improving the efficiency of the semiconductors but has only little impact on the overall efficiency of the IPT system and mainly academic work has been done [25, 26]. However, a higher frequency also provides more freedom in the coil design and helps to improve the power transfer over the coil system [27]. At the 85 kHz, the Society of Automobile Engineers (SAE) Standard J2954 is going to ask for, SiC becomes inevitable for high-power systems with, respectively, high DC voltages. An example is reported in [27], where a 50-kW all-SiC system for up to

800 V on both sides showed a DC-to-DC efficiency of 95.8% and a power density of 9.5 kW dm^{-3}. Apparently, also system advantages like reduced size or reduced cooling effort on board or at stations, i.e. remote locations, might justify the utilisation of SiC components already. Given the potential number of systems, this might become an interesting application for SiC devices.

15.5 Inductive Heating

15.5.1 Domestic Systems

One could think of an induction heating system as a wireless charging system with the secondary winding being permanently shorted by an ohmic resistor converting the transferred energy into heat. But depending on the exact application, there are substantial differences. The well-known induction cookers at home operate in the frequency range above 25 kHz to avoid audible noise, but usually also well below 50 kHz to keep switching losses low. This rather low frequency requires the use of ferromagnetic cookware, which has a rather high resistivity to generate sufficient ohmic heat out of the induced eddy currents and which adds additional heating (about one-third of the total heating) due to hysteresis loss in the cyclic reversal of the magnetic field. Such frequencies can still be handled by silicon (reverse conducting) IGBTs optimised for soft switching and operated e.g. in a single-ended quasi-resonant topology [28]. Thus, SiC devices can indeed improve the efficiency of induction cookers [29], but due to the higher cost and due to the anyway dominant induction coil losses, SiC devices are not yet widespread in this application. However, given the large number of cookers in the world, SiC devices envisage a large potential market once the device cost is coming down – and if GaN devices are not providing superior solutions. GaN devices might also be the strongest competition in the trend towards all metal (e.g. aluminum, copper, or even multi-layer) capability, which requires frequencies up to the megahertz range [30]. However, due to the increasing coil losses, the overall efficiency would not profit significantly and also the trend towards areal induction or flexible cooking surface [30] is neither fostering SiC application nor is improving overall efficiency.

15.5.2 Industrial Systems

Industrial heating systems are different not only in power level, from a few kilowatts to several megawatts, but in some cases also in frequency, from 500 Hz to some megahertz. The frequency is in general dependent on the application and on the material to be heated. Melting and forging require very high power (several megawatts and very low frequency in the range of 0.5–5 kHz), while brazing, surface hardening, and induction shrink fitting [31] require frequencies in the range of 10–100 kHz and tube welding requires very high frequency and power (150–400 kHz and 0.2–2 MW). In medical systems, the frequency is usually even higher with some systems going far beyond 1 MHz [31]. The IGBT can be applied up to about 100 kHz if operated

in a resonant circuit [32] and can go beyond only if several IGBTs are working in parallel in an interleaved mode [32], i.e. distribute the losses by reducing the duty cycle for an individual device. Higher frequencies beyond the reach of IGBTs used to be the realm of the silicon MOSFET for its low switching losses. However, the high conduction losses especially at higher voltage levels and the anyway increasing switching losses establish a limitation for the frequency and to rather low efficiency. Here, the SiC MOSFET can achieve a massive improvement. On the one hand, the efficiency can be higher, especially when operated in zero-voltage switching (ZVS) and reduces the operational expenditure in terms of energy consumption and cooling effort [32, 33]. On the other hand, the number of devices, i.e. total chip area, can be much smaller and compensates for the higher cost of SiC devices per chip area. This effect is even boosted by the reduced cooling effort, reduced occupied space, and smaller driving circuitry, which can already now lead to a system advantage and reduced capital expenditure [32]. However, the mission profile of induction heaters has often a stop-and-go characteristic and would require a high power-cycling capability, which is still a challenge for SiC devices if not counterbalanced by the usually lower temperature swings or more elaborate assembly technologies. Together with the reduced number of devices, even an improved reliability is predicted and would reduce operational expenditure even further. Based on all the advantages mentioned earlier, industrial or medical induction heating seems to be a promising, though small market for SiC devices. An example of a novel SiC-based technology for induction heating converters is shown in Figure 15.7.

15.6 Photovoltaic

15.6.1 Residential Systems

A simple PV inverter for residential systems (<10 kW) is a two-stage system with one (or more) boost converter and maximum power point (MPP) tracker in the first stage (Figure 15.8a) feeding a DC-link capacitor. For this stage, the advantages for DC/DC converters apply, i.e. increasing the frequency would allow for shrinking the coils and capacitors. However, for cost and loss reasons, residential systems tend to be transformer-less and the DC-link voltage for direct grid connection has to be at least slightly higher than the 325 V peak value of the 230 V_{RMS}. Usually, the window for the DC-link voltage is 350–500 V, but can go up to 600 V under some operation conditions. In that case, silicon SJ MOSFETs or rather silicon IGBTs are good enough (antiparallel diode operation not required) and cheaper, while the free-wheeling diode is indeed preferably a unipolar SiC Schottky diode for their low conduction losses and very low switching losses as well as the low stress it imposes on the switch due to the missing reverse recovery peak. The switching frequency is, however, usually not much higher than 50 kHz. The case for SiC switches is getting even weaker, if the first stage is composed of series connected DC/DC converters of even lower voltage. Here, silicon is clearly advantageous and GaN might offer an even superior solution. However, such topologies are yet irrelevant.

Today's IH converter technology	The SiC inverter	Technological improvements	Benefits to the customer
Mostly Si (IGBT/MOS) technology	SiC technology	Efficiency improvement to 99.5%	Less OPEX, due to lower electricity and cooling water consumption
Power module technology 	Discrete devices technology 	Lower stray inductance Higher efficiencies Higher frequency range No complex control strategies	Cost reduction Lower electricity consumption Lower cooling water consumption
Electrolytic or film caps technology 	Antiferroelectric ceramic capacitor technology 	Allows significant size reduction	Less industrial space requirements Converter easy handling
Distributed converter architecture (power section, controller, sensing circuits... in different blocks that have to be cabled)	Embedded or semi-embedded converter architecture 	Automatized production Production costs reduction Size reduction Production stability Improvement of reliability	Significant cost reduction Allows significant size reduction Less OPEX, due to higher reliability
Single power port converter architecture	Universality: multi power port technology	Improves usability of the converter	Allows different IH applications with a single converter
Analogue or digital controller	Cyber-physical controller 	Advanced process features Remote FW/SW updating Preventive and predictive maintenance	Converter set-up time reduction Lower OPEX Allows a user friendly use of the converter
Conventional mechanical architecture	Mechanical Plug & Go technology		Allows a very fast substitution of a power converter in the case of failure

	Standard tech.	New tech.	Reduction
Size (mm)	450 × 200 × 750	210 × 300 × 25	
Volume	70 l	1.5 l	98%
Power density	1.4 kW/l	65 kW/l	
Weight	50 kg	2.5 kg	95%
kW/kg	2 kW/kg	20 kW/kg	
Efficiency	98%	99.1% @ 400 kHz	

Figure 15.7 Advantages of a novel SiC-based technology for induction heating converters and improvements achieved with a 100-kW system. Source: Courtesy of SiCtech Induction, Valencia.

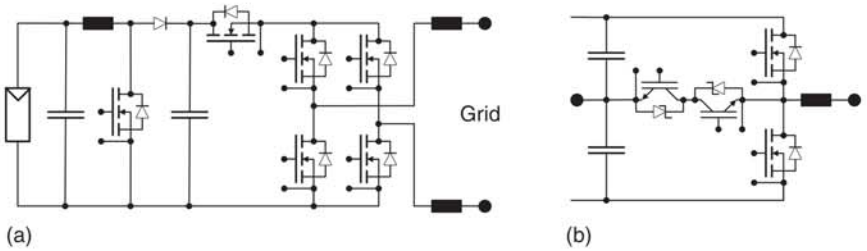

Figure 15.8 (a) Transformer-less single-phase PV converter with an H5 topology on the inverter side to cope with capacitive ground currents. Such converters are usually equipped with silicon IGBTs, but here SiC MOSFETs are shown as proposed in [34]. (b) Advanced T-type NPC hybrid (silicon/SiC) phase leg for a three-phase inverter [35]. Source: Based on Saridakis et al. [34], (b) Freiche et al. [35]. © 2017 VDE-Verlag.

The low DC-link voltage has also an impact on the second stage, i.e. the grid-connected inverter. Based on the feed-in tariffs, lower conduction losses pay back directly, while higher switching frequency has only an indirect advantage. Because the grid has a fixed frequency of 50 or 60 Hz, the higher frequency only helps to reduce the DC-link capacitor and the main line choke or filter size and their cost. This system advantage would compensate at least partially for the higher cost of the SiC components, but at the same time higher switching frequency increases switching losses and reduces efficiency again. Thus, there is a small window for overall optimisation, and the switching frequency of the inverter is usually not even close to the 200 kHz "optimised" for SiC in [34] reaching overall peak efficiencies exceeding 99%, a value that had been achieved with early commercial SiC switches already [36].

However, PV inverters based on silicon devices are already quite efficient as well and offer peak efficiencies of more than 98% or even beyond 99%, the latter admittedly at a substantially higher part count and higher cost [37]. Thus, the higher cost of SiC converters is paying back over time only slowly by feeding in less than 1% more energy. Consequently, market penetration of SiC-equipped inverters is still low, i.e. awaits cost reduction of SiC components due to economy of scale without contributing to the scale. At the same time, GaN makes significant progress and might be the better alternative for residential systems in the long run, especially at lower mains voltage.

15.6.2 Commercial, Industrial, and Utility Size Systems

For larger systems, the situation is different, as the power is too high to be fed into the single-phase mains. Instead, a three-phase connection is required, which results in more components in the inverter. At least, the MPP trackers remain the same, though they are operating at higher voltage and might be more numerous. Furthermore, capacitive currents towards ground potential are easier to control in a three-phase system. Again, SiC has a positive impact on the losses, but the overall optimum including cost and system benefits might lead to other solutions. An inverter leg of one advanced solution [35] is shown in Figure 15.8b. Here, the phase

leg of SiC MOSFETs is supplemented by an active so-called T-type three-level neutral point clamp (NPC), consisting of silicon IGBTs and SiC Schottky diodes of half the rated voltage. With the additional output level, the voltage and current waveforms are improved and additional system benefits can be achieved. In other words, a full SiC solution is not necessarily superior.

For even larger professional systems, the DC-link voltage is not directly coupled to the mains voltage because the power has to be fed in at the medium voltage level (10/20 kV or higher), which requires a transformer anyway. However, to profit from the relaxed low voltage regulations inside the solar park, the peak voltage has to observe the 1000 V limit and, thus, 1000 V_{DC} and 400 V_{RMS} (Europe) or 480 V_{RMS} (United States of America) including safety margin used to be the typical voltage levels from the MPP trackers to the inverters and from the inverters to the transformers, respectively. At these voltage (and power) levels, SiC starts to have a clear advantage over competing technologies and the trend is going towards even higher voltage like the new 1500 V standard for the DC level inside the solar park because at higher voltage, cost is reduced for the DC cabling [38]. Unfortunately, 1500 V requires series connection of semiconductors or more sophisticated topologies like three-level NPC or the modern ANPC both with inherent series connection because neither silicon IGBTs nor SiC MOSFETs with the required blocking capability of about 2.5 kV exist due to the lack of other applications requiring this voltage class (only recently 2.3-kV IGBTs were announced [39]). Nevertheless, due to reduced passives and cooling effort, the system cost for a 150-kW 1500 V_{DC} SiC inverter can already be lower than with silicon alternatives [40], and further advantages like a higher reliability due to lower part count of the then simpler converter might come on top [41, 42]. Thus, medium- and large-size solar inverters are an attractive and substantial market for SiC components and, after all, could become a driving market for the SiC technology.

However, the exact system layout of a solar park is another important consideration and defines the power level of the individual units. In fact, the MPP tracking and the voltage boosting can be done for an individual string or for several strings (decoupled by diodes) together. Likewise, a single centralised inverter can feed in the entire power or several smaller inverters can share the job. On the one hand, a single inverter is better for averaging (over load) and reliability (less components) reasons, but, on the other hand, a bit of redundancy is also good, and doing the MPP tracking individually might be advantageous as well. For commercial and industrial systems into the megawatt range, something in between with one inverter per a few string MPP trackers seems to be the optimum [43] and can be served with the SiC converter mentioned earlier [40]. On the contrary, for utility scale systems in the multi-megawatt range, usually all strings are connected together and a single inverter also taking over the task of MPP tracking feeds in the entire power – through the directly attached medium voltage transformer. This gives the lowest system cost, and individual MPP tracking is not required because the stings are very homogeneous anyway (similar solar radiation, no shadowing, same temperature). Unfortunately, for SiC that means that the power level is yet too high. However, that will change over time and, thus, SiC is supposed to excel in larger solar parks, too [44, 45].

15.7 DC Grids

In solar parks, the DC cabling is neither exactly DC nor a grid with potentially bidirectional current flow because the cables are a number of point-to-point connections between the strings and their respective MPP trackers or from decoupled stings to the central MPP tracker. A true DC grid is not beneficial here because it would require a decentralised MPP tracking with many satellite installations. Furthermore, a single failure would trip the entire solar park or a number of DC breakers would be required to handle such cases, introducing more complexity and more conduction losses. However, there are cases in which DC grids indeed make sense.

15.7.1 Low- and Medium-Voltage DC Grids

One classical, though small, example is the shared DC-link for drives. In case, there are inverters, which are mainly taking out energy from the DC-link, and others, which are mainly feeding energy back, the shared DC-link is equalising the fluctuation and only the net energy consumption has to be replenished by the mains via the rectifier stage. The benefit over individually AC-coupled converters originates from the reduced number of conversion stages for the recovered energy, i.e. one inversion and one rectification less, and also the grid coupling can be a simple bridge rectifier.

This example shows a typical finding when considering DC grids or DC microgrids. The systems profit most, when loads and local feed-in are similar, i.e. the system has a low net consumption, and equalisation is done inside the grid. Then the power conversion losses are smaller and overall efficiency is increased [46]. Typical examples could be residential or commercial buildings with PV systems and battery storage. As this advantage is purely due to the structure and operation of the microgrid, the improvement by utilising SiC components is limited to the efficiency increase of the individual conversion stages, as discussed in Section 15.2, with the DC voltage level as the main driver for the case of SiC. In fact, there is no ideal voltage level as many loads are at 5, 12, 24 and 48 V, respectively, while high-power load requires a higher voltage level like 380 V, and the installation would have to provide two or more levels maybe even mixed with the traditional AC [47]. This would require many rectifiers/inverters or DC/DC converters, most of them operating in partial load, which compromises the overall efficiency. Nevertheless, SiC components could improve the efficiency of some of the individual converters and will be widely used once the cost has come down. However, advanced designs allow for reduced system cost in the kilowatt range already ([48]: 5 kW, 50 kHz, 99% peak efficiency) and should boost the utilisation of SiC devices for microgrid applications.

A completely different kind of DC grid is found in data centres. Those grids are almost entirely traditional distribution grids with solely top-down power flow from the mains in tree-like structures to the individual computers, with decreasing voltage levels. The efficiency is better than in the microgrids because large-size central inverters can be used. However, the number of DC/DC conversion steps and the individual efficiency of the steps define the overall efficiency, with the lower steps clearly unsuited for the application of SiC devices. For the higher steps, SiC technology

is indeed well suited and, given the high utilisation of the equipment, even small efficiency improvements will save substantial energy justifying the higher cost of SiC devices, if the system advantages are not sufficient already. However, an even bigger step forward would be reducing the number of steps. A good example is an SST supplying 400 V directly from the medium-voltage mains; in this case, 3.8 kV_{RMS} via a 7-kV DC-link utilising 10-kV SiC MOSFETs [15]. Although this is an exotic application, yet it could be a promising application for very high-voltage SiC devices.

15.7.2 DC Breakers

The systems discussed in the previous section were either small and very local or had unidirectional power flow. Nevertheless, already in this case a protection scheme is required to disconnect a defective part and keep the rest of the grid operational. The protection scheme is getting even more important in case of larger and meshed grids [49]. Fuses and electromagnetic circuit breakers are the traditional components, but they cannot be reset electronically, they need the capability to extinguish the arc without the zero-crossing missing in DC, and their reaction time in the milliseconds range is rather slow. In fact, a protection scheme needs to be quick in case the short circuit is low inductive and the current is rising quickly but needs also the capability to dissipate high energy in case the short circuit is high inductive. Semiconductor-based solutions are the method of choice to achieve short tripping times and a number of solutions have been proposed, mainly with differences in their triggering mechanism [50–52]. In those circuit breakers, SiC switches, ideally normally on devices, can only utilise their low on-resistance, while the switching speed is more than sufficient with any semiconductor solution and the switching losses are no longer determined by the semiconductor itself. However, semiconductor solutions can be designed to offer additional features like soft start or current limitation, to cope with inrush currents during start up [53, 54]. This can be a useful system advantage because then the individual loads do not need this feature anymore. However, the main challenge for semiconductor-based solutions is the vast amount of energy, which needs to be dissipated in worst case and which is dissipated in the arc of mechanical switches. Even for the most robust silicon-IGCT-based solutions, the energy is too high to be dissipated in the semiconductor [55] and has to go somewhere else. For SiC devices with their smaller device volume, the energy, which can be dissipated, is even smaller. Usual approaches are RCD snubbers, transient voltage suppression (TVS) diodes, or metal-oxide varistors (MOVs) [49].

15.8 High-Voltage DC (HVDC)

15.8.1 HVDC Transmission

Today, high-voltage DC systems are still predominately point-to-point transmissions, although multiterminal installations exist [56, 57]. The DC voltage level of such high-voltage direct current (HVDC) systems is mainly determined by the insulation

capability of the transmission line, i.e. cables or overhead lines, and goes beyond 1 MV vs. ground in some installations already [56, 57]. The blocking capability of the individual semiconductor devices is rather a free parameter because the extremely high-voltage levels require massive series connection anyway. In thyristor-based line commutated converters (LCC), the blocking capability ranges up to almost 10 kV because the switching losses are low and the thyristors can be optimised for low conduction losses. In the IGBT-based self-commutated voltage source converters (VSC), the switching losses in two-level topologies are substantially higher and the trade-off between conduction and switching losses led to lower blocking capabilities of the IGBTs like 2.5 kV. Nevertheless, the converters suffer from higher overall losses and were installed only in cases of a weak grid on one side, e.g. land connections of off-shore wind parks, or in cases of black-start capability was required. In all other cases, especially in bulk power transmission, the more efficient thyristor-based converters were deployed. In none of the cases, SiC devices would have been an (economically) viable alternative, if they had been available at the time.

However, the introduction of the modular multi-level converter (MMC or M^2LC) [58] changed HVDC completely and within a few years only. In the MMC, the semiconductors of one branch do not switch simultaneously anymore, but only one semiconductor switches at the time or a few series connected switches together. This way, large voltage leaps are avoided and the filter requirements are greatly reduced. Furthermore, an individual cell switches only rarely during a 50-Hz or 60-Hz cycle, i.e. two to maximum five times. The switching frequency of an individual semiconductor is reduced from e.g. 1350 Hz (27 pulses in a 50-Hz cycle) to only 100–300 Hz, and the switching losses are reduced by about an order of magnitude, too. Accordingly, there is full focus on reducing the conduction losses and quite relaxed requirements for the losses of a single switching event. Consequently, the voltage class of the IGBTs went up to e.g. 4.5 kV and the devices are optimised for good conduction. In such converters, SiC MOSFETs cannot profit from their low switching losses, and conduction losses are a matter of chip area, i.e. cost, while plasma-flooded bipolar SiC devices are particularly unattractive in those voltage classes due to the 3 V junction voltage in on-state. Thus, SiC devices do not play any role in MMCs for HVDC, although MOSFETs are better and could indeed reduce losses, volume, and weight [59].

However, the situation will change if the voltage rating of an individual device is much higher than in today's silicon-based MMC cells. Many systems still rely on series connection of several individual IGBTs to form an MMC cell. Devices offering blocking capability beyond 15 kV can reduce the required number of series connected devices and can be advantageous even in terms of losses. Of course, for such high blocking capabilities, even SiC devices have to be plasma-flooded bipolar devices, preferably IGBTs, and have to compensate the 3 V junction voltage by lower series resistant. A simple example shows the potential advantage: a 4.5-kV press-pack IGBT module used for HVDC has an on-state voltage drop of 3.7 V at rated current and 125 °C [60]. A series connection of four such silicon IGBTs could be replaced by an 18-kV SiC IGBT of the same current rating. To be on par with the four series connected silicon IGBTs regarding the conduction losses, the SiC

IGBT would need an on-state voltage of less than $4 \times 3.7\,\text{V} = 14.8\,\text{V}$. Simulations of 18-kV SiC IGBTs show that on-state voltages clearly below 10 V are feasible and that the switching losses are still a factor of five lower than with the silicon IGBTs. The effect can be even more pronounced at partial load. Published results, e.g. [61], support these findings. Of course, there are a number of challenges to be solved, like the limited minority carrier lifetime, the low injection efficiency of the substrate material, and especially all kinds of packaging issues, but in total the benefit could be substantial and the higher device cost would then be paid back over time by energy, which is not converted into heat. Thus, HVDC is technically challenging but might become a financially viable, though small, market for SiC devices.

15.8.2 HVDC Breakers

While HVDC is still mainly point-to-point transmission, the future will see more and more multiterminal installations and then also meshed HVDC grids. It sounds simple to just connect more terminals to anyway constant DC lines, but every failure of a terminal or a line would immediately lead to a shutdown of the entire system. While this might be acceptable for a point-to-point connection, it is not for a large-scale system. To keep the unaffected parts of the system operational, the affected parts have to be disconnected, before a cascaded shutdown takes place. This requires DC breakers [62], which are able to interrupt the current and support the high voltage – bidirectionally, because the current might flow in either direction and because a ground fault might occur on either side of the breaker.

This sounds an easy task for a mechanical switch, if it was quick enough and could extinguish the arc, but for semiconductor switches with their usually unidirectional operation, it requires workarounds like an anti-serial connection with anti-parallel diodes for the individual switches. Another unusual operation characteristic of the breakers is the rareness of switching events throughout the breakers' entire service live. The breakers stay either turned on or turned off, and thus, the switching losses are of no concern as long as they do not endanger the proper switching operation. The latter is particularly important because the energy dissipated in the breaker is not just its own switching losses but also a part of the energy stored in the DC lines or converters the breaker is trying to disconnect. Usually, the stored energy is much too high to be dissipated in the semiconductors alone and requires a surge arrestor. In other words, the full focus is on the conduction losses of the breaker, and neither silicon nor SiC devices are close to a sufficiently low on-state voltage.

One workaround is the hybrid breaker sketched in Figure 15.9 [63]. Under normal operation, the current is flowing through a fast mechanical switch and a few semiconductor devices. In a breaking event, the semiconductor devices are turned off and the voltage across them increases, while the current is still forced through them by the grid impedance. However, the additional voltage is sufficient to commutate the current into an auxiliary path with many semiconductor switches in series, enough that they can support the overvoltage during turn-off. Once the current has commutated into the auxiliary path, the mechanical switch is opened and interrupts the main path. Then the auxiliary path is carrying the full current and can

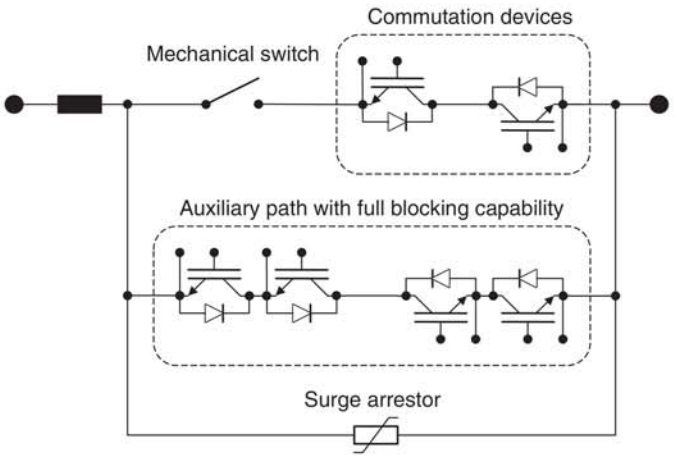

Figure 15.9 Hybrid HVDC breaker according to [63]. Source: Based on Hassanpoor et al. [63].

be turned off without the current commutating back to the main path. When the rising voltage reaches the trigger level of the surge arrestor, the current commutates into the surge arrestor and the remaining energy of the grid impedance is dissipated there. The switching losses of the semiconductor devices are of no concern and the only parameter that matters is the on-state voltage of the semiconductors in the main path. SiC devices could benefit from their lower conduction losses but that is a matter of chip area and cost. The low switching losses of SiC devices are of no advantage at all, and thus, SiC devices do not seem to be of particular benefit for HVDC breakers. Even worse, semiconductor breakers face a strong competition by gas insulated mechanical breakers, which are very compact and much cheaper than semiconductor solutions [62]. Thus, it is at least questionable if semiconductor-based breakers can excel in HVDC, not to mention SiC-based ones.

15.9 Drives

15.9.1 Industrial Drives

Electric drives cover a wide range of power levels and applications. Low-power applications and home appliances operate at lower voltage and/or current levels. For those applications, silicon or GaN devices usually offer better, in particular cheaper, solutions and SiC devices will not gain a significant market share anytime soon (cf. Figure 15.3). At higher power levels, the situation is more promising for SiC devices. However, the grid side and the motor side have different mission profiles and restrictions, which usually lead to different optimisations and also different perspectives for SiC devices.

At first glance, the situation for the grid side is similar to photovoltaic systems. However, the majority of grid connections of drives are still passive rectifier bridges

or sometimes thyristor based. In those cases, a SiC solution is hardly competitive because silicon rectifiers can have quite a low on-state voltage drop and switching is not relevant. In case of an active grid connection using active components, the power factor can be controlled, the harmonics content can be limited, and a reversal of the energy flow is enabled, such that energy can be transferred back from the DC-link to the grid. Like in case of the photovoltaic inverter, the main benefits of the SiC components for those active grid connections are reduced conduction losses and smaller passives due to higher switching frequency. The smaller passives are the main line choke and the DC-link capacitor. For the grid connection, a lower inductance value is sufficient and the choke tends to be smaller in volume and cheaper. However, the choke requires a good high-frequency performance, i.e. a low parasitic capacitance for good EMI performance and a core material with low losses as well as a good cooling as the harmonics will cause high losses in the choke's core. Both factors will increase the cost again such that the financial gain on the choke is quite limited. With the shorter period in between switching events, also the necessity to store energy in the DC-link is reduced and, thus, the DC-link capacitor could be smaller, too. However, the storage of energy is not necessarily the limiting factor, but ripple currents and the losses they cause at the equivalent series resistor (ESR) of the capacitor are. Like with the choke, a better capacitor (technology) or at least a better cooling or less compact design would be required and limits the potential benefit.

Furthermore, the DC-link capacitor has to fulfill the requirements of the motor side in an analogous way, and reducing the size of the capacitor is subject to also higher switching frequency on the motor side. Unfortunately, increasing the switching frequency on the motor side is not as beneficial as on the grid side because the size of the motor is rather given by mechanical restrictions, while the high switching frequency will change the composition of nonideal currents and losses in the motor in a nonlinear way. Furthermore, the high voltage transients required to keep the switching losses low increase capacitive currents in the motor and towards ground, which do not just increase losses but can be even dangerous for the motor because part of the current can flow over the bearings, which might degrade over time. The steep voltage transients, sometimes even aggravated by travelling wave phenomena on the cable and resulting over voltage peaks, might also degrade the insulation of the windings, eventually causing a complete breakdown. However, the capacitance of the motor cable is a natural filter element damping the voltage transient. Unfortunately, the capacitance also increases the switching losses of the SiC components and might require their own damping elements – with additional losses in those elements but lower losses in the motor. At the end, the exact design is a complex optimisation and requires special attention in each case [64]. Although electrical drives might already profit from reduced switching losses of the SiC components even when they are not switching faster than IGBTs, it requires progress on the motor, its connection, and on the main line choke to fully exploit the advantages of the SiC components. In fact, the situation is even more demanding because further components inside the converter have to be optimised, namely, the gate drivers, which have to be capable of controlling the fast switching events without causing overshoots and

preventing short circuit events and the overall parasitics of the circuitry [65]. In other words, SiC has a potential for drives but it comes at significant cost, and at lower voltages (<1000 V), again silicon or GaN [66] might offer even better (integrated) solutions.

Of course, the situation is again completely different when going to medium voltage drives and applying the MMC principle. In case the output frequency is high like in [67], the higher switching frequency achievable by SiC components without deteriorating the overall efficiency of the converter can reduce the cell-capacitor and the total volume of the MMC as well as the total harmonic distortion. However, even though SiC components can improve the converter in such particular applications, it is questionable if that could be a (financially) viable solution and the efficiency is already high with silicon components.

15.9.2 Wind Energy

In general, converters for wind turbines are not much different from high-voltage industrial converters and as a first approximation it does not matter, if they are converters for doubly-fed induction generators, for multipole generators without a gear box or just full-scale converters. Consequently, most of the considerations above hold true for wind turbine converters, too, and weight and size are an argument for the generator side converters in the nacelle only, although the converter is usually not a major fraction of the weight. For those generator side converters, the same restrictions imposed by the generator apply like in case of the motor side converters of drives. Given the low speed of the generators, high switching frequency is of less advantage and the main benefit would be lower conduction losses, especially under partial load conditions. However, this would require SiC MOSFETs with a large total chip area and would increase cost substantially.

If the switching frequency of the generator side converter remains low, the DC-link capacitor cannot be shrunk and the only benefit from higher switching frequency of the grid side converter would be a smaller main line choke. However, the higher switching frequency would again require a good high-frequency performance, i.e. low parasitics and an advanced core material, and that would mostly cancel the financial advantage.

After all, higher switching frequency is of less benefit and the main advantage for wind power converters would be higher efficiency, originating from lower conduction losses and much lower switching losses of the SiC components. Especially if going up in blocking capability and reducing complexity of the converter SiC devices could excel, then maybe even as SiC IGBTs [68]. For the time being, the cost of SiC components is still too high to justify their application [69], and, consequently, there is no market penetration yet and not expected anytime soon. However, the situation changes if the wind turbines are not coupled to an AC grid but to a (local) DC grid with consecutive DC transmission, e.g. in case of a remote off-shore wind farm. This would require DC/DC converters, and here SiC devices might have an edge, in particular, if the DC-voltage level is much higher than 10 kV.

15.9.3 Traction

Like many other mobile applications, traction profits not only from a better efficiency of the converters equipped with SiC components but also from the smaller size and the lower weight of those converters. The most prominent example is the Japanese Shinkansen bullet train series N700S [70], which uses 1500 A, 3.3-kV SiC MOSFETs and started regular service in July 2020 – in time for the original schedule of the Olympics in Tokyo, just like the first Shinkansen did for the 1964 Olympics. Besides these advertising aspects, the SiC deployed for this application offers indeed several advantages. Based on the mission profile of a 515-km ride from Tokyo to Shin–Osaka, the losses of the converter were 30% lower than with the conventional solution. This result is particularly impressive because hybrid modules were used, i.e. still silicon IGBTs, but already SiC Schottky diodes. Due to the lower losses, the cooling could be reduced from forced air cooling to train draft cooling, which reduces the size of the converter considerably by omitting the fan and the air channels. Together with other improvements, the converter is only half the size of the original one (Figure 15.10) and has 30% less weight. This way, the converter fits underfloor of the carriage that carries the main transformer already, while previously the converter for the transformer carriage had to go into a neighbouring carriage causing additional wiring.

While the Shinkansen is cruising most of the time beyond 200 km h^{-1} [70] and, thus, profits from the better efficiency in partial load, similar results have been reported for light rail applications with their cruise-stop-idle-go-again mission profile. Using also hybrid modules for urban trains [71] yielded 35% reduced losses (+4% efficiency), 32% reduced volume, and 25% reduced weight, and using full SiC modules for a metro [72] yielded 51% reduced volume and 22% reduced weight as well as 63% reduced temperature increase over ambient, i.e. losses. Those are only first steps into SiC technology, and even larger improvements are expected while progressing on the learning curve. Together, with the longevity of rolling stock, the payback of higher efficiency over that period and, consequently, the willingness of train operators to invest into future-proof technology, this field of application is obviously one of the most promising for SiC devices. Due to the additional impact on the range or the storage size, the advantage is even larger in case of offline systems like diesel-electric, battery, or fuel cell trains and also off-road vehicles.

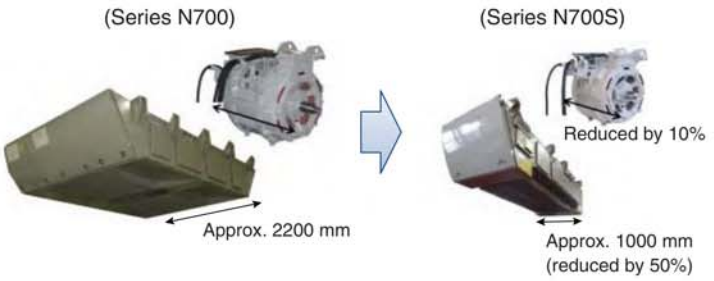

Figure 15.10 Traction converter and motor of a Shinkansen N700 and their improvement due to the application of full SiC semiconductor devices (N700S). Source: Sato et al. [70].

15.10 Conclusions

After almost 20 years of commercialisation and almost 10 years of the MOSFET being available, SiC technology is on the one hand well established, but on the other hand also still rapidly developing. The economic progress is documented by large-scale investments [73] as well as extensive cooperation and supply agreements, e.g. [74], and drives the economy of scale. The resulting cost reduction of SiC devices makes additional applications economically viable for SiC and increases the market even further. This way, SiC has moved out of the hen-and-egg situation and out of the high-end niche markets into the main stream.

Technologically, the progress goes into several directions. Lower channel resistance allows to produce competitive low-voltage devices, in particular in the 650-V class, targeting an even bigger market, including EVs/hybrid electric vehicles (HEVs) and challenging silicon SJ MOSFETs and GaN HEMTs. On the other end of the voltage range, better material and processes enable higher blocking capability, which in turn provides SiC with an advantage over IGBTs and thyristor-based solutions in heavy traction, induction heating, or HVDC applications. Another direction of progress is the packaging. Initially, the TO-247 was good enough to start the business with a known footprint, but to fully exploit the advantages of the material beyond lower on-resistance, i.e. extremely fast switching and high temperature capability, low parasitic and temperature stable packages are required and progressively available. Furthermore, hybrid integration as well as higher voltage and higher currents are required to serve additional markets. With half-bridges of 6.5 kV and/or 1 kA, such devices are in sight already and just a matter of actually producing them. Finally and after some teething troubles, SiC is building up a track record of good reliability. This is a prerequisite for availability sensitive applications like automotive and, even more, aerospace, which already started to use SiC devices.

Thus, SiC is targeting an ever-growing range of applications. On the one hand, only very few of those applications would be unfeasible without the advantages of SiC devices. On the other hand, SiC devices are not yet a general replacement of silicon devices either, although SiC can beat silicon in more and more applications as the cost is coming down and by gaining system advantages. At the end, it is a case-to-case decision to use SiC devices, while silicon is improving as well and GaN shows an even more dynamic development, establishing a strong and for some applications even superior competition. And the decision to take is not necessarily an either or one. Like the examples in DC/DC converters and photovoltaic show, the optimum might be a mixed assembly, with e.g. silicon for high-current switches and SiC for high-frequency ones. Furthermore, the combination of silicon and SiC chips into one switch might be advantageous – at least economically and at least as an intermediate step [75, 76]. In any case, SiC devices have to keep the pace of their technical development, and at the same time, cost has to come down to prevail. As none of the fields of required improvement shows general road blocks, it is just a matter of actually doing it, of smart ideas on the way and of time to implement. SiC is here to stay – and to grow.

Acknowledgements

The author is grateful to a number of esteemed colleagues and friends for their helpful inputs, valuable discussion, and discerning reviews. These individuals are (alphabetic order): Gerald Deboy (Infineon Technologies Austria AG, Austria), Enrique J. Dede (Universitat de Valencia, Spain), Hans-Günter Eckel (Universität Rostock, Germany), Peter Friedrichs (Infineon Technologies AG, Germany), Elmar Herweg (E.G.O. Elektro-Gerätebau GmbH, Oberderdingen, Germany), Klaus F. Hoffmann (Helmut-Schmidt-Universität Hamburg, Germany), Mike Meinhardt (SMA Solar Technology AG, Germany), Axel Mertens (Leibniz Universität Hannover, Germany), Klaus Rigbers (SMA Solar Technology AG, Germany), Roland Rupp (Infineon Technologies AG, Germany), Irma Villar (IKERLAN, Spain), as well as my predecessor Dieter Silber and my assistant Birgit Höft.

References

1 Kaminski, N. (2017). The ideal chip is not enough: Issues retarding the success of wide band-gap devices. *Jpn. J. Appl. Phys.* 56: 04CA03.

2 Kaminski, N. and Hilt, O. (2014). SiC and GaN devices – wide bandgap is not all the same. *IET Circuits Devices Syst.* 8 (3): 227–236.

3 Y. Furukawa et al. (2016). Matrix converter with sinusoidal input-output filter and filter downsizing using SiC devices. *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI.

4 Kinzer, D. and Oliver, S. (2016). Monolithic HV GaN power ICs: performance and application. *IEEE Power Electron. Mag.* 3 (3): 14–21.

5 European Centre for Power Electronics (ECPE) (2018). WBG roadmap - lead applications for SiC and GaN.

6 IEA Implementing Agreement on Energy Efficient End-Use Equipment (4E) - Power Electronic Conversion Technology Annex (PECTA). (2020), Wide band gap technology: efficiency potential and application readiness map.

7 Zverev, I., Treu, M., Kapels, H. et al. (2001). SiC Schottky rectifiers: performance, reliability and key application. In: *European Conference on Power Electronics and Applications (EPE'01) (27–29 August 2001)*. Graz: IEEE.

8 Deboy, G., Treu, M., Haeberlen, O., and Neumayr, D. (2016). Si, SiC and GaN power devices: an unbiased view on key performance indicators. In: *2016 IEEE International Electron Devices Meeting (IEDM) (3–7 December 2016)*, 20.2.1–20.2.4. San Francisco, CA: IEEE.

9 Siemieniec, R., Mente, R., Jantscher, W. et al. (2019). 650 V SiC Trench MOSFET for high-efficiency power supplies. In: *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe) (3–5 September 2019)*. Genova, Italy: IEEE.

10 Kortazar, I., Larrazabal, I., and Mendizabal, L. (2017). Isolated DC–DC converter based on silicon carbide for advanced multilevel topologies. In: *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe) (11–14 September 2017)*. Warsaw: IEEE.

11 Morel, F. et al. (2019). Power electronic traction transformers in 25 kV/50 Hz systems: optimisation of DC/DC isolated converters with 3.3 kV SiC MOSFETs. In: *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (7–9 May 2019)*. Nuremberg, Germany: VDE.

12 Zhao, C. et al. (2014). Power electronic traction transformer – medium voltage prototype. *IEEE Trans. Ind. Electron.* 61 (7): 3257–3268.

13 Hu, Y., Shao, J., and Ong, T.S. (2019). 6.6 kW high-frequency full-bridge LLC DC/DC converter with SiC MOSFETs. In: *2019 IEEE Energy Conversion Congress and Exposition (ECCE) (29 September–3 October 2019)*, 6848–6853. Baltimore, MD: IEEE.

14 Helsper, M. and Ocklenburg, M. (2018). SiC MOSFET based auxiliary power supply for rail vehicles. In: *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe) (17–21 September 2018)*. Riga: IEEE.

15 Rothmund, D., Guillod, T., Bortis, D., and Kolar, J.W. (2019). 99% efficient 10 kV SiC-based 7 kV/400 V DC transformer for future data centers. *IEEE Trans. Emerg. Sel. Top. Power Electron.* 7 (2): 753–767.

16 Huber, J.E. and Kolar, J.W. (2016). Solid-state transformers: on the origins and evolution of key concepts. *IEEE Ind. Electron. Mag.* 10 (3): 19–28.

17 Huber, J.E. and Kolar, J.W. (2019). Applicability of solid-state transformers in today's and future distribution grids. *IEEE Trans. Smart Grid* 10 (1): 317–326.

18 Boys, J.T. and Covic, G.A. (2015). The inductive power transfer story at the University of Auckland. *IEEE Circuits Syst. Mag.* 15 (2): 6–27.

19 Machura, P. and Li, Q. (2019). A critical review on wireless charging for electric vehicles. *Renewable Sustainable Energy Rev.* 104: 209–234.

20 Jiang, H., Brazis, P., Tabaddor, M., and Bablo, J. (2012). Safety considerations of wireless charger for electric vehicles – a review paper. In: *2012 IEEE Symposium on Product Compliance Engineering Proceedings (5–7 November 2012)*. Portland, OR: IEEE.

21 Kim, J.H. et al. (2015). Development of 1-MW inductive power transfer system for a high-speed train. *IEEE Trans. Ind. Electron.* 62 (10): 6242–6250.

22 Iruretagoyena, U., Villar, I., Garcia-Bediaga, A. et al. (2017). Design and characterization of a meander-type dynamic inductively coupled power transfer coil. *IEEE Trans. Ind. Appl.* 53 (4): 3950–3959.

23 Foote, A., Onar, O.C., Debnath, S. et al. (2019). System design of dynamic wireless power transfer for automated highways. In: *2019 IEEE Transportation Electrification Conference and Expo (ITEC) (19–21 June 2019)*. Detroit, MI: IEEE.

24 Villar, I., Garcia-Bediaga, A., Iruretagoyena, U. et al. (2018). Design and experimental validation of a 50 kW IPT for railway traction applications. In: *2018*

IEEE Energy Conversion Congress and Exposition (ECCE) (23–27 September 2018), 1177–1183. Portland, OR: IEEE.

25 Omori, H., Iga, Y., Morizane, T. et al. (2012). A novel wireless EV charger using SiC single-ended quasi-resonant inverter for home use. In: *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC), Novi Sad (4–6 September 2012)*, LS8b.2-1–LS8b.2-7. IEEE.

26 Xuan Bac, N., Vilathgamuwa, D.M., and Madawala, U.K. (2014). A SiC-based matrix converter topology for inductive power transfer system. *IEEE Trans. Power Electron.* 29 (8): 4029–4038.

27 Bosshard, R. and Kolar, J.W. (2017). All-SiC 9.5 kW/dm^3 on-board power electronics for 50 kW/85 kHz automotive IPT system. *IEEE Trans. Emerg. Sel. Top. Power Electron.* 5 (1): 419–431.

28 Sheikhian, I., Kaminski, N., Voss, S. et al. (2014). Optimisation of the reverse conducting IGBT for zero-voltage switching applications such as induction cookers. *IET Circuits Devices Syst.* 8 (3): 176–181.

29 Mangkalajarn, S., Ekkaravarodome, C., Sukanna, S. et al. (2019). Comparative study of Si IGBT and SiC MOSFET in optimal operation class-E inverter for domestic induction cooker. In: *2019 Research, Invention, and Innovation Congress (RI2C) (11–13 December 2019)*. Bangkok, Thailand: IEEE.

30 Sarnago, H., Burdío, J.M., and Lucia, O. (2019). High-frequency GaN-based induction heating versatile module for flexible cooking surfaces. In: *2019 IEEE Applied Power Electronics Conference and Exposition (APEC) (17–21 March 2019)*, 448–452. Anaheim, CA: IEEE.

31 Lucía, O., Maussion, P., Dede, E.J., and Burdío, J.M. (2014). Induction heating technology and its applications: past developments, current technology, and future challenges. *IEEE Trans. Ind. Electron.* 61 (5): 2509–2520.

32 Dede, E.J., Jordán, J., and Esteve, V. (2016). The practical use of SiC devices in high power, high frequency inverters for industrial induction heating applications. In: *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC) (5–8 December 2016)*. Auckland: IEEE.

33 Ogiwara, H., Itoi, M., and Nakaoka, M. (2016). Highly efficient high frequency inverter for induction heating using SiC power module. In: *2016 IEEE International Power Electronics and Motion Control Conference (PEMC) (25–28 September 2016)*, 116–121. Varna: IEEE.

34 Saridakis, S., Koutroulis, E., and Blaabjerg, F. (2015). Optimization of SiC-based H5 and conergy-NPC transformerless PV inverters. *IEEE Trans. Emerg. Sel. Top. Power Electron.* 3 (2): 555–567.

35 Freiche, R., Franz, S., Fink, M., and Liese, S. (2017). A 70 kW next generation three-phase solar inverter with multiple MPPTs using advanced cooling concept and stacked-PCB architecture. In: *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (16–18 May 2017)*. Nuremberg, Germany: VDE.

36 SMA Datasheet DEN123715. (2013). Sunny Tripower 20000TL HE.

37 Anderson, J.A., Hanak, E.J., Schrittwieser, L. et al. (2019). All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter. *CPSS Trans. Power Electron. Appl.* 4 (1): 50–61.

38 SMA Whitepaper AEN1639. (2019). True 1500 V Technology for the New Generation of PV Power Plants.

39 Umbach, F., Brandt, P., Mansueto, S. et al. (2020). 2.3 kV – a new voltage class for Si IGBT and Si FWD. In: *PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, virtual (7–8 July 2020)*. VDE.

40 SMA & Infineon Press Release 2020-01-21. (2020). SMA and Infineon reduce system costs for inverters.

41 Cunningham, D.W., Carlson, E.P., Manser, J.S., and Kizilyalli, I.C. (2020). Impacts of wide band gap power electronics on photovoltaic system design. *IEEE J. Photovoltaics* 10 (1): 213–218.

42 Singh, A., Reese, S., and Akar, S. (2019). Performance and techno-economic evaluation of a three-phase, 50-kW SiC-based PV inverter. In: *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC) (16–21 June 2019)*, 0695–0701. Chicago, IL: IEEE.

43 SMA Whitepaper AEN1919. (2019). Centralized system layout – decentralized system layout.

44 Todorovic, M.H. et al. (2016). SiC MW PV inverter. In: *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (10–12 May 2016)*. Nuremberg, Germany: VDE.

45 Fujii, K., Noto, Y., Oshima, M., and Okuma, Y. (2015). 1-MW solar power inverter with boost converter using all SiC power module. In: *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe) (8–10 September 2015)*. Geneva: IEEE.

46 Hofer, J., Svetozarevic, B., and Schlueter, A. (2017). Hybrid AC/DC building microgrid for solar PV and battery storage integration. In: *2017 IEEE Second International Conference on DC Microgrids (ICDCM) (27–29 June 2017)*, 188–191. Nuremburg: IEEE.

47 Shenai, K. (2015). Wide bandgap (WBG) semiconductor power converters for DC microgrid applications. In: *2015 IEEE First International Conference on DC Microgrids (ICDCM) (7–10 June 2015)*, 263–268. Atlanta, GA: IEEE.

48 Burkart, R.M. and Kolar, J.W. (2017). Comparative η-ρ-σ pareto optimization of Si and SiC multilevel dual-active-bridge topologies with wide input voltage range. *IEEE Trans. Power Electron.* 32 (7): 5258–5270.

49 Beheshtaein, S., Cuzner, R., Savaghebi, M., and Guerrero, J.M. (2019). Review on microgrids protection. *IET Gener. Transm. Distrib.* 13 (6): 743–759.

50 Würfel, A., Adler, J., Mauder, A., and Kaminski, N. (2016). Over current breaker based on the dual thyristor principle. In: *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD) (12–16 June 2016)*, 143–146. Prague: IEEE.

51 Shen, Z.J., Sabui, G., Miao, Z., and Shuai, Z. (2015). Wide-bandgap solid-state circuit breakers for DC power systems: device and circuit considerations. *IEEE Trans. Electron Devices* 62 (2): 294–300.

52 Sato, Y., Tanaka, Y., Fukui, A. et al. (2014). SiC-SIT circuit breakers with controllable interruption voltage for 400-V DC distribution systems. *IEEE Trans. Power Electron.* 29 (5): 2597–2605.

53 Zhou, Y., Feng, Y., and Shen, Z.J. (2018). iBreaker: intelligent tri-mode solid state circuit breaker technology. In: *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC) (4–7 November 2018)*. Shenzhen: IEEE.

54 Schulz, M., Kaiser, J., Gosses, K. et al. (2019). Bidirectional bipolar electronic overcurrent safety elements for bipolar DC grids. In: *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (7–9 May 2019)*. Nuremberg, Germany: VDE.

55 Cairoli, P., Qi, L., Tschida, C. et al. (2019). High current solid state circuit breaker for DC shipboard power systems. In: *2019 IEEE Electric Ship Technologies Symposium (ESTS) (14–16 August 2019)*, 468–476. Washington, DC: IEEE.

56 ABB reference list of HVDC Classic thyristor valve projects. 2019.

57 ABB reference list of HVDC Light® VSC technology projects. 2019.

58 Lesnicar, A. and Marquardt, R. (2003). An innovative modular multilevel converter topology suitable for a wide power range. In: *2003 IEEE Bologna Power Tech Conference Proceedings (23–26 June 2003)*, vol. Vol. 3. Bologna, Italy: IEEE.

59 Ishii, Y. and Jimichi, T. (2018). Verification of SiC based modular multilevel cascade converter (MMCC) for HVDC transmission systems. In: *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia) (20–24 May 2018)*, 1834–1839. Niigata: IEEE.

60 ABB Data Sheet, StakPak IGBT Module 5SNA 3000K452300, Doc. No. 5SYA 1450-03. 2017.

61 Yonezawa, Y. et al. (2018). Progress in high and ultrahigh voltage silicon carbide device technology. In: *2018 IEEE International Electron Devices Meeting (IEDM) (1–5 December 2018)*, 19.3.1–19.3.4. San Francisco, CA: IEEE.

62 Ito, H. (2019). Innovation of switching technologies in power systems. In: *2019 5th International Conference on Electric Power Equipment – Switching Technology (ICEPE-ST) (13–16 October 2019)*, 772–779. Kitakyushu, Japan: IEEE.

63 Hassanpoor, A., Häfner, J., and Jacobson, B. (2015). Technical assessment of load commutation switch in hybrid HVDC breaker. *IEEE Trans. Power Electron.* 30 (10): 5393–5400.

64 Müller, J., Brinker, T., Friebe, J., and Mertens, A. (2018). Output dv/dt filter design and characterization for a 10 kW SiC inverter. In: *IECON 2018 – 44th Annual Conference of the IEEE Industrial Electronics Society (21–23 October 2018)*, 2122–2127. Washington, DC: IEEE.

65 Morya, A.K. et al. (2019). Wide bandgap devices in AC electric drives: opportunities and challenges. *IEEE Trans. Transp. Electrif.* 5 (1): 3–20.

66 Hirota, T., Inomata, K., Yoshimi, D., and Higuchi, M. (2018). Nine switches matrix converter using bi-directional GaN device. In: *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia) (20–24 May 2018)*, 3952–3957. Niigata: IEEE.

67 J. Pan (2020) et al., "7-kV, 1-MVA SiC-based modular multilevel converter prototype for medium-voltage electric machine drives," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10137-10149, doi: https://doi.org/10.1109/TPEL.2020.2978657.

68 Dey, R. and Nath, S. (2016). Replacing silicon IGBTs with SiC IGBTs in medium voltage wind energy conversion systems. In: *2016 7th India International Conference on Power Electronics (IICPE) (17–19 November 2016)*. Patiala: IEEE.

69 Neumann, C., Schmidtke, R., Plötz, T., and Eckel, H. (2020). An economic evaluation of SiC-MOSFET modules in wind turbine converters. In: *PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (7–8 July 2020)*. Virtual, Germany: VDE.

70 Sato, K., Kato, H., and Fukushima, T. (2018). Development of SiC applied traction system for Shinkansen high-speed train. In: *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia) (20–24 May 2018)*, 3478–3483. Niigata: IEEE.

71 Rujas, A., Lopez, V.M., Villar, I. et al. (2019). SiC-hybrid based railway inverter for metro application with 3.3 kV low inductance power modules. In: *2019 IEEE Energy Conversion Congress and Exposition (ECCE) (29 September–3 October 2019)*, 1992–1997. Baltimore, MD: IEEE.

72 Lindahl, M., Velander, E., Johansson, M.H. et al. (2018). Silicon carbide MOSFET traction inverter operated in the Stockholm metro system demonstrating customer values. In: *2018 IEEE Vehicle Power and Propulsion Conference (VPPC) (27–30 August 2018)*. Chicago, IL: IEEE.

73 Cree Press Release 2019-05-07. Cree to Invest $1 Billion to Expand Silicon Carbide Capacity.

74 Cree Press Release 2019-11-19. Cree and STMicroelectronics Expand and Extend Existing Silicon Carbide Wafer Supply Agreement.

75 Kicin, S. et al. (2019). Characterization of 1.7 kV SiC MOSFET/Si IGBT cross-switch hybrid on the LinPak platform. In: *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (7–9 May 2019)*. Nuremberg, Germany: VDE.

76 Kochoska, S., Neyer, T., and Park, K.-S. (2020). Breaking the IGBT E_{loss}/V_{CEsat} trade off relationship by wedding Si IGBT + SiC MOSFET. In: *PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (7–8 July 2020)*. Virtual, Germany: VDE.

16

Special Focus on HEV and EV Applications: Activities of Automotive Industries Applying SiC Devices for Automotive Applications

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16.1 Background (PDPlus LLC)

The automotive industry is said to undergo a major revolution once every 100 years. In 1876, the world's first steam-powered car was invented, and in 1886, the world's first car with an internal combustion engine, said to have pioneered modern cars, was invented. For more than 100 years since the invention, automotive industries have continued to improve engine performance, and comfortable and high-performance automobiles have been developed and produced. However, during this time, it is also true that negative impacts such as the consumption of fossil fuels, the emission of CO_2, traffic accidents, and air pollution have increased. Until now, automotive industries have been expanding mainly in developed countries and regions, but it is expected that the number of vehicles will increase in newly developed countries and regions in near future. It is feared that the negative impact will further increase while contributing to the improvement of the quality of life of people in those regions. A new movement in automotive industry is CASE (connected cars, autonomous driving, sharing, and electrification). Among them, electrification is an activity that aims to introduce electric power to the power section and dramatically reduce fuel consumption, that is, CO_2 emissions. Until now, mainly hybrid electric vehicles (HEVs) have been prevalent in markets, but in the future, plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs),

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

which are expected to reduce CO_2 emissions drastically, are expected to expand rapidly, and another type of zero-emission vehicle of fuel cell vehicles (FCVs) development and dissemination have begun.

Global vehicle production in 2017 was 91 million. However, the ratio of electrified vehicles was only 4%. To realize the below 2 °C scenario agreed at COP21, more than half of the expected production of 130 million vehicles in 2040 will be required to be electrified vehicles [1]. On the other hand, many economic analysts expect an electric vehicle ratio of 7–16% in 2030 [2]. Although there is a big gap between expectation and forecast, at least it is expected that the ratio of electrified vehicles will rapidly increase in the future.

For the further spread of electrified vehicles, it is required to improve the efficiency of electric power train components and to reduce the size, weight, and price of them. At present, Si power devices such as insulated-gate bipolar transistors (IGBTs) and PIN diodes are mainly used for electric power components in electrified vehicles. By replacing these Si power devices with silicon carbide (SiC) power devices, it becomes possible to satisfy these technical requirements. As a result, the performance of the power train is improved and the appeal of the electrified vehicles is increased. It is thought that SiC power devices will be able to contribute to the further spread of electrified vehicles.

At first, the efficiency improvement by introduction of SiC power devices in actual vehicles was evaluated for HEVs, and after that, SiC power devices were firstly introduced in FCVs as the mass-produced vehicle applications and mounted on a mass-produced EV motor inverter. Expectations are growing for big volume introduction of SiC power devices on vehicles now. On the other hand, despite the advantages of introducing SiC power devices on vehicles are great and clear and application of SiC power devices to vehicles has expected for the long term, SiC power devices have not spread into automotive applications so far. The main reason is that SiC power device cost is extremely high compared to Si power devices. In order to introduce SiC into electric vehicles, which are expected to explode in the near future, it is necessary to put further effort on the development of applications suitable for SiC, as well as the study of packaging technology and application technology to fully exploit the performance of SiC power semiconductors. These activities will contribute to reduce the total cost by downsizing the device by improving the performance and reducing the loss.

In this chapter, the very important five topics for automotive applications of SiC power devices are shown. The topics are “the challenge of SiC power devices introductions on prototype HEVs and FCVs”, “Introduction of Boost Converter Using SiC Semiconductor for New FCV Drive”, “development of module technologies to bring out SiC power device performances”, “SiC-MOSFET switching characteristics and gate driver circuits for automotive application”, and “R&D of SiC Power Devices for Automotive Applications”.

16.2 The Challenge of SiC Power Devices Introductions on Prototype HEVs and FCVs (TOYOTA MOTOR CORPORATION)

16.2.1 Progress of Electrification

With increasing awareness of environmental issues, reducing CO_2 emissions has become a major challenge for automotive industries. Figure 16.1 shows the milestones of Toyota Motor Corporation. It has set a long-term goal of reducing CO_2 emissions from new cars during driving by 90% in 2050 compared to 2010 [3]. As a milestone, it expects its sales of new electrified vehicles to be more than 5.5 million units in 2030, consisting of a combined 4.5 million units or more of HEVs and PHEVs, and a combined 1 million units or more of battery electric vehicles (BEVs) and fuel cell electric vehicles (FCEVs). The progress of electrification has been taken place faster than expected in 2018. In June 2019, Toyota announced that it would reach its forecasted numbers nearly five years earlier (Figure 16.2) [4]. A lot of car manufacturer is planning to launch some BEVs in the first half of the 2020s to meet the growing expectations for BEVs around the world. With the rapid progress of electrification, application of SiC devices is also being studied.

At present, the cost of a SiC device is more than twice as high as that of a Si device, and thus the SiC device is being adopted from more effective applications. Figure 16.3 shows the percentage of electrical energy loss for each type of electrified vehicle and each of the driving inverter, power generation inverter, and boost converter [5]. BEV driving inverters and FCEV boost converters are components that can significantly reduce energy loss. It is expected that the loss can be reduced by 70% or more by replacing Si devices with SiC devices.

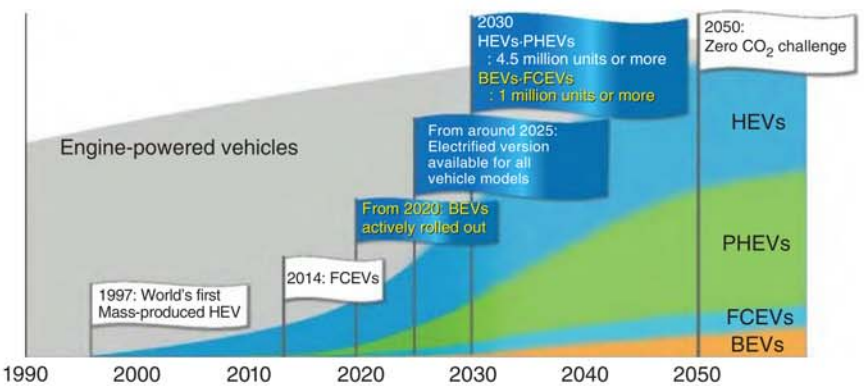

Figure 16.1 Milestones in popularizing electrified vehicles (announced in December 2017).

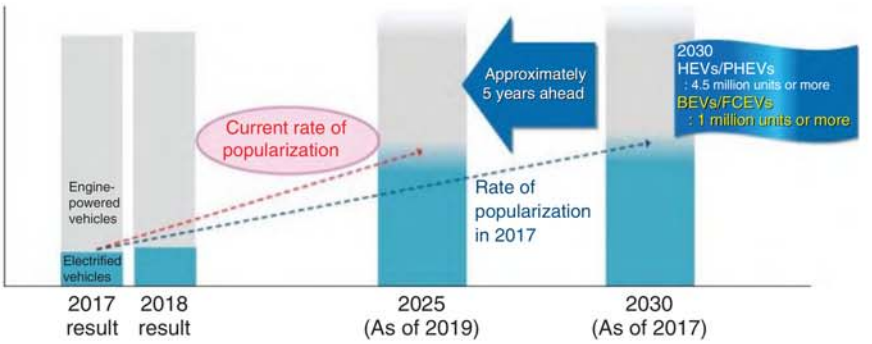

Figure 16.2 Rate of popularization of Toyota's electrified vehicles (announced in June 2019).

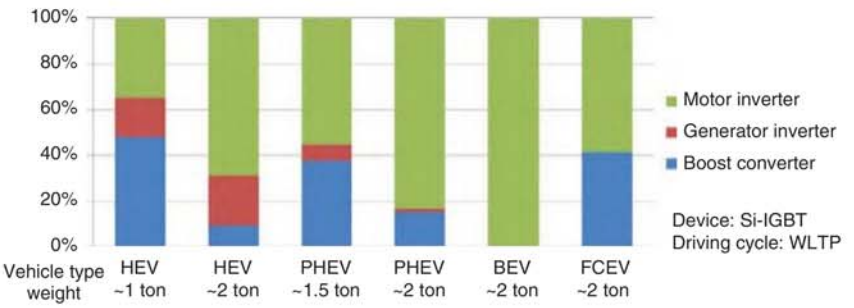

Figure 16.3 The ratio of the electrical loss of power control unit (PCU).

A secondary effect of improving fuel efficiency is to reduce the amount of battery installed in the case of BEV and to reduce the FC tank capacity in the case of FCEV. In addition, the FC boost converter that extracts high power from the FC stack has a considerably large volume and thus has a large size reduction effect. The adoption of SiC is determined by comparing the effects of using SiC devices, such as reducing expensive components and the volume, with the increased cost using SiC devices. In autonomous driving, which is being promoted at the same time as electrification, many sensors are used, and as a result, much power is required. As a DC–DC converter for converting to 12 V, 100 A class converter is used at present, but the current capacity is expected to increase rapidly and double.

16.2.2 Demonstration of Electrified Vehicles

In 2014, Toyota Motor showed that using SiC devices for inverter and boost converter of Prius, fuel efficiency could be improved by about 10% [6, 7]. Switching loss was measured to be reduced by 70–85%. In 2015, we prototyped a CAMRY using

Figure 16.4 SORA: Tokyo Toei FC bus.

Two Mirai fuel cell stacks
(with six hydrogen bombe)
Power : 670 HP
Torque : 1325 pound feet
Driving range : 300 miles

Figure 16.5 Heavy-duty FC trucks @LA Port.

SiC-metal–oxide–semiconductor field-effect transistor (MOSFET) and SiC-Schottky barrier diode (SBD) for inverters and a boost converter. All-SiC CAMRY can run on public roads and measured the effect of improving fuel economy on public roads [8]. Improvement of efficiency by applying SiC diodes to FC bus boost converters was also studied. By changing the diode to SiC-SBD, the efficiency was improved by 0.5% [9]. At present, FC buses are used on routes on the Toei Bus from Tokyo Station to Big Sight (Figure 16.4). At the Tokyo Olympics in 2020, many FC buses will be introduced and used for personnel transport.

In the fall of 2017, using this FC system, a demonstration was started to reduce CO_2 by changing the trailer truck at Los Angeles Port to an FC truck [10]. Two FC stacks used by Mirai were used, and a 670-horsepower driving system was prepared to electrify the trailer truck. The initial mileage for one charge was 320 km, but in 2018, by increasing the number of hydrogen tanks from four to six, it was possible to drive 480 km (300 miles) with one hydrogen charge (Figure 16.5). As described above, various demonstrations have been performed since about 2015, and preparations for using SiC devices on electrified vehicles in earnest are being made.

16.3 Introduction of Boost Converter Using SiC Semiconductor for New FCV Drive (HONDA MOTOR CO., LTD.)

16.3.1 Introduction

In order to expand the use of FCVs that run on energy generated from hydrogen inside the vehicle, it is necessary to develop a convenient vehicle with a package that is the same as conventional internal combustion engine vehicles. In order to achieve this, further reduction in the size of the electric power train including the fuel cell (FC) stack is needed. To reduce the number of cells in the FC stack while still increasing the output of the traction motor, it is necessary to increase the voltage that is supplied from the FC stack to the traction motor. For this purpose, Honda has developed a large-output fuel cell voltage-boosting converter (fuel cell voltage control unit, hereafter referred to as "FCVCU") was developed that boosts the output voltage of the FC stack. Here, we will describe the circuit technology and structure of the voltage-boosting converter that was adopted to achieve reductions in size and weight.

16.3.2 Configuration of the Electric Power Plant System for New FCV

In the earlier 2009 model, the FC stack was positioned in the center tunnel in order to achieve a sedan package with low floor, low center of gravity, and low overall height [11]. However, the maximum occupancy was four persons. With the new model FCV, the FC stack and surrounding systems are more compact and are positioned together with the electric power train inside the front hood. This results in a roomy interior space that can seat five adults. The FCVCU provides large output while also adopting a thin, compact design that contributes to the layout. With the 2009 model, only the inverter and motor were mounted in the front motor room (Figure 16.6). However, in the new model FCV, the layout mounts all of the following components inside the front hood (Figure 16.7).

- FC stack
- Fuel cell voltage-boosting converter (FCVCU)
- Traction motor
- Inverter
- Battery voltage-boosting converter (BATVCU)

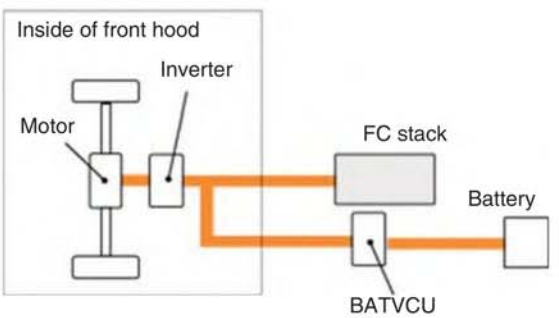

Figure 16.6 Conventional electric power plant (2009 model FCV).

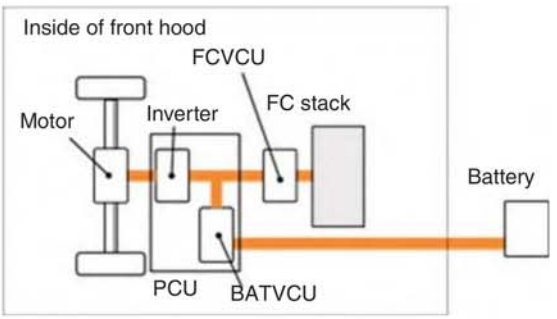

Figure 16.7 New FCV electric power plant.

In the electric power plant system, the output voltage from the FC stack is boosted by the FCVCU and supplied to the traction motor inverter. This made it possible to achieve higher motor output and reduce the number of FC stack cells, creating a vehicle system that is compact and lighter weight.

16.3.3 FCVCU

In the 2009 model, the FC stack output section was connected directly to the traction motor inverter. In the new model FCV, the number of FC stack cells has been reduced by approximately 30% compared to the 2009 model. This results in lower FC stack output; however, the voltage boost provided by the FCVCU increases the inverter drive voltage to a maximum of 500 V. This achieves higher maximum motor output, which was increased from 100 to 130 kW (Table 16.1).

16.3.3.1 Circuit Configuration

Figure 16.8 shows the FCVCU circuit diagram. The primary components are the intelligent power module (IPM), reactor, and smoothing capacitor. It also contains a 4-phase interleave circuit consisting of four single-phase chopper circuits in parallel [12]. The IPM is a full SiC-IPM composed of SiC-SBD and SiC-field-effect transistor (FET) next-generation power semiconductors, and the voltage control unit (VCU) achieves high efficiency through smaller passive component sizes and reduced loss achieved by increasing the frequency to above the audible range. Further reduction in size was achieved by adopting a 2-phase magnetic coupling reactor composed of a 2-phase reactor with a single core [13]. The secondary-side smoothing capacitor uses an indirect water cooling structure in consideration for generated heat (Table 16.2).

16.3.3.2 Full SiC-IPM

With Si, IGBT and other minority carriers were primarily used in order to improve the increase in on-resistance resulting from higher withstand voltages. However, these components suffered from the problem of large switching losses, and as a result there were limits on high-frequency drive due to the generated heat. The FCVCU uses a full SiC-IPM as well as a high-speed device structure with SiC-SBD and SiC-FET majority carrier devices. This results in lower loss compared with the Si-IGBT and Si-FWD that were used in previous models (Figure 16.9). In particular, the large reduction in switching loss makes higher frequencies possible (Figure 16.10).

Table 16.1 Major specifications.

Model	New FCV	2009 model
Length/width/height	4915 × 1875 × 1480 mm	4845 × 1845 × 1470 mm
Wheel base	2750 mm	2800 mm
Vehicle weight	1890 kg	1630 kg
Number of passengers	5	4
Maximum motor power	130 kW (177 PS)	100 kW (136 PS)
Maximum motor torque	300 Nm (30.6 kgm)	256 Nm (26.1 kgm)
Fuel cell stack	PEFC[a)]	PEFC[a)]
Power assist	Li-ion battery	Li-ion battery
Hydrogen supply system	High-pressure hydrogen tank	High-pressure hydrogen tank
Hydrogen filling pressure	70 MPa	35 MPa
Hydrogen storage volume	141 l	171 l
Driving range	750 km[b)]	620 km[c)]

a) Polymer electrolyte fuel cell.
b) JC08 mode.
c) 10/15 mode.

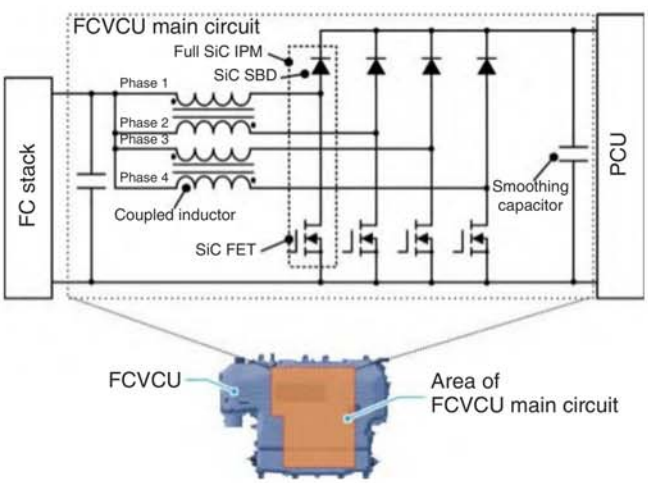

Figure 16.8 FCVCU circuit.

16.3.3.3 Magnetic Coupling and Interleave Operation

A 2-phase magnetic coupling reactor is used, with Phase 1 and Phase 2 constituting one pair, and Phase 3 and Phase 4 constituting the other. The use of two reactors produces a 4-phase configuration. Each phase wraps a single core with two coils, reducing DC magnetic flux by applying current so that the magnetic fluxes generated by DC current in the core are oriented in opposite directions to each other. Displacing

Table 16.2 Specifications of FCVCU.

Item	Specification
Max output power	100 kW
Max boost voltage	500 V
Volume	15.8 l
	*FCVCU main circuit
Circuit system	4-phase interleave
Power module	Full SiC
Inductor	2-phase magnetic coupling
Capacitor	Indirect water cooling

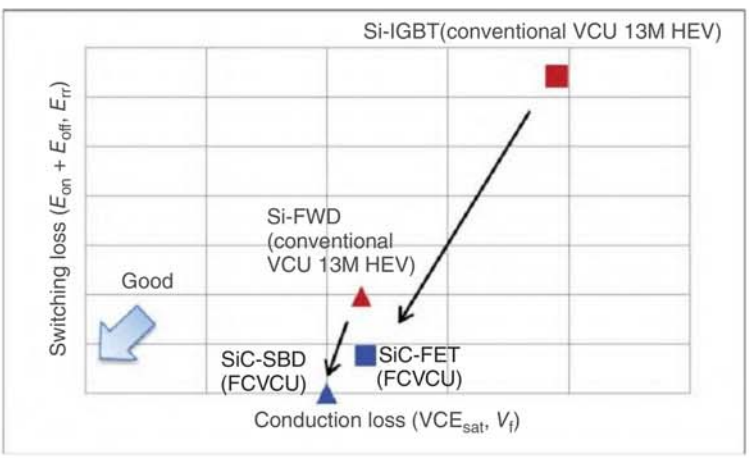

Figure 16.9 Power loss in semiconductor device.

the switching timing of the coupled phases by 180° also reduces the AC component. The effects of the former allow a smaller reactor size, and the effects of the latter causes the ripple currents of the 4-phase reactor to cancel each other out, allowing a smaller smoothing capacitor. Figure 16.11 shows the switching waveform and phase current waveform for each phase in the 4-phase interleave circuit. The phases that operate displaced by 90° from each other in the following order: Phase 1 → Phase 3 → Phase 2 → Phase 4. This causes the ripple currents generated by each phase to cancel each other out, reducing the composite ripple of the four phases.

16.3.3.4 Control Methods

In order to perform a high-efficiency voltage conversion with a multiphase converter, it is preferable to switch the number of operating phases according to the operating conditions. Where to set the points for switching the number of operating phases is related to the FCVCU input voltage, output voltage, and input current. The FCVCU

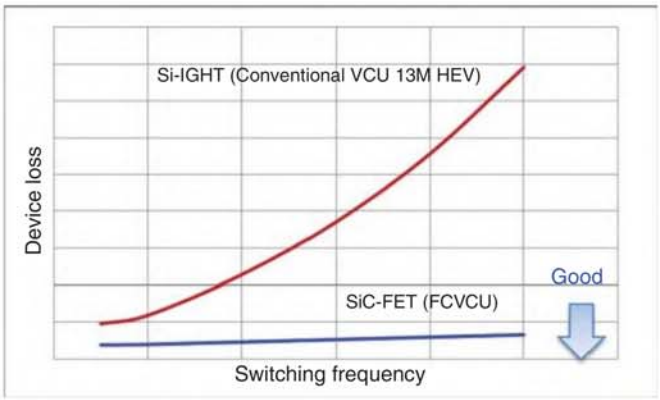

Figure 16.10 Switching loss in semiconductor device.

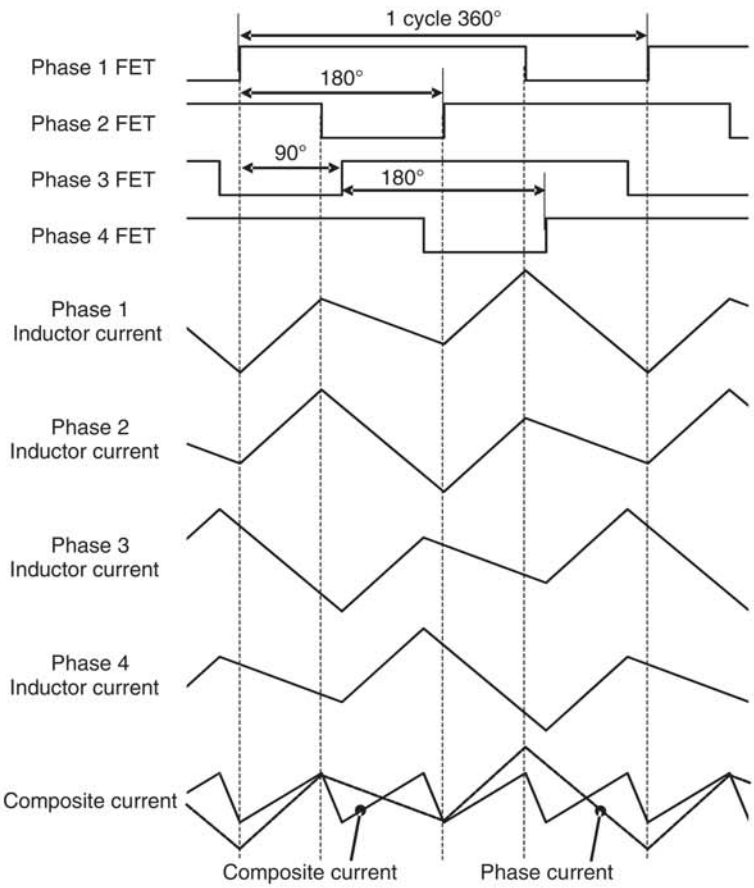

Figure 16.11 Switching waveform.

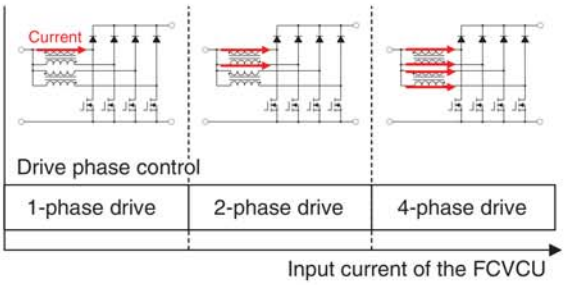

Figure 16.12 Image of drive phase control.

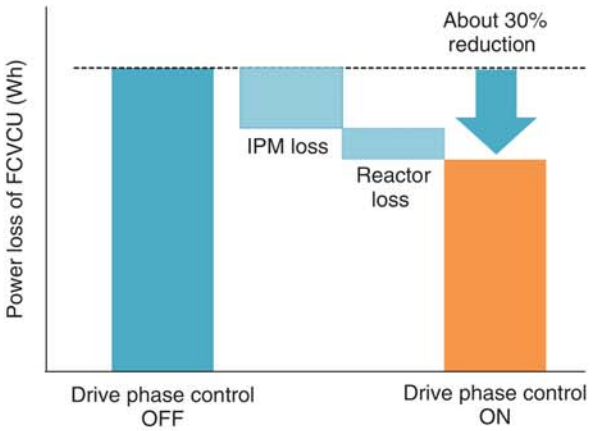

Figure 16.13 Effects of drive phase control.

sets a number of operating phases that is suitable for the above three parameters in advance and performs control that switches the number of operating phases based on the input current value. By setting switching points in this way, it is possible to achieve efficient control while using only the current as the monitoring parameter. However, 3-phase operation is not performed with this control. As described above, the reactor is a 2-phase magnetic coupling reactor and it is necessary to apply equal current to the two coupled phases. For example, if phase switching control operated at three phases (Phase 1 to Phase 3), because no current would be applied to Phase 4 that is coupled to Phase 3, the effects of the magnetic coupling would be lost and the Phase 3 ripple current would increase compared to Phase 1 and Phase 2. As a result, if operation continues with three phases, Phase 3 will generate an increasing amount of heat. In order to avoid this, the control that switches the number of operating phases selects 1-phase, 2-phase, or 4-phase operation and does not perform 3-phase operation, (Figures 16.12 and 16.13).

16.3.3.5 Effects on Smaller Size and Higher Efficiency

Figure 16.14 shows the effects on downsizing the FCVCU. The use of full SiC-IPM, a magnetic coupling reactor, and cooled capacitors achieves an overall FCVCU size that is approximately 40% smaller than previous technologies. Figure 16.15 shows the effects on increased FCVCU efficiency. For the same output, loss is reduced by approximately 70% compared to the HEV (13M HEV) VCU in the previous 2013 model, achieving both smaller size and higher efficiency [14].

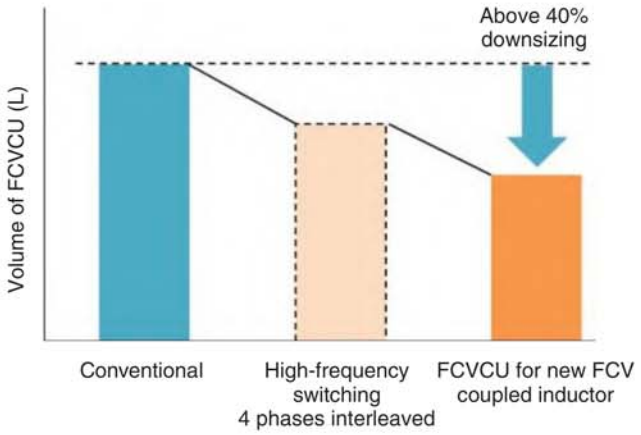

Figure 16.14 Downsizing effect on FCVCU.

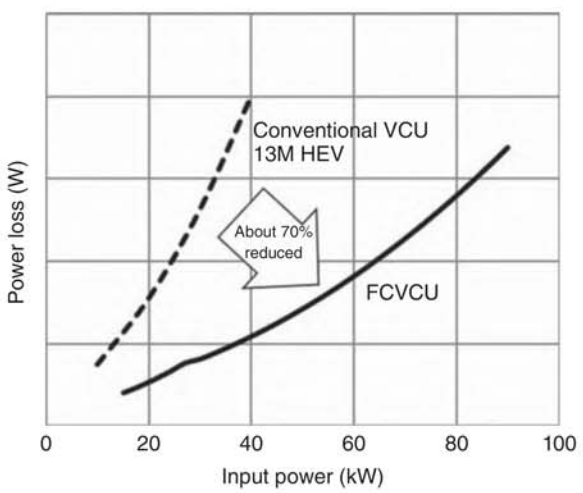

Figure 16.15 Power loss comparison with conventional VCU.

16.3.3.6 Quietness

Ordinarily, the inverter and converter in an electric vehicle are driven at a switching frequency that is within the audible range (generally 20 Hz to 20 kHz), and measures are needed to counter the high-frequency noise that is generated by the reactor and capacitors. Because the FCVCU uses a SiC-IPM, it is capable of driving at higher frequencies than before. Driving the inverter and converter at frequencies higher than 20 kHz produces drive noise that is inaudible to human beings and contributes to improving vehicle quietness.

16.3.3.7 Noise Countermeasures

In order to ensure voltage boost operation, switching operation in the chopper circuit is used to produce a drive voltage waveform that has a trapezoidal wave with prescribed, limited rise time t_r (Figure 16.16). The use of SiC makes it possible to set higher switching frequencies than conventional Si, shortening the transition

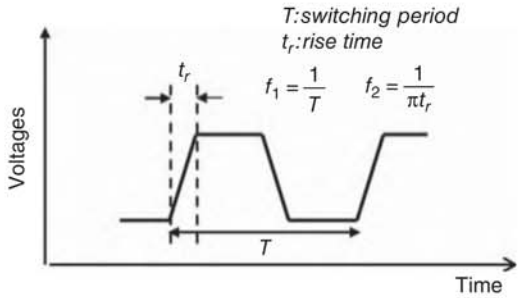

Figure 16.16 Schematic of voltage waveform resulting from voltage boost.

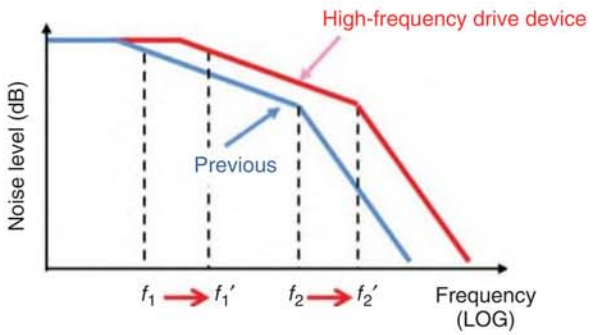

Figure 16.17 Change in higher harmonic trapezoidal wave resulting from high-frequency drive.

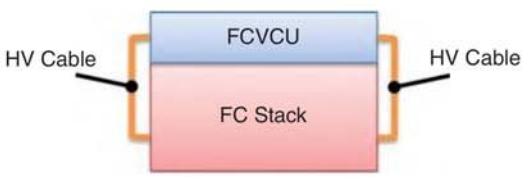

Figure 16.18 High-voltage cable layout of FC stack and FCVCU.

time (t_r) resulting from the higher switching frequencies. As a result, the noise level is as shown in Figure 16.17, and the frequency of the generated noise is higher. Because the FC stack uses a structure in which there are electric output terminals on both sides of the stack, the output terminal positive and negative electrodes are largely separated. From a noise perspective, this increases the size of the current loop on the power input side and tends to increase the noise that is radiated from it (Figure 16.18). Therefore in this development, we placed a Y capacitor (ground capacitor) on the FCVCU high-voltage primary side (FC stack side) as a noise countermeasure. The electrostatic capacitance of the Y capacitor was set to a lower value than previous models in order to counter high-frequency noise.

16.3.3.8 Structure of the FCVCU

By placing the FCVCU on top of the FC stack, it is possible to ensure the same bottom surface area as the FC stack. However in terms of height, it is necessary to place the FCVCU in a position that secures the necessary clearance from the front hood in order to satisfy the requirements for pedestrian collision protection performance. This means that the components must be positioned below this position, and it was therefore decided to create a thin design. Figure 16.19 shows the cross

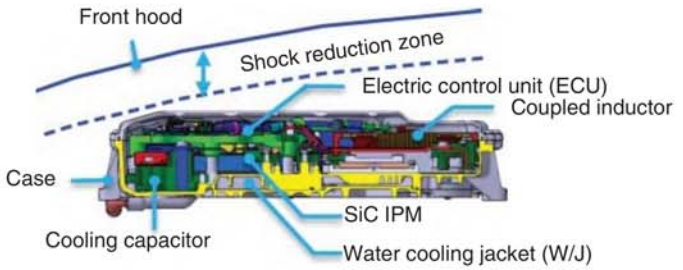

Figure 16.19 Cross section of FCVCU.

Figure 16.20 FCVCU components.

section of the FCVCU. Figure 16.20 shows an exploded view of the FCVCU components. In order to reduce the FCVCU height, a thin design and parallel layout are used for the 4-phase reactor with 2-phase magnetic coupling. The 4-phase SiC-IPM is mounted next to the reactor, and furthermore the secondary-side smoothing capacitor is mounted next to the 4-phase SiC-IPM so that they are positioned on the same horizontal plane within the VCU case. In addition, the size and the position of the electric control unit (ECU) were adjusted so that it could be placed below the target line which traces the front hood.

16.3.4 Conclusions

The following two approaches were used to achieve reduced size during the development of the FCVCU for the new model FCV.

(1) The high-frequency drive using a SiC-IPM and the 4-phase interleave circuit resulted in smaller capacitors and reactor.
(2) The reactor was further downsized through the use of 2-phase magnetic coupling.

As a result, this reduced the size of the fuel cell voltage-boost converter and enabled us to achieve the objective of installing the FCVCU on the FC stack inside the vehicle front hood. This also achieved high output of 100 kW and volume of 15.8 l. The higher output and technologies for a more compact, thinner design of

this FCVCU contributed to improving the drive performance, fuel economy, and product appeal of the new model FCV.

16.4 Development of Module Technologies to Bring Out SiC Power Device Performances (TOYOTA MOTOR CORPORATION)

16.4.1 Power Card Structure for Double-Side Cooling Technology

To take full advantage of the inherent high-frequency switching of SiC devices and the ability to use them at 200 °C or higher temperature, new technologies are required for mounting. For example, in a module, a parasitic inductance and a parasitic capacitance should be small so that the characteristics can be utilized, and a highly reliable configuration at a high temperature is required. The current fourth-generation Prius uses a 2-in-1 power card, realizing a compact, high-heat dissipation inverter [15]. In this power card, the upper-arm IGBT and diode and the lower-arm IGBT and diode are contained in one card. Initially, we examined the U-shaped structure shown on the upper left side of Figure 16.21, which has a simple structure. However, it was found that the placement of the chips on the left side and the right side upside down, making soldering difficult. Therefore, as shown in the upper right of Figure 16.21, an N-type structure was adopted, in which the chips could be arranged in the same direction. The N-type requires a joint to connect the left and right, but the soldering process is the same for the left and right chips, making it easier. In this structure, solder is used for joining; therefore, improvement of high-temperature resistance of resin and solder and reduction of parasitic inductance are key issues.

16.4.2 New Transient Liquid Phase Structure for High-Temperature Applications

As for bonding materials, development of new bonding technologies such as silver sintering and transient liquid phase (TLP) bonding is underway [16]. A structure in which an Al sheet with a thickness of about 100 μm is inserted into the TLP layer has been developed. It has become possible to decrease the stress which impacts TLP. Figure 16.22 shows a schematic of TLP bonding process. Sn layer is placed between nickel layers by sputtering or plating. These layers are heated to 300 °C with pressuring of 0.5 MPa. The only Sn layer melts at this temperature. Then, tin and nickel start to diffuse into each other. After the diffusional reaction is completed, Sn layer changes into Ni_3Sn_4 intermetallic compound (IMC). The melting point of TLP layer is about 800 °C. This structure has high-temperature resistance. TLP layer is very stiff, so power device was cracked after power cycle test. Lower part of Figure 16.22 shows the countermeasure for this issue. Aluminum sheet was placed between TLP layers as a buffer layer for thermal stress. We call this method TLP-Ai (TLP bonding with aluminum interlayer).

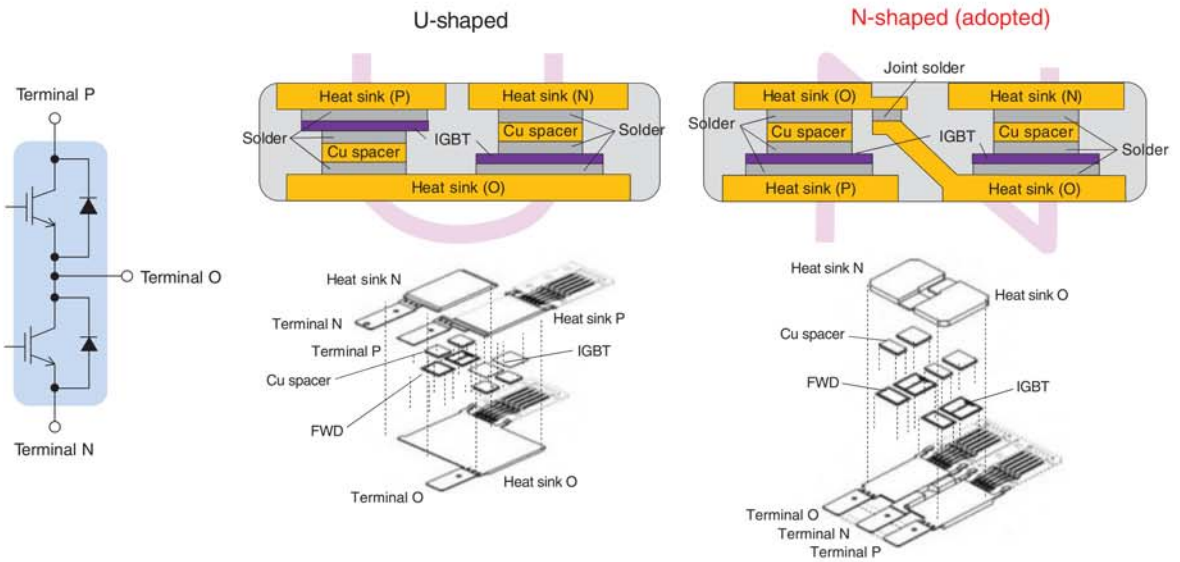

Figure 16.21 Structure of 2-in-1 power card.

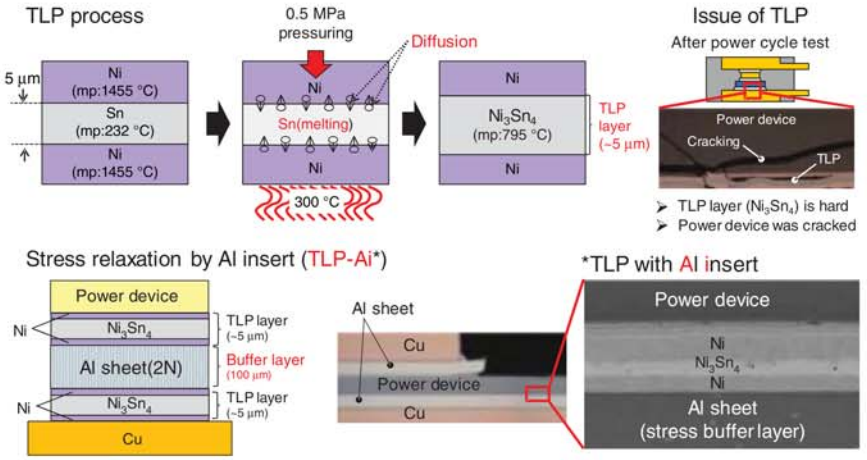

Figure 16.22 TLP bonding for power module.

16.4.3 Ni Micro-Plating Bonding

We developed a packaging technology which is called "Ni Micro-Plating Bonding (NMPB)" for SiC power module. That is one of the achievements of Strategic Innovation Promotion Program (SIP: 2014–2019), Japanese National Project. The leader of this project was Professor Tatsumi of Waseda University [17]. The die bonding and the wire bonding can be simultaneously bonded by nickel plating, so that the degree of freedom in designing the module is greatly improved. And also the high-temperature resistance of the bonding is significantly improved. The lead surface was designed to have chevron shape specially for NMPB. Structure of 2-in-1 module in this research and cross-sectional view of chevron-shaped lead frame are shown in Figure 16.23. The strong bonding interface was achieved thanks to this chevron shape. The plating solution was selected for the process of NMPB which has a property of preferentially plating a narrow gap.

Not only the miniaturization of the module is promoted, but also noise reduction is studied, which is a problem when the frequency is increased. And the heat

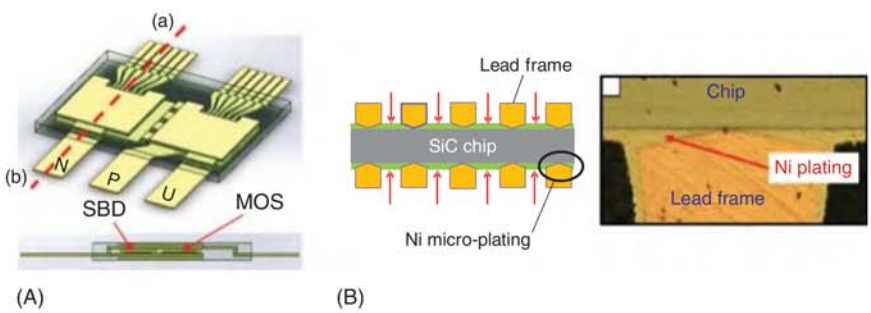

Figure 16.23 Ni micro-plating bonding (NMPB) technology. (A) Structure of 2-in-1 module and (B) cross section of NMPB.

radiation property should be improved because it is reduced due to the miniaturization. For these reasons, it is necessary to review the configuration of the entire inverter instead of simply replacing the Si element with the SiC element. Keio University proposed a circuit configuration to reduce common mode noise [18]. In this study, a full-bridge inverter circuit configuration was proposed (Figure 16.24). The wiring from the inverter to the motor was constructed by pairing cables with currents in completely opposite layers to cancel noise. Since the noise from the wiring is suppressed and the configuration is a full bridge, the noise due to the common mode is theoretically not generated. As a contradiction, there is a cost increase using the chip 4/3 times, but it can be expected that the cost of noise protection can be reduced by noise reduction, so it will not increase significantly. For example, at present, the wiring from the inverter to the motor is covered and shielded with a metal tube, but it is expected that such noise protection will not be necessary or can be simplified. In addition, it has been pointed out that it is necessary to make the characteristics of the paired chips uniform because the switching timing shift due to the variation in the characteristics of the chips is a factor of generating noise.

As the cost reduction of SiC devices progresses, many electric vehicles will use SiC. In addition, by adopting new technologies that can bring out the inherent characteristics of SiC devices, such as module and circuit configuration, the benefits of

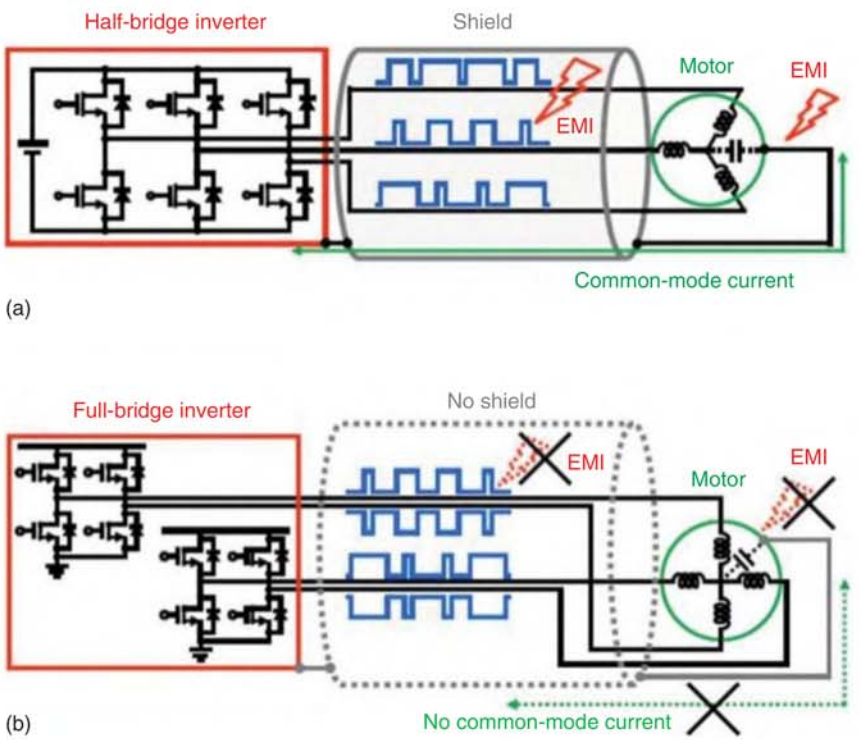

Figure 16.24 Inverter circuits. (a) Conventional half bridge inverter circuit and (b) EMI-less full-bridge inverter circuit.

SiC devices will be even greater. With regard to the electrification of aircraft, which is attracting attention now, the merit of weight reduction is even greater than that of automobiles. So, the merits to apply SiC devices are significantly large compared to automobile.

16.5 SiC-MOSFET Switching Characteristics and Gate Driver Circuits for Automotive Application (NISSAN MOTOR CO., LTD.)

16.5.1 Introduction

Since the switching speed of SiC-MOSFETs is faster than that of Si-IGBTs, the former has the potential to provide lower switching loss and higher efficiency. However, high-speed switching of SiC-MOSFETs causes electromagnetic interference (EMI) and voltage and current surges. This section discusses the switching characteristics and gate driver circuits for EV/HEV applications.

16.5.2 Basics of Switching Characteristics

Figure 16.25 shows a 3-phase inverter circuit which has been commonly adopted for the traction inverters used on many of the EVs/HEVs commercialized to date. A double-pulse test circuit like that shown in Figure 16.26 is used to measure the switching characteristics of one phase of 3-phase inverters. The test circuit can measure the switching characteristics of the lower-arm transistor and the recovery characteristics of the upper diode. Schematic waveforms of the gate–source voltage (V_{gs}), drain–source voltage (V_{ds}), and drain current (I_d) of the lower-arm transistor

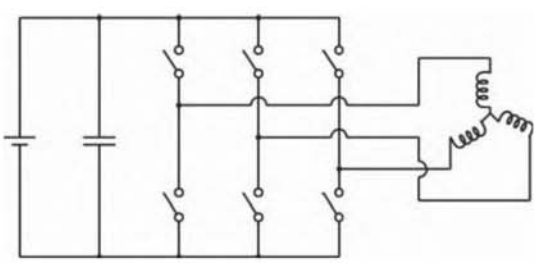

Figure 16.25 Three-phase inverter circuit for EVs/HEVs.

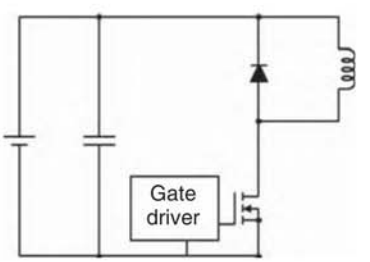

Figure 16.26 Double-pulse test circuit.

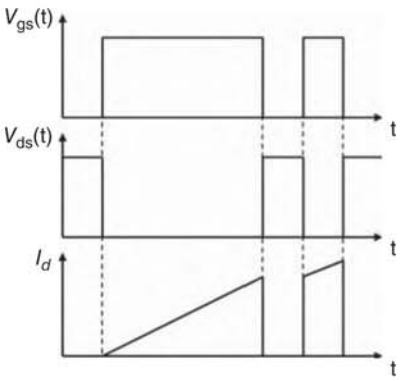

Figure 16.27 Schematic waveforms in double-pulse test.

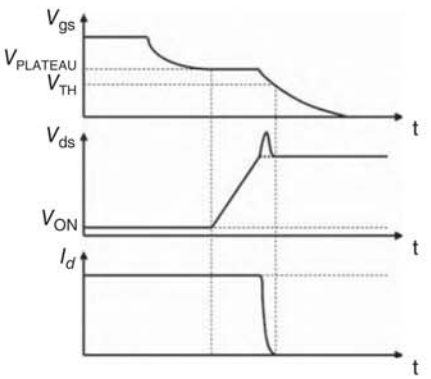

Figure 16.28 Schematic waveforms of the turn-off characteristics.

obtained in a double-pulse test are shown in Figure 16.27. Turn-off and turn-on characteristics at the required current are measured by turning off and on the transistor at the specified current.

Figures 16.28 and 16.29 show schematic waveforms of the turn-off and turn-on characteristics of V_{ds}, V_{gs}, and I_d. Parasitic inductance of the power loop consisting of the DC link capacitor, the transistor, and the diode in Figure 16.26 affects the switching waveforms. If the parasitic inductance is ideally zero, the V_{ds} waveform resembles the dotted line in Figures 16.28 and 16.29. However, since the actual parasitic inductance of the inverter is from several nanohenry to several tens of nanohenry, the V_{ds} waveform resembles the solid line in the figures. At turn-off, firstly V_{ds} increases as V_{gs} decreases. After V_{ds} becomes the same as the supply voltage, current starts to flow to the diode and I_d begins to decrease. V_{ds} increases and excessive voltage is applied to the transistor while I_d decreases because of $L\mathrm{d}I/\mathrm{d}t$, where L is the parasitic inductance. At turn-on, firstly I_d begins to increase as V_{gs} increases. During the increase in I_d, V_{ds} decreases because of $L\mathrm{d}I/\mathrm{d}t$. After I_d becomes the same as the load current, V_{ds} starts to decrease. The reverse recovery current (I_{rr}) of the diode is added to I_d. Subsequently, a sudden change in $\mathrm{d}I/\mathrm{d}t$ may cause a voltage surge and current ringing with the resonant circuit formed by the parasitic inductance and the capacitance of the diode.

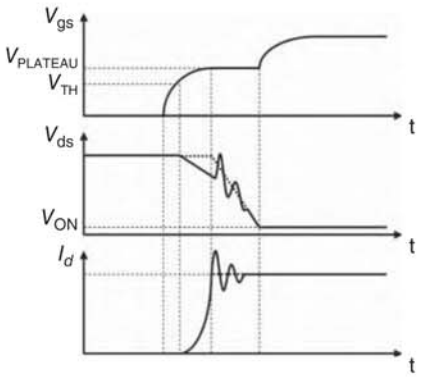

Figure 16.29 Schematic waveforms of the turn-on characteristics.

16.5.3 Various Gate Driver Circuits

To suppress voltage surge at turn-off and ringing at turn-on, the gate resistance (R_g) of the gate driver circuit is sometimes increased. A conventional gate driver circuit is shown in Figure 16.30. The gate current can be limited by increasing the gate resistance. As a result, dI/dt decreases and voltage surges and ringing can be suppressed. However, increasing the gate resistance leads to a longer switching time and higher switching losses. One proposed way of overcoming this trade-off is to add a speed-up capacitor (C_g) connected in parallel to the gate resistance as shown in Figure 16.31 [19, 20]. The speed-up capacitor increases the gate current at the beginning of switching, thereby reducing switching losses. After that, the gate current is reduced gradually to suppress the voltage surge and ringing.

Figure 16.30 Conventional gate driver circuit.

SiC
MOSFET

R_g

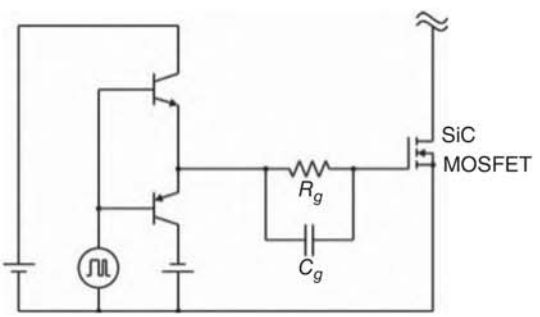

Figure 16.31 Gate driver circuit with speed-up capacitor.

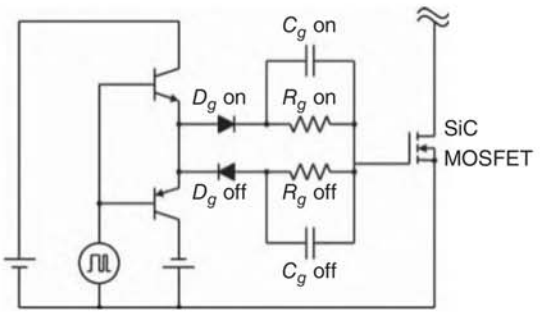

Figure 16.32 Gate driver circuit with gate current paths separated by diodes.

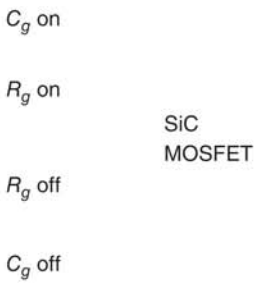

Figure 16.33 Gate driver circuit with gate current paths separated by output terminals of push–pull transistors.

The circuit in Figure 16.32 also has gate current paths for turn-off and turn-on that are separated by diodes (D_g off and D_g on), enabling the gate resistances (R_g off and R_g on) and speed-up capacitances (C_g off and C_g on) to be optimized for turn-off and turn-on. The circuit in Figure 16.33 is proposed for eliciting the high-speed switching potential of SiC-MOSFETs [21]. The output terminals of the push–pull transistors are separated, enabling the gate resistances (R_g off and R_g on) and speed-up capacitances (C_g off and C_g on) to be optimized for turn-off and turn-on. In addition, the voltage drop at the diodes (D_g off and D_g on) can be eliminated and parasitic inductances in the gate current path can be suppressed compared with the circuit in Figure 16.32.

Figures 16.34 and 16.35 present experimental results obtained with the circuit in Figure 16.33 for turn-off and turn-on at V_{ds} of 200 V and I_d of 40 A. The relationship between turn-off loss and voltage surge is shown in Figure 16.34. The reference gate driver indicated by the dashed line in Figure 16.34 was adjusted only by R_g off. The proposed gate driver indicated by the solid line in the figure was adjusted only by C_g off with fixed R_g off of 20 Ω. The results indicate that the proposed gate driver can reduce turn-off loss by 65% at the same level of surge voltage compared with the loss obtained by adjusting only R_g off of the reference gate driver. The relationship between turn-on loss and current surge is shown in Figure 16.35. The reference gate driver indicated by the dashed line in Figure 16.35 was adjusted only by R_g on. The proposed gate driver indicated by the solid line in the figure was adjusted only by C_g on with fixed R_g on of 20 Ω. The results indicate that the proposed gate driver can reduce turn-on loss by 29% while maintaining surge current equal to that of the reference gate driver.

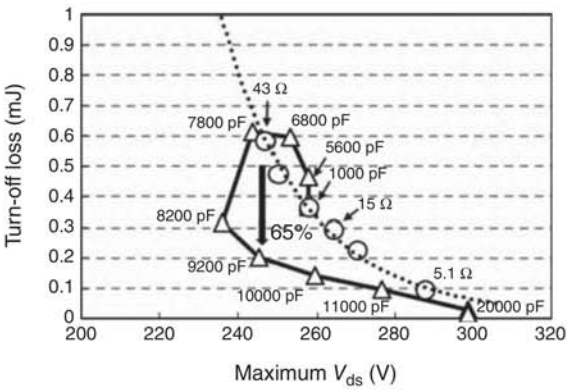

Figure 16.34 Turn-off loss as a function of maximum V_{ds}.

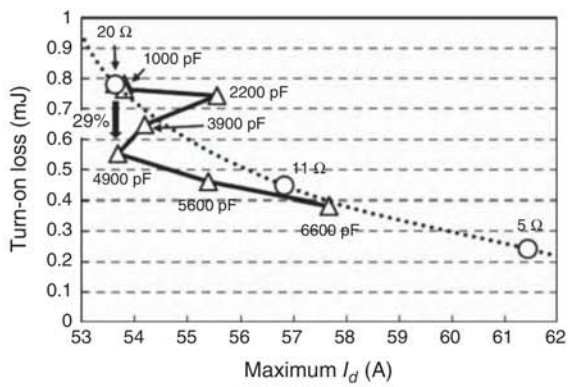

Figure 16.35 Turn-on loss as a function of maximum I_d.

16.5.4 Conclusion

As discussed here, these auxiliary technologies not only enable high-speed switching of SiC-MOSFETs but also solve the issues of EMI and voltage and current surges, which is essential for applying SiC-MOSFETs to EVs/HEVs.

16.6 R&D of SiC Power Devices for Automotive Applications (DENSO CORPORATION)

16.6.1 Introduction

To prevent global warming, the regulation of CO_2 emissions has become stricter over the past several decades. Therefore, the electrification of automotive power train systems has become a global trend, and the popularization of environmentally friendly vehicles, such as HEVs, PHEVs, and EVs powered via batteries, among others has increased. For next-generation HEVs, PHEVs, and EVs, more compact, efficient, and low-cost invertor units are required. SiC power semiconductor devices are expected to be applicable in such units. In automotive invertor units with output powers of approximately 100 kW, MOSFET chips composed of SiC that possess a

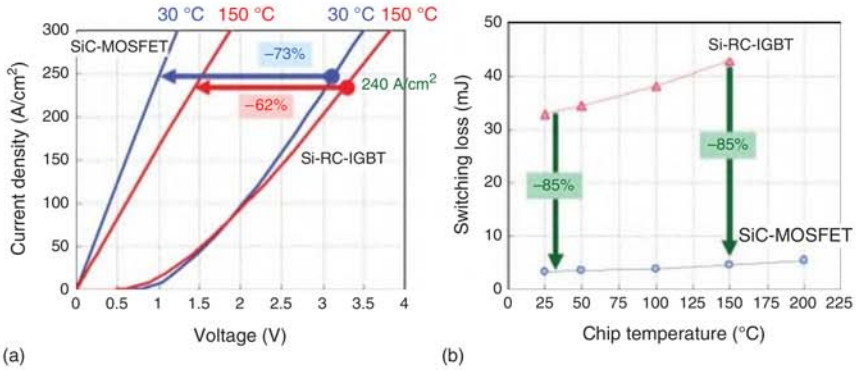

Figure 16.36 Device characteristics comparisons between the Si-IGBT and SiC-MOSFET. (a) Current–voltage characteristics and (b) switching loss.

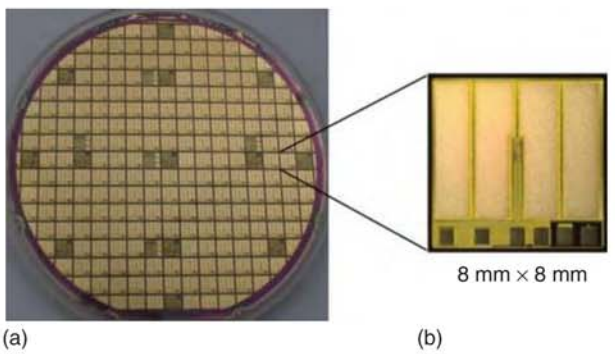

Figure 16.37 (a) An SiC-MOSFET wafer with $\phi = 150$ mm and (b) an 8 mm × 8 mm SiC-MOSFET chip.

breakdown voltage of 600–1200 V and a rated current of 100–600 A are required. Such SiC-MOSFETs that are superior to the Si IGBTs used in conventional automotive invertor units have been realized, as shown in Figure 16.36. SiC-MOSFET chips with sizes of 8 mm × 8 mm on a 150-mm-diameter SiC wafer have also been fabricated as R&D samples, as shown in Figure 16.37. These SiC chips are equipped with current and temperature sensors, similar to conventional Si chips, to ensure their safe operation in automotive systems. Through experimentation involving the replacement of the inverter unit of a commercial HEV with SiC-MOSFETs, the mileage of these vehicles was effectively improved (http://newsroom.toyota.co.jp/jp/detail/2657262). SiC-MOSFETs were subsequently used in conjunction with boost converters and in the inverters of commercial vehicles such as FCVs and some EVs (http://newsroom.toyota.co.jp/en/detail/5725437; http://www.honda.co.jp/factbook/auto/CLARITY_FUEL_CELL/201603/P14.pdf).

To ensure a further increase in the use of SiC power devices in commercial vehicles, the reliabilities of these devices must be improved and their associated costs must be reduced. The evaluation and analysis of the influence of crystal dislocations

in SiC wafers is required to guarantee the long-term lives of these SiC devices in the severe operation environments in vehicles, as well as to ensure that accidental failure does not occur.

In addition, these SiC wafers with 150-mm diameters may be mass-produced via automated line processes, such as those used for Si devices. However, the cost of SiC devices is currently several times higher than that of Si devices. These costs must therefore be reduced to permit the application of SiC devices in automobiles.

In the following section, the R&D of SiC power devices in terms of their automotive applications from the DENSO CORPORATION is described.

16.6.2 Ultra-Low-Loss SiC-MOSFET for Cost Reduction

The realization of the required current capacity in a small-sized chip is important to achieve low-cost SiC-MOSFETs. Therefore, trench-gate-type MOSFETs was developed in this study. It is necessary to apply SiC-MOSFETs in the vehicles to further improve their on- and off-state characteristics, in addition to their long-term reliability. Compared with other Si devices, SiC has a high breakdown field (about 10 times higher than that of Si), and it is therefore important to reduce the gate oxide field. Although several groups have already reported original structures that may be used to decrease the gate oxide field, these structures may increase the junction gate field-effect transistor (JFET) resistance of these devices. SiC-MOSFETs that outperform the theoretical limits of Si unipolar devices have recently been demonstrated [22–24] (http://global-sei.com/technology/tr/bn80/pdf/80-16.pdf). However, there remains room for improvement in the trade-off between the on-resistance and the breakdown voltage.

In this study, we focus on improving the trade-offs between the on-resistance ($R_{on}A$) and the gate oxide field (E_{OX}). An original structure to suppress the gate oxide breakdown at the off-state is proposed. The remarkable on-state characteristics of the developed 4H-SiC trench MOSFETs with original structures will be demonstrated, while their high breakdown voltage will be maintained.

16.6.3 Proposed 4H-SiC Trench MOSFET Structure

Figure 16.38a,b show the 3D schematic views of the conventional 4H-SiC trench MOSFET (https://www.denso.com/jp/ja/products-and-services/industrial-products/sic) and the proposed Deep-P encapsulated 4H-SiC trench MOSFET, respectively. Both MOSFETs have a p-region, referred to as Deep-P, under the trench that serves to protect the gate oxide at the bottom of the trench from the high electric field in the off-state. The conventional MOSFET has a Deep-P structure (PDS) parallel to the trench gate, while the proposed MOSFET has an orthogonal Deep-P structure (ODS) [25].

For devices with a PDS, it is difficult to reduce the JFET resistance (R_{JFET}) because the current paths of the JFET resistance depend on the cell pitch of the transistor. In contrast, the pitch of the Deep-P region in an ODS can be designed freely without depending on the cell pitch. The key area in an ODS is the space between the Deep-P

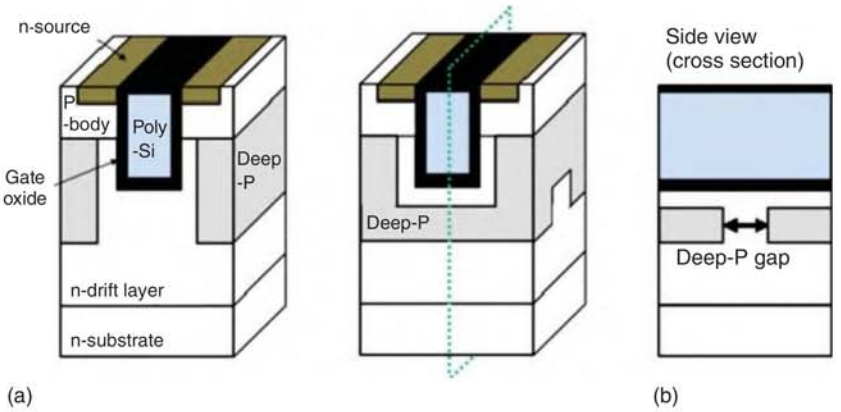

Figure 16.38 3D sketch of (a) the conventional structure and (b) the proposed structure (Deep-P encapsulated 4H-SiC trench MOSFET).

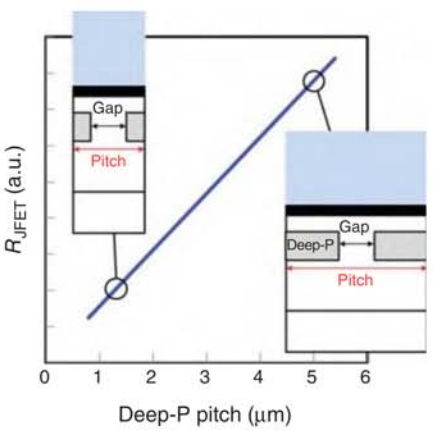

Figure 16.39 Relationship between the on-resistance and the Deep-P pitch. The concentration and gap of the Deep-P are constant.

region and the trench that permits the distribution of electrons from the channel region. In the case of an ODS without such a space, the Deep-P region will contact the bottom of the trench, and the electrons from the channel region will not be well distributed because the electron path is limited by the Deep-P region. Thus, it is important to separate the Deep-P region from the bottom of trench to reduce the on-resistance.

Figure 16.39 shows the simulated results of the relationship between the Deep-P pitch and the JFET resistance. The JFET resistance generally decreases as the Deep-P pitch is reduced because the density of the current paths increases (in the case of a constant Deep-P gap and concentration). Figure 16.40 shows the dependence of the JFET resistance and the gate oxide field on the gap between the Deep-P regions calculated by the device simulator. Selecting a suitable Deep-P gap results in a low JFET resistance without increasing the gate oxide field. Therefore, an adequate Deep-P gap and reduced Deep-P pitch result in a low JFET resistance.

In addition, to reduce the switching loss, it is important to reduce the gate–drain capacitance and gate–drain charge. The electric potentials and depletion regions

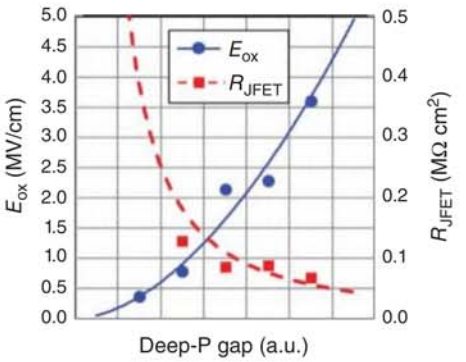

Figure 16.40 Dependence of the JFET resistance and gate oxide field on the gap between the Deep-P regions. The concentration and width of the Deep-P region are constant.

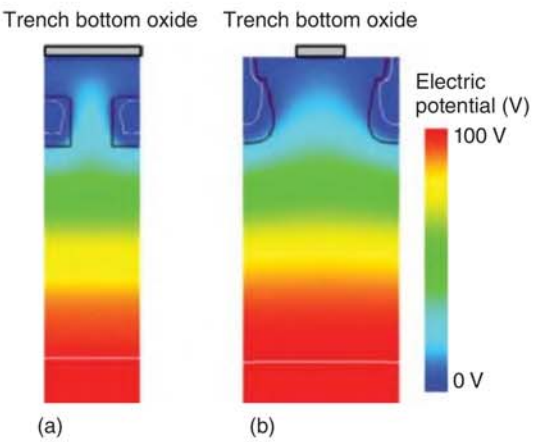

Figure 16.41 Electric potentials of the (a) front view of the conventional structure and (b) side view of the presented structure at $V_d = 100$ V and $V_g = 0$ V.

of the conventional and presented MOSFETs were calculated using a device simulator [26]. Figure 16.41a,b show the electric potentials of the conventional and proposed structures, respectively, under a drain voltage of 100 V and a gate voltage of 0 V. The depletion region for each structure expands toward the drift region to almost the same depth. Compared with the conventional structure, the presented structure possesses a non-depleted Deep-P region under the trench gate oxide. The non-depleted region acts as the shield against the drain bias, which can reduce the effective gate–drain capacitance area. Therefore, a low gate–drain capacitance and low gate–drain charge are achieved in the proposed structure. This cell construction inherently has a small ratio of the gate–drain charge with respect to the gate–source charge. This feature is essential to suppress the parasitic turn-on phenomena that may cause the fatal failure of these devices in applications using the half bridges. In addition, the presented structure can avoid the switching delay of the Deep-P charge by connecting the Deep-P region closely to each P-base region [27].

The Deep-P gap should be selected to retain a low JFET resistance and a low gate–drain capacitance. Figure 16.42 shows the simulated results of the dependences of the gate–drain capacitance and the JFET resistance on the Deep-P gap. As can be seen in Figure 16.42, while the gate–drain capacitance increases by increasing the Deep-P gap, the JFET resistance, which directly affects the conduction loss,

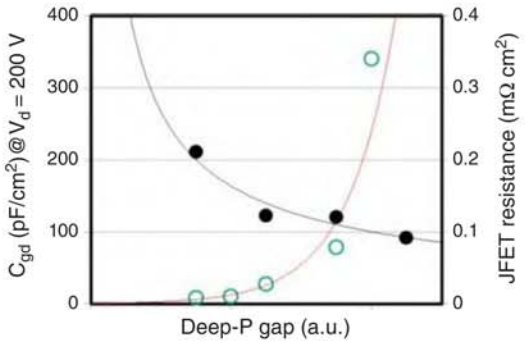

Figure 16.42 Deep-P gap dependences of C_{gd} and JFET resistance.

decreases. For DC–DC converter or high-speed applications, it is more important to reduce the switching losses rather than the conduction losses, and a low gate–drain charge is generally the best choice for minimizing the switching losses. Therefore, it is considered that a narrow Deep-P gap is preferable. In contrast, a wide Deep-P gap is suitable for low-speed applications because the reduction of the conduction losses is more important than that of the switching losses. In that case, the Deep-P gap is limited up to the acceptable level of electric field crowding at the gate oxide. Therefore, the device design can be optimized by selecting an appropriate Deep-P gap for each specific application without the modification of the channel layout.

16.6.4 Characteristics of the Developed MOSFET

16.6.4.1 Static Characteristics of the Optimized Structure

By utilizing the optimized conditions, 4H-SiC trench MOSFETs with an ODS were fabricated. Figure 16.43a,b show the on-state forward I_d–V_{ds} characteristics at

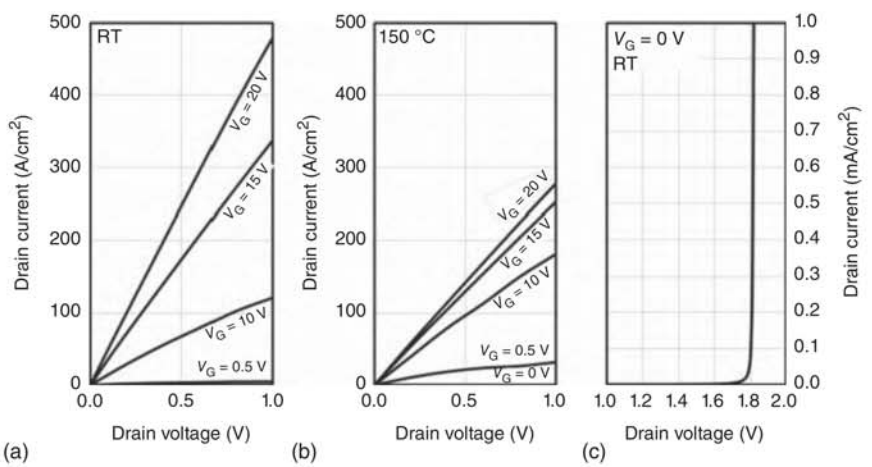

Figure 16.43 On- and off-state characteristics of the fabricated MOSFET with an optimized Deep-P gap at room temperature and 150 °C. (a) On-state characteristics at room temperature. (b) On-state characteristics at 150° C. (c) Off-state characteristics at room temperature.

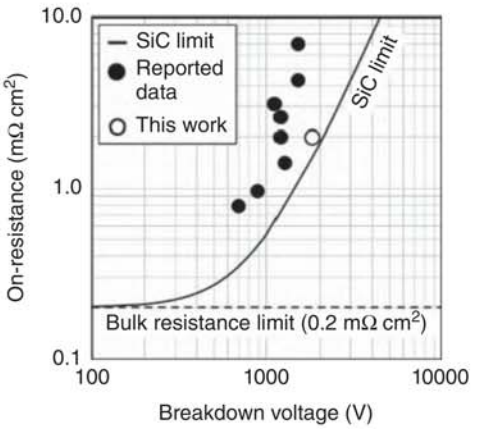

Figure 16.44 Plot of the breakdown voltage vs. the on-resistance for 4H-SiC MOSFETs.

room temperatures and 150 °C for this device. The measured specific on-resistance was 2.04 mΩ cm^2 at room temperature and 3.47 mΩ cm^2 at 150 °C. The specific on-resistances were calculated at a gate voltage of 20 V and a drain current of 300 A/cm^2. The breakdown voltage at room temperature was above 1800 V, as shown in Figure 16.43c. The specific on-resistance of the conventional structure was 3.5 mΩ cm^2 (not shown). A significantly low on-resistance could be achieved by applying an ODS with miniaturized patterns without deteriorating the off-state characteristics.

Figure 16.44 shows the plot of the breakdown voltage vs. the on-resistance for 4H-SiC MOSFETs. The plot shows the experimental results obtained in this work and the reported data for 4H-SiC MOSFETs in the literature. The SiC unipolar limit is also shown in Figure 16.44. Our results are shown to approach the SiC unipolar limit. MOSFETs with a superjunction structure would require further improvement in terms of the MOSFET performance.

16.6.4.2 Dynamic Behavior of the Optimized Structure

Capacitance–voltage measurements, gate charge tests, and double-pulse tests for the presented structure with an optimized Deep-P gap and the conventional structure were performed to confirm the shielding effect. Figure 16.45 shows the measured gate–drain capacitance and drain–source capacitance. The gate–drain capacitance of the presented structure at a drain voltage of 200 V was about 30 pF/cm^2, while that of the conventional structure was about 200 pF/cm^2.

Figure 16.46a,b show the test results of the gate charge (Q_g) for the presented structure and the conventional structure, respectively. The presented structure achieved a gate–drain charge of 65 nC/cm^2, which is lower than that of the conventional structure (143 nC/cm^2). Gate–drain charges were calculated within the 10–90% range of the drain voltage. To estimate only the gate–drain charge, measurements were performed at low load current. The turn-on and turn-off waveforms are depicted in Figure 16.47. Owing to the low gate–drain capacitance and charge, the presented structure could reduce E_{on} by 32% and E_{off} by 40% compared to the conventional structure. Figure 16.48a,b show the drain current dependence of $E_{on} + E_{off}$ and the

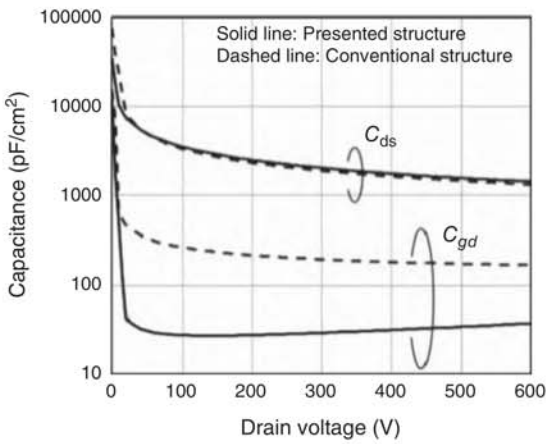

Figure 16.45 Measured results for C_{gd} and C_{ds} of the conventional and presented structures.

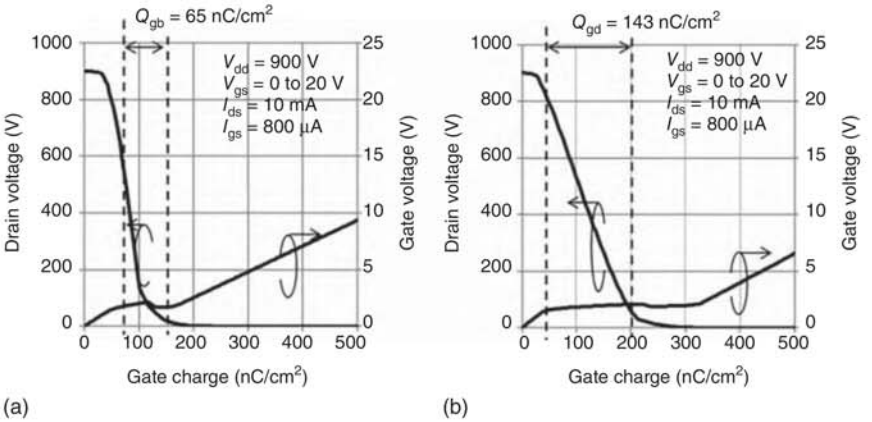

Figure 16.46 Measured gate charges of the (a) presented and (b) conventional structures.

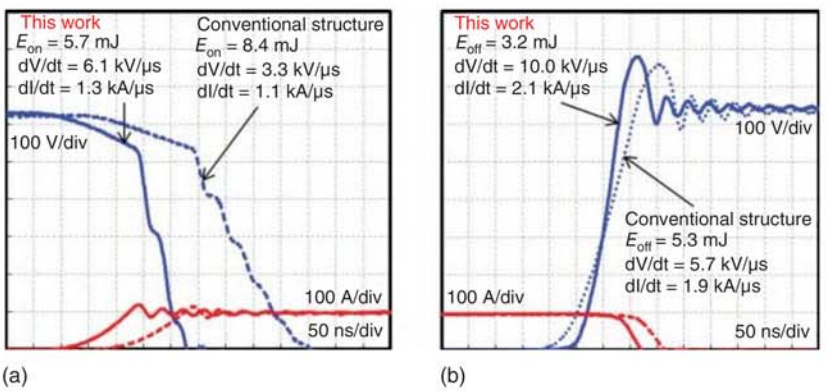

Figure 16.47 Double-pulse waveforms of the (a) turn-on and (b) turn-off of the conventional and presented structures ($V_d = 650\,V$; $V_g = -5/20\,V$; $I_d = 100\,A$; $R_g = 30\,\Omega$; room temperature).

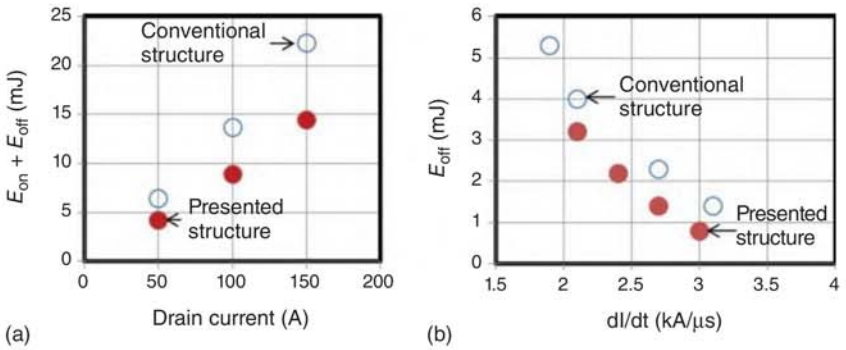

Figure 16.48 (a) Drain current dependence of $E_{on} + E_{off}$ ($V_d = 650$ V; $V_g = -5/20$ V; $I_d = 50$, 100, or 150 A; $R_g = 30\,\Omega$; room temperature) and (b) dI/dt dependence of E_{off} ($V_d = 650$ V; $V_g = -5/20$ V; $I_d = 100$ A; $R_g = 5$, 10, 20, or 30 Ω; room temperature) for the conventional and presented structures.

dI/dt dependence of E_{off}, respectively, for the fabricated MOSFETs with an optimized Deep-P gap and the conventional structure. Compared with the conventional structure, the total losses were effectively reduced in the presented structure. The improvement of the trade-off between dI/dt and E_{off} must be considered to minimize E_{off}, given that the drain voltage surge is well suppressed during the turn-off period. As shown in Figure 16.48b, E_{off} was effectively reduced at the same dI/dt, indicating that the high dV/dt of the presented structure may be attributed to the improvement of this trade-off.

16.6.5 Measurements of Reliability

Important reliability issues for SiC-MOSFETs include (i) the dielectric breakdown lifetime of the gate oxide and (ii) the characteristic degradations caused by crystal dislocations in SiC devices. Considering the dielectric breakdown lifetime, adequate lifetimes were achieved using the above-mentioned presented structure. Therefore, in this section, the second issue is considered.

The major issue associated with the characteristic degradations in SiC-MOSFETs is the body diode current degradation [28, 29]. When the body diode is conducting, hole injection occurs from the top p-type layer into the n-type drift layer, which causes hole–electron recombination at various basal plane dislocations (BPDs). The BPD gains energy from this recombination process, and consequently, the stacking faults grow into the drift region. The stacking faults act as a resistance, which results in an increase in the conduction loss. Therefore, the bipolar degradation at the body diode conduction should be addressed.

16.6.6 Suppression of Bipolar Degradation in the Presented MOSFETs [30]

Figure 16.49a–c show the schematic cross-sectional illustrations of a PN diode, conventional MOSFET, and the presented Deep-P encapsulated MOSFET, respectively.

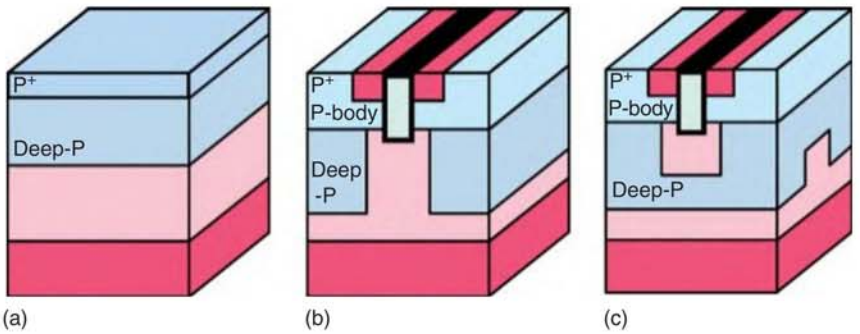

Figure 16.49 Schematic cross-sectional illustrations of the (a) PN diode, (b) conventional MOSFET, and (c) Deep-P encapsulated MOSFET.

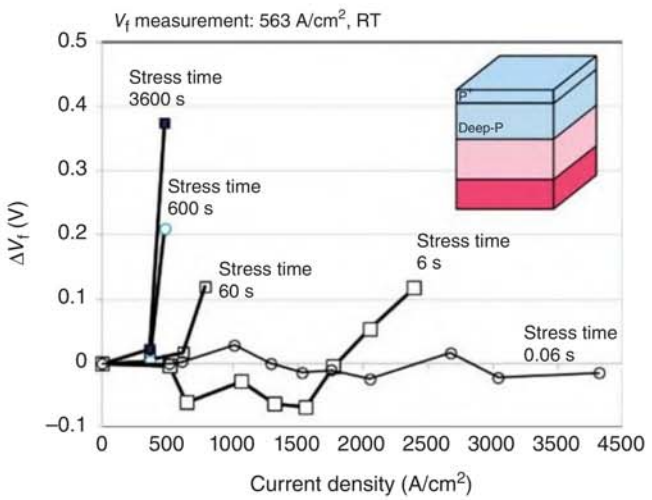

Figure 16.50 Forward voltage degradation as a function of the current density and PL mapping images of the PN diodes. V_f was defined as a forward current of 563 A/cm^2 at room temperature.

The concentration and thickness of the drift layer are selected to achieve a blocking voltage of over 1200 V. All the structures used commercial wafers of the same specifications to focus on the structural differences.

(a) *PN diodes*: Over a stress time of 0.06 seconds, no degradation of the forward voltage up to a current density of 4000 A/cm^2 occurred, as shown in Figure 16.50. Consequently, the stacking faults were not observed in the photoluminescence (PL) image, which indicates that this stress time is insufficient to initiate the forward degradation process. In contrast, the forward voltages were degraded over stress times of 6, 60, 600, and 3600 seconds, and stacking faults were observed at each of these stress times. For the six-second case, the current density when forward degradation occurred was much larger than those at 60, 600, and 3600 seconds. As the stress time increases, the forward degradation appears to saturate. In previous studies [31, 32], it has been noted that the forward

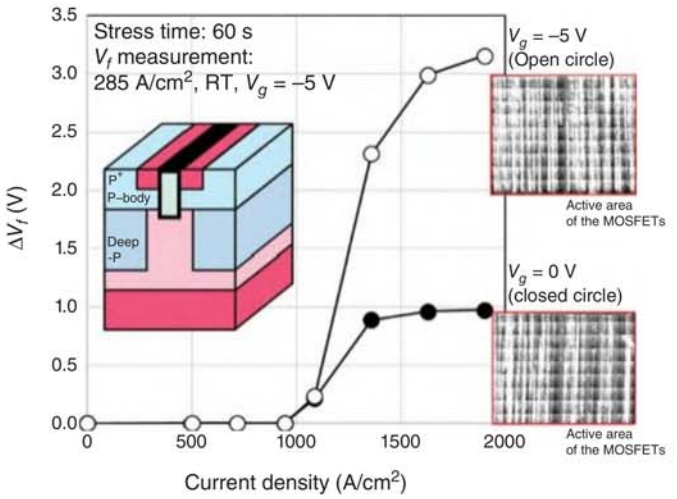

Figure 16.51 Forward voltage degradation of $V_g = 0$ V and $V_g = -5$ V as a function of the current density and PL mapping images of the conventional MOSFET. V_f was defined as a current of 285 A/cm^2 at room temperature and a gate voltage of −5 V. The PL images of only the active areas are shown in this figure.

degradation has a threshold hole density depending on the temperature and concentration of the electron and hole densities, although the absolute values of these densities remain uncertain. The stress time was fixed at 60 seconds for subsequent tests to reduce the measurement time. The forward degradation strength of the PN diode was estimated to be around 500–800 A/cm^2.

(b) *Conventional MOSFETs*: Figure 16.51 shows the forward voltage degradation at gate voltages of 0 and −5 V as a function of the current density. The corresponding PL mapping images are also shown. The forward voltage degraded at a current density of 1000–1100 A/cm^2 for both gate voltages, although the degree of forward voltage degradation at the gate voltage of −5 V was about three times larger than that at 0 V. Since the forward voltage degradation threshold is determined by the hole concentration, this result suggests that the hole concentrations at both gate voltages do not differ at high current densities. As shown in the PL mapping image, the number of the stacking faults at a gate voltage of −5 V is greater than that at 0 V. Because the forward voltage degradation values depend on the number of defects in the substrate and drift layer, it is assumed that the differences between these degradations are contributed to by the defect numbers in the drift layer and/or substrate.

(c) *Deep-P encapsulated MOSFETs*: Figure 16.52 shows the forward voltage degradation at gate voltages of 0 and −5 V as a function of the current density. The corresponding PL mapping images are also shown. In contrast to the results of the PN diodes and conventional MOSFETs, the forward voltage degradation did not occur up to a current density of 3000 A/cm^2 for the presented MOSFET, and stacking faults were not observed. These results indicate that the hole injections in the Deep-P encapsulated MOSFETs are much smaller than those of the PN diodes and conventional MOSFETs.

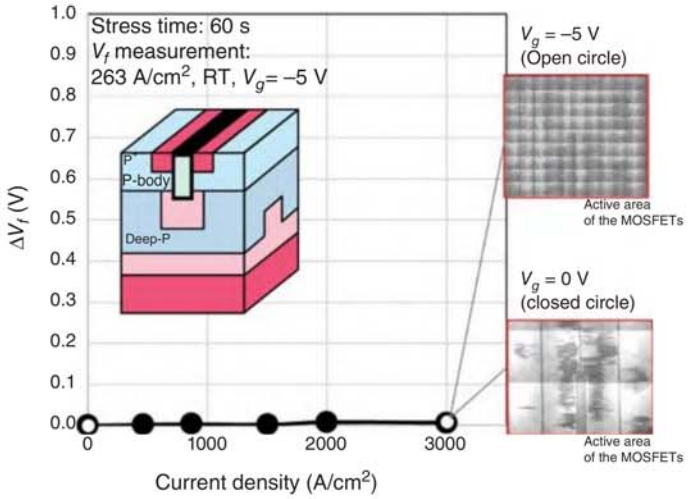

Figure 16.52 Forward voltage degradation of $V_g = 0$ V and $V_g = -5$ V as a function of the current density and PL mapping images of the Deep-P encapsulated MOSFET. V_f was defined as a current of 263 A/cm^2 at room temperature and a gate voltage of −5 V. The PL images of only the active area are shown in this figure.

Simulations of the devices were performed and the injected hole density was estimated for each structure. By accounting for the traps and geometrical effects, it was revealed that the injected hole density of the Deep-P encapsulated MOSFETs was much smaller than those of the PN diodes and conventional MOSFETs.

16.6.7 Summary

4H-SiC trench MOSFETs with an ODS were proposed and fabricated. The proposed SiC-MOSFETs demonstrated lower losses and higher reliabilities than the conventional SiC-MOSFETs. According to the superior results of the presented SiC-MOSFETs, the acceleration of the use of SiC power devices in commercial vehicles may be achieved.

Acknowledgments

This chapter was co-authored by members from companies actively working on SiC development and its application to vehicles in Automotive Power Electronics Technology Committee in the Society of Automotive Engineers of Japan, Inc. (JSAE). The committee members act as co-authors on behalf of each company, but the text could be completed thanks to the many colleagues who contributed in each company. We, the co-authors on behalf of each company, are very grateful to our colleagues for providing valuable information and cooperating with us on this writing activities.

References

1 The International Energy Agency (IEA) (2017). IEA Energy Technology Perspective 2017, Chapter 5 Steering transport towards sustainability, p. 223.

2 Ministry of Economy, Trade and Industry (2019). "Automobile Energy Carrier Strategy in Japan", presentation at Waseda University-AVL symposium, Japan World energy strategy 2019, http://www.f.waseda.jp/jin.kusaka/2019_meti.pdf.

3 Terashi, S. (2017). Toyota's challenge to promote widespread use of electric vehicles. *Toyota Motor Corporation*, Press Release (18 December).

4 Terashi, S. (2018). Aiming to popularize BEVs. *Toyota Motor Corporation*, Press Release (7 June).

5 Sugiura, T. (2019). Toyota electrified vehicles. *Toyota Motor Corporation*, SIA PARIS 2019, Power Train & Electronics, Invited Talk (12–13 June).

6 Hamada, K., Nagao, M., Ajioka, M., and Kawai, F. (2015). SiC – Emerging Power Device Technology for Next-Generation Electrically Powered Environmentally Friendly Vehicles. *IEEE Trans. Electron Devices* 62 (2): 278–285.

7 Ogawa, T. et al. (2016). Verification of fuel efficiency improvement by application of highly effective silicon carbide power semiconductor to HV inverter. SAE Technical Paper 2016 (5 April). https://doi.org/10.4271/2016-01-1230.

8 Hamada, K. (2015). Toyota to trial new SiC power semiconductor technology. *Toyota Motor Corporation*, Press Release (29 January).

9 Sugiura, T. et al. (2016). Efficiency improvement of boost converter for fuel cell bus by silicon carbide diodes. *SAE Int. J. Altern. Power.* 5 (2) https://doi.org/10.4271/2016-01-1234.

10 Yokoo, T. (2018). Toyota Project PORTAL. Toyota Motor North America R&D, *PPCAC Conference*, San Pedro Ports (20 March 2018). http://ppcac.org/2018agenda.html.

11 Matsunaga, M., Fukushima, T., Ojima, K. et al. (2009). FCX clarity fuel cell powertrain. *Honda R&D Tech. Rev.* 21 (1): 7–14.

12 Wen, W. and Lee, Y.-S. (2004). A two-channel interleaved boost converter with reduced core loss and copper loss. In: *2004 IEEE 35th Annual Power Electronics Specialists Conference, 2004. PESC 04*, (20–25 June 2004, vol. 2, 1003–1009. IEEE.

13 Hirakawa, M., Watanabe, Y., Nagano, M. et al. (2010). High power DC/DC converter using extreme close-coupled inductors aimed for electric vehicles. In: *International Power Electronics Conference (IPEC)*, (21–24 June 2010), vol. 2010, 2941–2948.

14 Saito, K. and Otsuka, H. (2013). Development of PCU for a new HEV drive. In: *Proceedings of the Society of Automotive Engineers of Japan Scientific Seminar, No. 46-13*, (22–24 May 2013), 13–16, 20135063.

15 Kadoguchi, T. (2017). Packaging technology of power module for environmentally-friendly vehicles. *Toyota Motor Corp.*, MES2017 Invited Talk (29 August).

16 Asai, R. et al. (2019). Development of TLP-AI technology to realize high temperature operation of power module. *Toyota Motor Corp.*, SAE Technical Paper 2019-01-0607.

17 Tatsumi, K. et al. (2019). High temperature resistant packaging technology for SiC power module by using Ni micro-plating bonding. *IEEE 69th Electronic Components and Technology Conference (ECTC), Waseda University,* (28–31 May 2019). https://doi.org/10.1109/ECTC.2019.00223.

18 Sakata, J. et al. (2018). EMI-less full-bridge inverter for high speed SiC switching devices. Keio University, APEC2018 Poster Session (5 March 2018).

19 Hochberg, M., Sack, M., and Mueller, G. (2016). A test environment for power semiconductor devices using a gate-boosting circuit. *IEEE Trans. Plasma Sci.* 44: 2030–2034.

20 Yamaguchi, K. and Sato, Y. Comprehensive evaluation of gate boost driver for SiC-MOSFETs, *IEEE ECCE 2016, Proceedings, Milwaukee, USA, IEEE* (18–22 September 2016).

21 Shimomura, T., Ikari, T., Okubo, A. et al. High-speed dV/dt control technology for SiC power modules for EV/HEV inverters. *IEEE ECCE 2017, Proceedings, Cincinnati, USA, IEEE*, (1-5 October 2017).

22 Peters, D., Siemieniec, R., Aichinger, T. et al. (2017). Performance and Ruggedness of 1200V SiC-Trench-MOSFET. In: *Proceedings of ISPSD 2017, Sapporo, Japan, IEEE,* (May 28–June 1 2017), 239–242.

23 Kobayashi, Y. et al. (2017). Evaluation of Schottky barrier height on 4H-SiC m-face {1 1 100} for Schottky barrier diode wall integrated trench MOSFET. *Jpn. J. Appl. Phys.* 56: 04CR08.

24 Nakano, Y. et al. (2012). *Mater. Sci. Forum* 717–720: 1069.

25 Ichimura, A., Ebihara, Y., Mitani, S. et al. (2018). 4H-SiC Trench MOSFET with Ultra-Low On-Resistance by using Miniaturization Technology. *Mater. Sci. Forum* 924: 707–710.

26 Ebihara, Y., Ichimura, A., Mitani, S. et al. (2018). Deep-P encapsulated 4H-SiC trench MOSFETs with ultra low $R_{on}Q_{gd}$. In: *Proceedings of ISPSD 2017, Shanghai, China, IEEE,* (19–23 May 2017), 89–92.

27 Kyogoku, S., Ariyoshi, K., Iijima, R. et al. (2018). Role of trench bottom shielding region on switching characteristics in 4H-SiC double-trench MOSFETs. *Mater. Sci. Forum* 924: 748–751.

28 Bergman, J.P., Lendenmann, H., Nilsson, P.A. et al. (2001). Crystal defects as source of anomalous forward voltage increase of 4H-SiC diodes. *Mater. Sci. Forum* 353–356: 299.

29 Skowronski, M. and Ha, S. (2006). Degradation of hexagonal silicon-carbide-based bipolar devices. *J. Appl. Phys.* 99: 011101.

30 Ebihara, Y., Uehara, J., Ichimura, A. et al. (2019). Suppression of bipolar degradation in deep-P encapsulated 4H-SiC trench MOSFETs up to ultra-high current density. In: *Proceedings of ISPSD*, 35–38.

31 Tawara, T., Matsunaga, S., Fujimoto, T. et al. (2018). Injected carrier concentration dependence of the expansion of single Shockley-type stacking faults in 4H-SiC PiN diodes. *J. Appl. Phys.* 123: 025707.

32 Iijima, A. and Kimoto, T. (2018). Theoretical and experimental investigation of critical condition for expansion/contraction of a single Shockley stacking fault in 4H-SiC. *Extended Abstracts (ECSCRM 2018), MO.04.02, Birmingham, UK, Materials Science Forum, (2–6 September 2018).*

17

Point Defects in Silicon Carbide for Quantum Technology

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17.1 Introduction

A new era in the fundamental and applied science on silicon carbide (SiC) has emerged in the field of quantum technology. This was inspired by the success of nitrogen-vacancy (NV) center in diamond [1–5] where the coherent control of single spin could be demonstrated at room temperature by means of optical readout and initialization that led to various sensor applications at the nanoscale. First principles calculations could identify the similarity between electronic structure of the NV center in diamond and divacancy in SiC in 2009 (see the conference proceedings of the International Conference of Silicon Carbide and Related Materials 2009 in Ref. [6] and a detailed publication in Ref. [7]). Indeed, the coherent control of the electron spin of divacancy defect in SiC was demonstrated in experiments in 2011 [8]. In addition, density functional theory (DFT) calculations combined with considerations of the presumed coherence time of the electron spin in various wide band gap materials identified SiC as a potential material to host optically addressable quantum bits [9]. Further experiments and theoretical studies have confirmed [10–13] that the electron spin coherence time can exceed 2 ms in SiC crystals with naturally abundant Si and C isotopes, including the single spin detection at room temperature of the silicon vacancy defect [11]. The big advantage of SiC is that this material can be grown at wafer scale with high purity and quality and acts as a wide band gap semiconductor. As a consequence, it can be envisioned that the combination of optical and electrical control of qubits in SiC is feasible, so the integration of semiconductor and quantum technologies can be realized within a single platform. Indeed, electrically driven single photon sources operating at room temperature have been realized in SiC diodes [14, 15]. The nature of these single photon sources was hinted from first principles calculations [15], as well as for the brightest solid-state single photon sources operating at room temperature [16].

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

Further advances in the SiC quantum technology have been flourished that are discussed in the other chapters in this book. The birth and development of SiC quantum technology relies on point defects with advantageous magneto-optical properties. In this review paper, we list the basic properties of these defects with short description of the most relevant ones. In particular, we will focus on the so-called divacancy, silicon vacancy, carbon antisite-vacancy (CAV) pair, and the NV pair defects, and other potential defects will be also considered.

17.2 Silicon Carbide: Polytypes and Types of Relevant Point Defects

SiC has more than 250 known polymorphs in which they are common with the hexagonal lattice in the basal plane forming an Si–C bilayer. These bilayers can be stacked on top of each other either hexagonal close packed or face center cubic configurations which results in quasihexagonal (h) or quasicubic (k) Si–C bilayers in the sequence (see Figure17.1). Because of the common basal plane structure, these different forms of SiC are also called polytypes. The chemical structure of these polytypes consists of tetrahedrons with sp^3 fourfold coordinated C and Si atoms as usual in semiconductor structures. SiC did not form on Earth and should be produced. High-quality SiC can be grown by chemical vapor deposition (CVD) by using

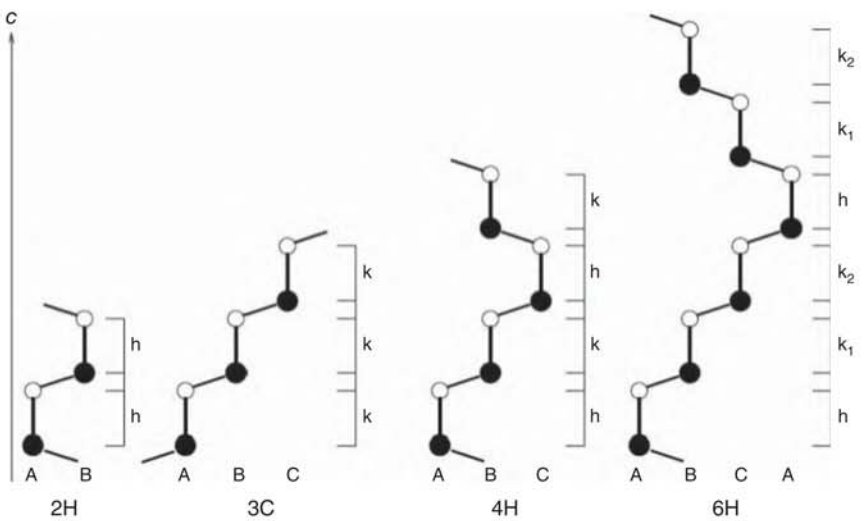

Figure 17.1 Important polytypes of SiC except for 2H. 2H SiC consists of only h Si–C bilayers and is shown only for didactic purposes. h and k labels refer to quasicubic and quasihexagonal bilayers where the indexes on k layers in 6H polytype distinguish the two quasicubic bilayers.

carbon and silicon precursors [17]. Depending on the conditions of CVD process or the substrate, the most common polytypes are the so-called 4H, 6H, and 3C SiC in Ramsdell notation, where H and C refer to hexagonal and cubic crystals, respectively. 4H and 6H SiC have four and six Si–C bilayers in their unit cell, respectively, in which sequences of hk and hk_1k_2 Si–C bilayers follow each other (see Figure 17.1). Any Si or C atom in the quasihexagonal and quasicubic layers has the same fourfold coordination but the second neighbor environment differs. Although, the slightly polarized covalent Si–C bonds are common in these SiC polytypes, but the band gap of SiC varies significantly from 2.4 eV (3C) to 3.0 eV (6H) and 3.23 eV (4H) [17]. The absolute value of the top of the valence bands (VBM) is about the same position for these polytypes, but the position of the bottom of the conduction band (CBM) varies significantly. The reason behind this large variation has been recently explained by *ab initio* DFT calculations in which they showed that the CBM state is not a usual antibonding combination of the wave functions constituting the covalent bonds but rather "floating" states delocalized in the interstitial region of the crystal that are confined in the cage of quasihexagonal layers with pushing up the level of the CBMs with respect to that of 3C SiC [18]. We further note that the position of the CBM also affects the electrochemistry of these polytypes as has been recently explained by the so-called no-photon exciton generation (electro)chemistry (NPEGEC) process [19].

SiC can be doped n-type and p-type as well, so the Fermi level can be well varied by doping conditions [17]. Nitrogen and boron are often unwanted n-type and p-type contamination in SiC CVD layers but can be also used intentionally to control the conductivity of SiC. Nitrogen donor has a maximum limit of concentration ($\approx 10^{19}$ 1/cm^3) because of the formation of a competing complex of four nitrogen around the silicon vacancy (V_{Si}) at high nitrogen concentration but phosphorus can be also employed as a donor at higher concentration [20]. The resistance of the contaminated SiC layers can be either improved by introducing vanadium (we label it by Van in the context, in order not to confuse it with the vacancy label) (see Ref. [21] and references therein) or high temperature CVD growth with forming of vacancies and vacancy clusters (see Ref. [22] and references therein) which introduce deep acceptor and donor states that compensate the residual donor and acceptor states. The latter SiC samples are called high-purity semi-insulating (HPSI) SiC layers. Nitrogen and phosphorus donors are substitutional point defects. Nitrogen prefers to substitute carbon (N_C) whereas phosphorus prefers to substitute silicon (P_{Si}) in SiC (see Refs. [20, 23] and references therein). In general, an impurity atom may prefer to substitute C or Si atom in SiC. We further note that the h and k bilayers are inequivalent lattice sites in 4H and 6H SiC. These inequivalent lattice sites create different environment to the defects which affects their properties. For instance, N_C donor has an ionization energy at around 100 and 45 meV [24] at k and h site in 4H SiC, respectively. In general, a single substitutional defect or a single vacancy may have two and three inequivalent configurations in 4H and 6H SiC, respectively, whereas a pair defect has four and six inequivalent configurations in 4H and 6H SiC, respectively.

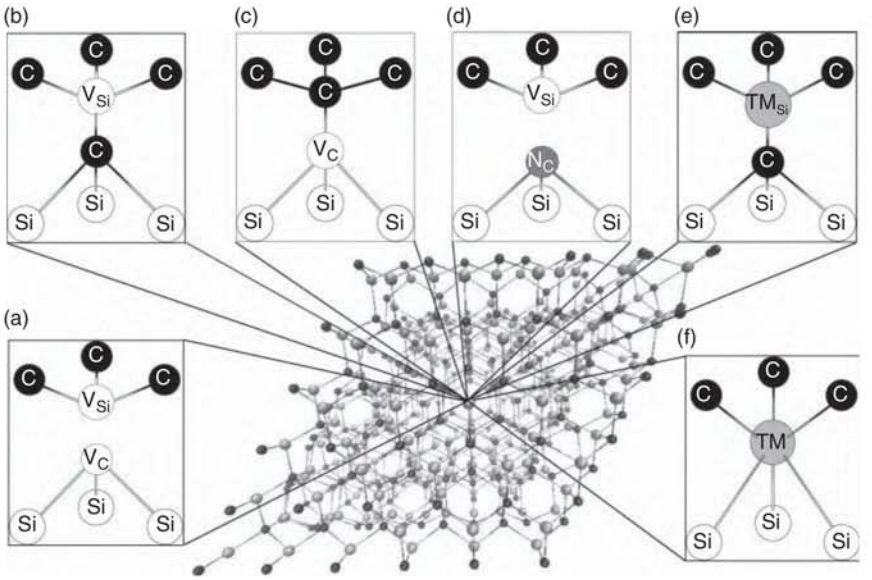

Figure 17.2 The considered defects in SiC. TM stands for transition metal ion, whereas V_{Si} and V_C labels the Si-vacancy and C-vacancy, respectively.

For instance, V_C–V_{Si} divacancy defect exists in hh, kk, hk, and kh configurations in 4H SiC (see Figure 17.2a and Table 17.1). An impurity ion may reside at a single vacancy (Figure 17.2e) or divacancy. The latter can be realized by placing the ion either on-site (similar to Figure 17.2d) or at interstitial position (Figure 17.2f), where the latter is called asymmetric split-vacancy (ASV) configuration [37]. We further note that carbon may substitute silicon (or vica versa) in SiC that is called antisite defect. A special case is that during the diffusion of V_{Si} (Figure 17.2(b)) may transform to carbon antisite-vacancy (CAV) pair defect, C_{Si}-V_C defect (Figure 17.2c) that can be a stable configuration over V_{Si} depending on the position of the Fermi level in SiC (see Ref. [38] and references therein).

We note that the identification of inequivalent configurations of a defect is highly nontrivial, in particular, from experiments. As 4H and 6H SiC have only a single quasihexagonal site, a common practice was for identification of configurations in experiments to pickup two similar signals and a distinct signal in 6H SiC and then the two similar signals were associated with the two quasicubic sites and the remaining one to the quasihexagonal site. By following this logic, the similar signals as observed in 6H SiC and 4H SiC were used to identify the corresponding configurations in 4H SiC. However, it has been shown for nitrogen donors by combining experimental data and DFT calculations that this practice is misleading because the signals of h and k_2 sites can be rather similar to each other and that of k_1 site is distinct in 6H SiC [39]. In general, the interpretation of defect lattice sites from pure experimental data should be taken very cautiously from the literature and should be verified by first principles calculations.

Table 17.1 Position of ZPLs and the ground state zero-field splittings (ZFS) of technologically important point defects in 3C and 4H SiC as obtained in experiments.

Polytype	Defect	Charge state	Spin state	Config. (PL signal)	ZPL (eV)	ZFS (GHz)
3C	$V_C V_{Si}$	0	1	kk	1.121 [25]	1.336 [25]
	$N_C V_{Si}$	1−	1	kk	0.845 [26]	1.303 [26]
4H	V_{Si}	1−	$\frac{3}{2}$	h(V1)	1.438 [27]	0.003 [28]
				k(V2)	1.352 [27]	0.035 [28]
	$V_C V_{Si}$	0	1	hh(PL1)	1.095 [29]	1.336 [29]
				kk(PL2)	1.096 [29]	1.305 [29]
				hk(PL3)	1.119 [29]	1.222 [29]
				kh(PL4)	1.150 [29]	1.334 [29]
	Unidentified		≥1	(PL5)	1.189 [29]	1.373 [29]
				(PL6)	1.194 [29]	1.365 [29]
	$V_C C_{Si}$(CAV)	1+	$\frac{1}{2}$	hh($A_{1,2}$)	1.911, 1.902 [16]	
				hk ($A_{3,4}$)	1.864, 1.855 [16]	
				kk ($B_{1,2}$)	1.842, 1.846 [16]	
				kh ($B_{3,4}$)	1.832, 1.836 [16]	
	$N_C V_{Si}$	1−	1	hh(PLX1)	0.998 [30, 31]	1.282 [30]
				kk(PLX2)	0.999 [30, 31]	1.331 [30]
				hk(PLX3)	1.014 [30, 31]	1.193 [30]
				kh(PLX4)	1.051 [30, 31]	1.328 [30]
	Van_{Si} a)	0	$\frac{1}{2}$	k(α)	0.969 [32]	540
				h(β)	0.929 [32]	<40
	Cr_{Si}	0	1	k(Cr_A)	1.158 [33, 34]	<1.2 [34]
				h(Cr_C)	1.190 [33, 34]	6.46 [33, 34]
	Mo_{Si}	1+	$\frac{1}{2}$	h	1.152 [35]	?
	$Nb_{Si}V_C$(Nb-ASV)	0	$\frac{1}{2}$	hh (Nb_0)	1.383 [36]	<72.54

a) Vanadium is denoted by Van in order to avoid confusing it with Si vacancy.
Unknown data are labeled by question mark.

17.3 Point Defect Single Photon Sources and Quantum Bits

Quantum emission may be realized by a fluorescent isolated single point defect in solids. In the exemplary NV center in diamond, this has been realized by CVD growth of pure diamond and controlled creation of NV center by nitrogen implantation and annealing (see Ref. [5] and references therein). The implantation

dose was varied in order to produce the NV centers apart from each other so then illumination through an objective could photoexcite only a single defect in the confocal spot. Similar single photon emitters can be formed in SiC too. One of the most characteristic properties of these single photon emitters is the zero-phonon line (ZPL) in the corresponding photoluminescence (PL) spectrum in which phonons may also couple to the optical transition resulting in phonon sideband in the PL spectrum. The fraction of ZPL emission vs. the total emission, i.e. the Debye–Waller (DW) factor, is an important feature of these emitters as quantum information can be transmitted only from the ZPL emission. If the single photon emitter is paramagnetic, then the electron spin can be principally employed as a resource of quantum information. For NV center in diamond, the fluorescence is spin selective that can be employed to initialize its electron spin state by optical pumping and read out the spin state by the detected fluorescence intensity where driving of the electron spin can be achieved by microwave alternating magnetic field generated close to the sample [2], which is briefly called optically detected magnetic resonance (ODMR). An alternative readout method of the electron spin state is the electrical detection of magnetic resonance (EDMR) through spin-selective photoionization [40]. Typically, the spin levels in the ground state split even the absence of external magnetic field which is called zero-field-splitting (ZFS), thus ODMR and EDMR measurements can be carried out at zero constant magnetic field. Besides ZPL, ZFS is a characteristic parameter of solid-state defect quantum bits. First, we list the characteristic parameters of the observed single photon sources and quantum bits in the most studied 4H and 3C SiC polytypes. As explained above, stable inequivalent configurations of a defect may exist in 4H polytype that are labeled by k and h sites. We note that the PL5/6 centers have been recently associated with the neutral divacancy with $S = 1$ spin state residing in the stacking fault of 4H SiC [41] but we keep the original claim of "unidentified" in Ref. [8] in Table 17.1.

Next, we list the defect quantum bits' basic parameters in the less studied 6H SiC. The number of configurations of a defect can be the largest among the considered SiC polytypes.

In sections 17.3.1–17.3.5, we briefly summarize the recent results on the most prominent quantum bits and single photon sources in SiC.

17.3.1 Divacancy

The coherent manipulation of defect spins in SiC has been first demonstrated for the neutral divacancy defects [8] (see PL1-6 centers in Table 17.1). Neutral divacancies have $S = 1$ ground state spin [42, 43] and near infrared optical transition at around 1100 nm of ZPL with broad emission in the phonon sideband with DW factor of about 0.03 that had been known as UD2 PL center in the literature [44]. It was previously predicted by combination of first principles calculations and group theory analysis of states [6, 7] that neutral divacancy is isovalent to NV center in diamond and the level structures (see Refs. [4, 5]) are also very similar which makes divacancy very promising quantum bits in SiC. The similarity between NV center in diamond and neutral divacancy in SiC has been later confirmed from photoluminescence

excitation (PLE) measurements [25] and highly accurate configuration interaction based first principles method [45], also in terms of Stark-tuning of the optical transition [46]. The typical coherence times are about 1.2 ms with ODMR readout contrast of about 15% [12, 25] in high-quality 4H SiC with optimized measurement conditions, whereas these parameters are about 0.9 ms and 3.5% in 3C SiC [25]. Simulations showed [13] that the nuclear spins of ^{13}C and ^{29}Si in natural abundant SiC crystals as the source of decoherence of the target divacancy electron spin results in about 2 ms coherence time for the divacancy spins, thus the low quality of crystals (possibly, too high concentration of residual nitrogen donors) may be responsible for the reduced coherence times in 3C SiC. Divacancy may exist in several charge states depending on the position of the Fermi level [30, 43, 47, 48]. The photoionization thresholds that have direct correspondence to the charge transition levels at low temperatures have been recently determined in experiments [48, 49] in which the correct and accurate first principles calculations imply [48] that $(+|0)$ and $(0|-)$ charge transitions levels are at $\approx E_V + 1.0$ eV and $\approx E_V + 2.0$ eV in 4H SiC, respectively. As a consequence, optical pumping with 960 nm laser results in the quenching of the PL1-4 centers into the "dark" negatively charged divacancy defect, in contrast to other interpretation [50, 51]. We note that the photoionization threshold should be polytype and temperature dependent as the band edges vary with polytypes and shift with temperature [52]. Divacancies may form in HPSI 4H SiC [8] but can be generated by, e.g. carbon implantation and annealing [29]. Most of the divacancy- related PL and ODMR centers can be observed at low temperatures in SiC, but room temperature signals can be also observed for some of the configurations (see a summary in Ref. [29]). The room temperature divacancy quantum bits are promising for quantum enhanced biosensing or hyperpolarization [53, 54]. The multiple divacancy quantum bits in 4H SiC [8] and 6H SiC [29] are challenging in terms of optimizing the measurement conditions for each configuration but can be used as a resource. Identification of the individual configurations was achieved by large-scale DFT calculations [55, 56]. For instance, the low symmetry of off-axis or basal divacancy configurations enables coherent optical and spin subsystems control and observation of Landau–Zener–Stuckelberg interference fringes in the resonant optical absorption spectrum [57]. In 3C SiC, a single divacancy center was found as expected [29, 58, 59]. We note that 3C SiC can be grown on Si substrate, and photonics crystals can be fabricated from SiC on a straightforward manner [59], but the in-built strain due to the mismatch between the Si substrate and SiC layers may reduce the potential of this heterostructure because the intrinsically good nonlinear optical properties of SiC cannot be fully harnessed. Strong optical nuclear spin polarization was found for divacancy configurations in 4H SiC [53] with applying a well-chosen constant, small magnetic fields, and illumination that were explained in details by combination of DFT and effective spin Hamiltonian simulations [53, 54]. Simulations predicted high-fidelity bidirectional nuclear quantum bit initialization with this technique for weakly coupled nuclear spins to the divacancy electron spin where this principles was confirmed in the experiments for stronger coupled nuclear spins [60]. The coupling of divacancy electron spin and nuclear spins was used as a resource to create solid-state spin ensembles

entanglement at ambient conditions with high fidelity [61]. Early measurements supported by DFT simulations shown an effective strain and electric field coupling to ground state divacancy spins [62] that lead to ODMR signals associated with "forbidden" electron spin resonance that can be driven by electrical fields [63]. The strain–spin coupling in the ground state was determined by DFT calculations and found significant coupling parameters connecting $\Delta ms = \pm 1$ transitions [64, 65] that could be harnessed in mechanical driving of spin states [65]. Theory predicts that the stress–spin coupling parameters of divacancy spins are, at least, equal or even greater than that for NV center in diamond [64], which can be utilized to fabricate very sensitive pressure or piezo sensors at the nanoscale. Electric field and spin coupling could be used to realize electrically driven optical interferometry [57]. All-optical electrometry at ambient conditions could be realized by optical charge conversion of the defects between their fluorescent and dark charge states, with conversion rate dependent on the electric field [66]. Furthermore, spatial three-dimensional maps of surface acoustic wave modes in a mechanical resonator were demonstrated with using this effect and the piezo property of SiC [66]. The electric field-dependent optical charge conversion combined with heterodyne detection enabled electrometry at radio frequency range [67] with a predicted sensitivity of 1.1 (V/cm)$\mathrm{Hz}^{1/2}$.

17.3.2 Si-vacancy

Silicon vacancy in hexagonal SiC has been known from decades (see a comprehensive review article in Ref. [68]). Early DFT calculations already identified that the negatively charged V_{Si} with $S = 3/2$ spin is responsible for the Si-vacancy-related EPR centers [68] with nonzero but small zero-field splittings [69], despite the existing alternative interpretations [70], that were nullified by recent accurate DFT calculations [28, 56]. $V_{\mathrm{Si}}(-)$ has an optical emission in the near infrared emission with ZPL at around 850 nm and a broad phonon sideband with a DW factor of about 0.15 [27] which are called $V_{1,2}$ and V_{1-3} lines in 4H and 6H SiC, respectively. Time-dependent DFT calculations confirmed that the internal optical transitions of $V_{\mathrm{Si}}(-)$ are responsible for these signals [71]. For V_1 center, a higher level excited state exists at about 4.5 meV (V_1') that no such a state was reported for the V_2 or V_3 configurations (e.g. Refs. [68, 72] and references therein).

Accurate DFT calculations identified the individual configurations (see Tables 17.1 and 17.2, and Refs. [28, 56, 76]) which is in contrast to previous interpretations based on the similarities of EPR signals in 4H and 6H SiC [77, 78]. The corresponding ODMR centers were labeled by Tv1a, Tv2a, etc. in the literature [27]. After early group theory analysis reports [68], recent studies [79, 80] have proposed the fine electronic structure of $\mathrm{V_{Si}}(-)$ that has been recently verified by configurational interaction-based first principles method [81]. It was predicted by a phenomenological theoretical study that the $\mathrm{V_1}$ center could be used to realize spin–photon interface [82], whereas the spin–strain interaction and the optical spin polarization of the $\mathrm{V_{Si}}(-)$ electron spin have been recently analyzed based on group theory arguments [80, 83]. Si-vacancy is a highly energetic defect

Table 17.2 Position of ZPLs and ground state zero-field splittings (ZFS) of technologically important point defects in 6H SiC as obtained in experiments.

Polytype	Defect	Charge state	Spin state	Config. (PL signal)	ZPL (eV)	ZFS (GHz)
6H	V_{Si}	1−	$\frac{3}{2}$	h(V1)	1.433 [27, 56]	0.028 [27, 56]
				k_2(V2)	1.398 [27, 56]	0.128 [27, 56]
				k_1(V3)	1.366 [27, 56]	0.028 [27, 56]
	V_CV_{Si}	0	1	k_1k_1(QL1)	1.088 [29, 56]	1.3 [29, 56]
				hh(QL2)	1.092 [29, 56]	1.334 [29, 56]
				hk_1(QL3)	1.103 [29, 56]	1.236 [29, 56]
				k_1k_2(QL4)	1.119 [29, 56]	1.317 [29, 56]
				k_2h(QL5)	1.134 [29, 56]	?
				k_2k_2(QL6)	1.134 [29, 56]	1.347 [29, 56]
	N_CV_{Si}	0	1	hh	0.96[1] [73]	1.328 [73]
				k_1k_1	0.95[1] [73]	1.278 [73]
				k_2k_2	1.00[1] [73]	1.355 [73]
	$Van_{Si}{}^2$	0	$\frac{1}{2}$	h(α)	≈0.946 [74]	526.14 [75]
				$k_{1/2}(\beta)^3$	≈0.919 [74]	?
				$k_{1/2}(\gamma)^3$	≈0.893 [74]	?
	Cr_{Si}	0	1	$k_{1/2}(Cr_A)^4$	1.156 [34]	<1.2 [34]
				$k_{1/2}(Cr_B)^4$	1.180 [34]	<1.2 [34]
				h(Cr_C)	1.189 [34]	5.396 [34]
	Mo_{Si}	1+	$\frac{1}{2}$	h	1.106 [35]	?
	$Nb_{Si}V_C$(Nb-ASV)	0	$\frac{1}{2}$	hh (Nb_0)	1.361 [36]	<72.54

a) Calculated values.
b) Vanadium is denoted by Van, in order to avoid confusing it with Si vacancy.
c) Signals of β and γ belong to the quasicubic Van_{Si} defects; however, they are not fully resolved so far.
d) Signals of Cr_A and Cr_B belong to the cubic Cr_{Si} defects; however, they are not fully resolved so far.
Unknown data are labeled by question mark.

which is stabilized in n-type 4H SiC when the defect is negatively charged (see latest accurate calculations from Refs. [9, 38, 84]). In p-type region, the carbon antisite-vacancy pair, a tautomer configuration of isolated Si-vacancy, is more stable (see Section 17.3.3 and references in Ref. [38]). For this reason, Si-vacancies are not formed in the growth of high-quality SiC but can be typically produced *a posteriori* by irradiation and implantation techniques [27, 85–94]. Implantation techniques were applied to engineer Si-vacancies into desired location in SiC samples, including mechanical resonators [95], photonic crystal structures [96–98] that can be used to significantly enhance the ZPL emission of Si-vacancies. We note that the electrically active carbon vacancies have much lower formation energies

than silicon vacancies [9, 38, 84, 99]; therefore, irradiation creates lots of unwanted defects. High-temperature annealing would remove the desired silicon vacancies; thus, those unwanted defects remain present together with silicon vacancies in SiC. This may compromise the quality of spin properties of $V_{Si}(-)$ quantum bits. Recently, it has been found [94] that the spin–lattice relaxation time remains constant up to high irradiation fluences, independently of the irradiation type (electron, proton, or neutron). On the contrary, the spin coherence time is very sensitive to the irradiation type and fluence. The longest spin coherence time for the same emitter density is observed for electron irradiation. The shortest spin coherence time was observed in neutron-irradiated samples, which, however, can be partially recovered using annealing. Very recently, it has been demonstrated that Si-vacancies can be created at a given location within ≈80 nm accuracy by femtosecond laser writing [100] with a single pulse without annealing. This process also presumably create nearby carbon vacancies too that affect the charge state stability of $V_{Si}(-)$ upon illumination [100]. Theory found that charge transition levels of the single, double, and triple acceptor state of Si-vacancies should be at $\approx E_V + 1.3$ eV, $\approx E_V + 2.5$ eV, and $\approx E_V + 2.8$ eV in 4H SiC, respectively [84], where the latter two are associated with the S2 and S1 deep level transient spectroscopy (DLTS) centers in n-type irradiated 4H SiC [84, 101]. The photoionization [66] and/or controlled Fermi-level shifts in SiC diodes [81] can be applied to switch the $V_{Si}(-)$ quantum bit on and off. The former process can be electric field dependent in given 4H SiC samples, thus can be used to realize all-optical electrometry [66]. Engineering of $V_{Si}(-)$ into diodes was reported at ensemble level [14]. Tight control of charge state of single $V_{Si}(-)$ (V2 center) quantum bit has been recently demonstrated in 4H SiC diode [81] which is a key step toward integrating the quantum technology with semiconductor technology. Off-resonant excitation of V_2 ODMR center in 4H SiC results in ∼1% ODMR contrast at room temperature [102–104]. Resonant excitation of single V_1 or V_2 center at low temperatures in 4H SiC leads to high fidelity spin and optical control [105, 106]. The coherence time of the electron spin is at around 1 ms [10, 11, 72, 107–111]. These near-infrared color centers are relatively dim (around 10 kcount/s); thus, solid immersion lens was produced by etching of SiC, in order to observe single V_2 centers in 4H SiC [11]. This defect may realize a maser [112], i.e. coherent emission of microwave photons, and subject for realizing a nanoscale vector magnetometer [113–117] and thermometer [113, 118]. The observed sensitivity of dc magnetometer is about 100 $nT/\sqrt{Hz}$, and it was proposed that engineering this magnetometer into an optimized light-trapping waveguide can improve the sensitivity to about 100 $fT/\sqrt{Hz}$ [117]. By harnessing the giant 2.1 MHz/K shift of the zero-field splitting in the excited state of V_2 center in 4H SiC, it was found that this effect results in an all-optical thermometry technique with temperature sensitivity of 100 $mK/\sqrt{Hz}$ for a detection volume of approximately 10^{-6} mm^3. V_1 center in 4H SiC has very promising properties for realizing quantum communication [82, 105, 119]: it shows a very stable zero-phonon-line emission against stray electric fields with nearby addressable nuclear spins for quantum memory. We note that $V_{Si}(-)$ is less known in 3C SiC than in hexagonal polytypes. Itoh et al. observed in irradiated 3C SiC layers grown on Si substrate an isotropic

$S = 3/2$ T1 EPR center with tetrahedral symmetry that was associated with $V_{Si}(-)$ [120]. A dominant PL line of 1.913 eV, also called E center, observed in this sample was found to disappear at annealing stages of ≈100 and 700 °C, similarly to the T1 EPR center [121]. Therefore, E center was assigned to $V_{Si}(-)$ [121]; however, DFT calculations showed that this PL line can be rather associated with its tautomer configuration, the carbon antisite-vacancy pair [122] (see Section 17.3.3). Later, a 1.121-eV PL center was observed in 3C SiC with an ODMR signal too with tetrahedral symmetry that is also called L2 center [123, 124]. As DFT calculations imply [122] that CBM to in-gap level optical transition may occur at this energy for the excited state of $V_{Si}(-)$, the 1.121-eV ODMR center might originate from $V_{Si}(-)$. We note that the early analysis of the ODMR line indicated an $S = 1/2$ effective spin which contradicts with the $S = 3/2$ spin of $V_{Si}(-)$ [123]. Further studies are necessary to resolve this issue. We note that multiconfigurational ab initio calculation predicted [125] that the neutral silicon vacancy has a singlet ground state with an $S = 1$ metastable state above which was also supported by a constraint spin DFT calculations [126]. Later, photo-EPR studies confirmed this prediction [127]; thus, $S = 1$ high spin state can be measured for neutral V_{Si} in 3C SiC.

17.3.3 Carbon Antisite–Vacancy Pair

The carbon antisite-vacancy (CAV) pair defect is a bistable conformation of the isolated silicon-vacancy defect [38, 99, 128, 129] which means that the relative stability of the two conformations depends on the position of the Fermi level. According to accurate calculations [38], the CAV defect is stable over V_{Si} for the range of the Fermi-level position between E_V and $\approx E_V + 2.0$ eV in 4H SiC. In n-type conditions of 4H SiC, the V_{Si} is more stable than CAV defect but the metastable CAV defect might coexist with V_{Si} depending on the formation condition of point defects in the SiC sample (e.g. Ref. [16]). Ab initio calculations predicts that the negatively charged CAV may be observed with Fermi-level position at $\approx E_V + 2.7$ eV with $S = 1/2$ spin in 4H SiC which was associated with EPR centers in irradiated HPSI material [129]. The calculated $(2 + |+)$ and $(+|0)$ charge transition levels are at $\approx E_V + 1.3$ eV and $\approx E_V + 2.1$ eV in 4H SiC [38], respectively. The positively charged CAV has $S = 1/2$ spin and the HEI9/10 EPR centers were associated with this defect [130]. Steeds observed PL centers in electron irradiated 4H SiC samples called A–B lines [16] with ZPL energies at around 1.9 eV (see Table 17.1) that were tentatively assigned to the neutral CAV defect. However, accurate calculations showed [16, 38] that the neutral CAV defect is ionized to (+) state upon such illumination. Rather, split CBM level to in-gap deep defect level optical transition may be associated with this PL signal [16]. Indeed, well-engineered electron irradiation of HPSI 4H SiC resulted in the formation of ultrabright (million photons per second) single photon emitters associated with this defect [16]. To date, this is among the brightest solid-state single photon emitters. As mentioned earlier, this defect has $S = 1/2$ ground state spin [130], but optical manipulation of its spin state has not yet been reported so far. Very recent photo-EPR measurements has confirmed, on the other hand, that the charge states of the ensemble of CAV defects can be switched by

photo-excitation [131], and the observed ionization thresholds are consistent with the ab initio results as given above. We note that the neutral CAV has $S = 0$ ground state but a metastable $S = 1$ state exists according to first principles simulations [38]. It was proposed that this defect may have a near-infrared optical transition in 4H SiC and optical pumping may lead to the population of the metastable triplet state [38]. Assuming a sufficiently long lifetime of this triplet state, quantum control of the electron spin and a nearby nuclear spin (either ^{13}C or ^{29}Si) is doable. Group theory analysis implies that spin-selective non-radiative decay may occur from the triplet substates toward the singlet ground state; thus; the spin state may be read out optically [38] similar to the so-called ST1 defect in diamond [132]. Finally, we note that the so-called *E* PL center [121] in 3C SiC was observed in nanocrystallites which emits with ZPL at 648 nm (1.913 eV) and the corresponding defects in 3C SiC nanocrystals formed ultrabright single photon sources [122]. The *E* PL center was originally associated with V_{Si} [121]; however, ab initio calculations strongly imply [122] that the *E* PL center is the PL transition between the split VBM and the defect level in the gap for the (2+) charge state of the CAV defect in 3C SiC. Interestingly, the calculated $(2 + |+)$ charge transition level is at $\approx E_V + 1.95$ eV, whereas the neutral CAV defect is marginally stable at highly n-type conditions in 3C SiC [122]. The (2+) charge state has a singlet ground state. A metastable triplet excited state might exist for this defect but has not yet been reported.

17.3.4 Nitrogen-Vacancy Pair

Recently, N_CV_{Si} defects have been observed in the most common SiC polytypes (3C, 4H, 6H) in N-doped particle- and ion-irradiated SiC crystals [26, 30, 31, 73, 133–135].

The different configurations in hexagonal polytypes and the corresponding negative charge state in each polytype were identified by combination of ab initio simulations and experimental data (see Table 17.3). The single negative charge state of the N_CV_{Si} defects, i.e. the NV centers show near infrared emission as found in experiments [26, 31, 73, 133] arising from the transition between the ^3E excited and $^3A_2$ ground state both exhibiting $S = 1$ spin state according to theory [9, 30, 47, 136, 137]. The observed PL spectra of N_CV_{Si} centers were broad even at cryogenic temperatures which implies relatively small DW factor similar to that of NV center in diamond. Optical spin polarization of the $^3A_2$ ground state has been demonstrated in all three polytypes at room temperature [26, 73, 133]. The spin coherence times are assumed to be long based on the observed characteristics of the N_CV_{Si} EPR spectra. According to ab initio results [9, 30, 47, 136, 137] NV centers are stable within the ingap positions of the Fermi level of around $\approx E_V$+1.5 eV and $\approx E_V$+2.6 eV in the hexagonal polytypes, and above E_V+1.5 eV in 3C SiC, where E_V stands for the valence band edge. Nevertheless, by using particle irradiation and subsequent annealing, neutral divacancies always form besides NV center in a comparable amount as found by theory [30] and earlier PL experiments [73, 133]. Consequently, the spin- and optically active $V_{Si}V_C(0)$ may be detrimental for the spectral and photostability of the NV center. Nevertheless, in a recent study [135], preferential formation of NV centers has been reported in ion-irradiated 4H SiC

Table 17.3 Experimental (exp) and calculated (DFT) values of g, D parameters in the ground state (see Ref. [73]) and ZPLs for axial NV center configurations in the most common polytypes of SiC.

Polytype	Config.	$g_{\perp}^{exp}$	$g_{\parallel}^{exp}$	$g_{\perp}^{DFT}$	$g_{\parallel}^{DFT}$	D^{exp} (MHz)	D^{DFT} (MHz)	ZPL^{exp} (eV)	ZPL^{DFT} (eV)
3C	kk	2.003	2.004	2.0029	2.0034	1303	1409	0.845 [26]	0.870 [30]
4H	hh	2.003	2.004	2.0029	2.0036	1313	1428	0.998 [30]	0.966 [30]
	kk	2.003	2.004	2.0029	2.0036	1270	1377	0.999 [30]	1.1018 [30]
6H	hh	2.003	2.004	2.0029	2.0036	1328	1404		0.96 [73]
	k_1k_1	2.003	2.004	2.0029	2.0035	1278	1348		0.95 [73]
	k_2k_2	2.003	2.004	2.0029	2.0036	1355	1431		1.00 [73]

samples by using annealing temperature of 1000 °C. Photoionization of NV centers might be detrimental for their photostability during single defect spectroscopy which is usually carried out by applying confocal microscope producing high excitation power. This might enhance two-photon absorption processes that may ionize NV centers to N_CV_{Si}(2-) charge state. In order to avoid destructive effects on the photo- and spectral stability in hexagonal SiC, excitation energy lower than ≈1.1 eV has been proposed for the optimal readout process of the ground state spin along with efficient reionization of NV centers [30].

17.3.5 Other Defects

Besides vacancy-related intrinsic point defects, other defects have been observed as single photon sources or quantum bits, or have been proposed as quantum bit candidates in SiC. One class of such point defects is the transition metal defects which may be considered as atomic like states embedded into the crystal potential in which relatively high DW factor may be expected. Indeed, chromium defect in hexagonal SiC has about 0.73 DW factor and $S = 1$ spin ground state spin that could be spin polarized upon illumination at ensemble level [33]. The spin state could be readout by ODMR. Spin polarization is made possible by the narrow optical linewidths of these ensembles, which are similar in magnitude to the ground state zero-field spin splitting energies of the ions at cryogenic temperatures [33]. The wavelength of the emission is at around 1.16 eV (see Tables 17.1 and 17.2) with long optical decay rates (∼100 μs) where the latter is due to the intraconfigurational spin-flip transition between the spin-singlet excited state and spin-triplet ground state [34]. The long optical decay rate may be not advantageous in many quantum protocols, but other optically active transition metal defects occur in SiC. For instance, molybdenum produces similar ZPL emission at around 1.15 eV in 4H SiC (see Table 17.1), but the observed optical lifetime is about 60 ns based on ensemble measurements [35]. On the other hand, the DW factor was estimated to only few percents [35]. The reason of the relatively small DW factor may be revealed by DFT simulations. The single

Mo configuration observed both in 4H and 6H SiC is associated with the ≈0.3 eV difference in the DFT formation energies favoring the quasihexagonal site over the quasicubic site(s) substituting the Si atom (Mo_{Si}) [35, 138] which results in a significantly higher concentration of quasihexagonal configuration. In the PLE measurements, multiple electronic levels were observed in the ground and excited state that were associated with the spin sublevels [35]. The magnetic field dependence of these lines was consistent with an $S = 1/2$ spin model which implied that the defect is in the single positive charge state [35]. By applying a small transverse magnetic field and well-chosen two-laser driving, a Λ system was established and coherent pair trapping of electron spins was realized for the ensemble of Mo defects [35]. The high-quality Mo-doped SiC resulted in a relatively long 0.32 μs coherence time for the $S = 1/2$ electron spin. We note that the observed g factor of the electron spin showed a large anisotropy and a large deviation from the value of the free electron [35]. This implies a contribution of the spin–orbit interaction to the g factor that also should result in a relatively large zero-field splitting that has not yet been reported so far. A promising candidate defect for quantum communication application is the neutral vanadium in 4H SiC (see Table 17.1) that have two configurations associated with the quasicubic and quasihexagonal sites substituting the Si atom, i.e. Van_{Si}, with optical emission at 1280 (α) and 1330 nm (β) [139]. The latter is in the O-band of the optical fibers which is compatible with the existing telecommunication and World Wide Web infrastructure. We note that three Van_{Si} centers with similar near infrared emission were observed in 6H SiC (see Table 17.2) [75]. This defect has $S = 1/2$ electron spin that was observed with showing linewidth smaller than 2 Gauss at 77 K in EPR measurements in old SiC samples [74]. This implies a sufficiently long coherence times of the electron spin at low temperatures. The ground-state orbital doublet together with $S = 1/2$ split due to spin–orbit interaction at zero magnetic field which is manifested in the observed number of ZPL lines in α and β emitters [74]. Recently, the optical properties of Van_{Si} have been revisited in pure, vanadium-doped 4H SiC samples mediated by DFT simulations [32]. Above band-gap excitation (at 441 nm) was applied in that study that created mobile excitons in SiC that recombined with Van_{Si} defect. This recombination is partially radiative that results in near-infrared fluorescence. After pulsed photoexcitation, the fluorescence decay signals were recorded [32]. The combination of results from DFT simulations and PL measurements indicates that the efficiency of emission is about 23% and 15% for α and β emitters under this excitation wavelength. The observed PL lifetimes were 163 and 43 ns, respectively. The measured DW factor is around 30% for each emitter. DFT simulation strongly implies that α and β emitters are the k and h configurations [32], respectively, that goes against previous assignments based on the spectral similarities of Van_{Si} defects in 4H and 6H SiC [139]. We note that very recently single Van_{Si} centers have been observed in 4H and 6H SiC [140]. The individual vanadium centers were created by vanadium implantation. Presumably, the other defects created in this process are responsible for the limited photostability of these single photon emitters which produces only 100–120 counts per second under these conditions at close-to-resonant photoexcitation [140]. The observed coherence times were about 1 μs at 3.3 K due to presumably fast dephasing between the two spin

sublevels caused by acoustic phonons [140]. Another likely quantum bit candidate could be the niobium defect in hexagonal SiC. Niobium produces a single line in the PL and EPR spectrum in hexagonal SiC [36, 37, 141] which is explained by DFT simulations [37]: the Mo creates an ASV configuration that is only stable in hh divacancy. This defect emits at ∼1.36 eV (ZPL) and has $S = 1/2$ spin state in its neutral charge state. Niobium is a contamination in the CVD growth of SiC but might be intentionally doped too. This magneto-optical system is similar to the neutral vanadium and positively charged molybdenum, thus is a subject of future quantum optics studies. Besides intentionally formed single photon sources, unintentional ones have been observed, in particular, at the interface of SiC/SiO_2. Besides electrically driven strong visible emission from D_1 PL center in 4H SiC [142], which is a common intrinsic defect in SiC (silicon antisite), was reported in a p–i–n junction [14]. Theory proposed [15] that this defect near stacking faults in 4H SiC diodes is responsible for the observed single defect electroluminescence with varying wavelengths where the variation depends on the distance of the D_1 defect from the stacking fault. This model was questioned in a later study [143] which showed that thermal oxidation of SiC leads to several single photon emitters in the visible. It was also reported that at the C-face of SiC/SiO_2 interface of the metal–oxide-semiconductor field-effect semiconductor (MOSFET) devices contain single photon emitters [144]. The single photon emitters at the SiC/SiO_2 interface have not yet been identified but most likely they originate from carbon antisite - carbon interstitial clusters [145, 146]. We further note that similar ultrabright and stable single photon emitters were reported in the visible with unidentified microscopic structure in HPSI 4H SiC which was electron irradiated and annealed in forming gas at ambient pressure at 600 °C [147]. Furthermore, near infrared single photon emitters with stable ∼MHz count rates were observed in 3C SiC CVD layers that operate at room temperature [148]. The polarization degree of both excitation and emission of these emitters can reach up to around 97%. The emitters have very broad PL spectra even at cryogenic temperatures; thus, the DW factor should be low though not determined in this study [148]. They found that the most efficient excitation wavelength is around 975 nm (1.27 eV) for a single photon emitter whose PL centered at around 1275 nm (0.97 eV). The origin of these emitters has remained unidentified as well as the spin properties. We also mention that defect spins were observed by electrical detected magnetic resonance in 4H SiC diodes which could be principally employed as light-weight magnetometers operating at harsh conditions, e.g. in space missions [149]. The origin of this defect has not yet been identified. Similarly, electrically detected magnetic resonance of carbon dangling bonds was reported at the Si-face 4H SiC/SiO_2 interface [150, 151].

17.4 Conclusion

We presented a brief summary about the recent advances of quantum technology research and development based on SiC platform. The advantageous electron spin coherence times of defects, the existing readout protocols, and other favorable magneto-optical properties of point defects make this platform very promising

in several fields, in particular, quantum sensing and quantum communication, integrated with semiconductor technology. The tight control of SiC growth and defect engineering should be further improved as well as understanding the intricate details of divacancies, Si-vacancies, and transition metal defects is a key to advance the field toward formation of SiC quantum industry.

Acknowledgments

A.G. acknowledges the Hungarian NKFIH Grant No. KKP129866 of the National Excellence Program of Quantum-coherent materials project, No. 127902 of the EU QuantERA Nanospin project, EU H2020 Quantum Technology Flagship project ASTERIQS (Grant No. 820394), the Quantum Information National Laboratory by the Ministry of Innovation of Hungary via NKFIH, as well as the National Quantum Technology Program (Grant No. 2017-1.2.1-NKP-2017-00001).

References

1 du Preez, L. (1965). Electron paramagnetic resonance and optical investigations of defect centres in diamond. PhD dissertation. University of Witwatersrand.
2 Gruber, A., Dräbenstedt, A., Tietz, C. et al. (1997). Scanning confocal optical microscopy and magnetic resonance on single defect centers. *Science* 276 (5321): 2012–2014. https://doi.org/10.1126/science.276.5321.2012.
3 Jelezko, F. and Wrachtrup, J. (2006). Single defect centres in diamond: a review. *Phys. Status Solidi A* 203 (13): 3207–3225. https://doi.org/10.1002/pssa.200671403.
4 Doherty, M.W., Manson, N.B., Delaney, P. et al. (2013). The nitrogen-vacancy colour centre in diamond. *Phys. Rep.* 528 (1): 1–45. https://doi.org/10.1016/j.physrep.2013.02.001.
5 Gali, A. (2019). *Ab initio* theory of the nitrogen-vacancy center in diamond. *Nanophotonics* 8: 1907–1934. https://doi.org/10.1515/nanoph-2019-0154.
6 Gali, A., Gällström, A., Son, N.T., and Janzén, E. (2010). Theory of neutral divacancy in SiC: a defect for spintronics. *Mater. Sci. Forum* 645–648: 395–397. https://doi.org/10.4028/www.scientific.net/MSF.645-648.395.
7 Gali, A. (2011). Time-dependent density functional study on the excitation spectrum of point defects in semiconductors. *Phys. Status Solidi B* 248 (6): 1337–1346. https://doi.org/10.1002/pssb.201046254.
8 Koehl, W.F., Buckley, B.B., Heremans, F.J. et al. (2011). Room temperature coherent control of defect spin qubits in silicon carbide. *Nature* 479: 84–87. https://doi.org/10.1038/nature10562.
9 Weber, J.R., Koehl, W.F., Varley, J.B. et al. (2010). Quantum computing with defects. *Proc. Natl. Acad. Sci. U.S.A.* 107 (19): 85138–518. https://doi.org/10.1073/pnas.1003052107.

10 Yang, L.-P., Burk, C., Widmann, M. et al. (2014). Electron spin decoherence in silicon carbide nuclear spin bath. *Phys. Rev. B* 90: 241203. https://doi.org/10.1103/PhysRevB.90.241203.

11 Widmann, M., Lee, S.-Y., Rendler, T. et al. (2015). Coherent control of single spins in silicon carbide at room temperature. *Nat. Mater.* 14 (2): 164–168. https://doi.org/10.1038/nmat4145.

12 Christle, D.J., Falk, A.L., Andrich, P. et al. (2015). Isolated electron spins in silicon carbide with millisecond coherence times. *Nat. Mater.* 14 (2): 160–163. https://doi.org/10.1038/nmat4144.

13 Seo, H., Falk, A.L., Klimov, P.V. et al. (2016). Quantum decoherence dynamics of divacancy spins in silicon carbide. *Nat. Commun.* 7: 12935. https://doi.org/10.1038/ncomms12935.

14 Fuchs, F., Soltamov, V.A., Väth, S. et al. (2013). Silicon carbide light-emitting diode as a prospective room temperature source for single photons. *Sci. Rep.* 3. https://doi.org/10.1038/srep01637.

15 Lohrmann, A., Iwamoto, N., Bodrog, Z. et al. (2015). Single-photon emitting diode in silicon carbide. *Nat. Commun.* 6: 7783. https://doi.org/10.1038/ncomms8783.

16 Steeds, J.W. (2009). Photoluminescence study of the carbon antisite-vacancy pair in 4H- and 6H-SiC. *Phys. Rev. B* 80: 245202. https://doi.org/10.1103/PhysRevB.80.245202.

17 Choyke, W.J., Matsunami, H., and Pensl, G. (2004). *Silicon Carbide: Recent Major Advances*. Berlin, Heidelberg: Springer-Verlag. ISBN 978-3-642-62333-2. https://doi.org/10.1007/978-3-642-18870-1.

18 Matsushita, Yu.-i., Furuya, S., and Oshiyama, A. (2012). Floating electron states in covalent semiconductors. *Phys. Rev. Lett.* 108: 246404. https://doi.org/10.1103/PhysRevLett.108.246404.

19 Beke, D., Károlyházy, G., Czigány, Z. et al. (2017). Harnessing no-photon exciton generation chemistry to engineer semiconductor nanostructures. *Sci. Rep.* 7 (1): 1–6. https://doi.org/10.1038/s41598-017-10751-x.

20 Bockstedte, M., Mattausch, A., and Pankratov, O. (2004). Solubility of nitrogen and phosphorus in 4H-SiC: a theoretical study. *Appl. Phys. Lett.* 85 (1): 58–60. https://doi.org/10.1063/1.1769075.

21 Son, N.T., Carlsson, P., Gällström, A. et al. (2007). Deep levels and carrier compensation in V-doped semi-insulating 4H-SiC. *Appl. Phys. Lett.* 91 (20): 202111. https://doi.org/10.1063/1.2814058.

22 Son, N.T., Carlsson, P., ul Hassan, J. et al. (2007). Defects and carrier compensation in semi-insulating 4H–SiC substrates. *Phys. Rev. B* 75: 155204. https://doi.org/10.1103/PhysRevB.75.155204.

23 Isoya, J., Katagiri, M., Umeda, T. et al. (2006). Pulsed EPR studies of phosphorus shallow donors in diamond and SiC. *Physica B* 376-377: 358361. https://doi.org/10.1016/j.physb.2005.12.092.

24 Götz, W., Schöner, A., Pensl, G. et al. (1993). Nitrogen donors in 4h-silicon carbide. *J. Appl. Phys.* 73 (7): 3332–3338. https://doi.org/10.1063/1.352983.

25 Christle, D.J., Klimov, P.V., de las Casas, C.F. et al. (2017). Isolated spin qubits in sic with a high-fidelity infrared spin-to-photon interface. *Phys. Rev. X* 7: 021046. https://doi.org/10.1103/PhysRevX.7.021046.

26 Zargaleh, S.A., Hameau, S., Eble, B. et al. (2018). Nitrogen vacancy center in cubic silicon carbide: a promising qubit in the 1.5 μm spectral range for photonic quantum networks. *Phys. Rev. B* 98: 165203. https://doi.org/10.1103/PhysRevB.98.165203.

27 Sörman, E., Son, N.T., Chen, W.M. et al. (2000). Silicon vacancy related defect in 4H and 6H SiC. *Phys. Rev. B* 61: 2613–2620. https://doi.org/10.1103/PhysRevB.61.2613.

28 Ivády, V., Davidsson, J., Son, N.T. et al. (2017). Identification of Si-vacancy related room-temperature qubits in 4H silicon carbide. *Phys. Rev. B* 96: 161114. https://doi.org/10.1103/PhysRevB.96.161114.

29 Falk, A.L., Buckley, B.B., Calusine, G. et al. (2013). Polytype control of spin qubits in silicon carbide. *Nat. Commun.* 4: 1819. https://doi.org/10.1038/ncomms2854.

30 Csóré, A., von Bardeleben, H.J., Cantin, J.L., and Gali, A. (2017). Characterization and formation of NV centers in 3C, 4H, and 6H SiC: an ab initio study. *Phys. Rev. B* 96: 085204. https://doi.org/10.1103/PhysRevB.96.085204.

31 Zargaleh, S.A., Eble, B., Hameau, S. et al. (2016). Evidence for near-infrared photoluminescence of nitrogen vacancy centers in 4H-SiC. *Phys. Rev. B* 94: 060102. https://doi.org/10.1103/PhysRevB.94.060102.

32 Spindlberger, L., Csóré, A., Thiering, G. et al. (2019). Optical properties of vanadium in 4H silicon carbide for quantum technology. *Phys. Rev. Appl.* 12: 014015. https://doi.org/10.1103/PhysRevApplied.12.014015.

33 Koehl, W.F., Diler, B., Whiteley, S.J. et al. (2017). Resonant optical spectroscopy and coherent control of Cr ˆ 4+ spin ensembles in SiC and gan.*Phys. Rev. B* 95: 035207. https://doi.org/10.1103/PhysRevB.95.035207.

34 Son, N.T., Ellison, A., Magnusson, B. et al. (1999). Photoluminescence and zeeman effect in chromium-doped 4H and 6H SiC. *J. Appl. Phys.* 86 (8): 4348–4353. https://doi.org/10.1063/1.371368.

35 Bosma, T., Lof, G.J.J., Gilardoni, C.M. et al. (2018). Identification and tunable optical coherent control of transition-metal spins in silicon carbide. *NPJ Quantum Inf.* 4 (1): 48. https://doi.org/10.1038/s41534-018-0097-8.

36 Gällström, A., Magnusson, B., Leone, S. et al. (2015). Optical properties and zeeman spectroscopy of niobium in silicon carbide. *Phys. Rev. B* 92: 075207. https://doi.org/10.1103/PhysRevB.92.075207.

37 Ivády, V., Gällström, A., Son, N.T. et al. (2011). Asymmetric split-vacancy defects in sic polytypes: a combined theoretical and electron spin resonance study. *Phys. Rev. Lett.* 107: 195501. https://doi.org/10.1103/PhysRevLett.107.195501.

38 Szász, K., Ivády, V., Abrikosov, I.A. et al. (2015). Spin and photophysics of carbon-antisite vacancy defect in 4H silicon carbide: a potential quantum bit. *Phys. Rev. B* 91: 121201. https://doi.org/10.1103/PhysRevB.91.121201.

39 Szász, K., Trinh, X.T., Son, N.T. et al. (2014). Theoretical and electron paramagnetic resonance studies of hyperfine interaction in nitrogen doped 4H and 6H SiC. *J. Appl. Phys.* 115 (7): 073705. https://doi.org/10.1063/1.4866331.

40 Bourgeois, E., Jarmola, A., Siyushev, P. et al. (2015). Photoelectric detection of electron spin resonance of nitrogen-vacancy centres in diamond. *Nat. Commun.* 6: 8577. https://doi.org/10.1038/ncomms9577.

41 Ivády, V., Davidsson, J., Falk, A.L. et al. (2019). Stabilization of point-defect spin qubits by quantum wells. *Nat. Commun.* 10: 5607. https://doi.org/10.1038/s41467-019-13495-6.

42 Baranov, P.G., Il'in, I.V., Mokhov, E.N. et al. (2005). EPR identification of the triplet ground state and photoinduced population inversion for a Si-C divacancy in silicon carbide. *J. Exp. Theor. Phys. Lett.* 82 (7): 441–443. https://doi.org/10.1134/1.2142873.

43 Son, N.T., Carlsson, P., ul Hassan, J. et al. (2006). Divacancy in 4H-SiC. *Phys. Rev. Lett.* 96: 055501. https://doi.org/10.1103/PhysRevLett.96.055501.

44 Carlos, W.E., Garces, N.Y., Glaser, E.R., and Fanton, M.A. (2006). Annealing of multivacancy defects in 4H−SiC. *Phys. Rev. B* 74: 235201. https://doi.org/10.1103/PhysRevB.74.235201.

45 Bockstedte, M., Schütz, F., Garratt, T. et al. (2018). Ab initio description of highly correlated states in defects for realizing quantum bits. *NPJ Quantum Mater.* 3 (1): 31. https://doi.org/10.1038/s41535-018-0103-6.

46 de las Casas, C.F., Christle, D.J., Ul Hassan, J. et al. (2017). Stark tuning and electrical charge state control of single divacancies in silicon carbide. *Appl. Phys. Lett.* 111 (26): 262403. https://doi.org/10.1063/1.5004174.

47 Gordon, L., Janotti, A., and Van de Walle, C.G. (2015). Defects as qubits in 3C− and 4*H* − *SiC*. *Phys. Rev. B* 92: 045208. https://doi.org/10.1103/PhysRevB.92.045208.

48 Magnusson, B., Son, N.T., Csóré, A. et al. (2018). Excitation properties of the divacancy in 4H-SiC. *Phys. Rev. B* 98: 195202. https://doi.org/10.1103/PhysRevB.98.195202.

49 Wolfowicz, G., Anderson, C.P., Yeats, A.L. et al. (2017). Optical charge state control of spin defects in 4H-SiC. *Nat. Commun.* 8 (1): 1876. https://doi.org/10.1038/s41467-017-01993-4.

50 Golter, D.A. and Lai, C.W. (2017). Optical switching of defect charge states in 4H-SiC. *Sci. Rep.* 7 (1): 13406. https://doi.org/10.1038/s41598-017-13813-2.

51 Beste, A., Taylor, D.C.E., Golter, D.A., and Lai, C.W. (2018). Charge state switching of the divacancy defect in 4H-SiC. *Phys. Rev. B* 98: 214107. https://doi.org/10.1103/PhysRevB.98.214107.

52 Cannuccia, E. and Gali, A. (2020). Thermal evolution of silicon carbide electronic bands, *Phys. Rev. Mat.* 4: 014601. https://doi.org/10.1103/PhysRevMaterials.4.014601.

53 Falk, A.L., Klimov, P.V., Ivády, V. et al. (2015). Optical polarization of nuclear spins in silicon carbide. *Phys. Rev. Lett.* 114 (24): 247603. https://doi.org/10.1103/PhysRevLett.114.247603.

54 Ivády, V., Szász, K., Falk, A.L. et al. (2015). Theoretical model of dynamic spin polarization of nuclei coupled to paramagnetic point defects in diamond and silicon carbide. *Phys. Rev. B* 92: 115206. https://doi.org/10.1103/PhysRevB.92.115206.

55 Davidsson, J., Ivády, V., Armiento, R. et al. (2018). First principles predictions of magneto-optical data for semiconductor point defect identification: the case of divacancy defects in 4H–SiC. *New J. Phys.* 20 (2): 023035. https://doi.org/10.1088/1367-2630/aaa752.

56 Davidsson, J., Ivády, V., Armiento, R. et al. (2019). Identification of divacancy and silicon vacancy qubits in 6H-SiC. *Appl. Phys. Lett.* 114 (11): 112107. https://doi.org/doi: 10.1063/1.5083031.

57 Miao, K.C., Bourassa, A., Anderson, C.P. et al. (2019). Electrically driven optical interferometry with spins in silicon carbide. *Sci. Adv.* 5 (11): eaay0527. https://doi.org/10.1126/sciadv.aay0527.

58 Bratus, V.Y., Melnik, R.S., Okulov, S.M. et al. (2009). A new spin one defect in cubic SiC. *Physica B* 404: 4739–4741. https://doi.org/10.1016/j.physb.2009.08.124.

59 Calusine, G., Politi, A., and Awschalom, D.D. (2014). Silicon carbide photonic crystal cavities with integrated color centers. *Appl. Phys. Lett.* 105 (1): 011123. https://doi.org/10.1063/1.4890083.

60 Ivády, V., Klimov, P.V., Miao, K.C. et al. (2016). High-fidelity bidirectional nuclear qubit initialization in SiC. *Phys. Rev. Lett.* 117: 220503. https://doi.org/doi: 10.1103/PhysRevLett.117.220503.

61 Klimov, P.V., Falk, A.L., Christle, D.J. et al. (2015). Quantum entanglement at ambient conditions in a macroscopic solid-state spin ensemble. *Sci. Adv.* 1 (10). https://doi.org/10.1126/sciadv.1501015.

62 Falk, A.L., Klimov, P.V., Buckley, B.B. et al. (2014). Electrically and Mechanically tunable electron spins in silicon carbide color centers. *Phys. Rev. Lett.* 112 (18): 187601. https://doi.org/10.1103/PhysRevLett.112.187601.

63 Klimov, P.V., Falk, A.L., Buckley, B.B., and Awschalom, D.D. (2014). Electrically driven spin resonance in silicon carbide color centers. *Phys. Rev. Lett.* 112: 087601. https://doi.org/10.1103/PhysRevLett.112.087601.

64 Udvarhelyi, P. and Gali, A. (2018). Ab initio spin-strain coupling parameters of divacancy qubits in silicon carbide. *Phys. Rev. Appl.* 10 (5): 054010. https://doi.org/10.1103/PhysRevApplied.10.054010.

65 Whiteley, S.J., Wolfowicz, G., Anderson, C.P. et al. (2019). Spin–phonon interactions in silicon carbide addressed by Gaussian acoustics. *Nat. Phys.* 15 (5): 490. https://doi.org/10.1038/s41567-019-0420-0.

66 Wolfowicz, G., Whiteley, S.J., and Awschalom, D.D. (2018). Electrometry by optical charge conversion of deep defects in 4H-SiC. *Proc. Natl. Acad. Sci. U.S.A.* 115 (31): 7879–7883. https://doi.org/10.1073/pnas.1806998115.

67 Wolfowicz, G., Anderson, C.P., Whiteley, S.J., and Awschalom, D.D. (2019). Heterodyne detection of radio-frequency electric fields using point defects in silicon carbide. *Appl. Phys. Lett.* 115 (4): 043105. https://doi.org/10.1063/1.5108913.

68 Gali, A., Janzen, E., Gällström, A. et al. (2009). The silicon vacancy in SiC. *Physica B* 404 (22): 4354–4358. https://doi.org/10.1016/j.physb.2009.09.023.

69 Son, N.T., Stenberg, P., Jokubavicius, V. et al. (2019). Ligand hyperfine interactions at silicon vacancies in 4H-SiC. *J. Phys.: Condens. Matter* 31 (19): 195501. https://doi.org/10.1088/1361-648x/ab072b.

70 Soltamov, V.A., Yavkin, B.V., Tolmachev, D.O. et al. (2015). Optically addressable silicon vacancy-related spin centers in rhombic silicon carbide with high breakdown characteristics and endor evidence of their structure. *Phys. Rev. Lett.* 115: 247602. https://doi.org/10.1103/PhysRevLett.115.247602.

71 Gali, A. (2012). Excitation spectrum of point defects in semiconductors studied by time-dependent density functional theory. *J. Mater. Res.* 27 (06): 897–909. https://doi.org/10.1557/jmr.2011.431.

72 Nagy, R., Widmann, M., Niethammer, M. et al. (2018). Quantum properties of dichroic silicon vacancies in silicon carbide. *Phys. Rev. Appl.* 9: 034022. https://doi.org/10.1103/PhysRevApplied.9.034022.

73 von Bardeleben, H.J., Cantin, J.L., Csóré, A. et al. (2016). Nv centers in 3C,4H, and 6H silicon carbide: a variable platform for solid-state qubits and nanosensors. *Phys. Rev. B* 94: 121202. https://doi.org/10.1103/PhysRevB.94.121202.

74 Schneider, J., Müller, H.D., Maier, K. et al. (1990). Infrared spectra and electron spin resonance of vanadium deep level impurities in silicon carbide. *Appl. Phys. Lett.* 56 (12): 1184–1186. https://doi.org/10.1063/1.102555.

75 Kaufmann, B., Dörnen, A., and Ham, F.S. (1995). Zeeman spectroscopy and crystal-field model of neutral vanadium in 6H-silicon carbide. In: M. Suezawa and H. Katayama-Yoshida, editors, *Defects in Semiconductors 18*, Materials Science Forum, vol. 196–201, 707–712. Trans Tech Publications. https://doi.org/10.4028/www.scientific.net/MSF.196-201.707.

76 Biktagirov, T., Schmidt, W.G., Gerstmann, U. et al. (2018). Polytypism driven zero-field splitting of silicon vacancies in 6H-SiC. *Phys. Rev. B* 98: 195204. https://doi.org/10.1103/PhysRevB.98.195204.

77 Mizuochi, N., Yamasaki, S., Takizawa, H. et al. (2002). Continuous-wave and pulsed epr study of the negatively charged silicon vacancy with $S=\frac{3}{2}$ and C_{3v} symmetry in n-type 4H−SiC. *Phys. Rev. B* 66: 235202. https://doi.org/10.1103/PhysRevB.66.235202.

78 Mizuochi, N., Yamasaki, S., Takizawa, H. et al. (2003). Epr studies of the isolated negatively charged silicon vacancies in n-type 4H- and 6H-SiC: identification of C_{3v} symmetry and silicon sites. *Phys. Rev. B* 68: 165206. https://doi.org/10.1103/PhysRevB.68.165206.

79 Soykal, O.O., Dev, P., and Economou, S.E. (2016). Silicon vacancy center in 4H-SiC: electronic structure and spin–photon interfaces. *Phys. Rev. B* 93: 081207. https://doi.org/10.1103/PhysRevB.93.081207.

80 Soykal, O.O. and Reinecke, T.L. (2017). Quantum metrology with a single spin-$\frac{3}{2}$ defect in silicon carbide. *Phys. Rev. B* 95: 081405. https://doi.org/10.1103/PhysRevB.95.081405.

81 Widmann, M., Niethammer, Fedyanin, D. Yu. et al. (2019). Electrical charge state manipulation of single silicon vacancies in a silicon carbide quantum optoelectronic device, *Nano Lett.* 19 (10): 7173–7180. https://doi.org/10.1021/acs.nanolett.9b02774.

82 Economou, S.E. and Dev, P. (2016). Spin–photon entanglement interfaces in silicon carbide defect centers. *Nanotechnology* 27 (50): 504001. https://doi.org/10.1088/0957-4484/27/50/504001.

83 Dong, W., Doherty, M.W., and Economou, S.E. (2019). Spin polarization through intersystem crossing in the silicon vacancy of silicon carbide. *Phys. Rev. B* 99: 184102. https://doi.org/10.1103/PhysRevB.99.184102.

84 Hornos, T., Gali, A., and Svensson, B.G. (2011). Large-scale electronic structure calculations of vacancies in 4H-SiC using the heyd-scuseria-ernzerhof screened hybrid density functional. In: E. V. Monakhov, T. Hornos, and B. G. Svensson, editors, *Silicon Carbide and Related Materials 2010*, *Materials Science Forum*, vol. 679–680, 261–264. Trans Tech Publications Ltd. https://doi.org/10.4028/www.scientific.net/MSF.679-680.261.

85 Bardeleben, H.J., Cantin, J.L., Henry, L., and Barthe, M.F. (2000). Vacancy defects in p-type 6H−SiC created by low-energy electron irradiation. *Phys. Rev. B* 62: 10841–10846. https://doi.org/10.1103/PhysRevB.62.10841.

86 Heinisch, H.L., Greenwood, L.R., Weber, W.J., and Williford, R.E. (2004). Displacement damage in silicon carbide irradiated in fission reactors. *J. Nucl. Mater.* 327 (2–3): 175–181. https://doi.org/10.1016/j.jnucmat.2004.02.012.

87 Fuchs, F., Stender, B., Trupke, M. et al. (2015). Engineering near-infrared single-photon emitters with optically active spins in ultrapure silicon carbide. *Nat. Commun.* 6: 7578. https://doi.org/10.1038/ncomms8578.

88 Bardeleben, H.J., Cantin, J.L., Vickridge, I., and Battistig, G. (2000). Proton-implantation-induced defects in n-type 6H- and 4H−SiC: an electron paramagnetic resonance study. *Phys. Rev. B* 62: 10126–10134. https://doi.org/10.1103/PhysRevB.62.10126.

89 Kraus, H., Simin, D., Kasper, C. et al. (2017). Three-dimensional proton beam writing of optically active coherent vacancy spins in silicon carbide. *Nano Lett.* 17 (5): 2865–2870. https://doi.org/10.1021/acs.nanolett.6b05395.

90 Wang, J., Zhang, X., Zhou, Yu. et al. (2017). Scalable fabrication of single silicon vacancy defect arrays in silicon carbide using focused ion beam. *ACS Photonics* 4 (5): 1054–1059. https://doi.org/10.1021/acsphotonics.7b00230.

91 Embley, J.S., Colton, J.S., Miller, K.G. et al. (2017). Electron spin coherence of silicon vacancies in proton-irradiated 4H-SiC. *Phys. Rev. B* 95: 045206. https://doi.org/10.1103/PhysRevB.95.045206.

92 Wang, J., Zhou, Yu., Zhang, X. et al. (2017). Efficient generation of an array of single silicon-vacancy defects in silicon carbide. *Phys. Rev. Appl.* 7: 064021. https://doi.org/10.1103/PhysRevApplied.7.064021.

93 Wang, J.F., Li, Q., Yan, F.F. et al. (2019). On-demand generation of single silicon vacancy defects in silicon carbide. *ACS Photonics* 6 (7): 1736–1743. https://doi.org/10.1021/acsphotonics.9b00451.

94 Kasper, C., Klenkert, Z., Shang, Z. et al. (2020). Influence of irradiation on defect spin coherence in silicon carbide, *Phys. Rev. Applied* 13: 044054. https://doi.org/10.1103/PhysRevApplied.13.044054.

95 Poshakinskiy, A.V. and Astakhov, G.V. (2019). Optically detected spin-mechanical resonance in silicon carbide membranes, *Phys. Rev. B* 100: 094104. https://doi.org/10.1103/PhysRevB.100.094104.

96 Bracher, D.O. and Evelyn, L.H. (2015). Fabrication of high-Q nanobeam photonic crystals in epitaxially grown 4H-SiC. *Nano Lett.* 15 (9): 6202–6207. https://doi.org/10.1021/acs.nanolett.5b02542.

97 Radulaski, M., Widmann, M., Niethammer, M. et al. (2017). Scalable quantum photonics with single color centers in silicon carbide. *Nano Lett.* 17 (3): 1782–1786. https://doi.org/10.1021/acs.nanolett.6b05102.

98 Lohrmann, A., Karle, T.J., Sewani, V.K. et al. (2017). Integration of single-photon emitters into 3C-SiC microdisk resonators. *ACS Photonics* 4 (3): 462–468. https://doi.org/10.1021/acsphotonics.6b00913.

99 Mattausch, A., Bockstedte, M., and Pankratov, O. (2003). Ab initio study of the migration of intrinsic defects in 3C−SiC. *Phys. Rev. B* 68: 205201. https://doi.org/10.1103/PhysRevB.68.205201.

100 Chen, Yu.-C., Salter, P.S., Niethammer, M. et al. (2019). Laser writing of scalable single color centers in silicon carbide. *Nano Lett.* 19 (4): 2377–2383. https://doi.org/10.1021/acs.nanolett.8b05070.

101 David, M.L., Alfieri, G., Monakhov, E.M. et al. (2004). Electrically active defects in irradiated 4H-SiC. *J. Appl. Phys.* 95 (9): 4728–4733. https://doi.org/10.1063/1.1689731.

102 Baranov, P.G., Bundakova, A.P., Soltamova, A.A. et al. (2011). Silicon vacancy in sic as a promising quantum system for single-defect and single-photon spectroscopy. *Phys. Rev. B* 83: 125203. https://doi.org/10.1103/PhysRevB.83.125203.

103 Riedel, D., Fuchs, F., Kraus, H. et al. (2012). Resonant addressing and manipulation of silicon vacancy qubits in silicon carbide. *Phys. Rev. Lett.* 109: 226402. https://doi.org/10.1103/PhysRevLett.109.226402.

104 Soltamov, V.A., Soltamova, A.A., Baranov, P.G., and Proskuryakov, I.I. (2012). Room temperature coherent spin alignment of silicon vacancies in 4H- and 6H-SiC. *Phys. Rev. Lett.* 108: 226402. https://doi.org/10.1103/PhysRevLett.108.226402.

105 Nagy, R., Niethammer, M., Widmann, M. et al. (2019). High-fidelity spin and optical control of single silicon-vacancy centres in silicon carbide. *Nat. Commun.* 10 (1): 18. https://doi.org/10.1038/s41467-019-09873-9.

106 Banks, H.B., Soykal, O.O., Myers-Ward, R.L. et al. (2019). Resonant optical spin initialization and readout of single silicon vacancies in 4H-SiC. *Phys. Rev. Appl.* 11: 024013. https://doi.org/10.1103/PhysRevApplied.11.024013.

107 Carter, S.G., Soykal, O.O., Dev, P. et al. (2015). Spin coherence and echo modulation of the silicon vacancy in 4H-SiC at room temperature. *Phys. Rev. B* 92: 161202. https://doi.org/10.1103/PhysRevB.92.161202.

108 Simin, D., Kraus, H., Sperlich, A. et al. (2017). Locking of electron spin coherence above 20 ms in natural silicon carbide. *Phys. Rev. B* 95 (16): 161201. https://doi.org/10.1103/PhysRevB.95.161201.

109 Fischer, M., Sperlich, A., Kraus, H. et al. (2018). Highly efficient optical pumping of spin defects in silicon carbide for stimulated microwave emission. *Phys. Rev. Appl.* 9: 054006. https://doi.org/10.1103/PhysRevApplied.9.054006.

110 Brereton, P.G., Puent, D., Vanhoy, J. et al. (2020). Spin coherence as a function of depth for high-density ensembles of silicon vacancies in proton-irradiated

4H-SiC. *Solid State Commun.* 320: 114014. https://doi.org/10.1016/j.ssc.2020.114014.

111 Soltamov, V.A., Kasper, C., Poshakinskiy, A.V. et al. (2019). Excitation and coherent control of spin qudit modes in silicon carbide at room temperature. *Nat. Commun.* 10 (1): 1–8. https://doi.org/10.1038/s41467-019-09429-x.

112 Kraus, H., Soltamov, V.A., Riedel, D. et al. (2014). Room-temperature quantum microwave emitters based on spin defects in silicon carbide. *Nat. Phys.* 10 (2): 157–162. https://doi.org/10.1038/nphys2826.

113 Kraus, H., Soltamov, V.A., Fuchs, F. et al. (2014). Magnetic field and temperature sensing with atomic-scale spin defects in silicon carbide. *Sci. Rep.* 4. https://doi.org/10.1038/srep05303.

114 Simin, D., Fuchs, F., Kraus, H. et al. (2015). High-precision angle-resolved magnetometry with uniaxial quantum centers in silicon carbide. *Phys. Rev. Appl.* 4 (1): 014009. https://doi.org/10.1103/PhysRevApplied.4.014009.

115 Lee, S.-Y., Niethammer, M., and Wrachtrup, J. (2015). Vector magnetometry based on $S = \frac{3}{2}$ electronic spins. *Phys. Rev. B* 92 (11): 115201. https://doi.org/10.1103/PhysRevB.92.115201.

116 Niethammer, M., Widmann, M., Lee, S.-Y. et al. (2016). Vector magnetometry using silicon vacancies in 4H-SiC under ambient conditions. *Phys. Rev. Appl.* 6 (3): 034001. https://doi.org/10.1103/PhysRevApplied.6.034001.

117 Simin, D., Soltamov, V.A., Poshakinskiy, A.V. et al. (2016). All-optical DC nanotesla magnetometry using silicon vacancy fine structure in isotopically purified silicon carbide. *Phys. Rev. X* 6 (3): 031014. https://doi.org/10.1103/PhysRevX.6.031014.

118 Anisimov, A.N., Simin, D., Soltamov, V.A. et al. (2016). Optical thermometry based on level anticrossing in silicon carbide. *Sci. Rep.* 6: 33301. http://dx.doi.org/10.1038/srep33301.

119 Udvarhelyi, P., Nagy, R., Kaiser, F. et al. (2019). Spectrally stable defect qubits with no inversion symmetry for robust spin-to-photon interface. *Phys. Rev. Appl.* 11: 044022. https://doi.org/10.1103/PhysRevApplied.11.044022.

120 Itoh, H., Yoshikawa, M., Nashiyama, I. et al. (1990). Radiation induced defects in CVD-grown 3C-SiC. *IEEE Trans. Nucl. Sci.* 37 (6): 1732–1738. https://doi.org/10.1109/23.101184.

121 Itoh, H., Yoshikawa, M., Nashiyama, I. et al. (1995). Photoluminescence of radiation induced defects in 3C–SiC epitaxially grown on Si. *J. Appl. Phys.* 77 (2): 837–842. https://doi.org/10.1063/1.359008.

122 Castelletto, S., Johnson, B.C., Zachreson, C. et al. (2014). Room temperature quantum emission from cubic silicon carbide nanoparticles. *ACS Nano* 8 (8): 79387947. https://doi.org/10.1021/nn502719y.

123 Son, N.T., Sörman, E., Chen, W.M. et al. (1996). Dominant recombination center in electron irradiated 3C SiC. *J. Appl. Phys.* 79 (7): 3784–3786. https://doi.org/10.1063/1.361214.

124 Son, N.T., Sörman, E., Chen, W.M. et al. (1997). Optically detected magnetic resonance studies of defects in electron-irradiated 3C SiC layers. *Phys. Rev. B* 55: 2863–2866. https://doi.org/10.1103/PhysRevB.55.2863.

125 Deák, P., Miró, J., Gali, A. et al. (1999). The spin state of the neutral silicon vacancy in 3C-SiC. *Appl. Phys. Lett.* 75 (14): 2103–2105. https://doi.org/10.1063/1.124930.

126 Zywietz, A., Furthmüller, J., and Bechstedt, F. (2000). Spin state of vacancies: from magnetic Jahn-Teller distortions to multiplets. *Phys. Rev. B* 62: 6854–6857. https://doi.org/10.1103/PhysRevB.62.6854.

127 Lefèvre, J., Costantini, J.-M., Gourier, D. et al. (2011). Characterization of a silicon-related defect detected by its excited triplet state in electron-irradiated 3C-SiC. *Phys. Rev. B* 83: 075201. https://doi.org/10.1103/PhysRevB.83.075201.

128 Rauls, E., Lingner, Th., Hajnal, Z. et al. (2000). Metastability of the neutral silicon vacancy in 4H-SiC. *Phys. Status Solidi B* 217 (2): r1–r3. https://doi.org/10.1002/(SICI)1521-3951(200002)217:2<R1::AID-PSSB99991>3.0.CO;2-3.

129 Umeda, T., Son, N.T., Isoya, J. et al. (2006). Identification of the carbon antisite-vacancy pair in 4H-SiC. *Phys. Rev. Lett.* 96: 145501. https://doi.org/10.1103/PhysRevLett.96.145501.

130 Umeda, T., Ishoya, J., Ohshima, T. et al. (2007). Identification of positively charged carbon antisite-vacancy pairs in 4H−SiC. *Phys. Rev. B* 75: 245202. https://doi.org/10.1103/PhysRevB.75.245202.

131 Son, N.T., Stenberg, P., Jokubavicius, V. et al. (2019). Energy levels and charge state control of the carbon antisite-vacancy defect in 4H-SiC. *Appl. Phys. Lett.* 114 (21): 212105. https://doi.org/10.1063/1.5098070.

132 Lee, S.-Y., Widmann, M., Rendler, T. et al. (2013). Readout and control of a single nuclear spin with a metastable electron spin ancilla. *Nat. Nanotechnol.* 8 (7): 487–492. https://doi.org/10.1038/nnano.2013.104.

133 Bardeleben, H.J., Cantin, J.L., Rauls, E., and Gerstmann, U. (2015). Identification and magneto-optical properties of the NV center in 4H−SiC. *Phys. Rev. B* 92: 064104. https://doi.org/10.1103/PhysRevB.92.064104.

134 Zargaleh, S.A., von Bardeleben, H.J., Cantin, J.L. et al. (2018). Electron paramagnetic resonance tagged high-resolution excitation spectroscopy of NV-centers in 4H-SiC. *Phys. Rev. B* 98: 214113. https://doi.org/10.1103/PhysRevB.98.214113.

135 Sato, S.-i., Narahara, T., Abe, Y. et al. (2019). Formation of nitrogen-vacancy centers in 4H-SiC and their near infrared photoluminescence properties. *J. Appl. Phys.* 126 (8): 083105. https://doi.org/10.1063/1.5099327.

136 Pan, F., Zhao, M., and Mei, L. (2010). First-principles prediction of the negatively-charged nitrogen-silicon-vacancy center in cubic silicon carbide. *J. Appl. Phys.* 108 (4): 043917. https://doi.org/10.1063/1.3471813.

137 Weber, J.R., Koehl, W.F., Varley, J.B. et al. (2011). Defects in SiC for quantum computing. *J. Appl. Phys.* 109 (10): 102417. https://doi.org/10.1063/1.3578264.

138 Csore, A., Gällström, A., Janzén, E., and Gali, A. (2016). Investigation of Mo defects in 4H-SiC by means of density functional theory. *Mater. Sci. Forum* 858–860: 261. https://doi.org/10.4028/www.scientific.net/MSF.858.261.

139 Baur, J., Kunzer, M., and Schneider, J. (1997). Transition metals in SiC polytypes, as studied by magnetic resonance techniques. *Phys. Status Solidi A* 162 (1): 153–172. https://doi.org/10.1002/1521-396X(199707)162:1<153::AID-PSSA153>3.0.CO;2-3.

140 Wolfowicz, G., Anderson, C.P., Diler, B. et al. (2020). Vanadium spin qubits as telecom quantum emitters in silicon carbide, *Sci. Adv.* 6 (18): eaaz1192. https://doi.org/10.1126/sciadv.aaz1192.

141 Tien Son, N., Thang Trinh, X., Gällström, A. et al. (2012). Electron paramagnetic resonance and theoretical studies of Nb in 4H- and 6H-SiC. *J. Appl. Phys.* 112 (8): 083711. https://doi.org/10.1063/1.4759362.

142 Egilsson, T., Bergman, J.P., Ivanov, I.G. et al. (1999). Properties of the D_1 bound exciton in 4H−SiC. *Phys. Rev. B* 59: 1956–1963. https://doi.org/10.1103/PhysRevB.59.1956.

143 Lohrmann, A., Castelletto, S., Klein, J.R. et al. (2016). Activation and control of visible single defects in 4H-, 6H-, and 3C-SiC by oxidation. *Appl. Phys. Lett.* 108 (2): 021107. https://doi.org/10.1063/1.4939906.

144 Abe, Y., Umeda, T., Okamoto, M. et al. (2018). Single photon sources in 4H-SiC metal-oxide-semiconductor field-effect transistors. *Appl. Phys. Lett.* 112 (3): 031105. https://doi.org/10.1063/1.4994241.

145 Johnson, B.C., Woerle, J., Haasmann, D. et al. (2019). Optically active defects at the SiC/SiO_2 interface. *Phys. Rev. Appl.* 12: 044024. https://doi.org/10.1103/PhysRevApplied.12.044024.

146 Knaup, J.M., Deák, P., Frauenheim, Th. et al. (2005). Defects in SiO_2 as the possible origin of near interface traps in the SiC/SiO_2 system: a systematic theoretical study. *Phys. Rev. B* 72: 115323. https://doi.org/10.1103/PhysRevB.72.115323.

147 Lienhard, B., Schröder, T., Mouradian, S. et al. (2016). Bright and photostable single-photon emitter in silicon carbide. *Optica* 3 (7): 768–774. https://doi.org/10.1364/OPTICA.3.000768.

148 Wang, J., Zhou, J., Wang, Z. et al. (2018). Bright room temperature single photon source at telecom range in cubic silicon carbide. *Nat. Commun.* 9: 4106. https://doi.org/10.1038/s41467-018-06605-3.

149 Cochrane, C.J., Blacksberg, J., Anders, M.A., and Lenahan, P.M. (2016). Vectorized magnetometer for space applications using electrical readout of atomic scale defects in silicon carbide. *Sci. Rep.* 6: 37077. https://doi.org/10.1038/srep37077.

150 Gruber, G., Cottom, J., Meszaros, R. et al. (2018). Electrically detected magnetic resonance of carbon dangling bonds at the Si-face 4h-SiC/SiO_2 interface. *J. Appl. Phys.* 123 (16): 161514. https://doi.org/10.1063/1.4985856.

151 Umeda, T., Kim, G.-W., Okuda, T. et al. (2018). Interface carbon defects at 4H-SiC(0001)/SiO_2 interfaces studied by electron-spin-resonance spectroscopy. *Appl. Phys. Lett.* 113 (6): 061605. https://doi.org/10.1063/1.5041059.

Part II

Gallium Nitride (GaN), Diamond, and Ga_2O_3

18

Ammonothermal and HVPE Bulk Growth of GaN

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18.1 Introduction

For the last three decades, the nitride community has struggled with crystallization of bulk gallium nitride (GaN) and fabrication of native substrates. The most popular GaN-based devices, light-emitting diodes (LEDs), are built on foreign sapphire substrates. Silicon wafers are often used by academic facilities, but no spectacular improvement in LEDs fabricated on Si is observed. In the case of nitride-based electronic devices, high electron mobility transistors (HEMTs) are prepared today mainly on silicon substrates. A few kinds of devices have already been commercialized https://www.infineon.com/cms/en/product/power/gan-hemt-gallium-nitride-transistor/. It seems, however, that a long and bumpy road is ahead of the industry in order to achieve a full commercial success, comparable to that of LEDs. No doubt, the lack of native wafers, of high structural quality and appropriate size as well as properties, limits the development of all GaN-based electronic devices. Highly conductive native substrates are required for preparing high-power vertical transistors or diodes. Obviously, availability of semi-insulating gallium nitride (SI-GaN) substrates for making lateral devices (i.e. HEMT transistors) also remains an open issue. Therefore, the nitride community is still looking for the best technology to fabricate GaN substrates. For many years, work on developing bulk GaN has mainly been motivated by the laser diode market. Today, the main driving force for crystallizing bulk GaN seems to be the electronic industry. However, synthesizing GaN is quite a challenging process. The compound melts at extremely high temperature (exceeding 2200 °C), and the nitrogen pressure necessary for congruent melting of GaN is expected to be higher than 6 GPa [1–3]. Thus, today, it is impossible to crystallize GaN from the melt. This compound should be grown by other techniques requiring lower pressure and temperature. Crystallization from gas phase, solution, or any combination

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

thereof must be included. Three main technologies are applied for obtaining GaN: sodium flux, ammonothermal, and halide vapor phase epitaxy (HVPE). The first two represent crystallization from solution, the third one from vapor phase. There are also some modifications of these methods, especially for vapor phase, i.e. halide free vapor phase epitaxy or oxide vapor phase epitaxy (HFVPE [4–6] and OVPE [7], respectively). Recently, a growing interest in GaN substrates has been observed as well as an increase in their production volume. They are mainly fabricated in Japan. Companies like SCIOCS by Sumitomo Chemical (https://www.sciocs.com/english/products/GaN_substrate.html), Sumitomo Electric Industries (SEI) (https://global-sei.com/sc/products_e/gan), Mitsubishi Chemical Corporation (MCC) (https://www.m-chemical.co.jp/en/products/departments/mcc/nes/product/1201029_9004.html), or Furukawa (https://www.furukawakk.co.jp/e/business/others) can produce 2-in. and even 4-in. HVPE-GaN substrates. Mostly, highly conductive (n-type) substrates (GaN doped with silicon or/and germanium) are sold. SI-GaN doped with iron is available too. HVPE-GaN wafers are also offered by the Chinese company Nanowin (undoped, highly conductive doped with silicon, and SI wafers doped with iron) (http://en.nanowin.com.cn/) as well as by the French company Lumilog (undoped, highly conductive doped with silicon, and SI wafers doped with iron) (https://www.ceramicmaterials.saint-gobain.com/lumilog). The latter belongs to the Saint Gobain concern. Obviously, many companies work on fabricating bulk GaN without any special publicity. They develop not only HVPE method but also ammonothermal or sodium flux ones. Herein, MCC, working on ammonothermal crystallization of GaN, can be a good example (https://www.m-chemical.co.jp/en/products/departments/mcc/nes/product/1201029_9004.html) [8, 9]. Besides, MCC the ammonothermal method is advanced by such companies as SixPoint Materials Inc. (USA) [10] or (most probably) Kyocera (formerly a crystal growth division at Soraa, Inc., USA/Japan) [11]. However, ammonothermal GaN (Am-GaN) substrates produced by these mentioned companies are not yet available on a large scale on the market. Am-GaN wafers, highly conductive and SI, are mainly sold by the Institute of High Pressure Physics of the Polish Academy of Sciences (IHPP PAS) (https://www.unipress.waw.pl/growth/index.php/ammono-gan-wafers-sales). The Institute is the owner of, formerly, company Ammono S.A. In turn, the sodium flux method is developed at Osaka University, an academic institution [12]. Any guesses that some companies are working on this method can only come from a detailed patent analysis. Two-inch sodium flux crystals of high structural quality were demonstrated [13]. However, they are not available on the market. In the academic world, many institutes and universities work on bulk GaN growth. They include Tokyo University of Agriculture and Technology [14], Tohoku University [15], Yamaguchi University [16], and University of California Santa Barbara [17]. It should, however, be noted that up to now, no one has demonstrated a real bulk GaN crystal yielding several 10 of wafers per boule as well as a convenient technology for obtaining it. Reasons for lack of thick GaN will be discussed in this chapter in detail. It will be shown that due to anisotropy of the growth and crystallization occurring in the lateral directions during the growth

process in the chosen vertical direction, obtaining real bulk of GaN is difficult, even if native high structural quality seeds are used.

In this chapter, results of GaN bulk growth performed in Poland will be presented. Our description will be based only on crystals obtained by the team working at IHPP PAS, unofficially called Unipress. Two technologies will be described in detail: HVPE and basic ammonothermal. The processes and their results (crystals) will be demonstrated. Some information about wafering procedures, thus the way from as-grown crystal to an epi-ready substrate, will be shown. Results of other groups in the world will be briefly presented as the background for our work. The beginning of the chapter will focus on the history as well as state of the art of HVPE and ammonothermal methods. Then, HVPE deposited on native seeds (ammonothermally grown crystals) will be demonstrated. The crystallization results will be compared to those of basic ammonothermal method. The advantages, disadvantages, and challenges of both technologies will be discussed. A few solutions for further development of bulk GaN growth will be shown. Since the HVPE technology enables to obtain high-purity material (low concentration of unintentionally incorporated dopants and carrier concentration), the doping procedures for crystallizing highly conductive and highly resistive crystals will be analyzed. Doping bases on introducing silicon or germanium (for obtaining n-type material) and carbon, iron, and manganese (for SI-GaN). At the end of the chapter, all the described results will be summarized.

18.2 HVPE Method – History and State of the Art

As mentioned in the Introduction, the HVPE method is the crystallization from gas phase. Hydrochloride reacts with liquid gallium at relatively low temperature (800–900 °C) forming gallium chloride (GaCl). In this temperature range, the partial pressure of GaCl is much higher than that of $GaCl_3$. Therefore, formation of GaCl is more favorable [14]. The latter is transported by the carrier gas (CG, mainly hydrogen or nitrogen) to the crystal growth zone (at temperature of 1000–1100 °C) where a seed is placed. Herein, GaCl reacts with ammonia (NH_3) to synthesize GaN. The scheme of HVPE method is presented in Figure 18.1.

GaN was crystallized for the first time by HVPE in 1968. Maruska and Tietjen [18] used a sapphire wafer as a seed. They grew a GaN layer and determined the energy of the direct bandgap of 3.39 eV. A high free carrier concentration (above 10^{19} cm^{-3}) was reported. It was suggested that the reason of such a high value was the presence of nitrogen vacancies. Most probably, this statement was not true. At that time, commercially available ammonia contained 1000 ppm of water [19]. It was impossible, thus, to fabricate high-purity GaN. Unquestionably, GaN grown by Maruska was unintentionally doped with oxygen. Today, the highest purity GaN crystallized by HVPE contains less than 10^{14} cm^{-3} of unwanted impurities [20]. All reactant gasses as well as gallium are of high purity (6 N or higher). Also, some new special materials, as pyrolytic graphite, boron nitride, tantalum carbide, tungsten carbide, and similar, are applied in place of commonly used quartz for building the

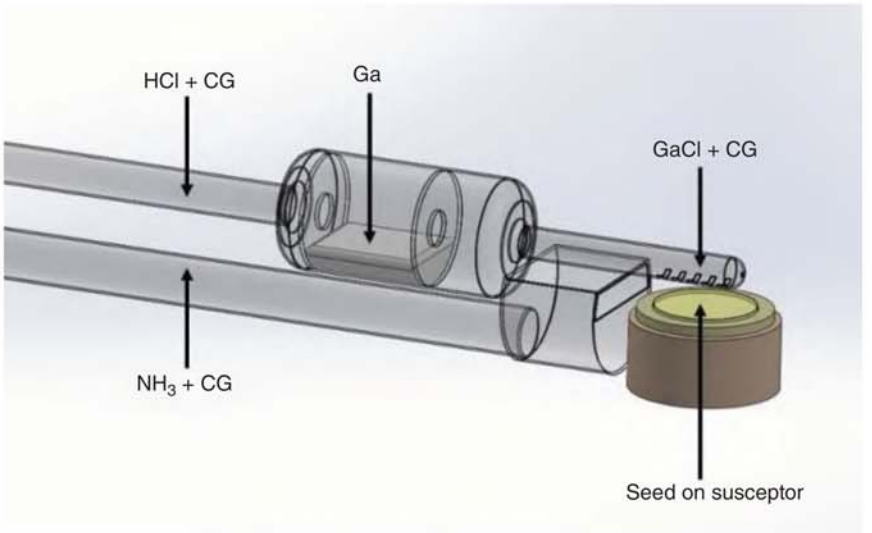

Figure 18.1 Scheme of the HVPE method; horizontal configuration is presented; similar configuration based on quartz material is applied at Unipress; CG, carrier gas.

entire reactor or its crystal growth zone. Next to the purity, the second advantage of the HVPE method is the high growth rate. It is relatively easy to crystallize GaN in the ⟨0001⟩ crystallographic direction (c-direction) with a rate of 100–200 μm/h. A record value was reported by SCIOCS. Yoshida et al. [21] crystalized 800-μm-thick GaN with a rate of 2 mm/h. The main problem in the HVPE technology is the kind of the used seed. As was already shown, the first "historical" candidate was sapphire. Since the 1990s, templates comprising a GaN layer grown by metal organic vapor-phase epitaxy (MOVPE) on sapphire have been used as seeds. Due to mismatch in both lattice constant and thermal expansion coefficient, GaN grown in the c-direction on sapphire templates was cracked. It was, however, observed that if a GaN layer was thick enough, it detached from the foreign seed. In order to obtain a regular habit of the separated crystal, it was necessary to control the lift-off process. One way of achieving that will be briefly described later. The next candidate for a foreign substrate in HVPE-GaN growth was gallium arsenide (GaAs). The value of its thermal expansion coefficient (at 1000 °C) is similar to the one of GaN. Gallium arsenide, unlike sapphire, can be easily removed by etching from the HVPE-GaN layer. Kumagai et al. [22] demonstrated a low-temperature GaN buffer layer on the GaAs(111)A surface. This accomplishment was a real breakthrough in HVPE-GaN growth. SEI developed dislocation elimination by the epitaxial growth with inverse pyramidal pits (DEEP) and advance-dislocation elimination by the epitaxial growth with inverse pyramidal pits (A-DEEP) technologies and fabricated quasi-bulk GaN. The substrates consisted of areas (e.g. arranged in stripes) of high (10^8 cm^{-2}) and low (10^4 cm^{-2}) dislocation density [23–25]. DEEP and A-DEEP approaches will not be described in detail in this chapter. It should be, however, noted that laser diodes applied in BluRay are built on the A-DEEP SEI GaN substrates [23]. In spite

of all, more companies and academic institutions prefer MOVPE-GaN/sapphire templates as seeds for HVPE-GaN growth. As mentioned above, some tricks to obtain the lift-off of the new-grown GaN from sapphire were needed. One of the proposed methods was void assisted separation (VAS) [26–28]. It involved the formation of voids between the template and the new-grown HVPE-GaN. A thin titanium layer was deposited on the surface of an MOVPE-GaN/sapphire template. The layer was annealed in ammonia atmosphere to form a TiN nanonet. Due to GaN, decomposition voids were formed under the nanonet. Next, during HVPE growth, the GaN layer nucleated through the openings in TiN and the voids remained on the GaN-sapphire interface. Stress induced by the difference in thermal expansion coefficients of HVPE-GaN and sapphire resulted in a well-controlled self-separation of GaN during the cooling process in HVPE. Free-standing (FS) crystals and then, after proper wafering procedures: grinding, lapping, mechanical, and chemo-mechanical polishing, GaN substrates were obtained. As mentioned in the Introduction, 2- and 4-in. GaN wafers, with their (0001) plane (c-plane) prepared to the epi-ready state, are offered by a few companies. They apply VAS or its derivatives for growing GaN. The main problem of such substrates is the bending of their crystallographic planes. The wafer is macroscopically flat and has two parallel surfaces. However, the angle between the crystallographic planes and the surface of the substrate (misorientation angle) changes. Therefore, a uniform misorientation of the wafer is difficult or often simply impossible. The main trick used to reduce the bending of the crystallographic planes is to start the crystallization process in a three-dimensional (3D) growth mode and change it in time (by changing the supersaturation) into a two-dimensional (2D) one. This solution was demonstrated by Geng et al. [29]. The intrinsic strain, the driving force of the wafer bending, can be reduced by the introduction of a 3D growth in the initial crystallization stage. Bending is, thus, controlled by the thickness of the 3D GaN layer. It is clearly shown in Figure 18.2a where the radius of curvature (bending of crystallographic planes) is presented as a function of the thickness of the 3D GaN layer. Figure 18.2b represents images of a cross section (m-plane) of GaN grown on a sapphire template at Unipress. The sample was photo-etched. In this technique, the etching rate depends on the free carrier concentration in the material and crystal sectors with different electrical properties can be visualized. The 3D and 2D growth modes can be well distinguished.

Figure 18.3a presents a typical morphology of 1-mm-thick GaN deposited on an MOVPE-GaN/sapphire template. Many hillocks are visible. Figure 18.3b shows a rocking curve of a FS GaN crystal (as-grown) obtained after crystallization on such a seed. The full width at half maximum (FWHM) for (00.2) reflection is close to 150 arcsec. The X-ray beam size was 1 mm × 10 mm. The etch pit density (EPD) and, correlated with it, threading dislocation density (TDD) in FS HVPE-GaN are on the order of $1–5 \times 10^6$ cm^{-2}. Generally, GaN crystals grown on foreign seeds have a thickness of 1–2 mm and one well-developed facet, c-plane. From a sapphire seed, one GaN crystal and, after wafering, one substrate are fabricated. Therefore, it usually is a wafer to wafer technology. Fujito et al. [30] succeeded, however, in presenting 2-in. in diameter and 5.8-mm-thick bulk GaN. It allowed to fabricate a few wafers from one HVPE process.

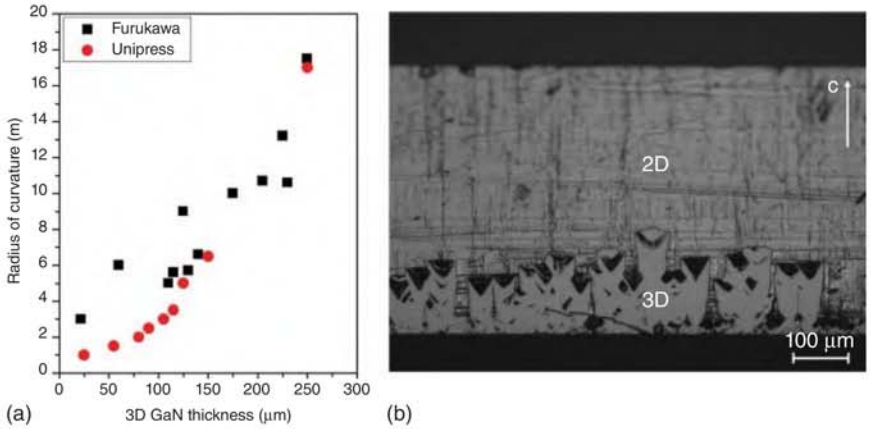

Figure 18.2 (a) Radius of curvature (bending of crystallographic planes) as a function of 3D GaN layer thickness; data from Unipress and Furukawa [29] are presented; (b) optical microscopy image of cross section of GaN grown on MOVPE-GaN/sapphire; sample was photo-etched; 3D and 2D growth modes are well visible. Source: Data from Geng et al. [29]

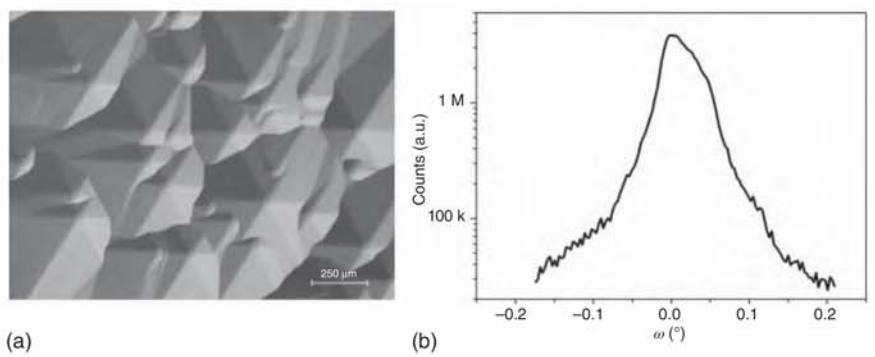

Figure 18.3 (a) Morphology of 1-mm-thick GaN grown by HVPE on MOVPE-GaN/sapphire; view on the c-plane; (b) X-ray rocking curve for FS HVPE-GaN (as-grown) crystallized before on MOVPE-GaN/sapphire; FWHM for (00.2) reflection is close to 150 arcsec.

Typical unintentionally doped (UID) GaN grown on a foreign (sapphire) seed by the HVPE method is n-type with the free carrier concentration on the order of 10^{16} cm^{-3}. Doping with silicon and/or germanium to obtain n-type crystals and iron or carbon for fabricating SI-GaN is commonly used and described in detail in the literature (e.g. [31–34]).

18.3 Ammonothermal Method – History and State of the Art

Ammonothermal crystallization is analogous to hydrothermal growth used for the production of quartz [35]. The difference lies in using supercritical ammonia instead of water. In an ammonothermal process, GaN feedstock is dissolved in supercritical

ammonia in one zone of a high-pressure autoclave. The dissolved material is transported to the second zone, in which the solution is supersaturated and GaN crystallization on native seeds takes place. The convection mass transport is enabled by an appropriate temperature gradient between the two zones. Different mineralizers can be added to ammonia in order to accelerate its dissociation and enhance the solubility of GaN. The choice of applied mineralizers determines the type of environment: acidic or basic. In ammonoacidic growth, halide compounds (with NH_4^+ ions) are introduced into the supercritical solution. Alkali metals or their amides (with NH_2^- ions) are used in the case of ammonobasic crystallization. In the latter approach, a negative temperature coefficient of solubility is observed (https://www.linkedin.com/pulse/mystery-solubility-retrograde-temperature-inverse-why-mukherjee). This results in the direction of the chemical transport of GaN from the low-temperature solubility zone (with feedstock) to the high-temperature crystallization one (with seeds). Figure 18.4 shows schemes of acidic and basic ammonothermal process. Typical pressures and temperatures during ammonothermal crystallization vary from 1000 to 6000 atm and 300–750 °C, respectively.

As mentioned, native seeds, usually FS HVPE-GaN, are used in the ammonothermal process. They are mainly up to 1-mm-thick crystals with well-developed c-planes. This results from a habit of HVPE-GaN deposited before on a foreign foundation (MOVPE-GaN/sapphire; see 18.2). Thus, the main growth directions in the ammonothermal method are ⟨0001⟩ or ⟨000$\bar{1}$⟩ (the −c-direction). Obviously, using FS HVPE-GaN as seeds does not allow to obtain high structural quality of Am-GaN since the crystallographic quality of the seed is low and can only be duplicated, but not improved. However, many results of such research were published (e.g. [36–38]). A breakthrough in the structural quality of Am-GaN was achieved by the Polish company Ammono (today IHPP PAS). Their solution involved seeded growth

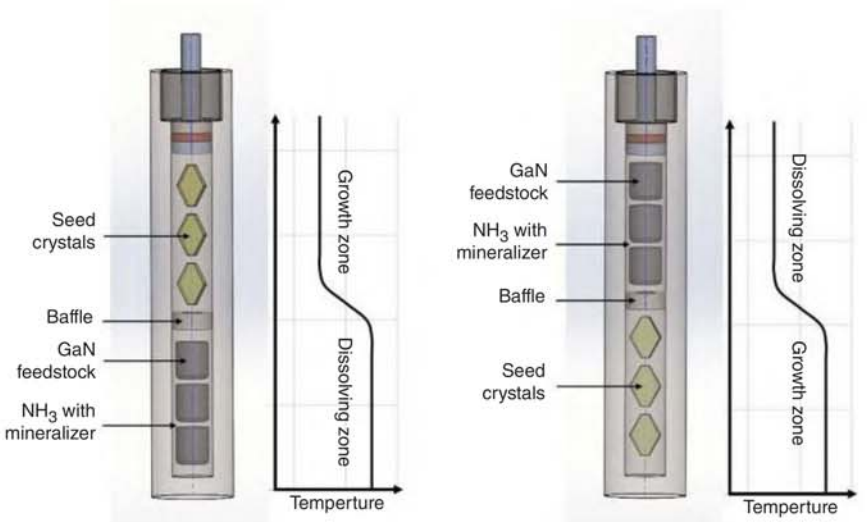

Figure 18.4 Scheme of the ammonothermal method (a) acidic; (b) basic.

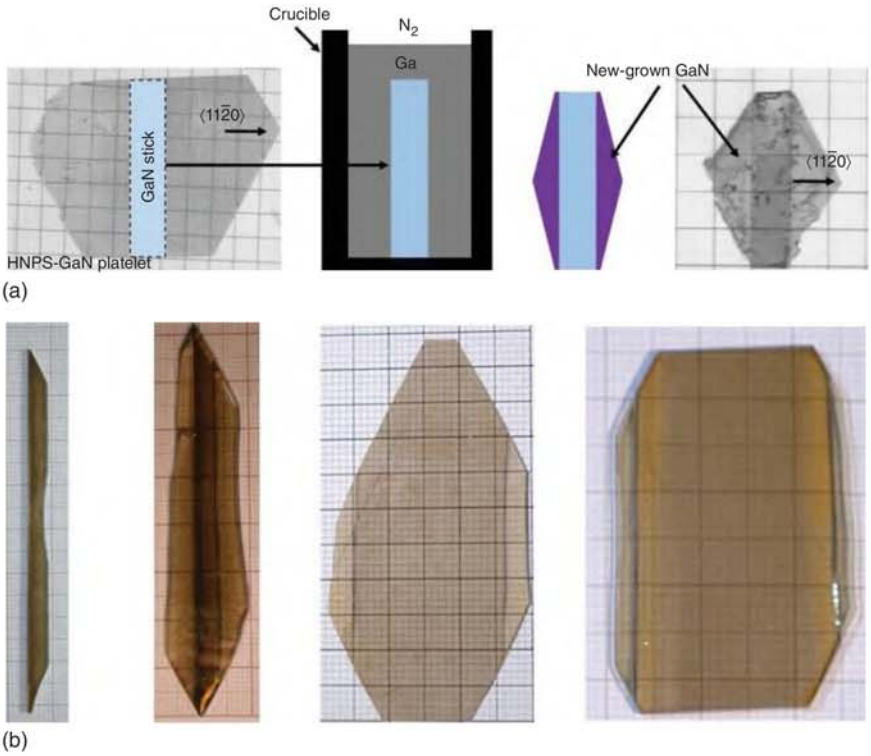

Figure 18.5 (a) Scheme of HNPS growth presented by Grzegory et al. [39]; the idea as well as resulting HNPS-GaN crystal are presented; GaN stick was overgrown in the a crystallographic directions; new-grown material was nucleated from the edges of the seed and was defect-free; grid 1 mm; (b) same growth method applied at Ammono Company; results of GaN stick overgrowth during many crystal growth processes; grid 1 mm. Source: Grzegory et al. [39].

and was based on an idea which had been presented in the high nitrogen pressure solution (HNPS) method [39]. Grzegory used a GaN stick, previously sliced from a bigger HNPS-GaN platelet crystal. Such a seed was vertically placed in a crucible with liquid gallium. The high nitrogen pressure crystallization process occurred mainly in the fastest growth directions $\langle 11\bar{2}0 \rangle$, the *a*-directions. The new-grown material was nucleated on the edges of the stick, and, therefore, it was defect-free. The scheme of the method applied by Grzegory is presented in Figure 18.5a. In turn, Figure 18.5b shows the approach of Ammono Company. A long HVPE-GaN stick was overgrown in the *a*-directions until the $(11\bar{2}0)$ facets disappeared and the $(10\bar{1}0)$ facets (m-facets) appeared. After many ammonothermal runs, a crystal with a big lateral surface could be obtained from a thin seed.

Today, the basic Am-GaN growth developed at IHPP PAS consists of two parts described below and schematically shown in Figure 18.6:

Part 1 – Enlargement of seeds: The seeds can be enlarged by taking advantage of lateral crystallization in the *a*-direction (the red part of the crystal in Figure 18.6a), and their diameter can reach more than 2 in.

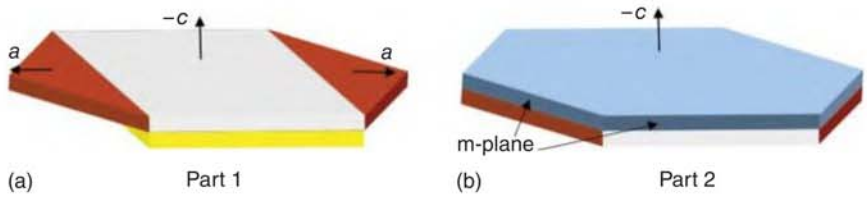

Figure 18.6 Basic ammonothermal growth method (two processes); (a) part 1 – the seed is enlarged in lateral directions; (b) part 2 – the seed is only grown in −c-direction; the $(10\bar{1}0)$ facets (m-planes) are visible.

Part 2 – Multiplication of seeds: Growth is performed mainly in vertical direction, along *c*-axis (the blue part of the crystal in Figure 18.6b). The crystal is sliced perpendicularly to the c-direction. Population of the seeds used for subsequent ammonothermal or/and wafering process (GaN substrate fabrication) is increased. The crystals are structurally flat, and the EPD is on the order of $5 \times 10^4\ \mathrm{cm}^{-2}$.

Figure 18.7a shows a typical growth morphology of basic ammonothermal grown crystal. Hillocks and huge macrosteps are well visible. Results of synchrotron white-beam X-ray topography (SWXRT) for Am-GaN are depicted in Figure 18.7b. It can be seen that the crystal is of extremely high structural quality and crystallographic uniformity. Figure 18.7c presents the etch pits created after defect selective etching (DSE, etching in KOH/NaOH solution at 500 °C) in the material grown in the −c-direction (the blue part of the crystal in Figure 18.6b). Value of EPD was $5 \times 10^4\ \mathrm{cm}^{-2}$.

Today, IHPP PAS crystallizes three kinds of Am-GaN. Their main electrical properties are presented in Table 18.1. Figure 18.8 shows substrates obtained by wafering procedures (slicing, grinding, lapping, mechanical polishing, and chemo-mechanical polishing) from material of properties analyzed in Table 18.1. The main dopant in Am-GaN crystals is oxygen. The free carrier concentration is usually equal to the concentration of this element. Using some getters, one can decrease the oxygen content to $1 \times 10^{18}\ \mathrm{cm}^{-3}$. For growing semi-insulating material, the donors are compensated by manganese acceptors. A lot of information about ammonothermal process and properties of Am-GaN crystals and substrates can be found in Refs [40–42].

An interesting feature of Am-GaN with the highest carrier concentration is the formation of star-like defects after annealing at temperature on the order of the 1000 °C. After this process (or epitaxial growth on an Am-GaN wafer), some defects can appear in the volume of the ammonothermal material. They are clearly shown in Figure 18.9a which presents an image from an optical microscope focused in the volume of the crystal. Horibuchi et al. [43] explained the process of their formation. As was reported [44, 45], ammonothermally grown crystals with a high oxygen (and free carrier) concentration contain a significant number of gallium vacancies ($10^{19}\ \mathrm{cm}^{-3}$) or their complexes with oxygen or hydrogen. At high temperature, the vacancies migrate to dislocation lines forming helical dislocations. It is interesting that these helical dislocations cannot propagate into the overgrown epitaxial

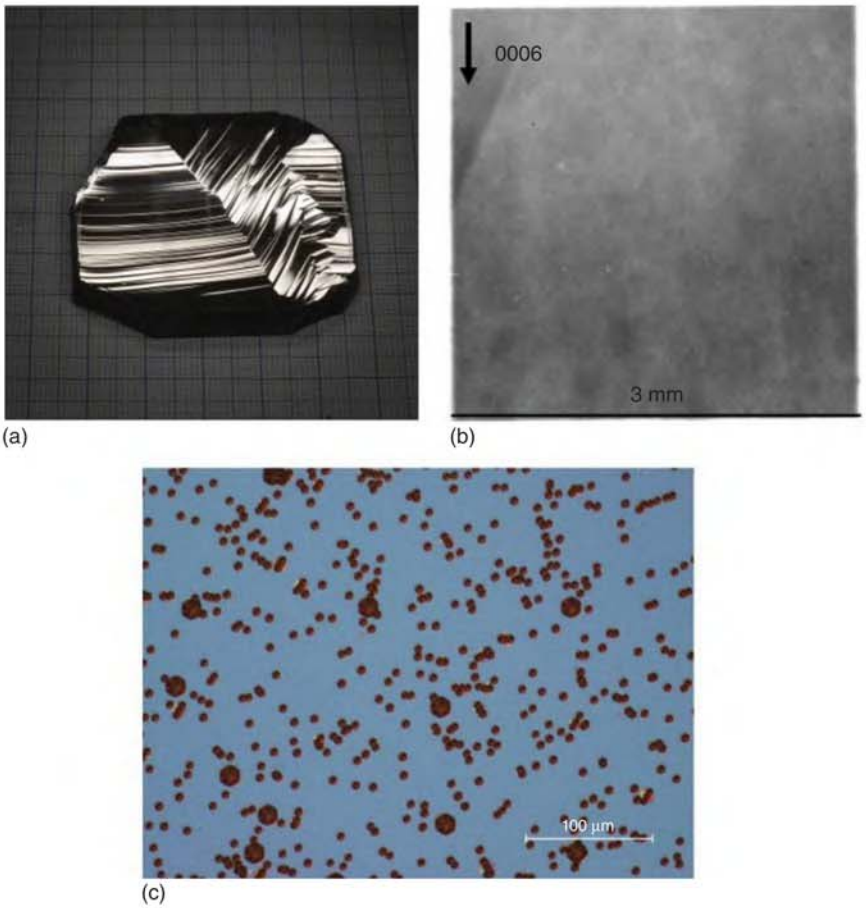

Figure 18.7 (a) Morphology of Am-GaN grown in the −c-direction; (b) synchrotron white-beam X-ray topography (SWXRT) for a 1-in. Am-GaN crystal; uniform gray contrast indicates a low defect density. Source: Courtesy of L. Kirste; grid 1 mm; (c) EPD in the material grown in the: −c-direction (the blue part of the crystal grown in Figure 18.6b); EPD = 5×10^4 cm^{-2}.

Table 18.1 Electrical properties (measured at room temperature using a home-built Hall effect system in van der Pauw configuration) of three types of ammonothermal GaN.

Material type	Conductivity type	Carrier concentration (cm^{-3})	Carrier mobility (cm^2/V s)	Resistivity (Ω cm)
High carrier concentration	n-type	~10^{19}	~150	10^{-3}
Low carrier concentration	n-type	~10^{18}	~250	10^{-2}
High resistivity (Mn-doped)	Semi-insulating	—	—	≥10^8

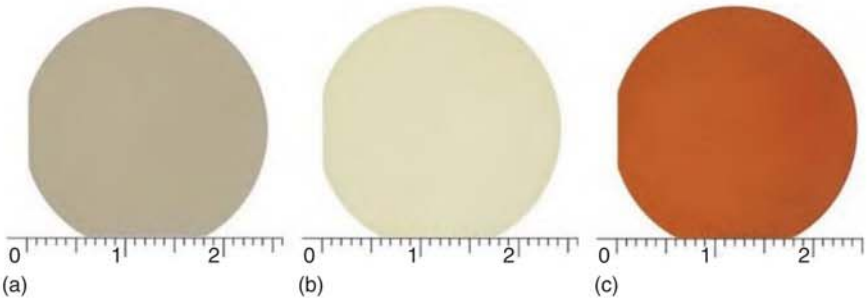

Figure 18.8 Am-GaN substrates prepared by IHPP PAS (a) n-type with a carrier concentration of 10^{19} cm^{-3}; (b) n-type with a carrier concentration of 10^{18} cm^{-3}; (c) semi-insulating doped with Mn; diameter in cm.

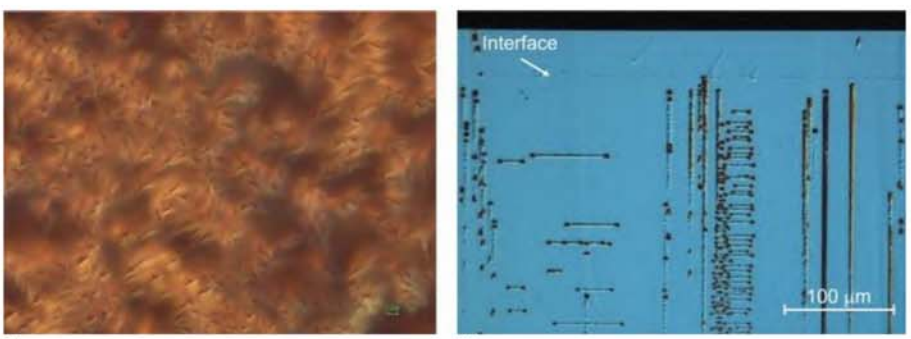

Figure 18.9 Star-like defects in highly conductive Am-GaN: (a) image from an optical microscope focused in the volume of the Am-GaN substrate after epitaxy process at 1100 °C; star-like defects are well visible; (b) cross section, m-plane, of HVPE-GaN grown on highly conducting Am-GaN after DSE; helical defects are well visible in the Am-GaN crystal; they do not propagate into the HVPE-GaN layer.

layer. The defects are stopped at the interface or just before it. It is clearly seen in Figure 18.9b. A differential interference contrast (DIC) microscopy image of an m-plane cross section of HVPE-GaN grown on highly conducting Am-GaN is shown after DSE. The helical defects are well visible in the Am-GaN crystal, but they do not propagate into the HVPE-GaN layer.

One of the most important factors limiting the Am-GaN crystallization in the −c-direction is associated with the anisotropy of the growth. Apart from the $\langle 000\bar{1} \rangle$ direction, crystallization also occurs in the lateral directions at the edges of the crystal, on the m-facets (see Figure 18.6b). This phenomenon was well described by Zajac et al. [42]. It was shown that kinds and concentrations of impurities incorporated into non-polar $(10\bar{1}0)$ facets as well as on the $(000\bar{1})$ plane are vastly different. This causes stress and finally leads to plastic deformation of the growing Am-GaN crystals. The donors' concentrations are higher on the −c-plane and much lower on the side facets. Additionally, higher concentrations of acceptors (C, Fe, Mn, Mg, and others) are detected in the laterally grown GaN.

Figure 18.10 Am-GaN crystal grown in one crystallization run: 6-mm-thick and with a 2.1-in. diameter; grid 1 mm.

In the basic ammonothermal method, the growth in the ⟨0001⟩ direction is treated as parasitic. As a result, the $(000\bar{1})$ surface is exposed, while the opposite (0001) face is completely masked. Similar approach can be used for blocking the crystallization on the side facets. In this case, mechanical blocking seems to be the best idea to hinder growth in directions other than the desired one. Figure 18.10 presents a 2.1-in. in diameter and 6-mm-thick GaN crystal obtained in one ammonothermal process with mechanically blocked side facets.

18.4 HVPE-GaN-on-Ammono-GaN – State of the Art

HVPE-GaN growth on native ammonothermal seeds seems to be a very perspective technology. First official communications about the combination of the two GaN crystallization methods came from Unipress [46, 47]. Using 1-in. Am-GaN substrates with their c-planes prepared to the epi-ready state, HVPE-GaN crystallization with high growth rate, up to 350 μm/h, was reported [48]. Up to 2-mm-thick HVPE-GaN was grown. In order to obtain FS material, the layer was sliced from the seed [49]. The observed morphology was one hillock on the entire crystal's growing surface (see Figure 18.11a). The almost perfect structural quality of ammonothermal seed was reflected by the HVPE layer (see Figure 18.11b) [49–51]. EPD on the c-plane was on the order of 5×10^4 cm^{-2} [52]. The main impurities in UID HVPE-GaN were silicon and oxygen, at the level not higher than 1×10^{17} cm^{-3}. Concentration of oxygen was often below the secondary ion mass spectrometry (SIMS) detection limit [53, 54]. Some traces of iron (1×10^{16} cm^{-3}) were found. In the photoluminescence (PL) spectra, weak signals from magnesium were also observed [53]. In general, PL displayed multiple bound and free exciton peaks. The spectra were dominated by two sharp donor-bound exciton emission lines with extremely low values of FWHM. Acceptor-bound exciton and free exciton emissions were also present [47]. A weak signal in the yellow luminescence (YL) range was detected. It could be correlated with the gallium vacancies or their complexes with silicon or oxygen. HVPE-GaN is usually carbon-free; thus, YL cannot be connected to the presence of this element. No structure close to the band edge was observed in the absorption spectra [47]. Optical-isothermal capacitance transient spectroscopy (OICTS) and deep level

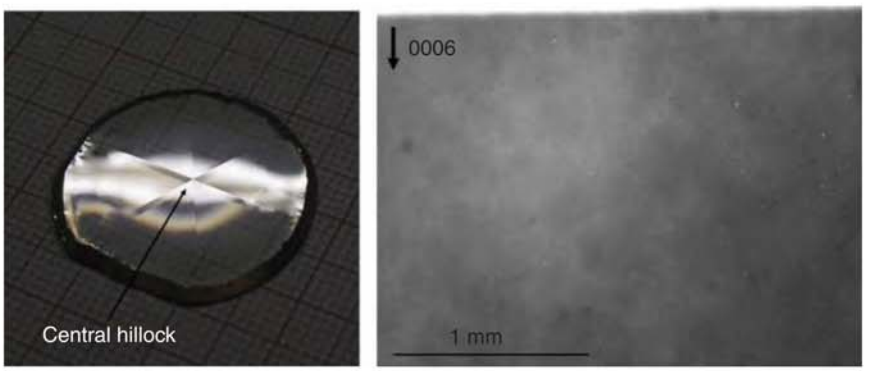

Figure 18.11 (a) Typical morphology of HVPE-GaN grown on Am-GaN seed; one hillock is formed on the surface of the growing crystal; grid 1 mm; (b) SWXRT for FS 1-in.-HVPE-GaN grown before on Am-GaN seed; uniform gray contrasts indicate a high degree of crystalline perfection. Source: Courtesy of L. Kirste.

transient spectroscopy (DLTS) were carried out at Kyoto and Nagoya Universities to investigate hole (OICTS) and electron (DLTS) traps. The main trap detected with OICTS was H1 (0.85 eV above the valence band maximum) with a concentration below 1% of the net carrier concentration. This trap can be connected to the presence of carbon in GaN, and the low concentration is due to no contamination with carbon in HVPE-GaN. However, concentration of the main electron trap detected, E3, comprises 24% of the net carrier concentration (K. Kanegae, M. Horita, J. Suda, private communication). This trap, placed 0.56 eV below the conduction band minimum, could be correlated with substitutional defects or iron impurity. As mentioned above, some traces of iron were found in our HVPE-GaN samples.

18.4.1 Bulk Growth – Challenges

It was presented that thick HVPE-GaN layers can be grown on native ammonothermal seeds. MCC demonstrated 5.8-mm-thick HVPE-GaN crystallized in the $\langle 10\bar{1}0 \rangle$ direction [9]. They used their own Am-GaN from the supercritical acidic ammonia technology (SCAAT) as a seed [8]. The technology was based on the already demonstrated result of growth of 5.8-mm-thick GaN on sapphire in the c-direction [30]. However, the results of MCC seem unique. In most research facilities and companies, despite the high growth rate and purity, HVPE still remains a wafer-to-wafer technology. According to our knowledge, crystallization of thick boules even on perfect ammonothermal seeds is limited by two factors: (i) parasitic deposition occurring in the growth zone and (ii) anisotropy of the crystallization. Since bulk GaN should be grown over a long period of time, the parasitic deposition needs to be completely eliminated. It seems to be a purely technical issue. However, it is a very serious problem. From the scientific point of view, the supersaturation driving the GaN growth should exist only at the surface of the crystal. In all other areas of the reactor as well as close to the HVPE layer, the supersaturation for GaN

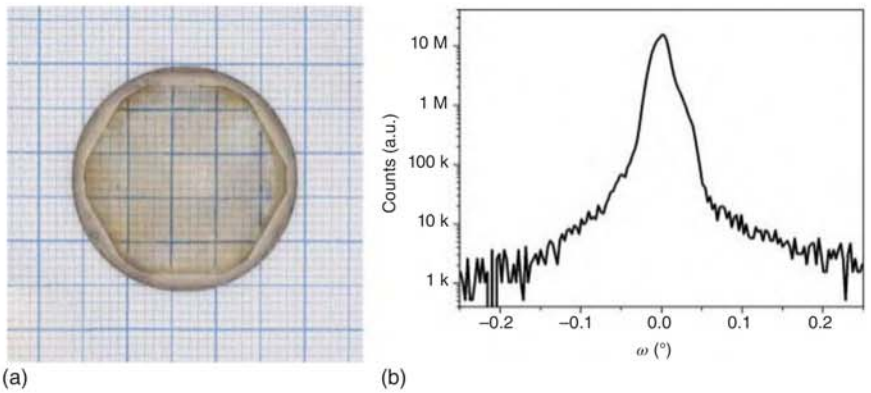

Figure 18.12 (a) Three-mm-thick HVPE-GaN grown on Am-GaN; equilibrium hexagonal crystal habit is well visible; c-plane is reduced; grid 1 mm; (b) rocking curve for (0002) reflection of the same crystal with FWHM of 77 arcsec and bowing radius of 18.6 m; X-ray beam size: 1 mm × 10 mm.

formation should be close to zero or even negative. This is the first issue that should be addressed in order to obtain bulk GaN. The second important factor limiting depositing HVPE-GaN in the c-direction is associated with the anisotropy of the growth and crystallization occurring in lateral directions. During deposition in the $\langle 0001 \rangle$ direction, even if it starts from a round shape of a seed, the natural hexagonal shape of GaN finally appears. As already mentioned, Fujito et al. [30] published a detailed discussion on the formation of a dodecagon shape of a crystal if a round substrate is used as a seed. For HVPE-GaN, the $\langle 11\bar{2}0 \rangle$ is the fastest growth direction and the $\langle 10\bar{1}0 \rangle$ direction is the slowest one. Therefore, during a crystallization process at first, all $(11\bar{2}0)$ facets disappear and all $(10\bar{1}0)$ facets appear and start to dominate. The inclined facets $(10\bar{1}1)$ and $(10\bar{2}2)$ on m-plane sides and $(11\bar{2}2)$ facets on a-plane sides are formed [30]. The formation of this equilibrium shape through the collapse of the growth facet reduces the size of the c-plane. It is clearly shown in Figure 18.12a where 3-mm-thick HVPE-GaN from an Am-GaN seed is presented. The dodecagon shape changes into a hexagonal one. The size of the c-plane is reduced. Figure 18.12b shows a rocking curve for the presented as-grown crystal.

The next problem concerning thick GaN deposited in the c-direction is growth in the lateral directions. It was shown that the kinds and concentrations of impurities incorporated on non-polar and semi-polar facets and on the c-plane are different [77, 78]. This causes stress and finally leads to plastic deformation of the HVPE-GaN layer [49, 52]. SIMS measurements showed that the concentration of oxygen in GaN grown in the c-direction was extremely low, at the level of 10^{16} cm^{-3}. In turn, oxygen concentration in the laterally crystallized material (called wings) always reached 10^{19} cm^{-3}. The large content of dopants and high free carrier concentration lead to an increase of the lattice constants in GaN [55]. It was shown that both a and c lattice constants increased in the laterally grown GaN [56]. The experimental data of lattice constants were used for numerical simulations in order to determine and examine the stress in HVPE-GaN and the seed [57]. Figure 18.13a

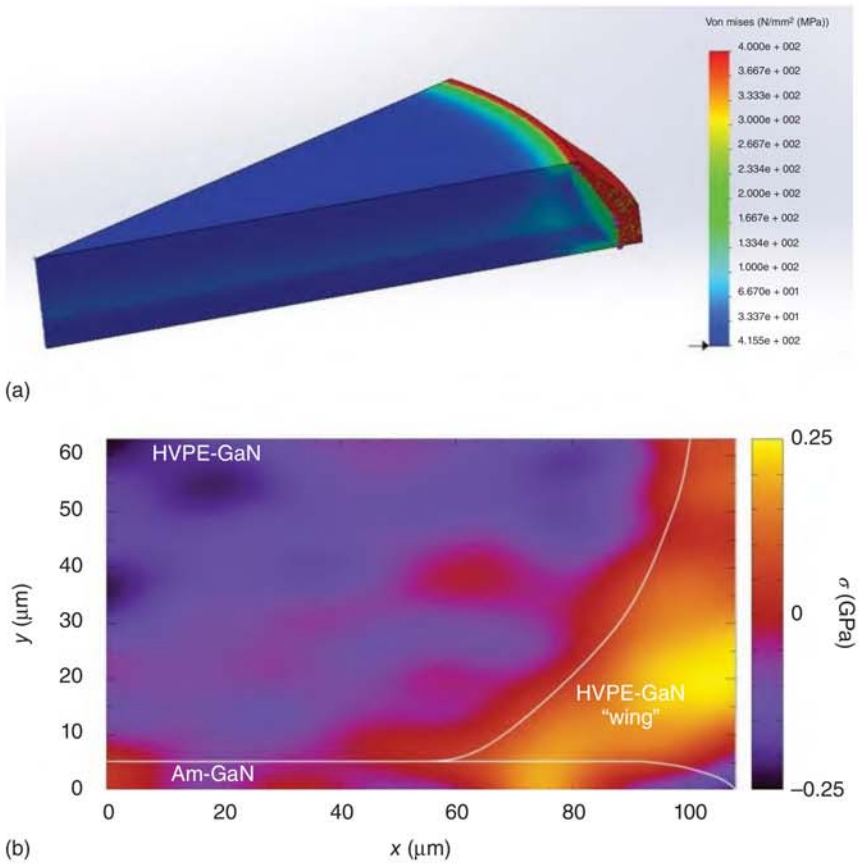

Figure 18.13 (a) Calculated Von Mises stress distribution in HVPE-GaN deposited on 1-in. Am-GaN seed; (b) Raman map of the stress distribution at the edge of the growing crystal (on 1-in. Am-GaN seed); the highest stress was detected in the material grown in lateral directions (wings).

shows the stress distribution in a 1.5-mm-thick layer crystallized on 600-µm-thick Am-GaN. The value of Von Mises stress in HVPE-GaN close to its center was very low, close to 2 MPa. At the interface between the crystal and laterally overgrown GaN, the stress reached 200 MPa. The highest value of maximum equivalent stress was obtained in the side area, and it exceeded 1200 MPa. The strain in HVPE-GaN grown in the c-direction on a native seed was also studied by Raman spectroscopy [58]. The stress of 200 MPa in the wing area was determined (see Figure 18.13b). Again, it was concluded that the non-polar and semi-polar growth of GaN leads to the formation of large stress in the crystal, close to its edges. This stress is much more significant than that generated by the lattice mismatch between the seed and the deposited layer. It should herein be noted that this is a common problem of GaN bulk growth. At the end of 18.3, a similar phenomenon was described for basic ammonothermal method. The situation, however, is opposite to the one described for HVPE. Concentrations of donors are higher on the -c-plane and much lower on the side facets. In the case of Am-GaN, it is difficult to control the conditions on

the particular surface of each crystal. There are too many seeds in the growth zone. Nevertheless, it seems possible in the HVPE technology. Herein, the supersaturation on the surface of the crystal can be strictly controlled. It can be drastically reduced on the edges and sidewalls. Only one growth facet (*c*-facet) can be stabilized and grown out for an arbitrary time period. According to a hypothesis by Professor Zlatko Sitar, this condition may be achieved by controlling the thermal field around the crystal. It has to reach its final shape by adapting to the thermal field rather than taking the equilibrium hexagonal habit. This was demonstrated for aluminum nitride (AlN) growth by physical transport deposition (PVT) and presented on HexaTech web page (http://www.hexatechinc.com/company.html). An AlN crystal assumes the round shape from the seed and expand as forced by the designed thermal field. Once the crystal reaches a constant thermal field, it resumes the equilibrium shape as dictated by the surface energetics, forming various facets. This clearly shows that the equilibrium shape can be overpowered by a proper thermal field design. In this case, the crystal will follow the thermal field and grow in a direction perpendicular to the isotherms. Obviously, there is a big difference in the formation of supersaturation in PVT and HVPE methods. The supersaturation is the difference of thermodynamic potentials at the interface between a crystal and its environment. In the case of PVT, it is almost unambiguous with the temperature distribution on the growing surface. In the case of HVPE, reactions of all vapor species should be considered.

First attempts to change the environment of deposited HVPE-GaN have already been made. Some metal (molybdenum, Mo) elements were added around the crystal. Molybdenum can switch the thermal field as well as catalyze ammonia decomposition in the growth zone. A large reduction in crystallization in lateral directions was observed. It is clearly seen in Figure 18.14. The edges of HVPE-GaN deposited without and with Mo are presented. The lateral growth was almost totally reduced when the HVPE process was additionally performed at a lower temperature, close to 1000 °C (in place of always applied 1045 °C). All these results allow to look optimistically into the future of bulk GaN growth. Still, the highest pressure must be put on obtaining the right temperature gradient on the crystal's growing surface.

18.4.2 Doping

As mentioned before, doping in HVPE method allows to fabricate highly conductive and semi-insulating GaN crystals and then substrates. Usually, growth is performed on foreign seeds, mainly MOVPE-GaN sapphire templates. Therefore, the stress in the layer is completely different than that in HVPE-GaN grown on native seeds. Below, the latter case will be described in detail for GaN doped with silicon, germanium, carbon, iron, and manganese. Some discrepancies with crystallization on foreign substrates will be pointed out.

18.4.2.1 Doping with Donors

The most common n-type dopant for GaN is silicon. However, it is observed that with increasing Si concentration in GaN grown on a foreign seed, the tensile strain in deposited layers increases. It was published (see e.g. [59, 60]) that the use of Ge

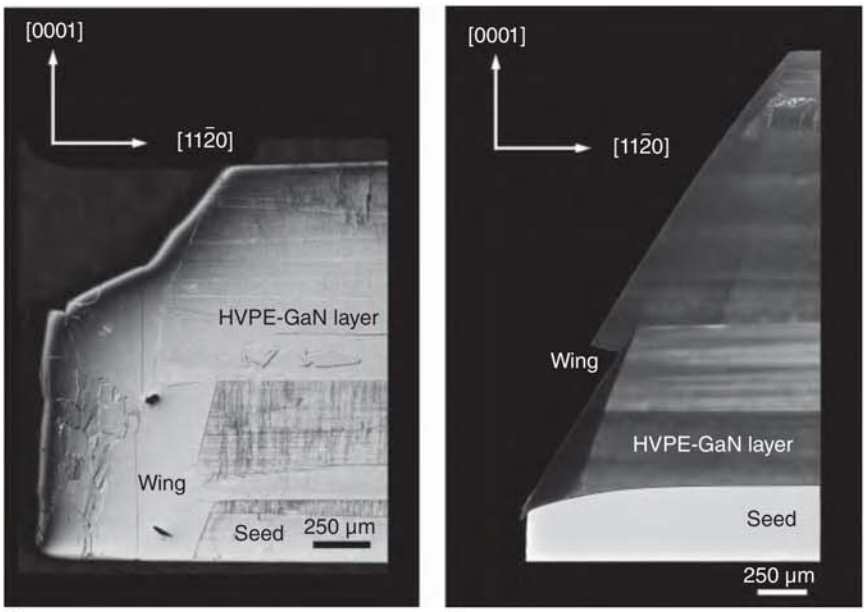

Figure 18.14 Edges of HVPE-GaN crystals grown (a) without Mo elements in the crystal growth zone; (b) with Mo elements in the crystal growth zone; reduction of the growth in the lateral directions is visible.

instead of Si as an n-type dopant can be helpful for solving this problem. The lattice distortion caused by Ge atoms substituting into Ga sites is very small due to their similar ionic radii [61]. Germanium is also a shallow donor in GaN, with an activation energy of 20 meV, which is similar to Si (17 meV) [62, 63]. Germanium can be introduced, thus, as a highly favorable n-type dopant in GaN. It leads to a smoother surface, lower film stress, and less TDD [64]. It should be noted that it was not observed in the case of GaN-on-GaN growth.

Dichlorosilane (H_2SiCl_2) was used as a precursor of Si in HVPE processes. The precursor was supplied to the gallium source zone of the HVPE reactor. Adding H_2SiCl_2 to the reactant gases caused no changes in the morphology of deposited crystals. The growth mode was governed by hillocks (see Figure 18.15a). The structural quality of the doped material was not deteriorated in comparison to the Am-GaN seed or UID HVPE-GaN. The EPD remained at the same low value. Opposite results were obtained for HVPE-GaN:Ge. In this case, the applied precursor was germanium tetrachloride ($GeCl_4$). Crystallization in hydrogen carrier gas resulted in formation of pits on the surface. A morphologically stable growth, with hillocks visible on the c-plane, was enabled by using nitrogen as the carrier gas. The significant difference in morphology of HVPE-GaN:Ge deposited in different carrier gas was explained with the use of thermodynamic calculations [65]. In hydrogen, the equilibrium partial pressure of Ge was higher than the saturated vapor pressure of Ge. This led to the formation of Ge droplets on the surface of the growing crystal and, consequently, to the formation of pits on these droplets. The pits were not observed when nitrogen

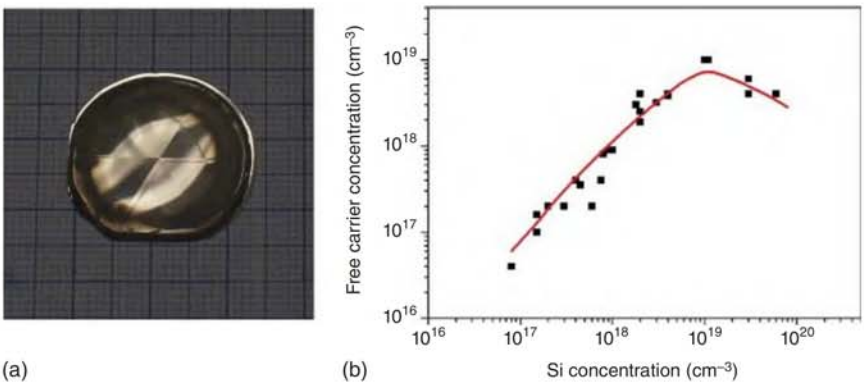

Figure 18.15 (a) Morphology of HVPE-GaN:Si; hillock growth mode; grid 1 mm; (b) free carrier concentration as a function of Si concentration in GVPE-GaN:Si; a knee of compensation is well visible.

was the carrier gas. In this case, the equilibrium partial pressure of Ge was lower than the saturated vapor pressure of Ge. Thus, germanium droplets could not be formed and disturb the crystallization run. Growth with nitrogen as the carrier gas resulted in high-quality HVPE-GaN:Ge layers. However, they were not thicker than 500 μm. When this value was exceeded, cracks appeared in the seed. The reason for this was the lattice mismatch between Am-GaN and HVPE-GaN:Ge. The a lattice parameter in HVPE-GaN:Ge was bigger that the a lattice parameter in Am-GaN. Therefore, the new-grown layer was always under compressive stress, and seed was under tensile stress. The stress force in GaN:Ge acted in an opposite direction than in the seed. Such phenomenon was never observed in the case of HVPE-GaN:Si. Herein, like in the case of UID-GaN, deterioration always started from the edges, due to the formation of wings (see Figures 18.13 and 18.14). Herein, it should be remarked that the role of wings has never been analyzed for HVPE-GaN:Ge.

The lattice parameters of GaN:Si were not strongly different from those of Am-GaN. In HVPE-GaN:Si, the free carrier concentration was on the order of $1–6 \times 10^{18}\,\mathrm{cm}^{-3}$ with mobility 300–170 $\mathrm{cm}^2/\mathrm{V\,s}$ for different Si contents in the crystals. SIMS measurements performed on the c-plane showed that the Si concentration exceeded $1 \times 10^{19}\,\mathrm{cm}^{-3}$. The free carrier concentration was 1 order of magnitude lower than that of silicon. Most probably, a large fraction of electrons from silicon was compensated by some acceptor state. A possible explanation is that gallium vacancies and their complexes with Si were responsible for this effect. Low-temperature (15 K) photoluminescence spectra measured for Si-doped samples showed that the intensity of the YL signal increased with Si content. As mentioned, the HVPE technology is carbon-free. Thus, gallium vacancies and/or their complexes could be responsible for the YL. The second fact that indicated the existence of gallium vacancies complexes was the behavior of the free carrier concentration as a function of Si incorporated in the crystals. This dependence is presented in Figure 18.15b. When more Si atoms are detected by SIMS, the free carrier concentration (determined by Raman spectroscopy) increases reaching its

maximum value and then starts to decrease. No doubt, the silicon donors were compensated by some point defects. A similar behavior was observed for AlGaN doped with Si and theoretically explained by the formation of Ga vacancies – Si complexes [66]. It is interesting that the YL has never been observed in the case of GaN:Ge crystals. Additionally, the free carrier concentration measured by different methods (Hall, capacitance–voltage, Raman) was always equal to the Ge content in GaN.

18.4.2.2 Doping with Acceptors

Methane (CH_4) was used as a carbon precursor for crystallizing HVPE-GaN:C on Am-GaN seeds. The layers were up to 1 mm thick with C concentration varying from 10^{17} to 10^{19} cm^{-3}. The morphology of the crystals was not changed; one or a few hillocks on the entire surface were always observed (see Figure 18.16a). The structural quality of the Am-GaN seeds was reflected by the layers. A dominating YL signal, much stronger than the near band edge luminescence, appeared in low-temperature PL spectra of GaN:C [67, 68]. Additionally, a small shift of the YL to higher energy (from 2.23 to 2.3 eV) was observed for highly doped (10^{19} cm^{-3}) material [68]. The crystals were highly resistive [69]. The value of resistivity at room temperature was too high to be measured, and it had to be extrapolated. HVPE-GaN:C showed p-type conductivity at high temperature. The hole concentration changed from ~10^{12} cm^{-3} at 600 K to ~10^{15} cm^{-3} at 1000 K. Hall method allowed to determine the activation energy of an acceptor level at around 1 eV [67]. This result was in good agreement with electron paramagnetic resonance (EPR) measurements [68, 70, 71]. They revealed the presence of a carbon-related defect in all samples which were photo-ionized with 1 eV light, thus, consistent with the presence of carbon at nitrogen site-C_N. These results were also in good agreement with theoretical predictions for C_N in GaN [72, 73]. An interesting experimental observation is presented in Figure 18.16b. The resistivity and hole concentration in HVPE-GaN:C are shown as a function of carbon content for a chosen temperature value (830 K). One can see that for more carbon, the resistivity increases but the hole concentration decreases. Content of other impurities remained at the same

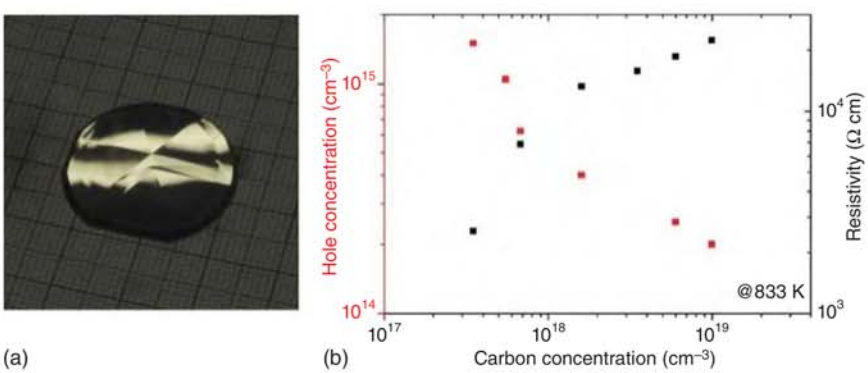

Figure 18.16 (a) Morphology of HVPE-GaN:C; (b) resistivity and hole concentration as a function of carbon concentration [C] in HVPE-GaN:C; results prove the existence of additional point defects compensating deep carbon acceptors.

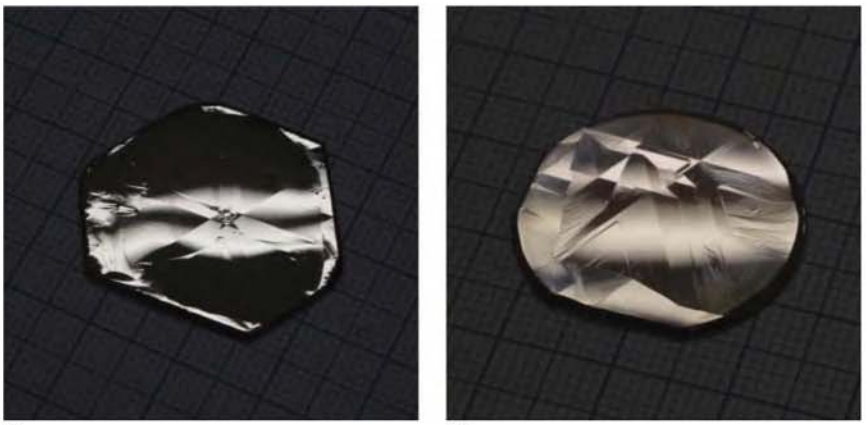

Figure 18.17 Morphologies of (a) HVPE-GaN:Fe; (b) HVPE-GaN:Mn.

level. It can be assumed that in the crystals with higher carbon doping, additional defects can be formed and they compensate the C_N deep acceptors. There are some indications that carbon is amphoteric in GaN [74]. Thus, it can also be a donor. This results in the self-compensation phenomenon in HVPE-GaN:C.

Semi-insulating HVPE-GaN can also be crystallized on native seeds by doping with iron or manganese [75, 76]. Hydrochloride was flown over solid metals used as sources for these elements. A typical morphology of HVPE-GaN:Fe and HVPE-GN:Mn is shown in Figure 18.17a,b, respectively. The high structural quality was kept (it did not differ from UID HVPE-GaN grown on a native seed) if the concentration of dopant did not exceed 10^{18} and 10^{19} cm^{-3} for Fe and Mn, respectively. Doping with Fe allowed for a decrease of free carrier (electron) concentration in GaN and increase of the resistivity. At 300 K, its value reached 10^8 Ω cm and the activation energy was 0.6 eV. All Mn-doped samples were very highly resistive at 300 K, and it was not possible to measure their resistivity. Electrical characterization was possible for temperatures higher than 550 K when the resistivity decreased to 10^8 Ω cm and the material exhibited n-type conductivity. Activation energy in the case of GaN:Mn was close to 1.8 eV. Figure 18.18 summarizes the temperature-dependent resistivity measurements for all presented above acceptor dopants. There are also data of HVPE-GaN co-doped with Mn and Mg. Magnesium was added unintentionally. The activation energy was changed and took a lower value: 1.2–1.3 eV. The GaN:Mn,Mg samples were p-type at high temperature.

18.5 Summary

Results of HVPE and basic ammonothermal GaN crystallization, performed in Poland, were presented and discussed. Both methods seem to be very perspective for obtaining bulk GaN and fabricating high-quality GaN substrates. No doubt, the ammonothermally grown GaN crystals demonstrate perfect structural quality. It can be transferred to HVPE-GaN when Am-GaN seeds are used for vapor phase crystallization. Both methods allow to obtain n-type and semi-insulating crystals.

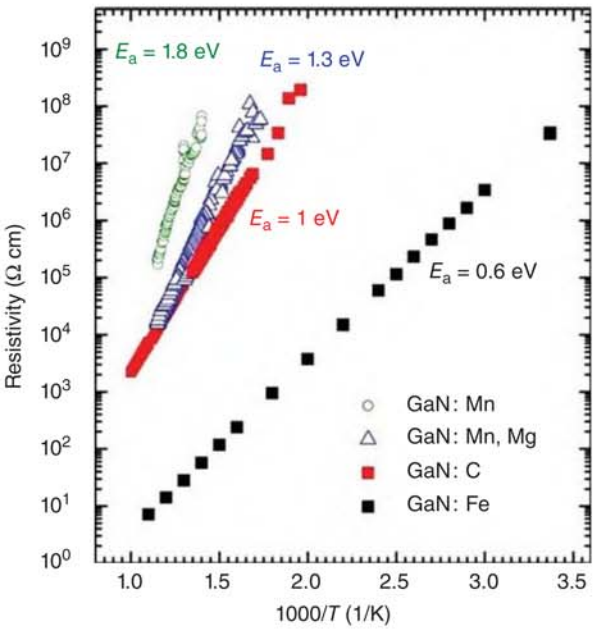

Figure 18.18 Resistivity as a function of inverse of temperature for HVPE-GaN:Mn, HVPE-GaN:Mn,Mg, HVPE-GaN:C, and HVPE-GaN:Fe; values of determined activation energies are shown.

Time will show which material is more beneficial for making GaN substrates for specific applications. Since the future will belong to GaN-on-GaN technology, crystallization of this nitride becomes a crucial problem for further development of high-power high-frequency electronic as well as optoelectronic devices. Bulk GaN crystals are needed. The main goal is to design a process that will overcome the equilibrium crystal shape in GaN growth. This will allow to demonstrate true bulk GaN, eventually yielding several 10 of wafers per boule. Both described crystal growth technologies are, today, ready for this breakthrough achievement.

Acknowledgments

This research was supported by the Department of the Navy, Office of Naval Research (ONRG-NICOP-N62909-17-12004), by the Polish National Science Center through projects No. 2017/25/B/ST5/02897 and 2018/29/B/ST5/00338, as well as by TEAM TECH program of the Foundation for Polish Science co-financed by the European Union under the European Regional Development Fund (POIR.04.04.00-00-5CEB/17-00).

References

1 Utsumi, W., Saitoh, H., Kaneko, H. et al. (2003). *Nat. Mater.* 2: 735.
2 Porowski, S., Sadovyi, B., Gierlotka, S. et al. (2015). *J. Phys. Chem. Solids* 85: 138–143.
3 Porowski, S., Sadovyi, B., Karbovnyk, I. et al. (2019). *J. Cryst. Growth* 505: 5–9.
4 Nakamura, D. and Kimura, T. (2018). *Appl. Phys Express* 11: 065502.

5 Kimura, T., Horibuchi, K., Kataoka, K., and Nakamura, D. (2018). *J. Cryst. Growth* 494: 17–25.
6 Lukin, G., Schneider, T., Barchuk, M. et al. (2017). *Phys. Status Solidi A* 214 (9): 1600753.
7 Takino, J., Sumi, T., Okayama, Y. et al. (2019). *Jpn. J. Appl. Phys.* 58: SC1043.
8 Mikawa, Y., Ishinabe, T., Kawabata, S. et al. (2015). *Proc. SPIE* 9363: 936302.
9 Tsukada, Y., Enatsu, Y., Kubo, S. et al. (2016). *Jpn. J. Appl. Phys.* 55: 05Fc18.
10 Hashimoto, T., Letts, E.R., Key, D., and Jordan, B. (2019). *Jpn. J. Appl. Phys.* 58: SC1005.
11 Ehrentraut, D. and Bockowski, M. (2015). *Handbook of Crystal Growth Second Edition: Bulk Crystal Growth: Basic Techniques, and Growth Mechanisms and Dynamics* (ed. P. Rudolph), 577–619. Elsevier.
12 Mori, Y., Imade, M., Maruyama, M. et al. (2015). *Handbook of Crystal Growth Second Edition: Bulk Crystal Growth: Basic Techniques, and Growth Mechanisms and Dynamics* (ed. P. Rudolph), 505–533. Elsevier.
13 Imanishi, M., Murakami, K., Yamada, T. et al. (2019). *Appl. Phys Express* 12: 045508.
14 Koukitu, A. and Kumagai, Y. (2010). *Technology of Gallium Nitride Crystal Growth* (eds. D. Ehrentraut, E. Meissner and M. Bockowski), 31. Heidelberg: Springer-Verlag.
15 Tomida, D., Bao, Q., Saito, M. et al. (2018). *Appl. Phys Express* 11 (9) 1002.
16 Okada, N., Ishikawa, A., Yamane, K. et al. (2014). *Phys. Status Solidi A* 211 (4): 736–739.
17 Pimputkar, S., Kawabata, S., Speck, J.S., and Nakamura, S. (2014). *J. Cryst. Growth* 403: 7.
18 Maruska, H.P. and Tietjen, J.J. *Appl. Phys. Lett.* 15 (10): 327.
19 Maruska, H.P. and Rhines, W.C. (2015). *Solid State Electron.* 111: 32–41.
20 Fujikura, H., Konno, T., Yoshida, T., and Horikiri, F. (2017). *Jpn. J. Appl. Phys.* 56: 085503.
21 Yoshida, T., Oshima, Y., Watanabe, K. et al. (2011). *Phys. Status Solidi C* 8 (7–8): 2110–2112.
22 Kumagai, Y., Koukitu, A., and Seki, H. (2000). *Jpn. J. Appl. Phys.* 39: L149–L151.
23 Motoki, K. (2010). *SEI Tech. Rev.* 70: 28.
24 Motoki, K., Okahisa, T., Nakahata, S. et al. (2002). *J. Cryst. Growth* 237: 912.
25 Motoki, K., Okahisa, T., Hirota, R. et al. (2007). *J. Cryst. Growth* 305: 377.
26 Oshima, Y., Eri, T., Shibata, M. et al. (2003). *Jpn. J. Appl. Phys.* 42: L1.
27 Usui, A., Ichihashi, T., Kobayashi, K. et al. (2002). *Phys. Status Solidi A* 194 (2): 572–575.
28 Oshima, Y., Yoshida, T., Eri, T. et al. (2010). *Technology of Gallium Nitride Crystal Growth* (eds. D. Ehrentraut, E. Meissner and M. Bockowski), 79. Heidelberg: Springer-Verlag.
29 Geng, H., Sunakawa, H., Sumi, N. et al. (2012). *J. Cryst. Growth* 350 (1): 44–49.
30 Fujito, K., Kubo, S., Nagaoka, H. et al. (2009). *J. Cryst. Growth* 311 (10): 3011.
31 Oshima, Y., Yoshida, T., Eri, T. et al. (2007). *Phys. Status Solidi C* 4 (7): 2215–2218. https://doi.org/10.1002/pssc.200674719.

32 Oshima, Y., Yoshida, T., Watanabe, K. et al. (2010). *J. Cryst. Growth* 312: 3569–3573.
33 Richter, E., Gridneva, E., Weyers, M., and Traenkle, G. (2016). *J. Cryst. Growth* 456: 97–100.
34 Ke, X., Jian-Feng, W., and Guo-Qiang, R. (2015). *Chin. Phys. B* 24 (6): 066105.
35 Byrappa, K. (2005). *Bulk Crystal Growth of Electronic, Optical and Optoelectronic Materials* (ed. P. Capper), 387–406. Wiley.
36 Wang, B. and Callahan, M.J. (2006). *Cryst. Growth Des.* 6 (6): 1227–1246.
37 Bao, Q., Hashimoto, T., Sato, F. et al. (2013). *CrystEngComm* 15: 5382–5386.
38 Ehrentraut, D. and Kagamitani, Y. (2010). *Technology of Gallium Nitride Crystal Growth* (eds. D. Ehrentraut, E. Meissner and M. Bockowski), 183–202. Heidelberg: Springer-Verlag.
39 Grzegory, I. (2001). *J. Phys. Condens. Matter* 13: 6875–6892.
40 Dwilinski, R., Doradzinski, R., Garczynski, J. et al. (2008). *J. Cryst. Growth* 310: 3911.
41 Doradziński, R., Dwiliński, R., Garczyński, J. et al. (2010). *Technology of Gallium Nitride Crystal Growth* (eds. D. Ehrentraut, E. Meissner and M. Bockowski), 137–158. Heidelberg: Springer-Verlag.
42 Zajac, M., Kucharski, R., Grabianska, K. et al. (2018). *Prog. Cryst. Growth Charact. Mater.* 64 (3): 63–74.
43 Horibuchi, K., Yamaguchi, S., Kimoto, Y. et al. (2016). *Semicond. Sci. Technol.* 31: 034002.
44 Tuomisto, F., Maki, J.-M., and Zajac, M. (2010). *J. Cryst. Growth* 312: 2620–2623.
45 Tuomisto, F., Kuittinen, T., Zajac, M. et al. (2014). *J. Cryst. Growth* 403: 114.
46 Sochacki, T., Amilusik, M., Lucznik, B. et al. (2013). *Proc. SPIE* 8625: 86250B-1.
47 Sochacki, T., Bryan, Z., Amilusik, M. et al. (2013). *Appl. Phys Express* 6: 075504.
48 Sochacki, T., Amilusik, M., Fijalkowski, M. et al. (2014). *J. Cryst. Growth* 407: 52.
49 Bockowski, M., Iwinska, M., Amilusik, M. et al. (2016). *Semicond. Sci. Technol.* 31: 093002.
50 Kirste, L., Danilewsky, A.N., Sochacki, T. et al. (2015). *ECS J. Solid State Sci. Technol.* 4 (8): P324–P330.
51 Kirste, L., Danilewsky, A.N., Sochacki, T. et al. (2015). *ECS Trans.* 66 (1): 93–106.
52 Sochacki, T., Amilusik, M., Fijalkowski, M. et al. (2015). *Phys. Status Solidi B* 252 (5): 1172.
53 Freitas, J.A. Jr., Culbertson, J.C., Mahadik, N.A. et al. (2015). *Cryst. Growth Des.* 15: 4837.
54 Freitas, J.A. Jr., Culbertson, J.C., Mahadik, N.A. et al. (2016). *J. Cryst. Growth* 456: 113.
55 Krysko, M., Sarzynski, M., Domagala, J. et al. (2005). *J. Alloys Compd.* 401: 261.
56 Domagala, J.Z., Smalc-Koziorowska, J., Iwinska, M. et al. (2016). *J. Cryst. Growth* 456: 80–85.
57 Lucznik, B., Iwinska, M., Sochacki, T. et al. (2016). *J. Cryst. Growth* 456: 86–90.
58 Amilusik, M., Wlodarczyk, D., Suchocki, A., and Bockowski, M. (2019). *Jpn. J. Appl. Phys.* 58: SCCB32.
59 Gu, H., Hu, C., Wang, J. et al. (2019). *J. Alloys Compd.* 780: 476–481.

60 Nenstiel, C., Bügler, M., Callsen, G. et al. (2015). *Phys. Status Solidi RRL* 9: 716–721.

61 Ueno, K., Arakawa, Y., Kobayashi, A. et al. (2017). *Appl. Phys Express* 10: 101002.

62 Gotz, W., Johnson, N.M., Chen, C. et al. (1996). *Appl. Phys. Lett.* 68: 3144–3146.

63 Gotz, W., Kern, R.S., Chen, C.H. et al. (1999). *Mater. Sci. Eng., B* 59: 211–217.

64 Ajay, A., Lim, C.B., Browne, D.A. et al. (2017). *Nanotechnology* 28: 405204.

65 Iwinska, M., Takekawa, N., Ivanov, V.Y. et al. (2017). *J. Cryst. Growth* 480: 102–107.

66 Harris, J.S., Baker, J.N., Gaddy, B.E. et al. (2018). *Appl. Phys. Lett.* 112: 152101.

67 Iwinska, M., Piotrzkowski, R., Litwin-Staszewska, E. et al. (2017). *Appl. Phys Express* 10: 011003.

68 Zvanut, M.E., Paudel, S., Glaser, E.R. et al. (2019). *J. Electron. Mater.* 48 (4): 2226–2232.

69 Bockowski, M., Iwinska, M., Amilusik, M. et al. (2018). *J. Cryst. Growth* 499: 1.

70 Willoughby, W.R., Zvanut, M.E., Paudel, S. et al. (2017). *J. Appl. Phys.* 123: 161547.

71 Zvanut, M.E., Paudel, S., Sunay, U.R. et al. (2018). *J. Appl. Phys.* 124: 075701.

72 Lyons, J.L., Janotti, A., and Van de Walle, C.G. (2010). *Appl. Phys. Lett.* 97: 152108.

73 Lyons, J.L., Janotti, A., and Van de Walle, C.G. (2014). *Phys. Rev. B* 89: 035204.

74 Deák, P., Lorke, M., Aradi, B., and Frauenheim, T. (2019). *Phys. Rev. B* 99: 085206.

75 Iwinska, M., Piotrzkowski, R., Litwin-Staszewska, E. et al. (2017). *J. Cryst. Growth* 475: 121–126.

76 Iwinska, M., Zajac, M., Lucznik, B. et al. (2019). *Jpn. J. Appl. Phys.* 58: SC1047.

77 Amilusik, M., Sochacki, T., Fijalkowski, M. et al. (2019). *Jpn. J. Appl. Phys.* 58: SC1030.

78 Amilusik, M., Sochacki, T., Lucznik, B. et al. (2014). *J. Cryst. Growth* 403: 48.

19

GaN on Si: Epitaxy and Devices

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19.1 Introduction

The history of GaN research fights against GaN crystal growth. Thanks to the pioneers' technical breakthroughs, GaN optoelectric devices such as light-emitting diodes (LEDs) have been bringing great benefits in our life as in lighting bulb, backlight of smartphones, and thin flat panel displays [1–8].

In addition to the GaN optoelectronic devices, GaN-based materials are very attractive for various electron devices taking advantages of its excellent electron transport properties such as high breakdown field, high thermal conductivity, and high carrier saturation velocity. AlGaN/GaN heterojunction generates two-dimensional electron gas (2DEG) at the interface induced by spontaneous and piezoelectric polarization effects without any intentional impurity doping. The 2DEG has high sheet-carrier density around $10^{13}\,\mathrm{cm}^{-2}$ and high mobility of 1200–2000 $\mathrm{cm}^2/\mathrm{V\,s}$, enabling extremely low on-state resistance (R_{on}) and gate charge (Q_{g}). The figure of merit $R_{\mathrm{on}}Q_{\mathrm{g}}$ for low conduction and low switching losses can be smaller than one to the tenth of that by conventional Si-based power devices, improving conversion efficiencies of power electronics systems. Converters and inverters with the efficiencies over 99% have been already demonstrated with the GaN devices, and some of them have been commercially available on the market such as power supplies and chargers for smartphones. These notable progresses of GaN power devices and converters have been led by significant progresses of GaN crystal growth especially on hetero-material substrates due to the lack of native GaN bulk substrates for a long time.

This chapter describes entire technology related to GaN power devices; GaN epitaxial growth, technical approaches of GaN lateral devices, device semiconductor processing, practical power applications, and device integrations utilizing advantages of GaN lateral devices.

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

19.2 GaN Epitaxy on Si Substrate

19.2.1 GaN Epitaxial Method and Doping

19.2.1.1 Metal–Organic Chemical Vapor Deposition (MOCVD)

For III-N epitaxial growth, both metal–organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) have been standard methods. So far, MOCVD has been mostly used for GaN-based optoelectric and electron devices and utilizes metalorganic precursors for group-III elements (Ga, Al, and In) and nitrogen precursor, typically ammonia (NH_3), which are transported with H_2, N_2, or those mixed gas as carrier gas into a growth chamber. The metal–organic precursors are trimethylgallium (TMG), trimethylaluminium (TMA), and trimethylindium (TMI) for gallium, aluminum, and indium elements, where they react with NH_3 on the surface of a substrate for formations of GaN, AlN, and InN as described by following chemical equations.

- $Ga(CH_3)_3 + NH_3 \rightarrow GaN + 3CH_4$
- $Al(CH_3)_3 + NH_3 \rightarrow AlN + 3CH_4$
- $In(CH_3)_3 + NH_3 \rightarrow InN + 3CH_4$

$Al_xIn_yGa_{1-x-y}N$ ternary or quaternary crystal (x, y, and $x+y$ are between 0 and 1) can be grown by adjusting the ratio of TMG, TMA, and TMI for the desired material composition. Practically, there is some composite limitation especially for high indium-composition AlInGaN due to material phase separation. The AlInGaN material system has a direct band gap from 0.7 eV (InN) to 6.2 eV (AlN) for any material composition. Typical growth temperature for GaN and AlN is 1000–1200 °C [3, 9] and that for Indium contained compounds such as InGaN can be lower around 700 °C [10]. The crystal growth on heterogeneous substrate such as sapphire requires low-temperature grown layer usually used as nucleation layer [3, 4]. The growth pressure in the growth chamber is lower than 760 Torr in order to avoid gas-phase pre-reaction at the upstream of the growth chamber

19.2.1.2 N, P-Type Doping

In general, n-type doping into III-N layers is achieved to replace the group III elements (Ga, Al, and In) with group IV elements, typically silicon, by using silane as a doping gas added in the gas source. Silicon acts as a shallow donor in the III-N layer, achieving high electron density of 10^{19} cm^{-3} [11, 12]. For p-type doping, magnesium (Mg) is the most common dopant provided from the metal–organic precursor of cyclopentadienyl magnesium $(C_5H_5)_2Mg$ replacing the group III elements. During the MOCVD growth of p-type GaN, Mg is inactivated by hydrogen of the carrier gas which can be eliminated during post-annealing process in nitrogen gas at 700–800 °C [6]. The acceptor level of magnesium in GaN is relatively high around 110–160 meV [13], so that the resultant hole density in p-GaN is limited around 10^{17} cm^{-3} at room temperature regardless of high Mg concentration of 10^{19}–10^{20} cm^{-3} [14]. The higher Mg doping over 10^{20} cm^{-3} results in decrease of hole density due to the formation of Mg cluster or inversion domain of crystal polarity [15, 16].

19.2.1.3 Doping for Semi-insulation Layer

In lateral GaN power devices, semi-insulation (SI) layers act as an important role of highly resistive buffer layer to achieve high breakdown voltage and low leakage current, which are introduced under the active layer of AlGaN/GaN. In general, the highly insulated semiconductor layer can be obtained by purifying the semiconductor layer without any intentional doping. However, in the MOCVD process, residual impurities, typically oxygen and carbon, exist in the growth chamber, originating from the metal–organic precursors, carrier gases, and air leakage. The oxygen impurity acts as shallow donor locating the group III sites [17, 18], while the carbon impurity mainly occupies N sites as a deep acceptor with the activation energy of 0.9 eV in GaN [19]. In addition to the residual impurities, the atomic vacancies of the group III elements and that of nitrogen also affect the conductivity, where the vacancies of the group III elements and that of nitrogen can be a deep acceptor and a shallow donor, respectively [20, 21]. Therefore, the unintentional doping of GaN can bring about unstable conductivity control. Thus, doping of carbon or iron (Fe) is used for the growth of the semi-insulated layers compensating residual carriers in GaN. The concentration of carbon contained in the group III precursor can be controlled to be 10^{16}–10^{19} cm^{-3} by adjusting growth parameters such as growth rate, V/III ratio, growth temperature, and pressure [22]. Fe can be doped in GaN by using ferrocene ($Fe(C_5H_5)_2$) as a precursor and can generate plural electrical states in the energy midgap of GaN which traps the residual carriers [23]. Memory effect of Fe doping, in which the Fe doping profile has a tail even to upcoming grow layers, has to be taken into account [24].

19.2.2 Substrates for GaN Epitaxy

In general, the III-N epitaxial layers have been fabricated on hetero-material substrates such as sapphire, SiC, and Si by using hetero-epitaxial growth because of the difficulty to obtain large-diameter GaN bulk substrates. Table 19.1 summarizes material characteristics of the substrates for the III-N epitaxial growth. The choice of the substrate significantly affects the quality of III-N epitaxial layers, device structures (lateral or vertical), those performance, and cost depending on related applications. GaN substrates enable to fabricate vertical GaN power devices as same as Si- and SiC-based vertical power devices, while a Si and a SiC can be used to fabricate the lateral GaN power devices taking advantage of superior electrical characteristics of the AlGaN/GaN hetero structure. The detailed features of each substrate are described below.

19.2.2.1 GaN

The GaN substrate is an ideal substrate due to the perfect matching of mechanical characteristics with the GaN epitaxial layers. However, GaN does not melt at ambient pressure due to its quite high vapor pressure as high as 6 GPa [25], and GaN has been difficult to be applied conventional melt-based crystal growth used for Si, GaAs, and InP such as Czochralski method and Bridgman method. Therefore, as of today, commercially available GaN substrates are mainly prepared by using hydride vapor

Table 19.1 Material properties of substrates for GaN epitaxy.

	Sapphire (α-Al_2O_3)	6H-SiC	Si	GaN
Crystal structure	Hexagonal	Hexagonal	Diamond	Wurtzite
Lattice mismatch (%)	16	3.1	17	—
Linear thermal expansion coefficient (TEC)				
($\times 10^{-6}$ K^{-1})	7.5	4.4	2.6	5.6
CTE mismatch				
(%)	−26	25	56	—
Thermal conductivity				
(mW/cm/K)	25	230–490	150	210
Energy gap				
(eV)	9.9	3.03	1.12	3.4
Substrate diameter				
(mm)	150	150	400	50–100
Substrate relative cost	Low	High	Very low	Very high

phase epitaxy (HVPE) with low dislocation density of 10^4 cm^{-2} [26], but the available diameter is limited up to 4 in. Recently, GaN power devices on the GaN substrate are reported with superior performances to those on heterogeneous substrates such as Si [27]. For a review on bulk growth of GaN, please see Chapter 18.

19.2.2.2 Sapphire

Historically, the initial technical breakthroughs of GaN epitaxial growth were achieved on sapphire substrates in 1980s through 1990s in order to overcome technical challenges of the large mismatches of the lattice constant (16%) and thermal expansion between GaN(0001) and c-plane sapphire due to the absence of GaN bulk substrate on those days [3, 4]. After that, GaN optoelectric devices such as green, blue, and white LEDs are main drivers for the sapphire substrate taking advantage of its transparency for wide-range wavelength up to ultraviolet, and the technical approaches of GaN crystal growth on sapphire have been also applied to fabricate GaN high electron mobility transistors (HEMTs) on sapphire of which diameter is up to 4–6 in. Although the sapphire substrate got an interest at the early stage of GaN HEMT development, the low thermal conductivity of sapphire has limited to extract the full potential of the extremely high power density of GaN HFETs. Therefore, the recent interest for the substrate has shifted to the cost-effective Si for wide-range applications and highly thermal-conductive SiC for high-frequency and military applications.

19.2.2.3 SiC

Since SiC substrates have superior thermal conductivity of around 300 W/mK as high as that of Cupper and are available to obtain the semi-insulation (SI)

characteristic, GaN HEMTs on SI-SiC have been widely used for high-frequency applications with high power density, high efficiency, and high operating temperature which cannot be achieved by GaAs-based HEMT devices [28, 29]. 6H-SiC is a suitable polytype of SiC for GaN epitaxial growth due to the closer mechanical properties to GaN, which differs from 4H-SiC mainly used for the fabrication of SiC vertical power devices. Although the mechanical characteristics of 6H-SiC are relatively close to those of GaN, the price of the 6H-SiC substrate has been still more expensive than sapphire and Si. Furthermore, the number of SiC-substrate suppliers has been quite limited now.

19.2.2.4 Si

Si is one of the most abundant materials on the earth, and the Si substrates are commercially available with the large diameter of up to 12 in. and various resistivities thanks to matured technologies for bulk crystal growth and wafer production. The GaN-on-Si technology is very promising to reduce the cost of GaN HFETs so as to widely spread for commercial use. Si has a good thermal conductivity as high as GaN, but which is lower than that of SiC. In addition to the substrate features, the advantage of GaN-on-Si technology is to utilize well-established Si complementary metal-oxide-semiconductor (CMOS) processes such as metallization, via-hole formation, and wafer grinding. This is the background that GaN-on-Si has been researched extensively regardless of its material challenges such as large mismatch of lattice constant and thermal expansion coefficient (TEC) between GaN and Si. So far, several technical approaches have been introduced to overcome challenges originated from these mismatches and achieved high-quality epitaxial layers with less wafer curvature which can be acceptable for processing equipment.

19.2.3 Epitaxial Growth Technology on Si Substrate

19.2.3.1 Crystal Orientation of Si Substrate

Typically, Si(111) is used for the growth of wurtzite GaN(0001), which is the most stable crystal structure of GaN. The epitaxial technologies to manage mechanical stress in GaN on Si is a key technology to suppress wafer curvature and cracks originated from the large mismatches of the lattice constant and the coefficient of thermal expansion (CTE) between Si(111) and GaN(0001). As shown in Figure 19.1, the GaN epitaxial layers on Si consist of the following parts: (i) nucleation layer to initiate the epitaxial growth on the heterogeneous substrate of Si, (ii) buffer layer to manage the internal stress to obtain a thick epitaxial layer for higher breakdown voltage, and (iii) active layer for the lateral electrical channel with the 2DEG. Each part is described in detail below.

19.2.3.2 Nucleation Layer

The past approaches to grow GaN directly onto Si resulted in insufficient crystal quality with three-dimensional GaN growth for the device fabrication. During the crystal growth, Ga species can easily diffuse into the Si substrate and roughen the surface of Si substrate, which is so-called Ga melt-back [30]. AlN is introduced as a

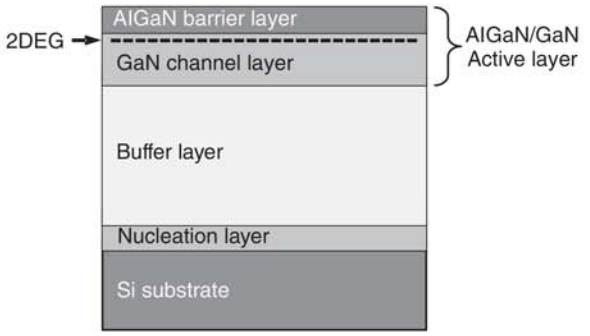


Figure 19.1 Epitaxial structure of GaN on Si substrate.

nucleation layer for GaN on Si to solve the Ga melt-back [31]. Aluminum reacts with nitrogen actively and has low diffusion velocity of the adatom on Si substrates. In result, lots of AlN nucleation occur simultaneously and coalesce each other including large amount of small AlN islands. Even though the initial AlN layer includes high-density dislocations of $10^{10}\,cm^{-2}$, the AlN initial layer can transfer the crystal orientation to upcoming grown layers. The thickness of AlN layer is typically 20–200 nm. AlN/Si material system has been researched actively in the crystallographic and electrical points of view, since the characteristics of the AlN initial layer can affect the crystal quality of GaN on Si in total [32].

19.2.3.3 Buffer Layer

The buffer layer is grown on the AlN nucleation layer in order to manage the mechanical stress to obtain the thick epitaxial layer for higher breakdown voltages. For 600-V rating devices, 3–5 μm thick epitaxial layers have been used for GaN on Si. During cooling-down process after the crystal growth, the GaN layer shrinks more than the Si substrate due to the larger CTE mismatch of 54% between GaN and Si, inducing high tensile stress in the GaN layer to lead cracks in GaN layer, wafer bowing, and break at the worst case. The magnitude of the tensile stress increases in proportion to the thickness of the epitaxial layers. The essential technology is to design the structure of the buffer layers to introduce compressive stress to cancel the tensile stress originated from the CTE mismatch between GaN and Si. So far, several buffer layers have been reported as shown in Figure 19.2. The step-graded AlGaN layers consist of several AlGaN layers with different Al compositions, starting from the first AlGaN layer on the AlN nucleation layer. The second AlGaN layer is grown on the first AlGaN layer, having lower Al composition than that of the first one to have larger lattice constant for the compressive stress [33]. Repeating the same way to reduce Al composition even more to be finally GaN, the next graded AlGaN and GaN layers can generate the compressive stress as well. Instead of the step-graded approach, the AlGaN buffer layer with continuously reduced Al composition is also reported [34]. The AlN/GaN superlattice structure, in which thin GaN and AlN layers are repeatedly grown with several tens of GaN/AlN layers, is practically demonstrated to obtain thick buffer layer [35]. The stress management by using low-temperature AlN interlayers between thick GaN layers is also reported [36]. Semi-insulated buffer layers doped with C or Fe can be used to achieve higher

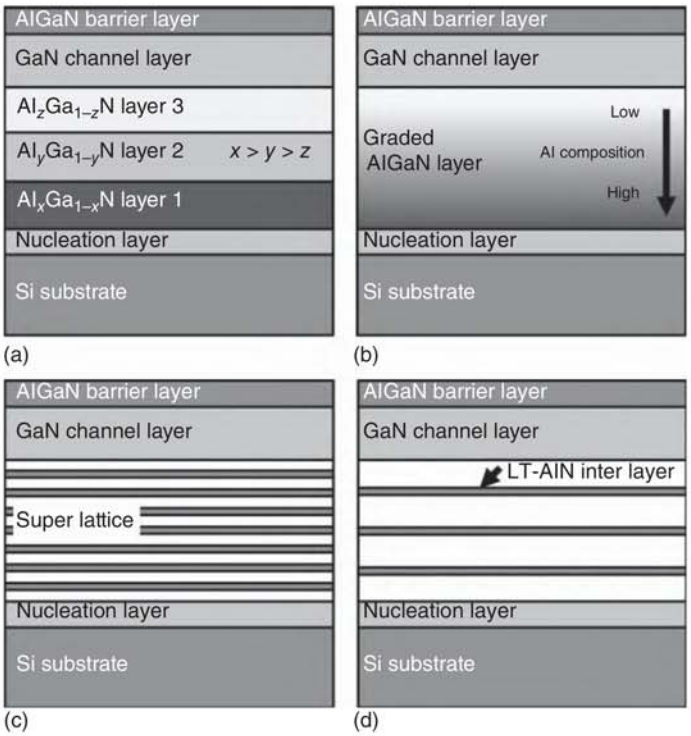


Figure 19.2 Structures of buffer layers for GaN on Si substrate. (a) Step-graded AlGaN, (b) graded AlGaN, (c) superlattice, and (d) low temperature AlN interlayers.

breakdown voltage and lower leakage current [37, 38]. A drawback of C and Fe doping into the buffer layer is carrier trapping by C- and Fe-related electrical states, where trapped electron acts as negative charge and lifts up the electrical potential in the vicinity of the 2DEG, reducing drain current of the GaN HFET [39, 40]. Therefore, the C- or Fe-doped layer is recommended to have certain distance from the AlGaN/GaN active layer.

19.2.3.4 AlGaN/GaN Active Layer with Polarization Effect

Wurtzite-type GaN, AlN, and InN have a hexagonal crystal structure, where the axis direction of the hexagonal column is called as *c*-axis. Wurtzite-type GaN has different faces perpendicular to *c*-axis which are Ga-face and N-face leading to different electrical characteristics. The Ga-faces is usually obtained by MOCVD, while the N-face can be grown by MBE. Since nitrogen has higher electronegativity than gallium, Ga and N atoms act as anion (+) and cation (−), respectively, causing electrical polarization. In the wurtzite crystal structure, the electrical polarization called as spontaneous polarization occurs along the *c*-axis, of which values are 0.081, 0.029, and 0.032 C/m^2 for AlN, GaN, and InN, respectively. In addition to the spontaneous polarization, internal mechanical stress between epitaxial layers with difference lattice constants generates piezo electric polarization. In wurtzite crystal structure as shown in Figure 19.3, the composition of polarization vectors $P_1 + P_2 + P_3 + P_4$

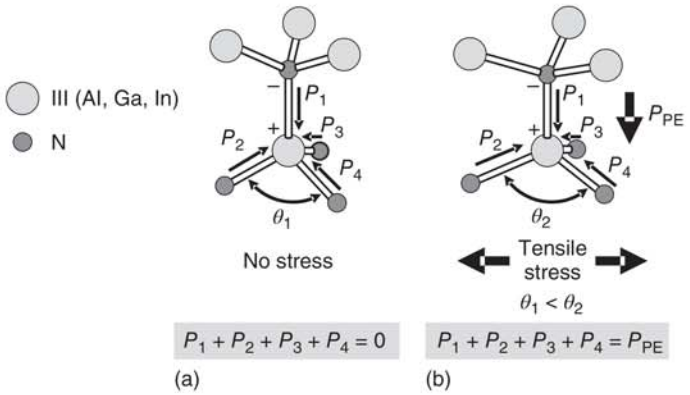


Figure 19.3 Polarization vectors of III-N semiconductor in the tetrahedron shape. The balanced polarization (a) and the unbalanced one with the piezoelectric polarization (b). (a) No stress and (b) tensile stress.

becomes zero because of crystal symmetry. However, mechanical stress due to the lattice mismatch between the epitaxial layers deforms the crystal symmetry and the balance of the composition vector. Thus, the piezo polarization P_{PE} appears as $P_{PE} = P_1 + P_2 + P_3 + P_4$. The detailed theoretical investigation on the piezoelectric polarization was done by Ambacher et al. [41].

Figure 19.4 shows charge distribution and band diagram of AlGaN/GaN hetero structure. Free carriers are generated at AlGaN/GaN interface to neutralize charges induced by the spontaneous and piezoelectric polarizations. In general, although semiconductor requires impurity doping to generate free carriers, the AlGaN/GaN material system can obtain high-density and high mobility 2DEG without any intentional impurity doping. Typically, AlGaN layer with the thickness of 20 nm, Al composition of 25% can yield the 2DEG density of $1 \times 10^{19}\,\mathrm{cm}^{-2}$, of which mobility can reach around $2000\,\mathrm{cm}^2/\mathrm{V\,s}$ depending on the smoothness at the AlGaN/GaN interface and the crystal quality of the epitaxial layers. Thanks to the superior electrical characteristics of AlGaN/GaN with any intentional doping, GaN power devices can achieve high current, low on-state resistance, and high breakdown voltage. The 2DEG density can be increased by increasing either the thickness or the Al composition of the AlGaN barrier. However, the critical thickness of the compressed AlGaN barrier can limit the 2DEG density. There are several approaches for higher 2DEG density taking the other barrier layers. The introduction of a thin AlN interlayer between the AlGaN barrier and GaN channel layers can increase both the 2DEG density and mobility [42]. The AlN layer has larger polarization than the AlGaN and can suppress alloy scattering of the 2DEG caused by the AlGaN alloy at the AlGaN/GaN interface. The thickness of the AlN interlayer is limited up to 2 nm due to the large lattice mismatch between AlN and GaN. The other approaches for barrier layers are to utilize highly Al-composition InAlN or InAlGaN replaced Ga with In to increase Al composition keeping lattice constants as long as AlGaN, which can have the lattice-matched growth on GaN as $In_{0.18}Al_{0.82}N$/GaN which generates quite

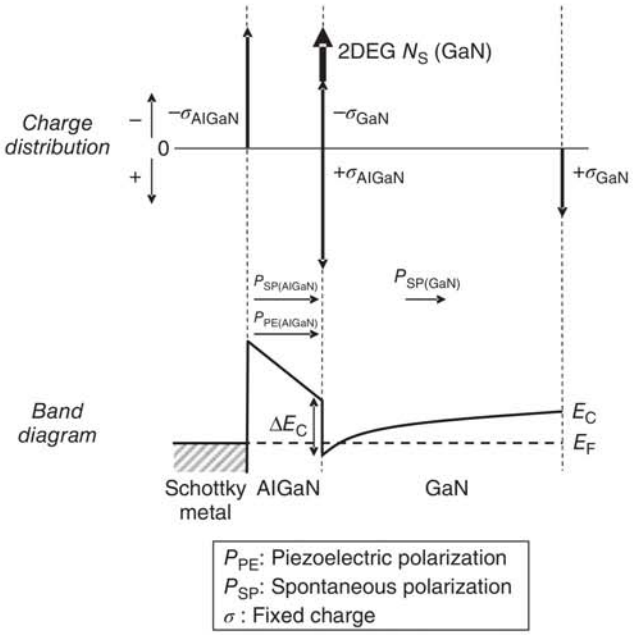


Figure 19.4 Charge distribution and band diagram of AlGaN/GaN structure.

high-density 2DEG of around 2×10^{19} cm^{-2} induced by high spontaneous polarization of Al [43, 44].

In addition to the top barrier layers on the GaN channel layer, a back barrier layer under the GaN channel layer can be used as AlGaN/GaN/AlGaN double hetero structure to improve the carrier confinement into the GaN channel layer to improve pinch-off characteristics especially for short gate devices, preventing so-called "short channel effect" [45]. In addition to the band offset at the lower GaN/AlGaN interface, polarization-induced negative charge can lift up the potential around the AlGaN back barrier layer which helps suppress carrier transport via the AlGaN back barrier layer as leakage current.

There is another approach to cover the AlGaN/GaN top barrier layer with GaN, InGaN, and InAlGaN capping layers for several purposes. First, the GaN cap layer can improve surface ununiformity of the sensitive AlGaN top barrier to avoid "current collapse" caused by carrier trapping of surface states [46]. Second, the InGaN cap layers on the AlGaN barrier layer generate negative polarization-induced charge at the interface between the cap layer and the AlGaN top barrier, which increase the effective Schottky barrier height resulting in the reduction of reverse leakage current and normally-off operation [47]. Third, n-type layers such as n-type AlGaN/GaN super lattice [48] and n-type InAlGaN cap layers [49] can decrease the ohmic contact resistance due to lower barrier height against the electrodes.

In addition to above III-N cap layers, surface passivation by in situ SiN thin layer can be grown with MOCVD continuously after III-N growth. The in situ SiN has a

crystalline structure [50] which increases 2DEG density and suppresses the current collapse by neutralizing surface states on the AlGaN top barrier layer [51].

19.3 Lateral GaN Devices on Si Substrate

19.3.1 Device Structure and Fabrication Process

As shown in Figure 19.5, GaN HFETs with 2DEG have a lateral structure. The device processing of GaN HFETs is similar to that of GaAs HEMTs which consists of (i) metallization of ohmic contact for source and drain, (ii) that of Schottky contact for gate, (iii) electrical isolation, (iv) device passivation, (v) metal plating, and (vi) final device passivation.

The ohmic contact for GaN HFET is Ti/Al-based material system which requires high-temperature post annealing typically around 800 °C for 30 seconds in nitrogen ambient to reduce ohmic contact resistance down to $10^{-6}\,\Omega/cm^2$ [52]. For further reduction of contact resistance, selective Si ion implantation into source and drain regions is used to fabricate n^+-type region. Although post-implant high-temperature

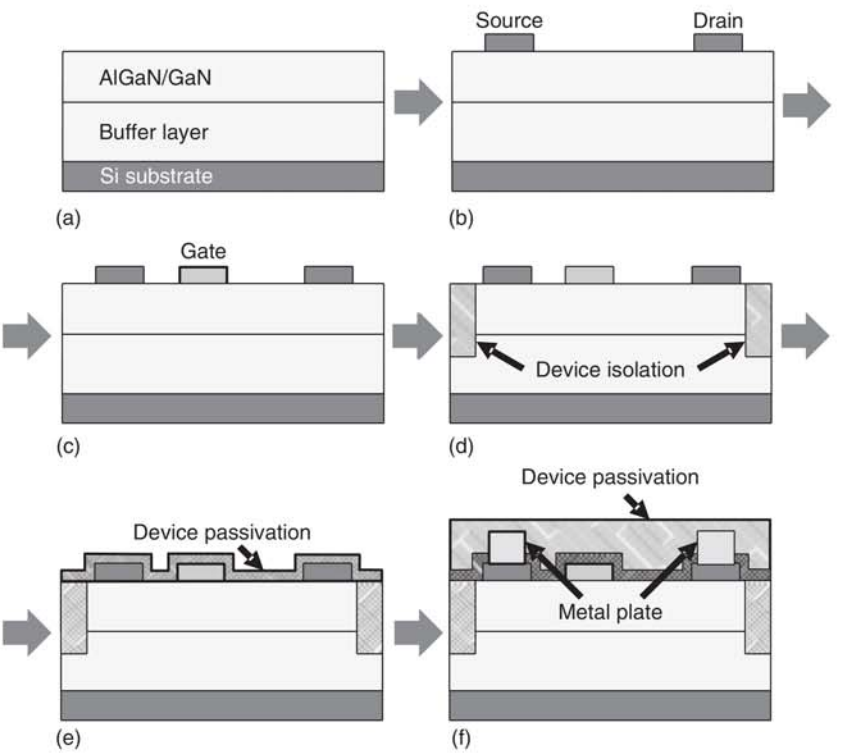


Figure 19.5 Sequence of GaN-HFET device process showing (a), (b) ohmic metalization, (c) gate metalization, (d) device isolation with ion implantation, (e) surface passivation, and (f) metal plating and final passivation.

annealing over 1200 °C is necessary to recover crystal damage for Si activation as n-type donor, the contact resistance with order of 10^{-7} Ω/cm^2 is reported [53].

Schottky contact as gate contact is preferred to consist of high work-function metal such as Ni, Pd, and Pt for high Schottky barrier height to suppress reverse gate leakage current [54, 55]. Practically, Ni/Au electrode has been used for gate metal due to its better adhesion to the AlGaN surface than that of Pd and Pt. The condition of the AlGaN surface such as nitrogen vacancy [56] can affect reverse electrical characteristics of the Schottky contact, and the introduction of insulate gate structures with SiO_2 and Al_2O_3 as alternative solutions has been reported [57, 58].

The device isolation is employed to define the active HFET region and electrically isolate the HFETs each other to avoid operational interferences among the HEMTs. There are mainly two approaches for the isolation, dry etching and ion implantation. Dry etching processes such as reactive ion etching (RIE) with chlorine-based gas have been used to etch GaN in order to eliminate the 2DEG, because GaN-based materials are quite chemically stable and cannot be etched by conventional acid-based wet etching processes as in Si- and GaAs devices. However, dry etching induces crystal damage that can degrade the HFET performance such as increasing of leakage current which results in inferior breakdown characteristics and worsens flatness of the device surface that affects coverage of metallization and passivation on the sidewall of the etched GaN layers.

Ion implantation technique has been also employed to isolate the HEMT with the device flatness kept. Implanted ions generate crystal damage of which energy states trap electrons and holes, which leads highly resistive regions with the resistance over 10^9 Ω/square. The ion-implanted isolation has been demonstrated by using various ion species from light element to heavy one such as H, He, N, O, F, P, Fe, and Zn [59–63]. Distribution of implanted ions and induced damage can be simulated by using Monte Carlo simulation [64] to select ion doses and acceleration energies for desired distribution of implanted ions and induced lattice damage. The simulated density of the induced damage becomes two orders of magnitude higher than that of implanted ion density. Practically, plural implantation steps with different doses and acceleration energies are employed to produce so-called box profile keeping constant ion density until certain depth of GaN layers. The resistance of the implanted region can be decreased by post-implanted annealing over 600 °C due to damage recovery. Therefore, temperatures of post processing after the ion implantation have to be selected carefully to maintain the high resistivity of the implanted regions.

Finally, the surface of GaN HFET is passivated with dielectric film, typically SiN, to protect the device surface from water and oxidation. The other purpose of the passivation is to deactivate surface states of the AlGaN barrier layer. The surface states can trap electrons accelerated by high electric field during the HEMT operation and then lift up the electrical potential in the vicinity of the 2DEG, resulting in decrease of drain current which is called as "current collapse" [65]. In addition to the surface passivation, another solution for the current collapse caused by high electric field has been proposed to form metal plates called as field plate to lower the electric field. The field plate is connected to source (source field plate, SFP) or gate (gate field plate,

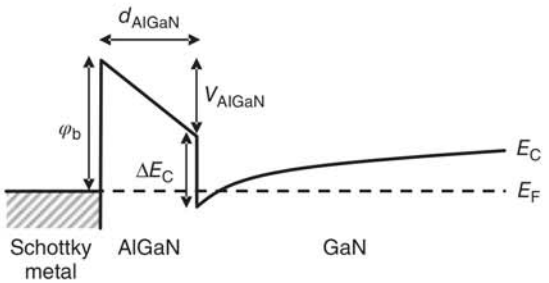


Figure 19.6 Band diagram of AlGaN/GaN structure with Schottky gate.

GFP) electrodes to reduce the peak electric field between gate and drain to avoid the electron trapping by the surface states, suppressing the current collapse [66].

19.3.2 Structures for E-Mode Operation

AlGaN/GaN HFETs usually show depletion-mode (D-mode, normally-on) characteristic which has negative gate threshold voltage and requires negative gate bias to deplete 2DEG under the gate. Figure 19.6 shows an energy band diagram of AlGaN/GaN with Schottky gate, and the threshold voltage of AlGaN/GaN HFET with Schottky gate can be described with the following equation.

$$V_T = \varphi_b - \Delta E_C - V_{AlGaN} = \varphi_b - \Delta E_C - \frac{qN_s d_{AlGaN}}{\epsilon_0 \epsilon_{AlGaN}} \tag{19.1}$$

where, φ_b, ΔE_C, N_s, d_{AlGaN}, ϵ_0, ϵ_{AlGaN}, and q are Schottky barrier height, conduction band offset between AlGaN and GaN, 2DEG density, AlGaN thickness, permittivity of vacuum, relative permittivity of AlGaN and electron charge, respectively. For power electronics application, enhancement-mode (E-mode, normally-off) characteristic with positive gate threshold voltage is required to keep power electronics systems safe even if gate driving circuit is failed. Referring to the above equation, following approaches are effective to obtain the E-mode characteristic.

1. Decreasing 2DEG density
   - Thinning AlGaN barrier layer
   - Reducing Al composition in AlGaN layer
2. Introducing negative charge into gate area
3. Increasing work function of gate material

Decreasing of 2DEG density by either thinning AlGaN barrier layer or reducing Al composition in AlGaN barrier is an effective way to obtain the normally-off operation [67]. However, the reduced 2DEG density can bring drawbacks to increase on-state resistance and decrease drain current of AlGaN/GaN HFETs. One of the methods to introduce negative charge to gate is fluorine treatment typically by carbon tetrafluoride (CF_4) plasma to introduce fluorine atom to interstitial sites of AlGaN barrier layer [68]. Due to the highest electronegativity of fluorine among all elements, an introduced fluorine atom can capture a free electron and act as a negative fixed charge which lifts up the gate potential and depletes the 2DEG. Addition to the abovementioned approaches, the method to increase work

function of gate material can lead to normally-off characteristic. Even though the highest work function metal of platinum (Pt, 5.12–5.93 eV) is insufficient to obtain E-mode operation of AlGaN/GaN HFET, using p-type wide-bandgap semiconductor such as p-GaN or p-AlGaN for gate material provides high built-in potential between p-type gate and AlGaN/GaN [69]. Since the gate threshold voltage of p-(Al)GaN/AlGaN/GaN can be determined with the thickness and Al composition of AlGaN barrier layer controlled by epitaxial growth technique, the device process has high controllability and high reproducibility which are preferred for device mass production. The next subsection of 19.3.3 and the session of 19.4 describe the p-type gate AlGaN/GaN HFET and related applications in detail, respectively.

19.3.3 E-Mode GaN Gate-Injection Transistor (GIT) on Si Substrate

19.3.3.1 Device Structure and Operational Principle

As shown in Figures 19.7 and 19.8, the E-mode gate-injection transistor (GIT) has a p-type gate onto the AlGaN/GaN HFET structure which lifts up the potential of the 2DEG under the gate and depletes the 2DEG there at the zero gate voltage. Figure 19.9 summarizes the basic operational principle of GIT. At the zero gate voltage, the electron channel under the gate is fully depleted to enable the E-mode operation. By increasing the gate voltage up to the forward voltage of the gate pn junction, the drain current starts to flow, which is based on the phenomena in conventional unipolar field effect transistors. When the gate voltage becomes higher than the forward voltage of around 3.5 V, holes can be injected from the p-type gate into the 2DEG, which is called conductivity modulation observed in Si-insulated gate bipolar transistor (IGBT) operation. Then the injected holes induce the same amount of electrons at the 2DEG to keep the charge neutrality. The induced electrons move to the drain side and contribute for increasing drain current while the injected holes stay underneath the gate due to the two order magnitude lower mobility of holes than that of the electrons. Figure 19.10 shows the I_{ds}–V_{gs} characteristics of a fabricated GIT in which the second peak of the transconductance g_m at higher

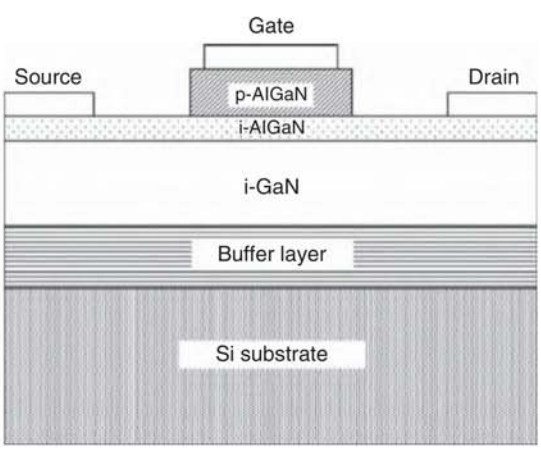


Figure 19.7 Schematic cross-section of GaN-GIT [69].

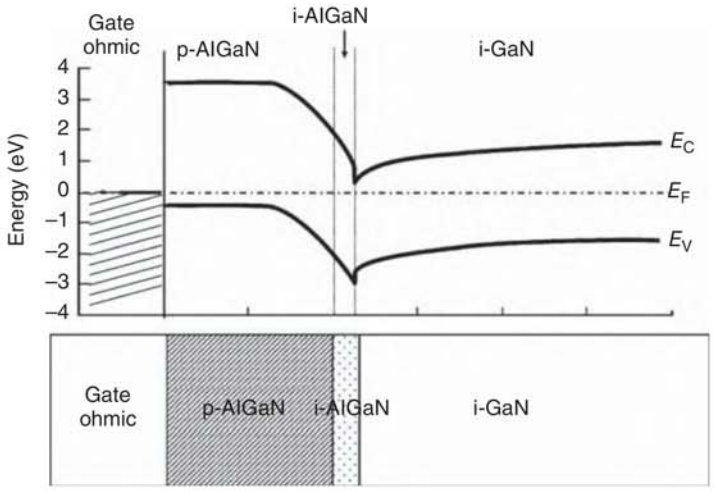


Figure 19.8 Band diagram of GaN-GIT at the gate bias of 0 V [69].

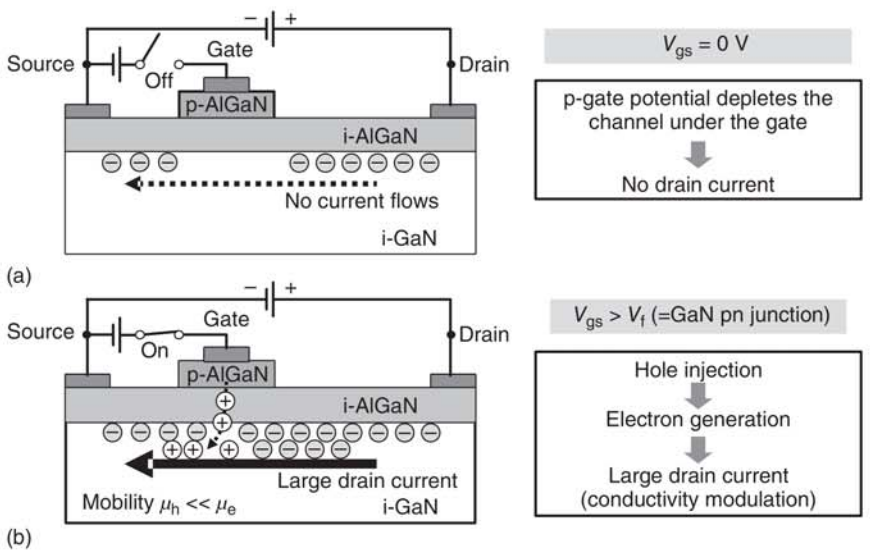


Figure 19.9 Cross-sectional structure of GaN-GIT showing operational principal at (a) off-state and (b) on-state.

gate voltage indicates the abovementioned conductivity modulation. The electroluminescence (EL) of the GIT around the p-type gate is also a proof of the operational principle [70], where the EL indicates the recombination of the injected holes and the electrons at the higher gate voltage.

19.3.3.2 DC Performance of GIT

One of features of GIT is the device fabrication on cost-effective Si substrate. A p-AlGaN/i-AlGaN/GaN heteroepitaxial structure for the GIT is grown on 6-in.

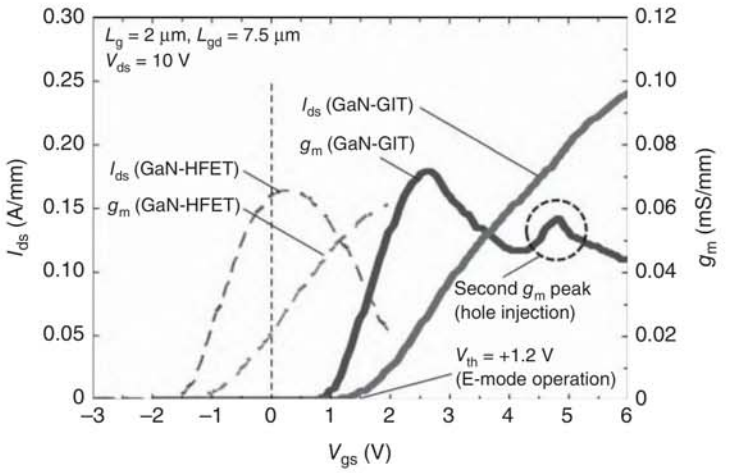


Figure 19.10 Measured $I_{ds}-V_{gs}$ characteristics of fabricated GaN-GIT on Si substrate.

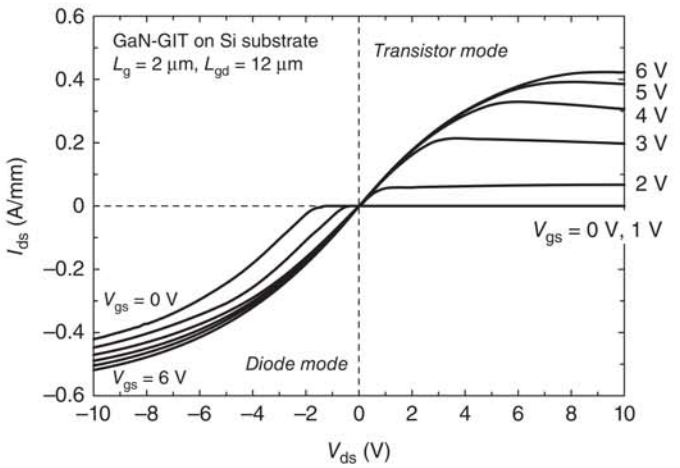


Figure 19.11 Measured on-state $I_{ds}-V_{ds}$ characteristics of fabricated GaN-GIT on Si substrate.

Si(111) substrate with buffer layers consisting of the GaN/AlN multilayers on top of the AlGaN/AlN initial layers. The p-gate is selectively formed by dry etching. GaN lateral HFETs have two conduction modes of "transistor mode" and "diode mode". The transistor mode has the drain current which flows from drain to source as conventional transistor operation, while the diode mode has the reverse conduction from source to drain through the 2DEG with drain offset voltage like diode even without any intrinsic body diode as in Si-metal oxide semiconductor field-effect transistors (MOSFETs). As shown in Figure 19.11, the transistor mode shows no drain offset voltage with the measured specific on-state resistance $R_{on}A$ of 2.3 mΩ cm^2. On the other hand, the diode mode has the drain threshold voltage of +1.5 V corresponding to the gate threshold voltage. By applying the gate voltage in

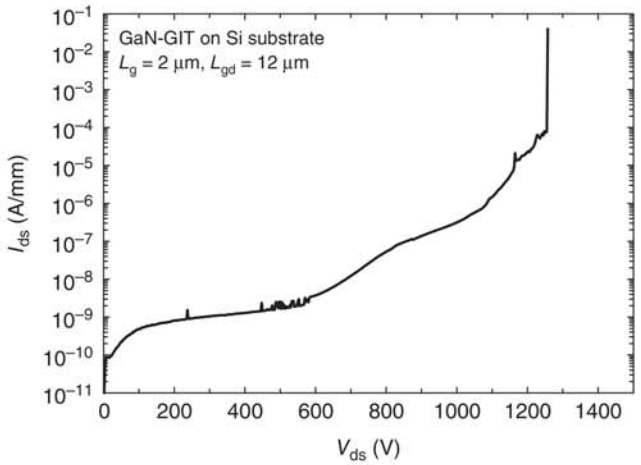


Figure 19.12 Measured off-state $I_{ds}-V_{ds}$ characteristics of fabricated GaN-GIT on Si substrate.

the diode mode, the GIT has no V_{ds} offset-voltage enabling low conduction loss. The 600-V-rating GIT shows a breakdown voltage of 1260 V at L_{gd} of 12 μm as shown in Figure 19.12. As shown in Figure 19.13, the breakdown voltage increases with extending L_{gd} and then saturates a certain value determined by the thickness of GaN epitaxial layers on Si, where the vertical electrical field in the device dominates the breakdown characteristics of GaN HFETs on Si. A 600-V rating GaN-GIT with wider gate width shows the on-state resistance R_{on} of 65 mΩ, the rating continuous current of 15 A and the gate charge Q_g of 11 nC. The figure of merit $R_{on}Q_g$ for low conduction and low switching losses is calculated to be 700 mΩ nC which is one thirteenth of that by state-of-art super junction Si-MOSFETs.

19.3.3.3 Switching Performance of GIT

In addition to the device performance, package and assembling technologies with low parasitic inductances are also important to extract full potential of the high-speed switching of GaN devices. Conventional packages such as TO-220 have long lead terminals of which parasitic inductances slow down switching speed of GaN devices. The flip-chip assembly can significantly reduce the parasitic inductance down to 2 nH in comparison with 25 nH obtained by TO-220 package. The flip-chip assembly enables the fast switching speed dV_{ds}/dt of 170 V/ns leading to low switching loss [71]. In addition to the conduction and switching losses, recovery losses of the diode mode induced by turning-off of diode operations are also taken into account for achieving higher conversion efficiency. Figure 19.14 shows a recovery characteristic of the GaN-GIT compared with that of an Si-based fast recovery diode (Si-FRD) [72]. The GaN-GIT has much smaller recovery charge than that of the Si-FRD because of unipolar characteristic in the GaN-GIT diode mode. In summary, the GIT has quite high potential for highly efficient and high-frequency power applications.

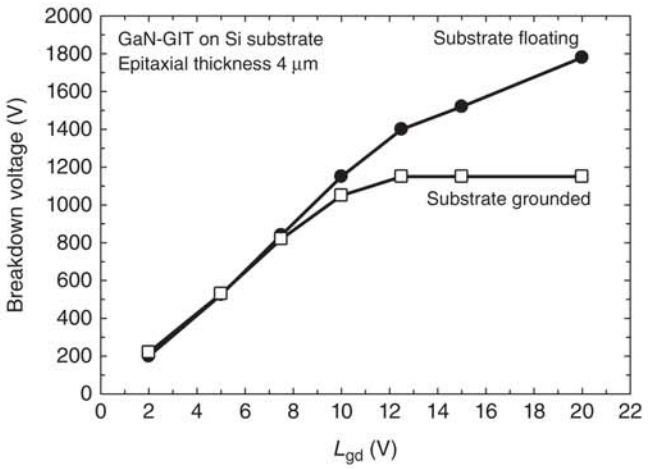


Figure 19.13 Breakdown voltages of fabricated GaN-GITs on Si substrate for various L_{gd}, comparing electrical potential of Si substrate.

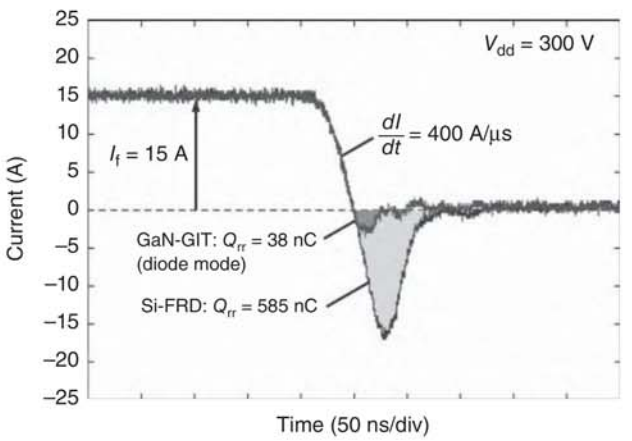
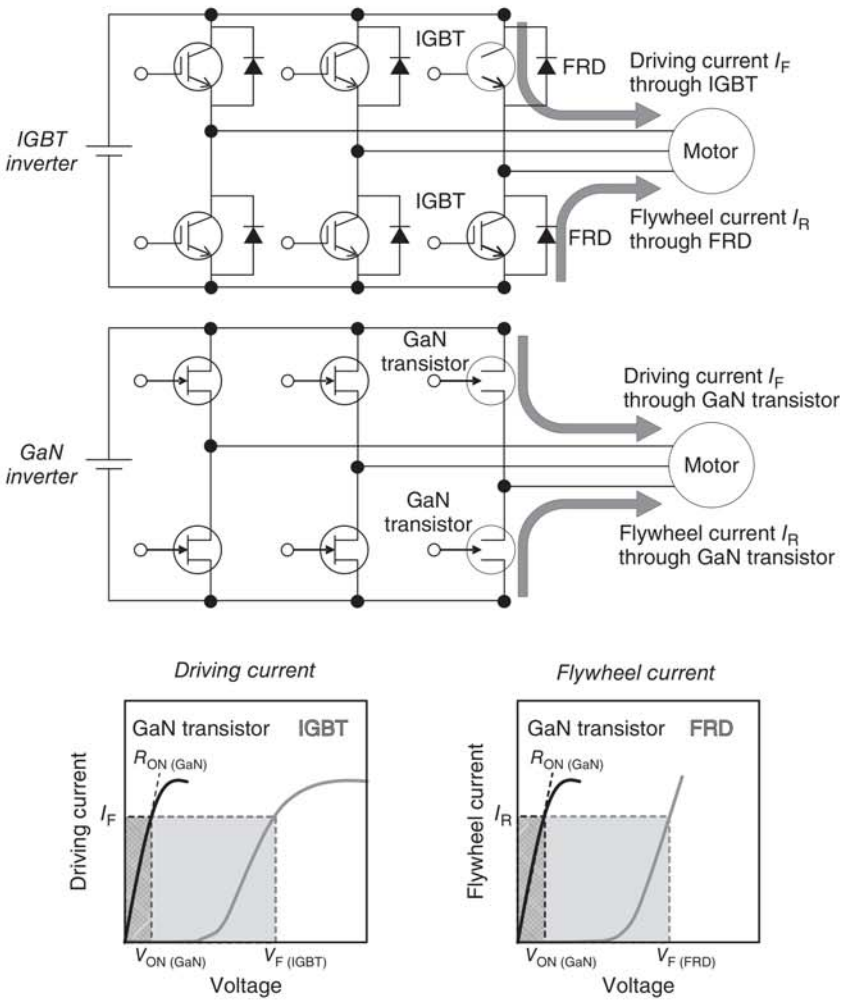


Figure 19.14 Measured recovery characteristics of GaN-GIT in diode-mode operation compared with that of a Si-based FRD.

19.4 Application of GaN HFET

GaN HFETs enable to make power conversion systems such as inverters and power supplies higher efficient and smaller size taking advantage of the superior device characteristics.

In the inverter application as shown in Figure 19.15, GaN HFETs can achieve low conduction loss by no drain-voltage offset and synchronous rectification utilizing the diode mode of the GaN-GIT. Furthermore, the GaN inverter requires no external diode such as Si-FRD as seen in the Si-based inverter, which can reduce the number of components, assembling area, and system cost. Figure 19.16 shows conversion efficiencies and loss analysis of GaN inverter with GaN-GITs compared with those



$$\text{IGBT loss} = V_{F\ (IGBT)} \times I_F + V_{F\ (FRD)} \times I_R$$

$$\text{GaN transistor loss} = V_{ON\ (GaN)} \times I_F + V_{ON\ (GaN)} \times I_R = R_{ON\ (GaN)} \times I_F^2 + R_{ON\ (GaN)} \times I_R^2$$

Figure 19.15 Operations of a IGBT-based inverter and GaN-based one showing forward and flywheel conduction losses.

by the Si-based inverter. The GaN inverter achieves the high conversion efficiency over 99% at 1.5 kW and significantly improves the efficiency in lower output region in comparison with that by Si-IGBTs due to the lower conduction loss of GaN-GITs. The reduction of the total loss in the GaN inverter by 60% at 500 W contributes to achieve the higher efficiency as analyzed in Figure 19.17 [72].

Power supplies such as DC/DC and AC/DC are also suitable applications for GaN HFETs, since high-frequency operation can reduce the system size by using smaller components such as capacitors, inductors, and transformers. So far, GaN DC/DCs

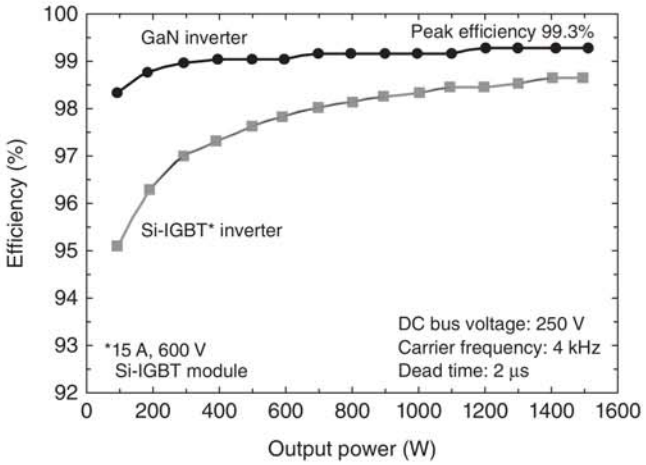


Figure 19.16 Measured power-conversion efficiency of three-phase inverter with GaN-GITs compared with that with Si-IGBTs.

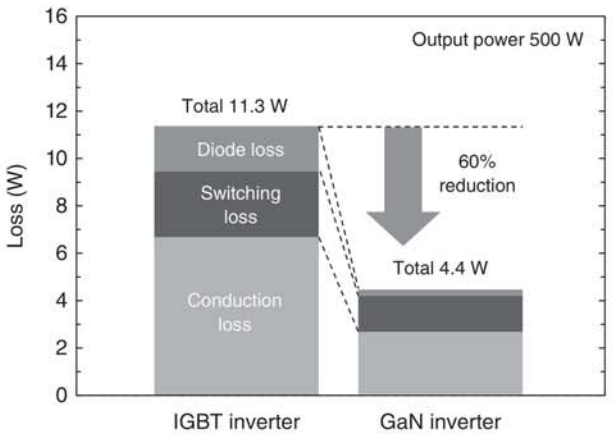


Figure 19.17 The analysis of operating losses in the GaN inverter system compared with that in the Si inverter system.

with 1–5 MHz operation [73] and with integrated small transformer into printed circuit board (PCB) are demonstrated [74].

19.5 Integration of Lateral GaN Devices

One of the biggest advantages of GaN lateral devices is integration of GaN devices and gate drivers onto the same substrate to build highly functional integrated circuits (ICs) which is technically difficult for other vertical power devices. Lateral GaN devices can be integrated into one chip with planer device isolation typically fabricated by ion implantation as shown in Figure 19.18. The integration eliminates wirings between the devices and minimizes parasitic inductances which are good to extract high potential of GaN devices for high-frequency operations. Figure 19.19

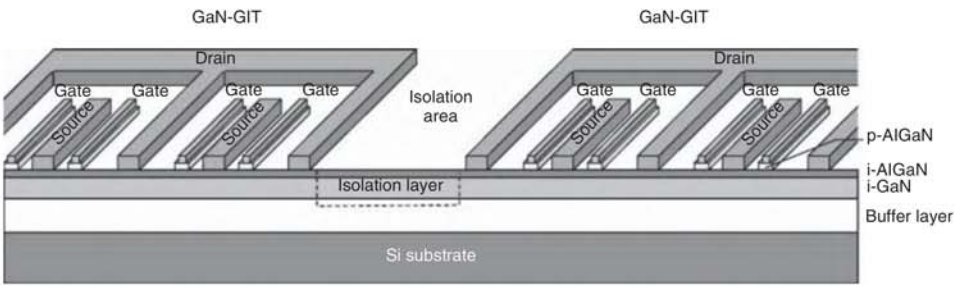


Figure 19.18 Schematic cross-section of GaN-GITs integrated into one chip with planer isolation.

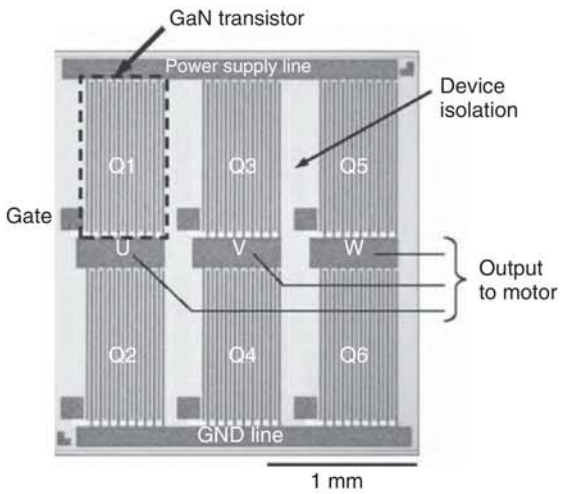


Figure 19.19 Photograph of the fabricated 6-in-1 GaN three-phase inverter IC.

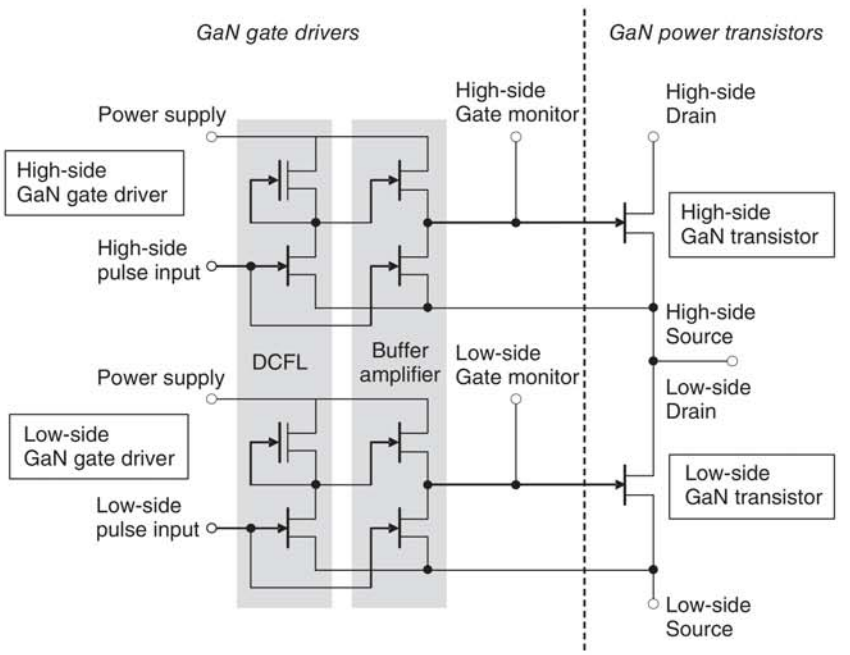


Figure 19.20 Circuit diagram of the DC/DC converter IC with integrated GaN gate drivers.

shows a GaN three-phase inverter IC consisting of six GaN-GITs integrated onto Si substrate [75]. Highly resistant region prepared by ion implantation achieves high-voltage electrical isolation between the devices, and the demonstrated conversion efficiency is higher than that obtained by conventional Si-IGBT inverters. Another example is low voltage GaN DC/DC integrated with GaN-based gate drivers [76]. The GaN gate drivers utilize direct coupled field-effect transistor logic (DCFL) circuit instead of CMOS circuit due to the extremely low hole mobility in GaN as shown in Figure 19.20. In addition, buffer amplifiers are also integrated to

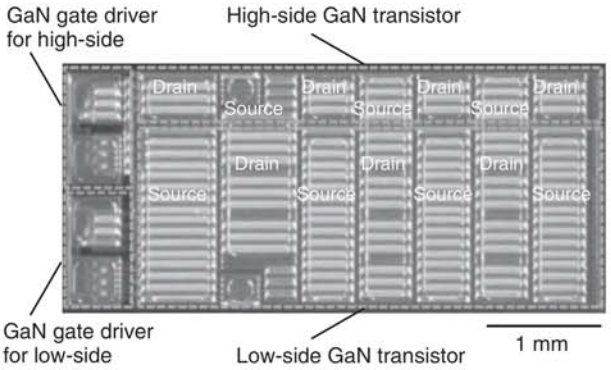


Figure 19.21 Photograph of the fabricated DC/DC IC in which two GaN power transistors and two GaN gate drivers are integrated into one chip.

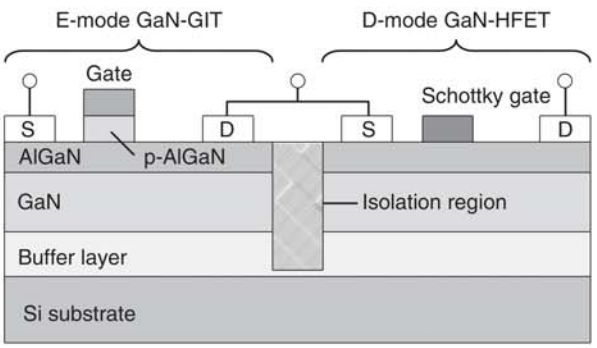


Figure 19.22 Schematic cross-section of E-mode and D-mode GaN HFETs integrated in GaN DC/DC IC.

enable lower power consumption for the gate driving. Figures 19.21 and 19.22 show the photograph and the cross-sectional schematic of the GaN DC/DC IC, where both E-mode and D-mode GaN devices are fabricated by a part of the entire device processing. One to three megahertz operations and peak conversion efficiency of 88.2% at 2 MHz are demonstrated. In summary, abovementioned integration of GaN devices is an essential solution to enable higher device performances and expands application potential of GaN devices.

19.6 Summary

This chapter summarizes entire technology related to GaN power devices from GaN epitaxial growth to the related power applications. The first part of the chapter summarizes GaN epitaxy on Si substrate including impurity doping, choice of substrates, detailed epitaxial structures to initiate epitaxial growth, manage mechanical stress, and generate 2DEG for GaN lateral power devices. In the second part of the chapter, the technologies on GaN lateral power devices are summarized, especially focusing on E-mode GaN-GIT device, which is suitable for practical power applications. The third part of the chapter shows power application

examples of GaN lateral power devices achieving higher conversion efficiency than that by conventional Si power devices. Finally, the fourth part of the chapter introduces integrations of GaN lateral devices on one chip which could expand applications of GaN devices furthermore. In summary, GaN-based power devices are very promising devices for power electronics applications due to the superior device performance surpassing conventional Si-based power devices. The technical breakthroughs of GaN epitaxial growth and device technologies by the pioneers in the early days have opened the door to expand the application of GaN optoelectric and power devices giving us lots of obvious benefits in our life. The maturity level of GaN power devices has been improving in the past years. Even though GaN market is still at the early stage so far, the author looks forward to big contribution of GaN power devices for future highly efficient energy society.

Acknowledgments

The author would like to sincerely acknowledge Dr. Tetsuzo Ueda, Dr. Tsuyoshi Tanaka, and other members of Panasonic Corporation for their technical advices and supports throughout the work. He also would like to thank Dr. Daisuke Ueda, Kyoto Institute of Technology, for his fruitful technical advices. The work is partly supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan, under the Strategic Development of Energy Conservation Technology Project and the Strategic Development of Energy Saving Innovative Technology Development Project.

References

1 Maruska, H.P. and Tietjen, J.J. (1969). The preparation and properties of vapor-deposited single-crystal GaN. *Appl. Phys. Lett.* 15: 327.
2 Pankove, J.I., Miller, E.A., and Berkeyheiser, J.E. (1971). GaN electroluminescent diodes. *RCA (Radio Corporation of America) Rev.* 32: 383.
3 Amano, H., Sawaki, N., Akasaki, I., and Toyoda, Y. (1986). Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer. *Appl. Phys. Lett.* 48: 353.
4 Nakamura, S. (1991). GaN growth using GaN buffer layer. *Jpn. J. Appl. Phys.* 30: L1705.
5 Amano, H., Kito, M., Hiramatsu, K., and Akasaki, I. (1989). P-type conduction in Mg-doped GaN treated with low-energy electron beam irradiation (LEEBI). *Jpn. J. Appl. Phys.* 28: L2112.
6 Nakamura, S., Mukai, T., Senoh, M., and Iwasa, N. (1992). Thermal annealing effects on p-type Mg-doped GaN films. *Jpn. J. Appl. Phys.* 31: L139.
7 Amano, H., Asahi, T., and Akasaki, I. (1990). Stimulated emission near ultraviolet at room temperature from a GaN film grown on sapphire by MOVPE using an AlN buffer layer. *Jpn. J. Appl. Phys.* 29 (2): L205.

8 Nakamura, S., Mukai, T., and Senoh, M. (1991). High-power GaN p-n junction blue-light-emitting diodes. *Jpn. J. Appl. Phys.* 30: L1998.

9 Saxler, A., Kung, P., Sun, C.J. et al. (1994). High quality aluminum nitride epitaxial layers grown on sapphire substrates. *Appl. Phys. Lett.* 64: 339.

10 Yoshimoto, N., Matsuoka, T., Sasaki, T., and Katsui, A. (1991). Photoluminescence of InGaN films grown at high temperature by metalorganic vapor phase epitaxy. *Appl. Phy. Lett.* 59 (18): 2251–2253.

11 Sayyah, K., Chung, B.C., and Gershenzon, M. (1986). The influence of TMA and SiH_4 on the incorporation rate of Ga in $Al_xGa_{1-x}N$ crystals grown from TMG and NH_3. *J. Cryst. Growth* 77 (1–3): 424–429.

12 Akasaki, I., Amano, H., Koide, N. et al. (1993). Conductivity control of GaN and fabrication of UV/blue GaN light emitting devices. *Phys. B: Condens. Matter* 185 (1–4): 428–432.

13 Nakayama, H., Hacke, P., Khan, M.R.H. et al. (1996). Electrical transport properties of p-GaN. *Jpn. J. Appl. Phys.* 35: L282.

14 Kaufmann, U., Schlotter, P., Obloh, H. et al. (2000). Hole conductivity and compensation in epitaxial GaN:Mg layers. *Phy. Rev. B* 62: 10867.

15 Romano, L.T., Kneissl, M., Northrup, J.E. et al. (2001). Influence of microstructure on the carrier concentration of Mg-doped GaN films. *Appl. Phys. Lett.* 79: 2734.

16 Romano, L.T., Northrup, J.E., Ptak, A.J., and Myers, T.H. (2000). Faceted inversion domain boundary in GaN films doped with Mg. *Appl. Phys. Lett.* 77: 2479.

17 Chung, B.-C. and Gershenzon, M. (1992). The influence of oxygen on the electrical and optical properties of GaN crystals grown by metalorganic vapor phase epitaxy. *J. Appl. Phys.* 72: 651.

18 Zywietz, T.K., Neugebauer, J., and Scheffler, M. (1999). The adsorption of oxygen at GaN surfaces. *Appl. Phys. Lett.* 74: 1695.

19 Lyonsa, L., Janotti, A., and Van de Walle, C.G. (2010). Carbon impurities and the yellow luminescence in GaN. *Appl. Phys. Lett.* 97: 152108.

20 Oila, J., Kivioja, J., Ranki, V. et al. (2003). Ga vacancies as dominant intrinsic acceptors in GaN grown by hydride vapor phase epitaxy. *Appl. Phys. Lett.* 82: 3433.

21 Look, D.C., Farlow, G.C., Drevinsky, P.J. et al. (2003). On the nitrogen vacancy in GaN. *Appl. Phys. Lett.* 83: 3525.

22 Parish, G., Keller, S., Denbaars, S.P., and Mishra, U.K. (2000). SIMS investigations into the effect of growth conditions on residual impurity and silicon incorporation in GaN and $Al_xGa_{1-x}N$. *J. Electron. Mater.* 29: 15–20.

23 Heikman, S., Keller, S., DenBaars, S.P., and Mishra, U.K. (2002). Growth of Fe doped semi-insulating GaN by metalorganic chemical vapor deposition. *Appl. Phys. Lett.* 81: 439.

24 Kumagai, Y., Murakami, H., Kangawa, Y., and Koukitu, A. (2005). Growth and characterization of thick GaN layers with high Fe doping. *Phys. Status Solidi C* 2 (7): 2058–2061.

25 Utsumi, W., Saitoh, H., Kaneko, H. et al. (2003). Congruent melting of gallium nitride at 6 GPa and its application to single-crystal growth. *Nat. Mater.* 2: 735–738.

26 Motoki, K., Okahisa, T., Matsumoto, N. et al. (2001). Preparation of large freestanding GaN substrates by hydride vapor phase epitaxy using GaAs as a starting substrate. *Jpn. J. Appl. Phys.* 40: L140.

27 Handa, H., Ujita, S., Shibata, D. et al. (2016). High-speed switching and current-collapse-free operation by GaN gate injection transistors with thick GaN buffer on bulk GaN substrates. *IEEE IEDM Technical Digest*, San Francisco, CA, USA, p. 10.3.1.

28 Ando, Y., Okamoto, Y., Miyamoto, H. et al. (2003). 10-W/mm AlGaN-GaN HFET with a field modulating plate. *IEEE Electron Device Lett.* 24 (5): 289291.

29 Gaska, R., Chen, Q., Yang, J. et al. (1997). High-temperature performance of AlGaN/GaN HFETs on SiC substrates. *IEEE Electron Device Lett.* 18 (10): 492494.

30 Ishikawa, H., Yamamoto, K., Egawa, T. et al. (1998). Thermal stability of GaN on (111) Si substrate. *J. Cryst. Growth* 189–190: 178–182.

31 Watanabe, A., Takeuchi, T., Hirosawa, K. et al. (1993). The growth of single crystalline GaN on a Si substrate using AIN as an intermediate layer. *J. Cryst. Growth* 128 (1–4): 391–396.

32 Dadgar, A., Poschenrieder, M., Reiher, A. et al. (2003). Reduction of stress at the initial stages of GaN growth on Si(111). *Appl. Phys. Lett.* 82: 28.

33 Cheng, K., Leys, M., Degroote, S. et al. (2006). Flat GaN epitaxial layers grown on Si(111) by metalorganic vapor phase epitaxy using step-graded AlGaN intermediate layers. *J. Electron. Mater.* 35: 592–598.

34 Able, A., Wegscheider, W., Engl, K., and Zweck, J. (2005). Growth of crack-free GaN on Si(111) with graded AlGaN buffer layers. *J. Cryst. Growth* 276 (3–4): 415–418.

35 Ishikawa, H., Zhao, G.Y., Nakada, N. et al. (1999). GaN on Si substrate with AlGaN/AlN intermediate layer. *Jpn. J. Appl. Phys.* 38 (5): 492–494.

36 Reiher, A., Blasing, J., Dadgar, A. et al. (2003). Efficient stress relief in GaN heteroepitaxy on Si(111) using low-temperature AlN interlayers. *J. Cryst. Growth* 248: 563–567.

37 Ikeda, N., Kaya, S., Li, J. et al. (2009). High-power AlGaN/GaN MIS-HFETs with field-plates on Si substrates.", *International symposium on power semiconductor devices and ICs (ISPSD)*, Barcelona, Spain.

38 Choi, Y.C., Pophristic, M., Cha, H.-Y. et al. (2006). The effect of an Fe-doped GaN buffer on off-state breakdown characteristics in AlGaN/GaN HEMTs on Si substrate. *IEEE Trans. Electron Devices* 53 (12): 2926–2931.

39 Klein, P.B., Binari, S.C., Ikossi, K. et al. (2001). Current collapse and the role of carbon in AlGaN/GaN high electron mobility transistors grown by metalorganic vapor-phase epitaxy. *Appl. Phys. Lett.* 79: 3527.

40 Meneghini, M., Rossetto, I., Bisi, D. et al. (2006). Role of buffer doping and pre-existing trap states in the current collapse and degradation of AlGaN/GaN HEMTs. *IEEE Int. Reliab. Phys. Sympos.* 53 (12): 2926–2931.

41 Ambacher, O., Smart, J., Shealy, J.R. et al. (1999). Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures. *J. Appl. Phys.* 85: 3222.

42 Shen, L., Heikman, S., Moran, B. et al. (2001). AlGaN/AlN/GaN high-power microwave HEMT. *IEEE Electron Device Lett.* 22 (10): 457–459.

43 Kuzmik, J., Kostopoulos, A., Konstantinidis, G. et al. (2006). InAlN/GaN HEMTs: a first insight into technological optimization. *IEEE Trans. Electron Devices* 53 (3): 422–426.

44 Medjdoub, F., Alomari, M., Carlin, J.-F. et al. (2008). Barrier-layer scaling of InAlN/GaN HEMTs. *IEEE Electron Device Lett.* 29 (5): 422–425.

45 Chen, C.Q., Zhang, J.P., Adivarahan, V. et al. (2003). AlGaN/GaN/AlGaN double heterostructure for high-power III-N field-effect transistors. *Appl. Phys. Lett.* 82: 4593.

46 Shen, L., Coffie, R., Buttari, D. et al. (2004). High-power polarization-engineered GaN/AlGaN/GaN HEMTs without surface passivation. *IEEE Electron Device Lett.* 25 (1): 7–9.

47 Mizutani, T., Ito, M., Kishimoto, S., and Nakamura, F. (2007). AlGaN/GaN HEMTs with thin InGaN cap layer for normally off operation. *IEEE Electron Device Lett.* 28 (7): 549–551.

48 Murata, T., Hikita, M., Hirose, Y. et al. (2005). Source resistance reduction of AlGaN-GaN HFETs with novel superlattice cap layer. *IEEE Trans. Electron Devices* 52 (6): 1042–1047.

49 Nakazawa, S., Ueda, T., Inoue, K. et al. (2005). Recessed-gate AlGaN/GaN HFETs with lattice-matched InAlGaN quaternary alloy capping layers. *IEEE Trans. Electron Devices* 52 (10): 2124–2128.

50 Takizawa, T., Nakazawa, S., and Ueda, T. (2008). Crystalline SiN_x ultrathin films grown on AlGaN/GaN using in situ metalorganic chemical vapor deposition. *J. Electron. Mater.* 37: 628–634.

51 Derluyn, J., Boeykens, S., Cheng, K. et al. (2005). Improvement of AlGaN/GaN high electron mobility transistor structures by in situ deposition of a Si_3N_4 surface layer. *J. Appl. Phys.* 98: 054501.

52 Lin, M.E., Ma, Z., Huang, F.Y. et al. (1994). Low resistance ohmic contacts on wide band-gap GaN. *Appl. Phys. Lett.* 64: 1003.

53 Nguyen, C., Shah, P., Leong, E. et al. (2010). Si implant-assisted ohmic contacts to GaN. *Solid-State Electron.* 54 (10): 1227–1231.

54 Zhang, B.J., Egawa, T., Zhao, G.Y. et al. (2001). Schottky diodes of Ni/Au on n-GaN grown on sapphire and SiC substrates. *Appl. Phys. Lett.* 79: 2567.

55 Wang, L., Nathan, M.I., Lim, T.H. et al. (1996). Pt/Pd high barrier height GaN Schottky diodes: Pt/GaN and Pd/GaN. *Appl. Phys. Lett.* 68: 1267.

56 Hashizume, T. and Nakasaki, R. (2002). Discrete surface state related to nitrogen-vacancy defect on plasma-treated GaN surfaces. *Appl. Phys. Lett.* 80: 4564.

57 Khan, M.A., Hu, X., Sumin, G. et al. (2000). AlGaN/GaN metal oxide semiconductor heterostructure field effect transistor. *IEEE Electron Device Lett.* 21 (2): 63–65.

58 Corrion, A.L., Shinohara, K., Regan, D. et al. (2011). High-speed AlN/GaN MOS-HFETs with scaled ALD Al2O3 gate insulators. *IEEE Electron Device Lett.* 32 (8): 1062–1064.

59 Binari, S.C., Dietrich, H.B., Kelner, G. et al. (1995). H, He, and N implant isolation of n-type GaN. *J. Appl. Phys.* 78: 3008.

60 Dang, G., Cao, X.A., Ren, F. et al. (1999). Oxygen implant isolation of n-GaN field-effect transistor structures. *J. Vac. Sci. Technol., B* 17: 2015.

61 Lo, C.F., Kang, T.S., Liu, L. et al. (2010). Isolation blocking voltage of nitrogen ion-implanted AlGaN/GaN high electron mobility transistor structure. *Appl. Phys. Lett.* 97: 262116.

62 Umeda, H., Takizawa, T., Anda, Y. et al. (2013). High-voltage isolation technique using Fe ion implantation for monolithic integration of AlGaN/GaN transistors. *IEEE Trans. Electron Devices* 60 (2): 771–775.

63 Oishi, T., Miura, N., Suita, M. et al. (2003). Highly resistive GaN layers formed by ion implantation of Zn along the c axis. *J. Appl. Phys.* 94: 1662.

64 Ziegler, J. (2008). SRIM & TRIM. http://www.srim.org/ (accessed 11 September 2020).

65 Kim, H., Thompson, R.M., Tilak, V. et al. (2003). Effects of SiN passivation and high-electric field on AlGaN-GaN HFET degradation. *IEEE Electron Device Lett.* 24 (7): 421–423.

66 Saito, W., Kakiuchi, Y., Nitta, T. et al. (2010). Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs. *IEEE Electron Device Lett.* 31 (7): 659–661.

67 Ohmaki, Y., Tanimoto, M., Akamatsu, S., and Mukai, T. (2006). Enhancement-mode AlGaN/AlN/GaN high electron mobility transistor with low on-state resistance and high breakdown voltage. *Jpn. J. Appl. Phys.* 45 (Part 2): 42–45.

68 Cai, Y., Zhou, Y., Chen, K.J., and Lau, K.M. (2005). High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment. *IEEE Electron Device Lett.* 26: 435.

69 Uemoto, Y., Hikita, M., Ueno, H. et al. (2006). Gate injection transistor (GIT) - a normally-off AlGaN/GaN power transistor using conductivity modulation. *IEEE Trans. Electron Device* 54: 3393.

70 Meneghini, M., Scamperle, M., Pavesi, M. et al. (2010). Electron and hole-related luminescence processes in gate injection transistors. *Appl. Phys. Lett.* 97: 033506.

71 Morita, T., Handa, H., Ujita, S. et al. (2014). 99.3% Efficiency of boost-up converter for totem-pole bridgeless PFC using GaN gate injection transistors. *PCIM Europe*, Nürnberg, Germany.

72 Morita, T., Tamura, S., Anda, Y. et al. (2011). 99.3% Efficiency of three-phase inverter using GaN-based gate injection transistors. *Proceedings of 26th IEEE Applied Power Electronics Conference and Exposition* (APEC 2011), Fort Worth, TX, USA, p. 481.

73 Umeda, H., Kinoshita, Y., Ujita, S. et al. (2014). Highly efficient low-voltage DC–DC converter at 2–5 MHz with high operating current using GaN gate injection transistors. *PCIM Europe*, Nürnberg, Germany, p. 45.

74 Huang, D., Ji, S., and Lee, F.C. (2013). Matrix transformer for LLC resonantconverters. *Proceedings of the 28th IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, pp. 2078–2083.

75 Uemoto, Y., Morita, T., Ikoshi, A. et al. (2009). GaN monolithic inverter IC using normally-off gate injection transistors with planar isolation on Si substrate. *IEEE IEDM Technical Digest*, Baltimore, MD, USA, p. 165.

76 Ujita, S., Kinoshita, Y., Umeda, H. et al. (2014). A compact GaNbased DC–DC converter IC with high-speed gate drivers enabling high efficiencies. *International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Wikoloa, HI, USA, B1L-A-1.

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Growth of Single Crystal Diamond Wafers for Future Device Applications

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20.1 Introduction

Diamond as a mineral is known for several thousand years. It was found in nature and was valued most of the time for its appearance and for its mechanical properties. Ultimate values of stiffness and hardness still form the base for many industrial applications, e.g., as material for cutting tools.

Later, it turned out that diamond excels in further characteristics comprising optical, thermal, and electronic properties. For electronic applications, carrier mobility μ, saturation drift velocity v_s, the breakdown field strength E_m, and the thermal conductivity λ are relevant quantities. In power electronics, the opposing requirements of minimum losses in ON state and highest blocking voltages in OFF state are summarized in Baliga's figure of merit (BFM) given by

$$\mathrm{BFM} = \frac{1}{4}\mu\varepsilon_r\varepsilon_0 E_m^3 \tag{20.1}$$

with ε_r and ε_0 the relative permittivity of diamond and the vacuum permittivity, respectively [1]. Normalized to the value of silicon, diamond's BFM is by more than 4 orders of magnitude higher and even compared to 4H-SiC there is a factor of 40. Thus, diamond's high breakdown field of ≈10 MV/cm and the cubic dependence in Eq. (20.1) form the base for its qualification as the *ultimate semiconductor material*, at least in the field of high-power devices.

Their realization first of all calls for techniques to grow single crystals with excellent structural quality and purity. Furthermore, appropriate dopants preferentially with low activation energy and adequate methods for a controlled insertion of defined quantities of the dopants are necessary. Here, it turns out that thermodynamic stability and the extreme properties of diamond pose specific restrictions as compared to standard semiconductor materials.

Diamond and graphite are two crystalline allotropes of pure carbon. The enthalpy of formation under standard conditions is 1.9 kJ/mol higher for diamond than for graphite. As a consequence, graphite is thermodynamically the stable modification

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

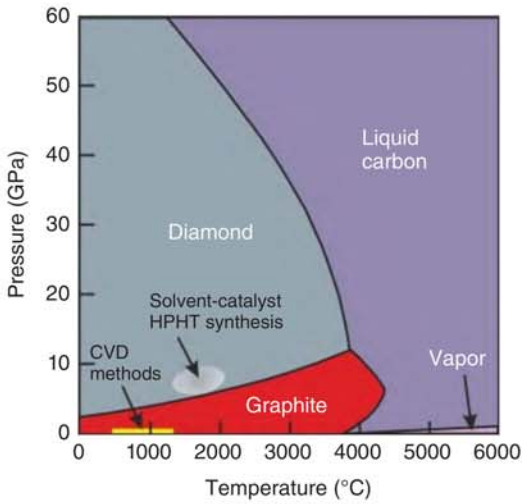

Figure 20.1 The phase diagram of carbon (restricted to the two solid allotropes diamond and graphite). The gray ellipse and the yellow bar indicate schematically the regions of the HPHT and CVD synthesis, respectively.

of carbon. The phase diagram of carbon in Figure 20.1 shows that the stability region of graphite extends at ambient pressure over the whole temperature region up to ≈4000 °C and up to pressures of several gigapascals.

According to the phase diagram, diamond is not stable at normal pressures. Nevertheless, spontaneous transformation does not occur due to the high kinetic barrier, e.g. an activation energy of 730 kJ/mol for the graphitization of the {110} surface [2]. This metastability explains that diamonds can have an age of several billion years, and it facilitates stable operation of diamond tools and devices even at elevated temperatures of several hundred degrees Celsius.

For the synthesis of diamond, two completely different concepts have successfully been developed. In the first one, the high-pressure high-temperature (HPHT) method, growth conditions are established under which diamond is the stable phase of carbon, while in the second one, the chemical vapor deposition (CVD) technique, diamond is metastable and growth is controlled by kinetics. The typical parameter regions are schematically indicated in Figure 20.1. In the following, both methods are described in detail, and their individual strengths and limitations are discussed with respect to the supply of the base material for power devices.

20.2 High-Pressure High-Temperature (HPHT) Synthesis

20.2.1 Basic Concepts and Technical Realizations

In the HPHT process, carbon material like graphite is filled into a growth capsule to transform it to diamond. According to the calculated Berman–Simon equilibrium line between graphite and diamond (see phase diagram), pressures of ≈2 GPa are sufficient to reach the stability region of diamond at room temperature [3].

However, due to the slow kinetics, temperatures well above 1000 °C are needed to obtain acceptable transformation velocities which in turn call for even higher pressures. For the direct conversion of pure graphite to diamond pressures >10 GPa and temperatures >2000 °C are required and the produced material is typically polycrystalline [4–6]. During the original elaboration of the HPHT process at the General Electric (GE) Research Laboratory, it already turned out that the presence of molten metals can drastically mitigate the necessary conditions [7]. For mass production of diamond nowadays, metal alloys like Fe–Ni, Fe–Co, Ni–Mn are added to grow diamond out of a metal–carbon solution at pressures of 5–6 GPa and temperatures of 1300–1600 °C [8, 9].

Concerning the specific role of the metal additives, two alternative models, i.e., the action as pure solvents for the carbon atoms and the action as catalyst were under debate for a long time [10]. While some authors claim that the metals serve purely as solvents [11], the term solvent catalyst is still common in literature [9, 12].

Development of technical setups that can produce and sustain the required pressures and temperatures in a sufficiently large volume for 50–100 hours or more was in the focus of R&D on the HPHT technology. The original high-pressure belt apparatus used for the first successful diamond synthesis [13][1] at GE labs in 1954 consisted of two opposing pistons tipped with anvils for the transfer of the pressure [11, 14] (see Figure 20.2a). The belt-type concept was further refined by companies like Element Six or Sumitomo for the commercial production of synthetic diamond

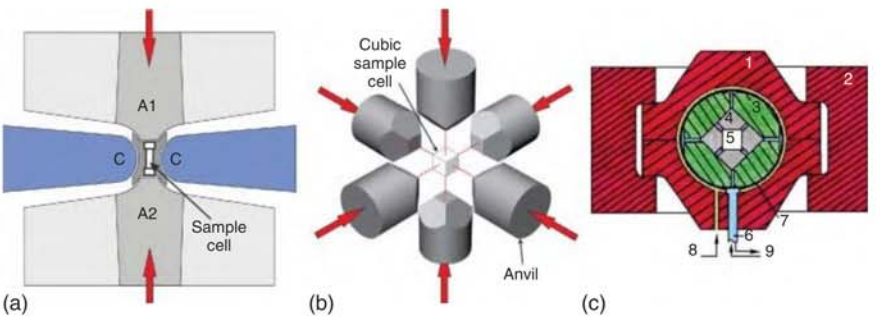

Figure 20.2 Schematic representations of three common HPHT growth setups: (a) In the belt-type apparatus, two anvils A1 and A2 compress the sample cell in the center in two opposing directions. These anvils and the belt C are made of WC-Co. (b) In the standard cubic apparatus, six anvils act along three perpendicular axes (adapted from [9]). (c) In the split sphere (BARS) arrangement, the pressure chamber (1) consisting of two half spheres is pressurized with oil (8). The eight large anvils (3) transfer the pressure via six pyramid-shaped WC-Co anvils (4) to the growth cell (5). (2) safety clamps, (6) power inlet, (7) rubber membrane, (9) cooling water. Source: (a) Adapted with permission from Nassau and Nassau [11]. © 1979 Elsevier. (c) Reprinted with permission from Abbaschian et al. [15]. © 2005 Elsevier.

1 Historically, the first diamond synthesis by man was achieved already one year earlier in 1953 by E. Lundblad and his team at Allmänna Svenska Elektriska Aktiebolaget (ASEA) in Sweden – since these results were kept secret for several years the credit for the first successful diamond synthesis went to the GE team (see Ref. [13]).

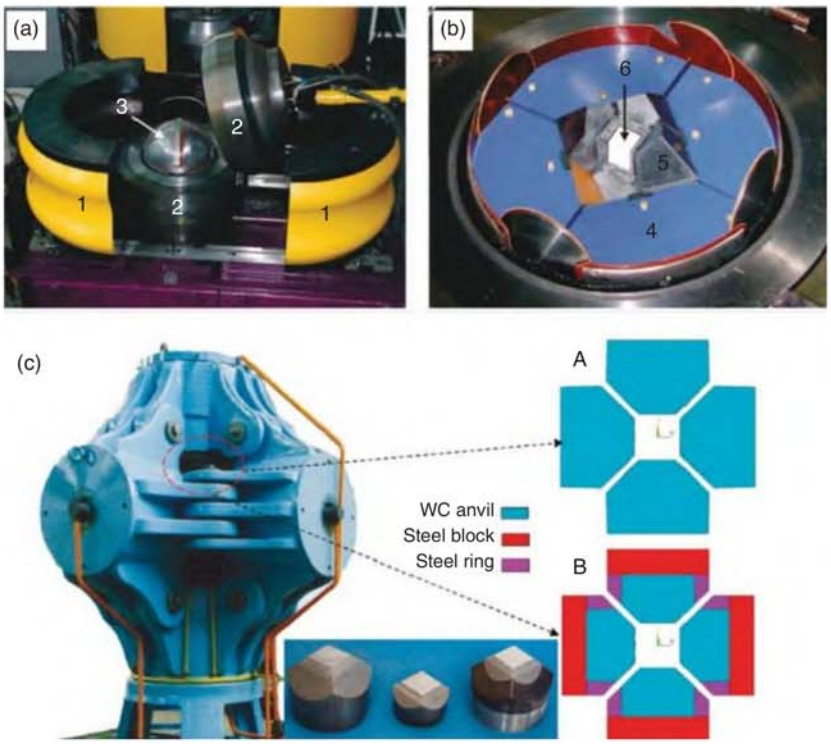

Figure 20.3 Photos of typical growth setups. (a, b) BARS setup with (1) clamps, (2) assembly with semi-sphere cavities, (3) multi-anvil block with a diameter of 300 mm, (4) steel anvils, (5) tungsten carbide anvils, and (6) high-pressure growth cell. (c) Photo of cubic high-pressure apparatus with schematic cross section of the multi-anvil assembly consisting of anvils with (A) traditional and (B) hybrid design. The inset shows an optical photo of different anvils. The overall height of the setup is >3 m [17]. Source: (a, b) Reprinted with permission from Palyanov et al. [18]. © 2010 American Chemical Society. (c) Reprinted with permission from Han et al. [19]. © 2011 American Chemical Society.

[4]. A modified version with uniaxial compression is the toroid anvil setup [4, 16]. Development of alternative multi-anvil geometries started already in the 1950s first with the invention of a tetrahedral press with four anvils [11]. Further technologically relevant multi-anvil-type setups are the standard cubic press that uses six anvils [9] (see Figure 20.2b) and its modification, the split sphere (also known by the Russian abbreviation BARS) setup [15], shown in Figure 20.2c.

Typical growth setups are shown in Figure 20.3.

20.2.2 The Temperature Gradient Method

Spontaneous nucleation of diamond from the supersaturated metal–carbon solution can be used to produce small grit for grinding and polishing applications. It should be avoided for the synthesis of large crystals with high structural quality. Instead,

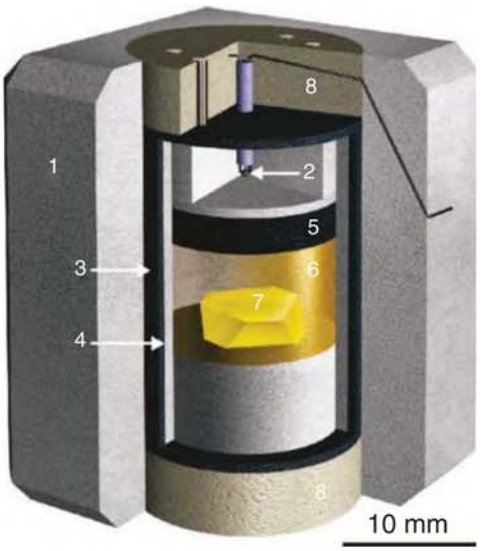

Figure 20.4 Schema of a high-pressure growth cell used in a BARS setup. (1) ZrO_2 container, (2) thermocouple, (3) graphite heater, (4) MgO sleeve, (5) graphite as carbon source, (6) metal melt, (7) diamond seed, (8) talc ceramics. Source: Reprinted with permission from Palyanov et al. [18]. © 2010 American Chemical Society.

a single crystal or an arrangement of sacrificial diamonds is used as seeds, and a well-defined temperature profile is realized within the pressure cell (temperature gradient method). This guarantees that the carbon is dissolved in the metal solution in the hot region and precipitates on the seed crystals located in the colder region in a kind of homoepitaxial growth process. The design of a typical high-pressure growth cell is shown in Figure 20.4.

20.2.3 Chemical Purity and Classification

The HPHT growth environment contains various chemical elements besides the indispensable carbon. Their relevance for the final crystal quality strongly depends on (i) the incorporation coefficient and (ii) their impact on the physical properties of the crystals.

The elements that form the solvent catalyst are present in stoichiometric concentrations at the liquid–solid interface of the growing diamonds. Their incorporation is, however, rather limited which is usually attributed to the low solubility in the dense crystal lattice, i.e. the extraordinary small covalent radius of sp^3-carbon which results in the highest atom number density of all solid materials (1.77×10^{23} cm^{-3}) [20]. Nevertheless, traces of Ni, Co, and various other elements are found in dispersed form in HPHT grown diamond giving rise to a huge number of color centers [21], some of them having attracted the interest of the quantum optics community [22].

Light elements like H, B, N are easily inserted into the diamond crystal lattice. Specifically, nitrogen incorporates over a large range of concentrations either as isolated substitutional point defect (called "C" center) or aggregated forming different complex centers (like "A" and "B" centers) [23, 24]. Both, absolute

Table 20.1 Classification of diamond.

Type	I			II	
	IaA	IaB	Ib	IIa	IIb
[N] in ppm	>1			<1	
N center	A	B	C		
[B]	Low	Low	Low	Low	Dominant
Electrical resistance	Very high	Very high	Very high	Very high	Low
Color			Yellow		Blue

The identification of the different types of centers in type I crystals is done via their signature in IR spectra. In type II crystals, nitrogen is below the detection threshold in IR. In IIb crystals, the concentration of uncompensated boron is high enough to turn them semiconducting.

concentration and type of involved complexes are classification criteria to assign the crystals to different types. The distinguishing criterion between type I and II is a critical nitrogen concentration of about 1 ppm which represents the detection threshold for nitrogen related defects by infrared (IR) spectroscopy [25]. For a classification of different types of diamond see Table 20.1.

Substitutional nitrogen gives rise to a yellow color (pale yellow for 5–10 ppm, golden yellow for 50–100 ppm, increasingly greener for high concentrations). In the case of boron, 1 ppm of B produce a light blue, 10 ppm a deep blue color [3]. Doping with concentrations approaching the metal-to-insulator transition (≈2500 ppm) [26] turns the crystals increasingly black.

Sources responsible for nitrogen incorporation during HPHT synthesis are nitrogen impurities in the solvent–catalyst metals and the carbon source material as well as gas inclusions in the growth cell [27]. Thus, the usual industrial diamond crystals are yellow as shown in Figure 20.5 (photos in upper row). To synthesize colorless high-purity crystals nitrogen getters like Al, Ti, and Zr are added. For the minimization of the boron content high-purity carbon sources are required. Finally, for the avoidance of Ni incorporation, high-purity Fe–Co provides a viable strategy. Examples of colorless IIa-type HPHT diamond crystals with impurity concentrations [N], [B], [Ni] < 0.1 ppm obtained in this way are shown Figure 20.5 (photos in the bottom row).

20.2.4 Morphology and Structural Quality

Crystal growth under HPHT conditions is generally a three-dimensional process that can involve several different families of crystallographic planes. For usual process parameters, the crystal habit is dominated by {111} and {100} facets. It can vary from purely cubic over cubo-octahedral to octahedral shape. With lower probability {110}, {113}, {117}, and even higher indexed planes can occur [29, 30]. Their appearance is controlled by the *P*–*T* conditions and the composition of the solvent–catalyst. Higher temperatures generally favor the formation of octahedral crystals [30]. Examples

Figure 20.5 Cubo-octahedral-shaped diamond crystals grown by the temperature gradient method at different temperatures. Substitutional nitrogen (≈100 ppm) causes the yellow color of the Ib-type crystals in the upper row. In the type IIa crystals in the lower row, the nitrogen concentration is <0.1 ppm. Source: Reprinted with permission from Sumiya and Tamasaku [28]. © 2012 The Japan Society of Applied Physics.

of various cubo-octahedral-shaped crystals which confirm this trend are shown in Figure 20.5.

The schema in the bottom of Figure 20.5 describes the development of the crystal shape starting from (001)-oriented seeds. With higher temperatures the ratio v_{001}/v_{111} between growth rates along the crystallographic ⟨100⟩ and ⟨111⟩ directions increases thus causing a relative decrease in size of the {100} cube facets as compared to {111} faces. The crystal habit changes toward octahedron shape.

The growth sectors do not only differ in growth velocity but also in the uptake of impurities and the incorporation of structural defects. This has the important consequence that plates cut out of HPHT crystals typically show clearly distinguishable regions with different color (in the case of Ib-type samples) and structural defects (like dislocation densities) which reflect the former growth sectors. {100} growth sectors typically show the highest structural quality facilitating under optimum conditions virtually extended dislocation-free regions (see Figure 20.6).

20.2.5 State of the Art in Crystal Size

Large synthetic single crystals like the yellow 9 ct crystal manufactured by Sumitomo around 1990 [31] and the yellow 34.8 ct crystal produced by De Beers in a 600 hours process and first presented 1992 at the Japan International Machine Tool

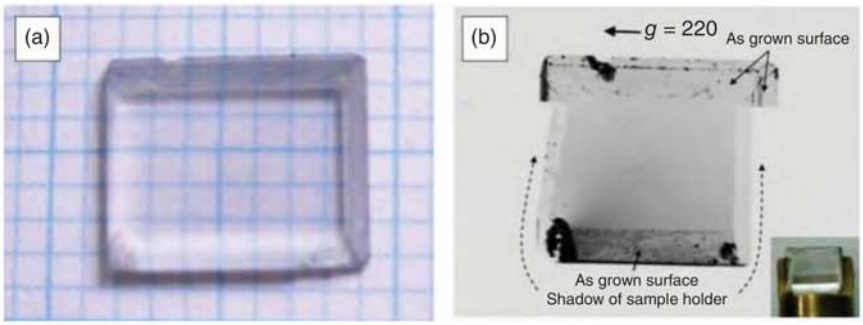

Figure 20.6 Diamond plate cut in (001) orientation from a IIa-type HPHT crystal. (a) Optical image and (b) transmission X-ray topograph. Crystal size: $7.5 \times 6 \times 0.7\ mm^3$. Source: Reprinted with permission from Sumiya and Tamasaku [28]. © 2012 The Japan Society of Applied Physics.

Fair in Tokyo [32] were rare objects manufactured in laboratory scale experiments. In 2012, Sumitomo described 8–10 ct large crystals of type IIa which facilitated the cutting of (001)-oriented slices with an edge length of 12 mm [28]. In the subsequent years, the St. Petersburg-based company New Diamond Technology (NDT) pushed the limit for IIa-type crystals to ever-larger size using the Chinese technology shown in Figure 20.3c. At the ICDCM diamond conference 2017 in Gothenburg [17], crystals with a size up to 61 ct (as-grown) were presented in the talk given by A. Katrusha and plates of $15 \times 15\ mm^2$ are commercially available on the company website (01/2020) (http://ndtcompany.com/products/single_crystal_diamond_plates). Evaluation of the dislocation densities revealed moderate values on the order of $10^3\ cm^{-2}$ [33].

20.2.6 Boron Doping

Boron doping to turn the crystals p-type semiconducting was successfully achieved already in the early days of HPHT research [34]. In contrast, the reliable realization of n-type conductivity, which is nowadays routinely done by in situ phosphorous doping during CVD diamond growth [35], is still a challenge for HPHT synthesis [36].

For the synthesis of boron-doped diamond, boron or boron-containing compounds are added to the HPHT growth system. Since substitutional nitrogen acts as a 1.7 eV deep donor, nitrogen getters like for the synthesis of colorless IIa crystals are needed to avoid a compensation of the B acceptors. In this way, boron-doped diamond with B concentrations ranging from few ppb to several thousand parts per million [37] have been synthesized. In heavily boron-doped diamond samples from the HPHT technique, superconductivity has been observed in 2004 [38].

Boron incorporation is highly growth sector dependent. Blank et al. report 6–8 times higher concentrations of uncompensated acceptors in {111} than in {100} growth sectors [39]. As a consequence, electronic properties will drastically vary

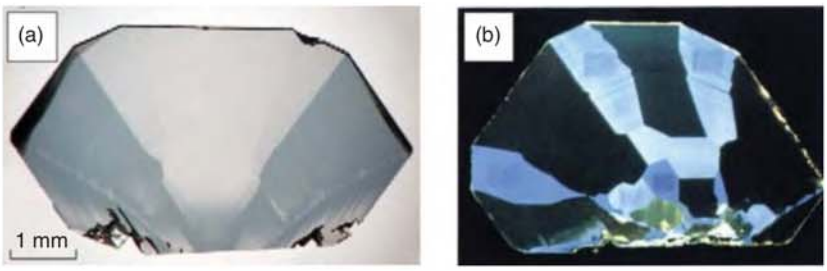

Figure 20.7 Boron-doped diamond crystals grown by the HPHT technique. The variations are due to drastic differences in incorporation efficiency for different growth sectors.
(a) Transmission optical micrograph of a 397-μm-thick slab cut parallel to (110).
(b) Cathodoluminescence topograph of a sample taken at room temperature looking along [110]. Source: (a) Reprinted with permission from Blank et al. [39]. © 2007 Elsevier.
(b) Reprinted with permission from Burns et al. [40]. © 1990 Elsevier.

laterally when substrates are employed which were grown on different sectors as for the examples shown in Figure 20.7.

In the context of high-power electronics, boron-doped substrates are of interest as growth substrates for the fabrication of vertical Schottky barrier [41] or p–i–n diodes [42] by subsequent CVD growth on top.

20.3 Chemical Vapor Deposition (CVD)

20.3.1 Basic Principles

20.3.1.1 The Mechanism of Diamond Growth by CVD

In contrast to the HPHT method, growth by CVD takes place at pressures of few to several hundred millibars and temperatures of 500–1200 °C. Under these conditions, graphite is the stable allotrope of carbon. Diamond formation is therefore controlled by kinetics instead of thermodynamics.

Atomic hydrogen plays the central role in CVD diamond growth, and the major technological challenge consists in its efficient generation and transport to the growth surface. Within the standard model, atomic hydrogen participates in the following crucial processes:

(a) Hydrogen atoms terminate the surface sp^3 bonds, thus stabilizing the diamond lattice and preventing a rearrangement to graphitic sp^2 carbon.
(b) Molecular hydrogen is dissociated into atoms that react with the carbon-containing molecules creating a complex mixture of hydrocarbon species. These include also the reactive hydrocarbon radicals that are required for the surface growth processes. So the whole gas phase chemistry is driven and controlled by the atomic hydrogen.
(c) At the diamond surface, the H radicals abstract adsorbed surface H-atoms, thus creating dangling bonds which can act as sites for the adsorption of C_xH_y growth species.

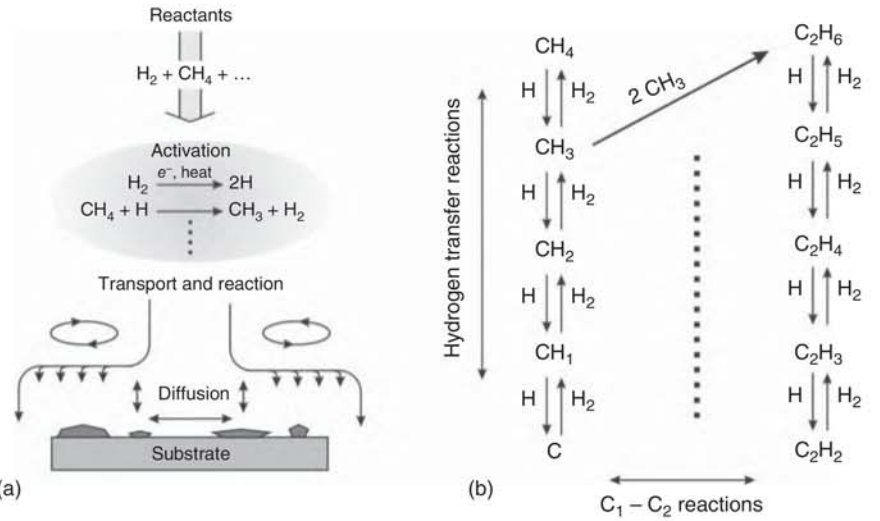

Figure 20.8 (a) A simple schema showing the principal elements of CVD diamond growth: process gases flowing into the reactor, activation of the reactants by thermal or plasma processes which induces the complex gas phase processes, transport of the activated species to the growth surface by convection and diffusion, and finally the surface growth processes. Source: Butler and Woodin [43, 44]. © 2017, Royal Society. (b) The principal gas phase reactions in a CH_4/H_2 feed gas mixture involve "H-shifting" reactions [45] amongst different C_1 or C_2 species and the bimolecular hydrocarbon reactions forming C_2 and higher species [43].

(d) Finally, to integrate the new carbon atom into the crystal lattice, the adsorbed hydrocarbon species (e.g. CH_3) have to be dehydrogenated in several consecutive hydrogen abstraction steps.

The general features of CVD diamond processes, as schematically summarized in Figure 20.8, comprise the flow of gaseous reactants typically containing 90–99% of hydrogen and 1–10% of a hydrocarbon gas like methane into a reactor where they are activated thermally or via a plasma to generate atomic hydrogen and C_xH_y species. These are transported via convection and diffusion to the growing diamond surface where they participate in the diamond growth processes and deliver the required carbon.

The gas activation processes dissociate the molecular hydrogen into atoms. These react with the inert hydrocarbon feed gas molecules like CH_4 and transform them into a complex mixture of other hydrocarbon species including reactive carbon-containing radicals which can act as growth species. The schema in Figure 20.8b shows the fast H-shifting reactions with C_xH_y ($x = 1, 2$) species which cause abstraction or addition of atomic hydrogen and indicates various transfer reactions between C_1 and C_2. Even for the simple CH_4/H_2 gas composition, 20–30 species and more than 100 reactions have to be considered to describe the chemistry adequately [46]. At high pressures and gas temperatures, C_2H_2 is the dominating species in the gas volume [45, 47].

A large number of studies have been devoted to the identification of the growth species [48] by evaluating correlations between growth rate and the concentrations of reactive species in direct vicinity to the crystal surface. Furthermore, the absolute arrival rates have to be high enough to deliver sufficient carbon, and the reactivity of the species has to be taken into account (which directly rules out CH_4). Most studies revealed a major role of CH_3. Under certain process and excitation conditions, C_2H_2 can yield relevant contributions.

Using the model proposed by Harris and Goodwin [49] in a simplified version which considers only two gas phase species involved in the growth processes (atomic hydrogen H and CH_3) and few surface reactions [50], it was possible to simulate the experimentally obtained growth rates consistently over more than 2 orders of magnitude [50, 51]. This result strongly supports CH_3 as dominating growth species under typical process conditions.

20.3.1.2 Gas Mixtures for Diamond CVD

A couple of variations and alternatives to the simple CH_4/H_2 gas mixtures have been explored. These included other carbon sources (larger hydrocarbon molecules, fullerenes), alternative chemistries based on halogens instead of hydrogen [52], the addition of oxygen containing molecules, and finally noble gases (Ar).

For the deposition of nanocrystalline diamond (NCD) and ultrananocrystalline diamond (UNCD) films, argon has been added [53] or pure Ar/CH_4 gas mixtures have been used [54]. In the context of high-quality single crystal growth, addition of Ar reduces the thermal conductivity of the gas mixture in plasma-activated processes thus increasing gas temperature, hydrogen dissociation, and as a consequence the growth rate [55].

Technologically most relevant is the addition of stoichiometric quantities of oxygen. With their C–H–O diagram, Bachmann et al. have introduced a general concept for the selection of gas mixtures appropriate for the growth of diamond (see Figure 20.9) [56].

Each point in the C–H–O triangle corresponds to a defined stoichiometric ratio [C]:[H]:[O]. The corners define the pure elements (100%), along the edges there is a continuous variation in the composition of only two elements. The middle of the C–O edge corresponds to CO. Only within a narrow region around the CO line, diamond growth is possible. Above this range, the excess of carbon causes the deposition of non-diamond graphitic phases, below etching prevails. The applicability of this diagram is based on the fact that the chemistry is independent of the specific precursors supplied into the growth reactor.

Based on the first data set, the authors predicted the wedge-shaped region (bright red in Figure 20.9). Subsequent refinement yielded the lens-shaped area (dark red in Figure 20.9). Posterior experiments by other authors at high gas pressures, high substrate temperatures, and especially during homoepitaxial deposition revealed that high-quality diamond can be grown with CH_4 concentrations up to 20% [58], proving that the diamond domain can be significantly wider around the H corner under specific conditions. As a consequence, the C–H–O diagram should only be taken as a useful but rough guideline.

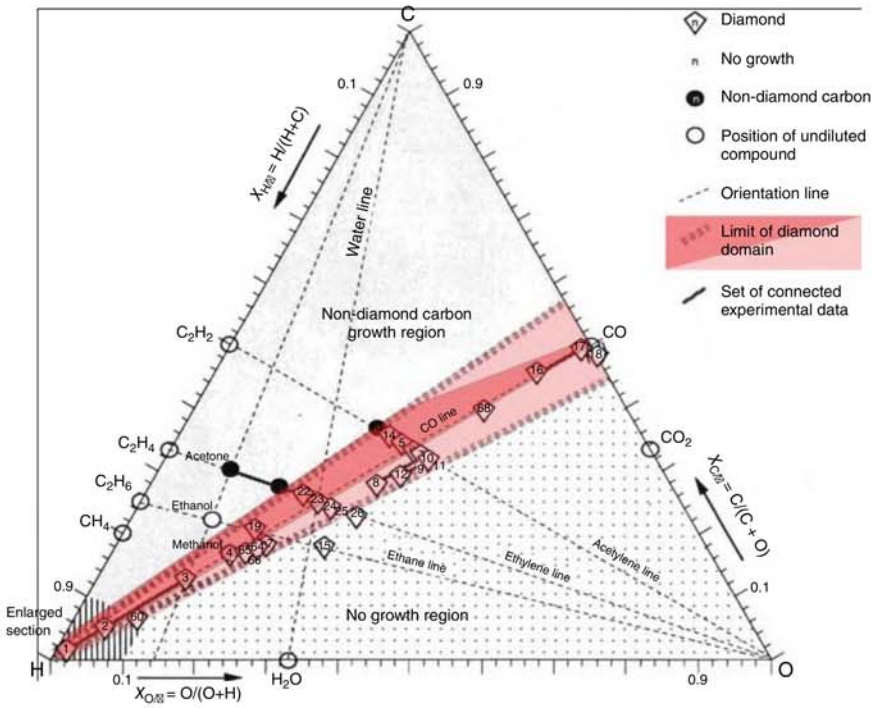

Figure 20.9 C–H–O diagram for the deposition of diamond. Highlighted in red are the regions of gas compositions appropriate for diamond growth. Bright red: original wedge-shaped region [56]. Dark red: refined data [57]. Source: Reprinted with permission from Bachmann et al. [56] and Bachmann et al. [57]. © 1991 Elsevier.

20.3.1.3 The Role of Trace Gases

To avoid impurities that can modify the optical properties or induce electronically active defect states, ultra-pure gases (99.9999% and better) are used in the synthesis of electronic-grade diamond material, and all reactor components are selected carefully. Prominent examples of detrimental impurities are nitrogen that acts as a 1.7 eV deep donor and boron that forms a 0.37 eV deep acceptor level in diamond. Besides this, their presence in trace concentrations in the gas phase can modify the growth velocity.

Nitrogen addition at ppm level can drastically accelerate diamond growth. For polycrystalline diamond, an increase by a factor of 6 was reported by addition of 25 ppm nitrogen [59]. For homoepitaxial growth on (001)-oriented crystals, recent experiments in the author's lab revealed factors of up to 13 for 400 ppm nitrogen in the process gas [60]. The effect is growth sector dependent and strongest on {100} faces [61]. This has a pronounced impact on the granularity and promotes the formation of textures with ⟨100⟩ fiber axis in polycrystalline films [62]. Furthermore, addition of nitrogen represents an efficient and widely used strategy to stabilize homoepitaxial growth on (001) substrates by suppressing non-epitaxial crystallites like twins.

The strength of the nitrogen effect is quite sensitive to the method used for the activation of the gas phase: While low ppm levels are sufficient in CVD reactors with plasma activation of the gas phase, hot filament (HF) methods require significantly higher concentrations (500–4000 ppm at 1% CH_4 in H_2) [63].

Concerning the responsible mechanisms, the low absolute concentrations that are sufficient to induce measurable effects exclude gas phase processes as a relevant explanation. Instead, catalytic effects directly at the growth surface yield a reasonable explanation [64].

Growth acceleration by nitrogen is extremely sensitive to the presence of even lower concentrations of boron [65]. In microwave (MW) reactors, below a critical threshold of $[N]/[B] \approx 10^3$, the effect of nitrogen is completely canceled by boron which acts as a kind of catalyst poison.

20.3.1.4 Experimental Setups

A crucial step toward technologically relevant growth rates in diamond CVD was the awareness that substrate surface temperature and gas phase temperature have to be decoupled so that the latter can be significantly higher [66]. Thereupon, various diamond CVD techniques have been developed which mainly differ in the method of gas phase activation with strong implications on the scalability to larger areas and growth rates. Four of the technologically most relevant techniques are schematically shown in Figure 20.10.

Hot Filament (HF) CVD In the hot filament method, the source gases interact with a hot surface which is usually a thin wire of refractory metals like Ta, W, or Re. The gases are decomposed into hydrocarbon radicals and atomic hydrogen which are transported by diffusion and convection to the substrate surface. Typical operating conditions are a pressure in the range of 1–100 mbar, a substrate temperature of 600–1200 °C, filament temperatures of 2000–2600 °C, a distance filament–substrate of 1–20 mm, and feed gas mixtures of 0.1–7% hydrocarbons in H_2 [67]. Oxygen can be added optionally (typically in the range of 0–3%). For very high filament temperatures and methane concentrations, growth rates of 10 μm/h are feasible [68]. However, these conditions limit filament lifetime and enhance incorporation of metal atoms from the filament into the films. Concentrations in the 0.1 at% range have been measured even for moderate filament temperatures [69]. Thus, in production setups, lower filament temperatures and growth rates in the 1 μm/h range are common. The huge advantage of the method is its comparatively easy scalability via extended arrays of parallel wires to large areas of up to $50 \times 100\,cm^2$ [70] and the feasibility to coat 3D bodies. Modifications of the technique are forced convection of the gas to accelerate the transport of the reactive species to the growth surface as well as bias assistance to accelerate the electrons emitted from the filament and to ignite a plasma thus enhancing the activation of the gas phase and increasing the growth rate to 3–5 μm/h [71].

DC-Plasma CVD The direct current (DC) plasma technique is a rather simple method to generate an electrical discharge and to ignite a plasma. The schema in

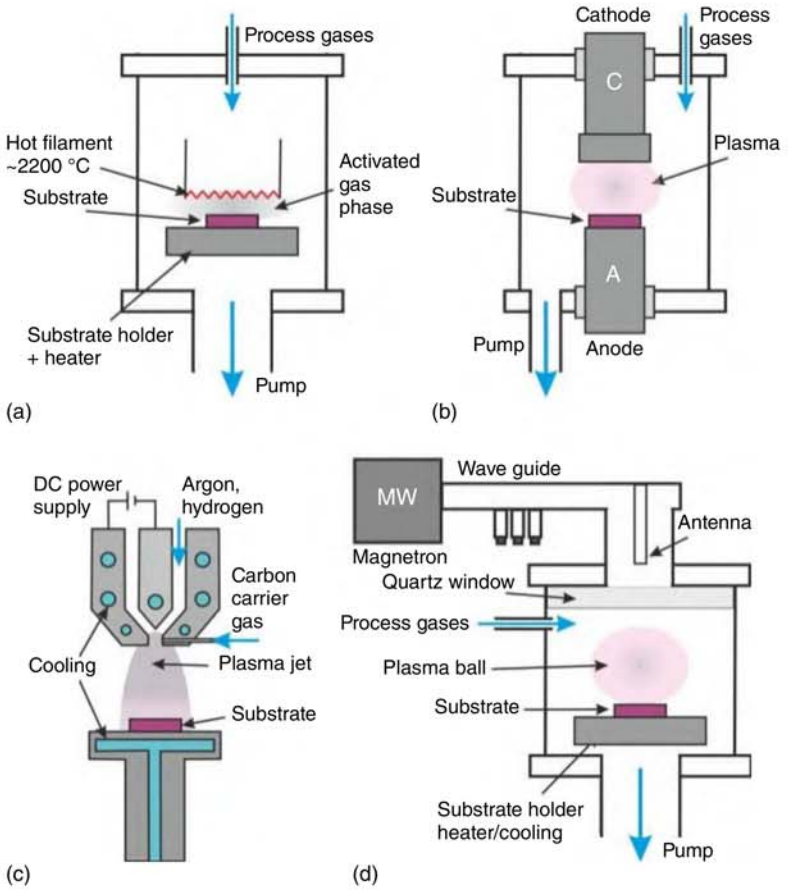

Figure 20.10 Schemata of different reactors: (a) hot filament CVD, (b) DC plasma CVD, (c) DC plasma jet CVD, (d) microwave plasma CVD.

Figure 20.10b shows the cylindrical cathode and anode with the DC power supply. The substrate is placed on the anode. If placed on the cathode, amorphous carbon is deposited [72] due to the intense bombardment with positive ions. The technique shows its greatest potential at high gas pressures: for 200 mbar and current densities of >10 A/cm^2, gas temperatures of ≈6000 °C with growth rates of 250 µm/h were reported. However, with increasing pressure, the deposition area shrinks severely (1–2 cm^2) [73]. In the meantime, scaling to 8-in. wafer size with growth rates of 9 µm/h for the deposition of polycrystalline diamond has been reported [74].

DC-Plasma Jet CVD A further increase in the pressure in a DC-plasma system can be achieved by separating the activation region from the diamond growth region as for the plasma torch [73]. In the DC-plasma jet (see schema in Figure 20.10c) that can operate up to atmospheric pressure a gas mixture of argon and hydrogen is ionized and heated to temperatures of >5000 °C by a DC arc discharge before it leaves the plasma generator through a nozzle and expands into the reactor vessel which

can be at significantly lower pressure. The carbon carrier gas is typically introduced into the gas mixture close to the gas exit. Growth rates of up to 930 µm/h have been reported for this technique [75]. The restriction to small deposition areas has been overcome by application of magnetic fields that induce a rotation of the arc root and by an appropriate design of the gas flow facilitating growth rates of 40–50 µm/h over an area of 110 mm in diameter [76]. Modifications of the plasma jet operate with inductively coupled radio-frequency (RF) or microwave (MW) excitation [77]. Both are electrodeless which means a lower risk of contamination by electrode material.

Microwave Plasma Chemical Vapor Deposition (MWPCVD) In microwave plasma chemical vapor deposition (MWPCVD), microwaves are fed into a reactor vessel through a dielectric window (typically quartz). Inside the reactor, at reduced pressure, an electrical breakdown occurs, and a plasma is ignited in the region of maximum electric field strength. The substrate is placed close to this position. After ignition of the discharge, the pressure can be increased and growth typically occurs at pressures of 20–400 mbar.

The first MWPCVD experiments were reported by Japanese researchers at the National Institute for Research in Inorganic Materials (NIRIM) in 1983 [78]. The used frequency of 2.45 GHz was identical to the operating frequency of the standard microwave oven present in virtually every kitchen. The original NIRIM-type reactor consisted of a quartz tube that was fed through the broad side of a fundamental mode rectangular metal wave guide. Inside the tube in the waveguide, a plasma was ignited. The setup is still used in the research area, but the schema shown in Figure 20.10d is more common: here, the microwaves generated by the magnetron propagate in the waveguide to the reactor where they are coupled into the chamber through a dielectric window (quartz). The inner chamber diameter was chosen so that it can sustain only one microwave radial mode at this frequency. The TE_{10} mode, which is the fundamental propagation mode in the waveguide, is converted into the cylindrical TM_{01} mode inside the reactor [79].

This reactor type originally developed and commercialized by Applied Science and Technology, Inc. (ASTeX, USA), now continued by Seki Diamond Systems (Cornes Technologies Ltd., Japan), has been used extensively in the research area. Substrates with a diameter up to 100 mm can be inserted and coated at low pressure (several 10 mbar). The setup has also successfully been applied to grow single crystals at pressures of 300 Torr with growth rates of 165 µm/h and final thicknesses of up to 18 mm [80].

Several alternative reactor designs based on the 2.45 GHz microwave frequency have been developed in the following. These comprise the overmoded cavity plasma reactor by ASTeX ("clamshell design") [79], the ellipsoidal plasma reactor developed by the Fraunhofer Institute [81] and the cylindrical resonator with annular slots (CYRANNUS) design commercialized by the Innovative Plasma Systems GmbH (www.iplas.de). The concepts for the coupling of the microwaves of the different reactors are shown in Figure 20.11.

Due to its ≈2.7 times larger wavelength, 915 MHz was chosen to scale the three reactor types (Figure 20.11b–d) to larger areas and higher absolute power. In

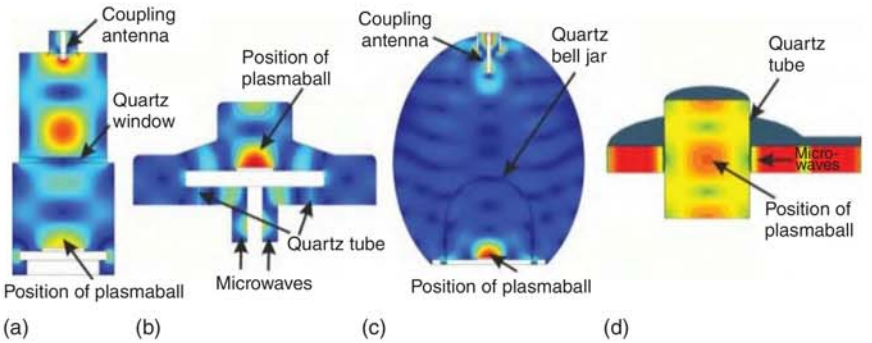

Figure 20.11 Simulations of the electric field distribution for different microwave reactor geometries. Depending on the design, the quartz windows through which the microwaves enter the reactors have the shape of a plate, a bell jar, or a tube. The field maxima (yellow-red) inside the reactors indicate where the dielectric breakdown will occur and the plasma ball will form. Ideal pressure conditions for the ignition are on the order of 10 mbar. Atmospheric pressure outside the reactor vessel prevents discharge formation in the waveguide or at the antenna. (a) The classical ASTeX reactor as schematically indicated in Figure 20.10d, (b) the overmoded ASTeX reactor, (c) the ellipsoidal reactor, and (d) the CYRANNUS reactor (simulated without substrate holder which is inserted from the bottom of the quartz tube). Source: Adapted with permission from Silva et al. [82]. © 2009 Institute of Physics IOP Publishing.

the opposite direction, i.e. toward higher frequency, millimeter waves of 30 GHz gyrotrons have been used to generate a plasma above the substrate by four or two crossing beams [83, 84]. The specific benefit of 30 GHz radiation is the higher penetration depth of the microwave field which facilitates high plasma densities (electron densities $>10^{13}$ cm^{-3}).

Besides the described technologically most relevant techniques, further approaches have been explored like the combustion flame growth (oxygen–acetylene torch) [85] or the photon plasmatron that uses CO_2 laser radiation to ignite an atmospheric plasma working even in air without reactor chamber [86, 87].

20.3.1.5 Growth Rate and Gas Temperature

A comparison between all the different deposition techniques yields the first conclusion that high growth rates require high gas temperatures in the activation zone (see Figure 20.12). In the case of MW activation, an increase in pressure at constant input power automatically results in a shrinking plasma ball and an increasing plasma temperature. For the transition from ≈50 mbar to ≈400 mbar, the absorbed power density changes from ≈5–10 W/cm^3 to 1000 W/cm^3 accompanied by a rise in H and CH_3 radical density by factors of 1000 and 10, respectively [51, 88]. This stronger activation of the gas phase, specifically the increase in atomic hydrogen, widens the range of useful methane concentrations up to 20% and facilitates growth well above 1000 °C where the density of dangling bonds which are adsorption sites for growth species is higher [44]. The combined action of all these effects explains the huge benefit of high pressures beyond the simple gas kinetic increase in arrival

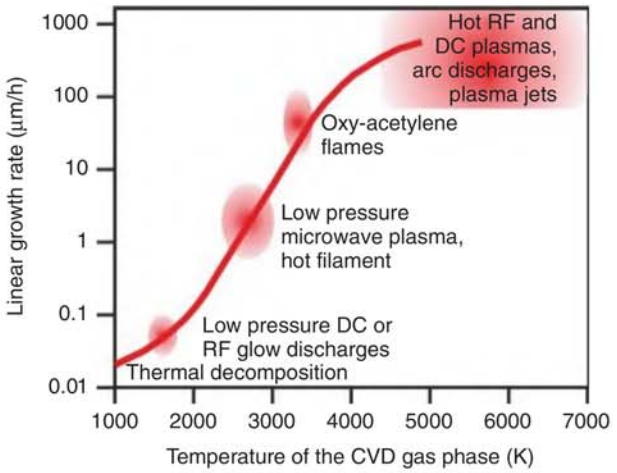

Figure 20.12 Correlation between temperature of the gas phase in the activation zone and typical growth rates for different activation methods. Source: Redrawn with permission from Bachmann et al. [56]. © 1991 Elsevier.

rate of particles at the surface [89]. To keep the size of the deposition area constant, the input power has to be increased appropriately.

In the field of semiconductor materials, purity is a further aspect of major relevance. Here the activation with the hot filament, besides its limited growth rates, shows major disadvantages. Among the plasma techniques, contactless concepts like MW activation are preferred. In the meantime, high-power 915 MHz reactors facilitate scaling of the deposition area to several 10 cm in diameter in combination with growth rates >10 µm/h so that they offer an attractive technical solution for the commercial production of high-quality diamond wafers.

20.3.1.6 Nucleation by Seeding

Diamond growth can immediately start on existing diamond surfaces. This also works on c-BN with diamond grains growing immediately with an epitaxial alignment [90]. On surfaces of other materials, the density of grains is usually very low. Nucleation occurs only sparsely and in an uncontrolled way at irregularities. This behavior is attributed to a high nucleation barrier as a consequence of a high surface energy [91]. For technical purposes like the coating of technical parts to form a protective layer, scratching with diamond powder is a well-established method. Many different variations of this concept have been explored, but in the end, diamond debris was always left on the surface that provided seeds for the subsequent homoepitaxial growth [92]. By the use of nanodiamonds, e.g., from the detonation synthesis, maximum nucleation densities $>10^{11}\,cm^{-2}$ have been obtained [93].

20.3.1.7 Bias-Enhanced Nucleation (BEN)

Real nucleation of a new phase is achieved by the bias-enhanced nucleation (BEN) procedure [94]. It works on different materials like elemental semiconductors

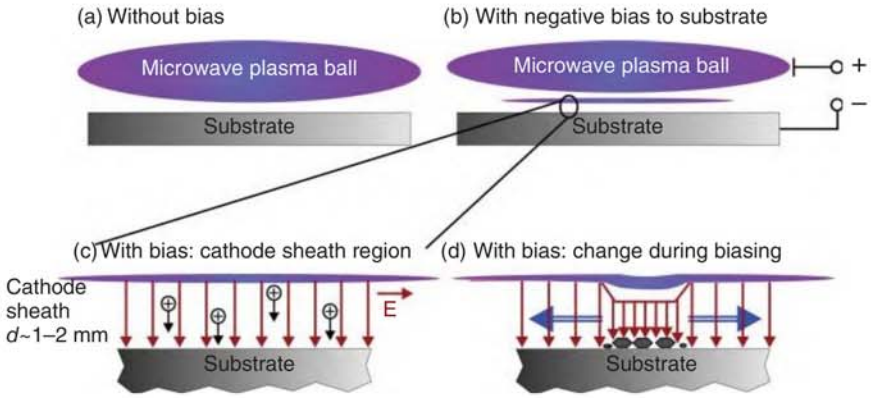

Figure 20.13 Schema of (a) a microwave plasma discharge above a substrate and (b) its modification during BEN. (c) The high electrical field in the cathode region accelerates positive ions toward the surface. (d) The local field enhancement above diamond-coated regions as typically observed for nucleation on Si (not on Ir). Source: Reprinted with permission from Schreck [106] © 2014 Elsevier.

(Si [94, 95]) and composite semiconductors (SiC [96]), metal carbides (TiC [97]), and pure metals (Mo [98], Ni [99, 100], Re [101], Ir [102]). In most cases, a carbide is formed at the surface during the BEN treatment, and the real nucleation finally occurs on this interlayer. For Ir, this scenario can definitely be ruled out.

The basic principle of the BEN procedure consists in the application of a negative bias voltage of 100–300 V to the substrate in MW plasma, in HF [103] or in DC plasma setups [102]. Under these conditions, the surface in contact with the plasma will be bombarded with positive ions. Few studies have been performed with positive bias. Some enhancement in nucleation density was found [104], but the effect was much weaker and nearly all the subsequent work was focused on negative bias.

In an MW plasma reactor, as shown schematically in Figure 20.10d, a negative bias voltage is applied to the substrate holder while the metallic chamber walls define the grounded reference. Alternatively, the substrate may stay at ground potential, and a positive voltage is applied to the plasma ball via an electrode, for example, a metal ring [105].

Figure 20.13 schematically shows the changes in the visible shape of the discharge that occur after application of a negative bias voltage to the substrate holder. Few millimeters above the cathode, a thin luminous layer separated by a dark space appears (Figure 20.13b). It resembles the negative glow in a classical glow discharge [107]. Measurements of the Stark splitting for the hydrogen Balmer lines directly above the biased substrate by optical emission spectroscopy (OES) reveal a field strength of several kilovolts per centimeter thus confirming that most of the applied voltage drops in this narrow region [108]. As a consequence, positive ions are accelerated (Figure 20.13c). In spite of a gas kinetic mean free path on the order of 10 µm, they can reach kinetic energies up to >100 eV as determined experimentally [109].

The hyperthermal particles hit the surface and induce several effects: first, they cause electron emission. Second, they can activate surface processes, and third, they can be deposited on the surface or implanted shallowly below the surface. This "subplantation" is typically the key process for the majority of models explaining the diamond nucleation by BEN which will be discussed later in context with the heteroepitaxy of diamond on iridium.

During BEN, small diamond grains can be found on the substrate surface after a short incubation time [110]. On nearly all substrate materials (except iridium), these tiny crystals immediately start to grow during BEN gradually covering the surface with a closed layer of diamond. This change can be noticed by a drastic rise in the biasing current by up to an order of magnitude [108]. The current increase is attributed to the significantly higher electron emission coefficient of hydrogen terminated diamond with its negative electron affinity as compared to other common substrate materials. As a consequence, the space charge density, the electric field strength, and the ion bombardment above diamond-coated regions increase as highlighted in Figure 20.13d.

While this feedback on the current provides a sensitive indicator for the status of the nucleation process, it also has severe negative implications: the field enhancement at the rim of a diamond covered area accelerates the nucleation in the immediate neighborhood. Thus, nucleation typically occurs first either in the center or at the edge of the substrate (the latter when the substrate holder is coated with diamond). This spot will then work as a starting point for a growth front that rapidly moves across the whole substrate inducing quite some inhomogeneity. Furthermore, the harsh ion bombardment is detrimental for the crystal quality. It can gradually change the crystal orientation, progressively increases the mosaic spread or nucleate crystals with completely new orientation [111–113]. Continuous renucleation can be desirable in the case of nano- or ultrananocrystalline diamond layers [114]. However, for the synthesis of homogeneous heteroepitaxial diamond wafers, all these phenomena are absolutely undesirable. The great success of Ir is therefore based not only on the significantly better alignment but also on the very weak feedback process (see below).

20.3.2 Examples of Polycrystalline CVD Diamond Layers

Figure 20.14 shows the surface of various polycrystalline diamond films grown by MWPCVD. The grain size of sample Figure 20.14a is well below 1 µm, while the other two samples consist of micrometer size crystals. The planar {100} facets in Figure 20.14c indicate a pronounced ⟨100⟩ fiber texture [115]. For microcrystalline layers with a surface morphology similar to Figure 20.14b, usually a ⟨110⟩ fiber texture is found [116, 117]. This also holds for nanocrystalline films [117].

The formation of textures with different fiber axes starting from randomly oriented seeds or nuclei can conclusively be explained by the principle of evolutionary selection of specific crystallite orientations. This concept, first proposed by Van der Drift [118], was successfully transferred to the growth of polycrystalline diamond by the definition of a growth parameter $\alpha = \sqrt{3}\, v_{100}/v_{111}$

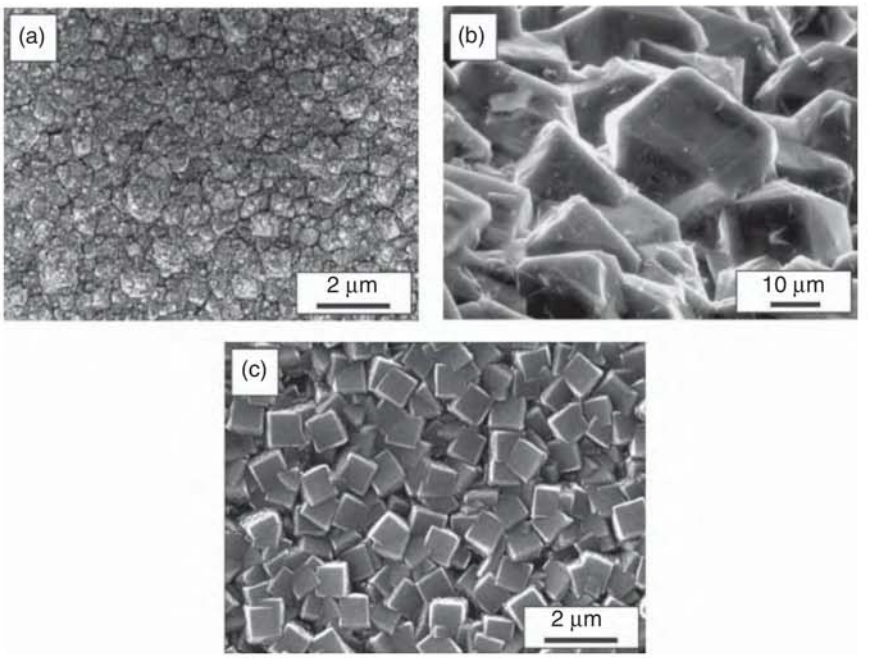

Figure 20.14 Scanning electron micrographs of the surface of polycrystalline diamond layers grown by MWPCVD. (a) Nanocrystalline, (b) polycrystalline, and (c) polycrystalline diamond film with pronounced ⟨100⟩ fiber texture.

with v_{100} and v_{111} the vertical growth rates on the {100} and {111} facets, respectively [115]. For cubo-octahedral-shaped crystals bounded only by {100} and {111} faces, it varies between 1 (cube) and 3 (octahedron). The parameter is also very useful to define regimes of stability toward twinning for homoepitaxial growth on these two growth sectors [119].

Besides these two low-Miller-index planes, in homoepitaxial growth on single crystal seeds stable {113} and {110} faces have been observed. For a correct modeling of the temporal development in 3D shape, it was therefore necessary to introduce two additional parameters $\beta = \sqrt{2}v_{100}/v_{110}$ and $\gamma = \sqrt{11}v_{100}/v_{113}$ [120, 121].

20.3.3 CVD Growth of Single Crystals

Polycrystalline diamond has been established in a range of high-tech applications such as wear-resistant coatings, cutting tools, heat spreaders, as well as optical components like windows for infrared, optical, UV, microwave, and X-ray radiation. However, in some fields, the polycrystalline nature prevents the devices from reaching the ultimate performance. This holds specifically for electronic devices which suffer from reduced charge carrier mobility [122] and detectors which show incomplete charge collection [123].

On the other hand, diamond single crystals synthesized by CVD methods have already demonstrated their unique potential in an impressing way by mobility

values of holes and electrons close to the theoretical limit [124, 125] and charge collection efficiencies close to unity [126]. As a consequence, strong efforts were directed toward a reproducible synthesis of high-quality single crystals in technologically relevant wafer size. Two fundamentally different approaches are currently being explored. The first one is based on homoepitaxial growth on high-quality crystals originally from the HPHT synthesis. It comprises typically the reuse of the substrates, the application of the CVD-grown crystals as new seeds, and various attempts to increase the lateral size. The second one uses heteroepitaxy on foreign substrates. Both concepts and their current state of the art will be described in the following.

20.3.4 Homoepitaxy

20.3.4.1 Homoepitaxial Growth on Different Crystals Faces

The initial seed for homoepitaxial growth is usually a HPHT crystal. It is cut as a plate with parallel faces and polished to provide a defined crystallographic plane for the CVD growth process. Already in the earliest experiment of homoepitaxial growth by MWPCVD on (001)-, (110)-, and (111)-oriented single crystals, it turned out that the different growth sectors behave completely different [127]. In subsequent studies, it was found that (110) growth surfaces show a trend to develop {111} microfacets [128] and (111) surfaces are prone to stacking faults and twinning [129]. The α-parameter concept described before provides a useful guide to identify growth conditions which suppress all twins on {100} faces and other conditions which facilitate the avoidance of penetration twins on {111} faces [119]. However, the contact twins for which the twin plane coincides with the growth surface cannot be avoided so easily.

In the meantime, dedicated growth strategies have been developed for (001), (110), (111), and (113) surfaces [130]. While growth on (001)-oriented crystals yields the highest crystal quality, incorporation of dopants is easier on the alternative crystal faces. Specifically, n-type doping by phosphorous is most efficient on (111). This face also offers the opportunity to incorporate nitrogen-vacancy (NV) centers with one preferential orientation, while (001) growth does not distinguish between four symmetry equivalent orientation variants.

An alternative strategy for an efficient avoidance of twins and other non-epitaxial crystallites consists in the deposition on vicinal faces which are tilted by few degrees away from the low Miller index crystal plane [131]. At a pressure of 200 mbar and 10% CH_4 in H_2 without any nitrogen a change of the off-axis angle from 0° to 6° increased the growth rate by a factor of 5 to ≈28 µm/h and completely suppressed non-epitaxial crystallites [58, 132]. This acceleration was attributed to the step flow growth mode, i.e., the lateral continuation of existing terrace edges without the necessity of nucleating new lattice planes as a rate-limiting step. The parameter space for the selection of growth conditions is widened, and there is no need for nitrogen as a measure to stabilize (001) growth. However, for small samples, the steps are consumed after a certain thickness and the surface gradually changes to lower off-axis angles closer to on-axis growth [58]. With larger wafer diameter, this restriction gets increasingly irrelevant.

20.3.4.2 Single Crystal Seed Recovery

HPHT single crystals of the type Ib with ≈100 ppm of substitutional nitrogen are still quite common as seeds for homoepitaxy. Colorless IIa crystals as shown in Figure 20.6 are also attractive growth substrates. In the meantime, CVD grown material itself is often used as new seeds for homoepitaxial deposition processes. In all these cases, reuse of the seeds is compulsory for an economically viable synthesis of diamond by homoepitaxy. It may also become relevant in the future for the duplication of crystals produced by heteroepitaxy. Currently, there exist two established methods and one novel technique.

Seed Recovery by Laser Cutting The standard procedure is based on horizontal slicing of the sample after the growth process with a laser to separate the grown part from the seed. The latter will be re-polished before it is applied as new seed in the next deposition run [133]. Nd:YAG pulse lasers working with the infrared fundamental line at 1064 nm or with the frequency doubled line at 532 nm are frequently used (www.bettonville.com). With larger lateral size a higher cutting depth is necessary and material loss due to the kerf increases. To cope with this problem, refined tools based on the guidance of a laser beam in a water jet have been developed (www.synova.ch) [134]. Limits for this new technique in terms of cutting depth are still under exploration.

Liftoff and Cloning of Seeds by Ion Implantation In an alternative approach, high-energy ion implantation is used to form a highly damaged sacrificial layer inside the sample that will later serve as predetermined breaking point. The method profits from the fact that the energy loss of ionized particles peaks at low energy (Bragg peak) causing maximum damage close to the end of the range. By careful choice of the implantation dose, amorphization can be achieved in the buried layer while the surface is still largely intact. In the original work, the top layer was split off after annealing to obtain a free standing few-micron-thick membrane [135]. Other researchers performed extended homoepitaxial growth before they induced the splitting and repeated the procedure to generate a set of nearly identical CVD crystals from one seed crystal [136]. Since the defect structure (specifically the density and distribution of threading dislocations) of all the grown crystals is quite similar and largely determined by the defect structure of the original seed, the term "cloning" has been introduced by the authors [137].

Liftoff by Epitaxial Lateral Overgrowth (ELO) Using SiO_2 Masks Recently, a new liftoff concept has been introduced [138]. It exploits the extremely low coefficient of thermal expansion (CTE) of SiO_2 which is even smaller than that of diamond. In a first step, a thin layer of SiO_2 is deposited on the surface of a seed crystal. This layer is then patterned by photolithography using a photoresist and reactive ion etching (RIE) to obtain an oxide mask with open windows and covered areas. In the subsequent epitaxial lateral overgrowth (ELO) process, diamond is grown homoepitaxially through the open windows and laterally across the SiO_2 regions until the mask is completely embedded in diamond. During cool down from deposition temperature

tensile stress develops in the diamond bridges, i.e., the diamond material that grew through the open windows of the mask. For small fill factor (FF), which is the fraction of surface area uncovered by mask material, the tensile stress is high enough to directly induce a cracking of the diamond bridges and a simple liftoff.

The ion implantation induced liftoff and the ELO process with SiO_2 masks are intrinsically scalable to wafer size.

20.3.4.3 Size Increase and Mosaic Growth

The quality of the homoepitaxial layer is usually not limited by small inclusions or point defects like chemical impurities in the seed crystals (provided that CVD growth is performed with ultrahigh purity gases). This rule does not apply to threading dislocations that end at the growth surface. They cannot simply stop at this interface but will be continued in the crystal lattice of the deposited material. Thus, HPHT crystals with ultralow dislocation density (down to zero) are the optimum starting point for the synthesis of CVD crystals. The intrinsic size limitations of the HPHT grown seeds stimulated activities to increase the sample size by the CVD processes. The three major concepts that have been explored comprise (i) the lateral expansion of the growth surface area by sophisticated growth protocols, (ii) the three dimensional enlargement by a sequence of growth steps on the {100} side faces [139], and (iii) the mosaic crystal wafer fabrication [137] (see Figure 20.15).

20.3.5 Heteroepitaxy

Heteroepitaxial deposition of a material on the surface of a foreign single crystal is a common approach when the synthesis of bulk crystals of the desired quality and size is not possible. Though some progress has been made during the last years, 3- or 4-in. size single crystal wafers synthesized by the HPHT technique do not appear feasible in the foreseeable future.

A viable heteroepitaxy system for diamond has to fulfill various requirements:

- a growth surface that facilitates the deposition of oriented diamond crystals, that withstands the harsh plasma environment and the required temperatures, and that finally guarantees a good adhesion
- a procedure for the generation of oriented diamond nuclei
- scalability of both, i.e., surface and nucleation procedure, to wafer size

20.3.5.1 Growth Substrates for Heteroepitaxy

The search for appropriate single crystal surfaces suitable for heteroepitaxial diamond growth started in the early 1990s. Figure 20.16 shows a selection of investigated substrates on which deposition of oriented diamond crystals has been achieved. The first three worked without any special treatment (a–c c-BN [90, 145] and Al_2O_3 [146]). The second group required a kind of seeding (d–f Ni [147] and Pt [148]). On the final three substrates, BEN was used to obtain epitaxial nucleation (g–i Si [91], 3C-SiC [96], and Ir [102]).

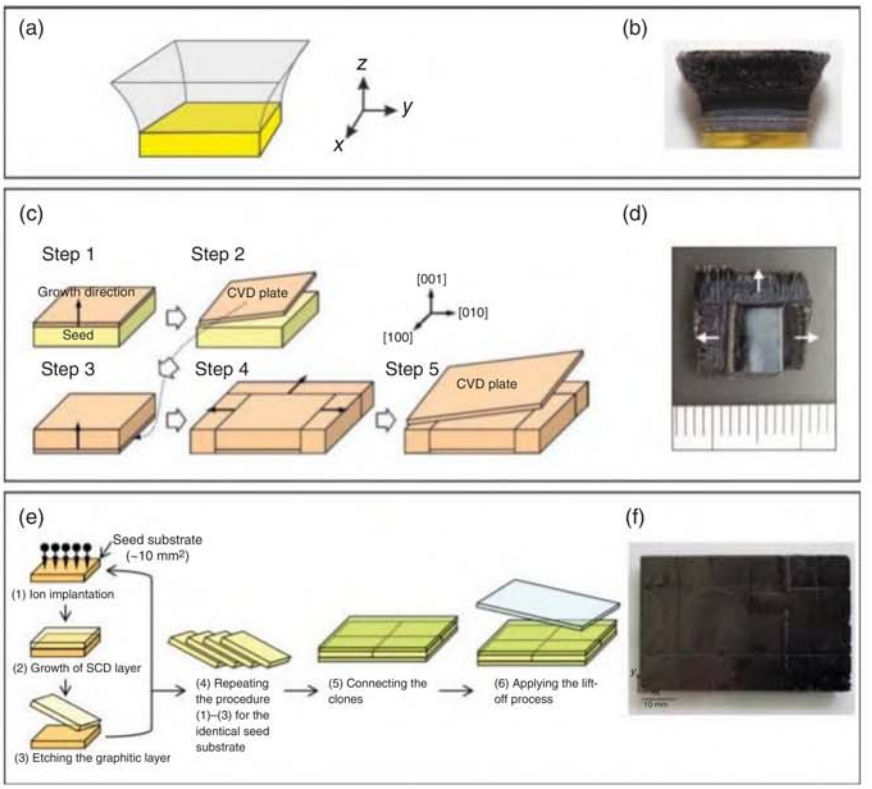

Figure 20.15 Different approaches for the lateral increase in crystal size by CVD growth. (a) Schema of lateral enlargement in *xy*-direction during growth in *z*-direction, (b) photo of a crystal with the growth surface enlarged by a factor of 2 (area of initial Ib crystal: 13.69 mm^2), (c) schema of sequential growth steps on {100} side faces, (d) photo of enlarged crystal ($12.6 \times 13.3 \times 3.7$ mm^3), (e) concept of liftoff and cloning by ion implantation followed by overgrowth of clones, (f) photo of a 2-in. mosaic wafer produced by overgrowth of a tiled arrangement of cloned crystals. Source: (b) Reprinted with permission from Nad et al. [140]. © 2016 AIP Publishing. (c, d) Reprinted with permission from Mokuno et al. [141]. © 2009 Elsevier. (e) Reprinted with permission from Yamada et al. [142]. © 2012 Elsevier. (f) Reprinted with permission from Yamada et al. [143]. © AIP Publishing.

While major activities were focused for several years on Si (and 3C-SiC), it finally turned out that this does not offer a viable route to real single crystals for the following reasons: high nucleation densities up to $\approx 10^{11}$ cm^{-2} could be obtained by BEN on Si, but typically only 10^8–10^9 cm^{-2} were epitaxially aligned. The initial mosaic spread of the oriented layers was on the order of $\Delta\omega \approx 10°$ (tilt) and $\Delta\varphi \approx 5$–$6°$ (twist). While appropriate growth steps facilitated the formation of closed layers consisting exclusively of aligned crystals and caused a significant decrease of $\Delta\omega$ down to few degrees, the azimuthal spread in orientation remained nearly unchanged [113]. Thus, small-angle grain boundaries persisted and prevented the transition to real single crystals. In addition, the immediate commencement of crystal growth after nucleation during BEN induced the feedback described in Figure 20.13d with all its

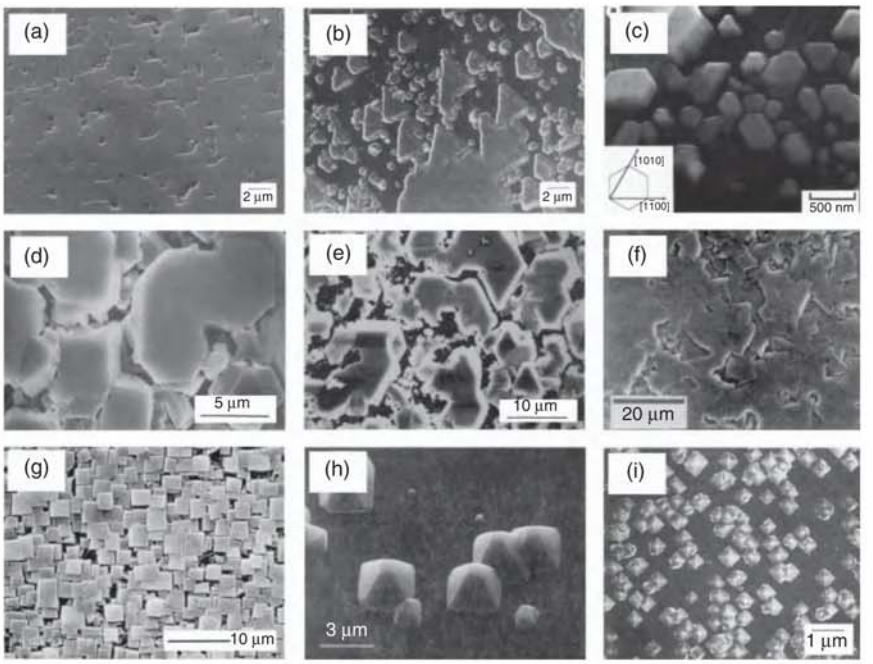

Figure 20.16 Heteroepitaxial diamond growth on different substrate materials: (a) c-BN(001), (b) c-BN(111), (c) Al_2O_3(0001), (d) Ni(001), (e) Ni(111), (f) Pt(111), (g) Si(001), (h) 3C-SiC(001), (i) Ir/MgO(001). Source: Reprinted with permission from Schreck [144]. © 2009 Wiley.

negative implications for the homogeneity. Furthermore, the harsh bombardment of the small grains caused that epitaxial orientation was only obtained within a defined process time window [149].

Iridium does not suffer from these drawbacks. The density of oriented grains shortly after BEN is up to 3×10^{11} cm^{-2}, the initial mosaic spread (600 nm thick layer) is $\Delta\omega$, $\Delta\varphi \approx 1°$, and the feedback is avoided since the grains cannot grow in z-direction due to the harsh ion bombardment (see next chapter).

20.3.5.2 Bias-Enhanced Nucleation on Iridium: Phenomenology and Mechanism

The most intriguing observations during a successful BEN process on Ir surfaces in contrast to all the materials studied before are the minimal changes in biasing current and surface morphology. Actually, scanning electron microscopy (SEM) facilitates clear identification of regions which contain diamond nuclei only by the in-lens detector which is specifically sensitive to work function contrasts. These regions were called "domains" [150].

The standard scenario for the processes occurring during BEN is summarized in Figure 20.17. Due to the harsh ion bombardment, the initially clean Ir surface (a) is quickly covered by a closed amorphous a-C:H layer with a thickness of 1–2 nm (b). This precursor layer is permanently etched by the atomic hydrogen

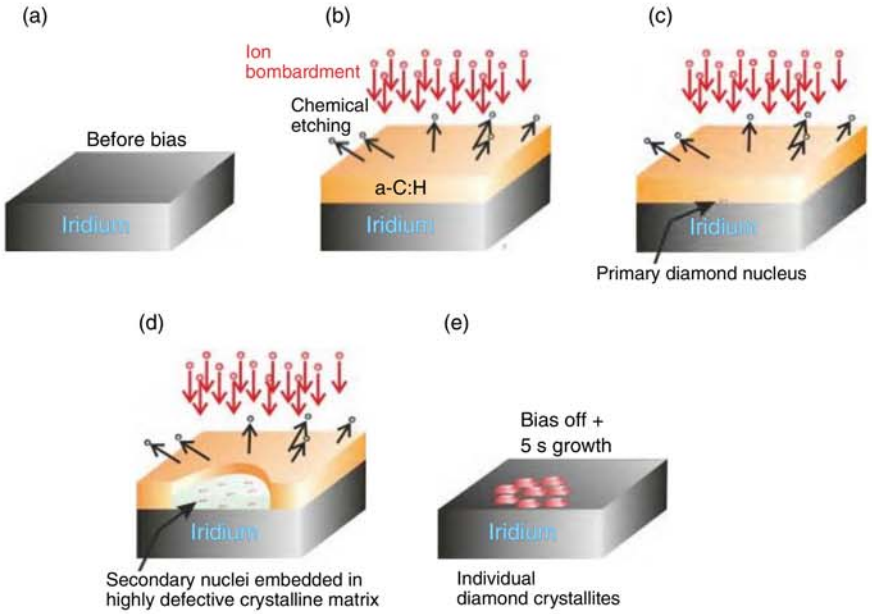

Figure 20.17 Schema describing the typical phenomenology of BEN on Ir. Source: Schreck et al. [151]. Licensed under CC BY 4.0. (a) Ir surface exposed to plasma before biasing. (b) An a-C:H layer is quickly formed after start of the BEN process. Dynamic equilibrium between deposition of hyperthermal particles and etching by atomic hydrogen limits layer thickness to a constant value of 1–2 nm. (c) Spontaneous formation of a primary diamond nucleus. (d) Lateral expansion of the domain and formation of secondary nuclei embedded in a highly defective crystalline matrix (domain), which is thinner than the surrounding a-C:H film. (e) During the first 5 s after termination of BEN, the atomic hydrogen etches completely the a-C:H precursor phase as well as the defective matrix in the domains. Simultaneously crystalline diamond grains with a height of 2 nm at a distance of 15–20 nm are formed.

leading to a dynamic equilibrium of deposition and etching. After some time, primary nuclei are spontaneously formed (c) and in their immediate neighborhood further nucleation events (secondary nuclei) occur (d). They are embedded in a highly defective crystalline matrix which is ≈1 nm thinner and denser than the surrounding precursor matrix. At this stage, the presence of carbon arranged in diamond crystal structure (i.e. the nuclei) can be detected by X-ray photoelectron diffraction (XPD) [152], by X-ray absorption near edge structure (XANES) spectroscopy [153], but not by high-resolution transmission electron microscopy (HRTEM). When the bias voltage is switched off (while the MW discharge is still on), the atomic hydrogen etches the whole a-C:H precursor layer completely within five seconds and the nuclei grow to 2-nm-high diamond grains (e) easily detectable by HRTEM [154].

The observations summarized in Figure 20.17 raise the crucial questions how nuclei are formed, why they are gathered in well-defined areas, and why growth of larger grains during BEN on Ir is prohibited in contrast to other substrate materials. The model of ion bombardment induced buried lateral growth (IBI-BLG) can

conclusively explain all the peculiarities that have been reported for BEN on Ir. The first step, i.e., the formation of the primary nucleus as indicated in Figure 20.17c, is a real nucleation event. It can be described, as recently proposed, in terms of a spontaneous precipitation of pure sp^3 clusters. These events occur in the dense a-C:H matrix with few of the clusters (1 in 10^4–10^6) being perfect diamond [155]. The nucleation is energetically favored directly at the interface to the iridium film in accordance with the observation that virtually all the nuclei are epitaxially oriented.

The atomic displacements and implantation of carbon atoms due to the ion bombardment does not only nucleate diamond, but it can also induce crystal growth. The basic effect of growth of tiny diamond crystals inside of carbon onions had been observed in former irradiation experiments with high-energy electrons [156] and ions [157]. Subsequent experiments revealed that this transformation is also possible for planar graphitic structures [158], and a model was developed to describe the kinetics of the involved processes quantitatively [159]. Extrapolation of this model suggests that the ion bombardment conditions during BEN on iridium facilitate an analogous growth now laterally over distances of several microns (see Figure 20.18).

Buried growth at the interface to the iridium – instead of the film surface where CVD growth usually takes place – is necessary to preserve the crystallinity and the perfect heteroepitaxial alignment. The particularly strong ion bombardment on Ir (higher bias voltages) as compared to other substrates suppresses any crystal growth perpendicular to the surface. Only very rarely, a continuous epitaxial layer is observed. Usually, a splitting into individual crystallites occurs with the consequence that >99% of the tiny grains in a micron-size domain (distance ≈15–20 nm) result from secondary nuclei formed by lateral growth and splitting instead of real independent nucleation events [151].

20.3.5.3 Structural Improvement with Film Thickness

After nucleation, diamond films on iridium pass through different phases until they reach the stage of single crystals (Figure 20.19). The nucleation density of 3×10^{11} cm^{-2} within domain regions usually guarantees that formation of a closed layer happens below a thickness of 50 nm (incomplete coverage of the surface with domains may delay this process). During the subsequent phase 2, the deposit resembles a perfect mosaic crystal, i.e., nearly dislocation-free regions are separated by a polygonized network of grain boundaries. The mosaic blocks increase in size until the network disintegrates after several 10 µm into individual or bands of dislocations (phase 3). Afterward, growth proceeds as single crystal (phase 4). Under appropriate growth conditions, growth can continue for many millimeters continuously improving the crystal quality.

Powerful methods to monitor the improvement in structural quality of heteroepitaxial diamond layers are µ-Raman spectroscopy with high spectral resolution, quantification of the dislocation density (by transmission electron microscopy TEM and etch pit counting), and X-ray diffraction (XRD rocking curves and azimuthal scans). Figure 20.20 summarizes the corresponding results for two ≈1-mm-thick

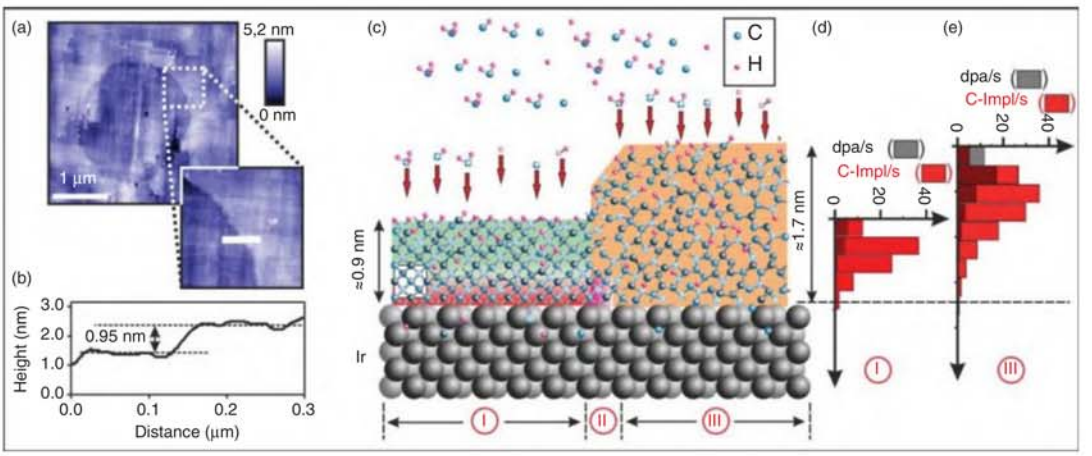

Figure 20.18 Detailed description of the IBI-BLG mechanism. (a) Atomic force microscopy (AFM) image and (b) surface line profile of a sample after BEN taken around a circular domain (comparable to stage (d) in Figure 20.17). (c) The model shows the Ir crystal covered in region (III) by the a-C:H precursor layer (orange), in region (I) by the domain area with the highly damaged diamond nuclei and in region (II) by the thin boundary between both. (d, e) Results of simulations by the SRIM code (Stopping and range of ions in matter) for implanted carbon atoms and displacements per atom (dpa) in the two regions I and III. Source: Schreck et al. [151]. Licensed under CC BY 4.0.

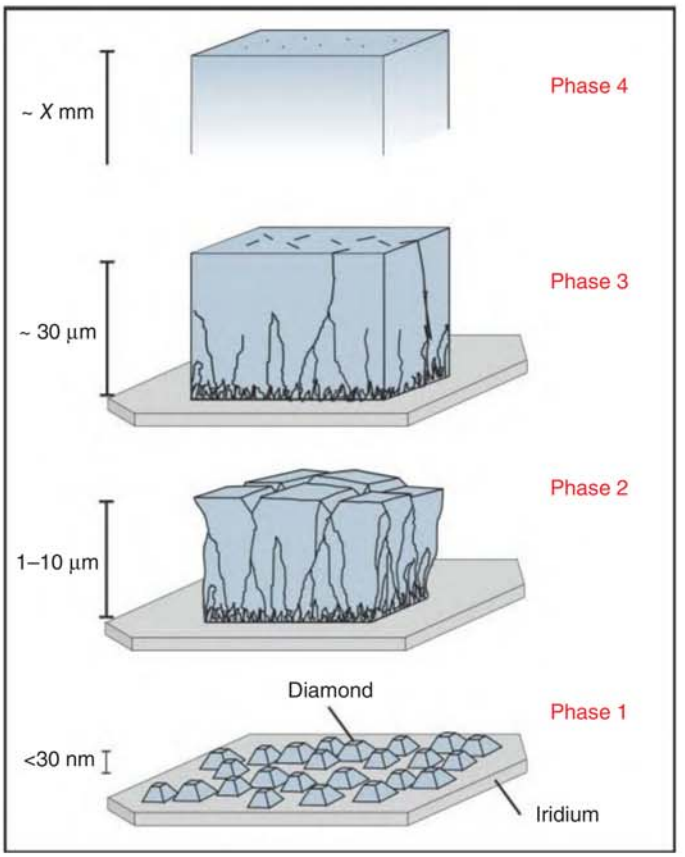

Figure 20.19 Schema of the different stages of epitaxial diamond growth on Ir.

samples. In sample #1, the Raman line width decreased from >10 to 1.86 cm^{-1} and the dislocation density from $\approx 10^{10}$ cm^{-2} to $\approx 5 \times 10^7$ cm^{-2} following a $1/d$ relationship (d = film thickness) [160]. In sample #2, full width at half maximum (FWHM) of tilt and twist decreased from $\approx 1°$ to $\approx 0.1°$.

Merging of neighboring grains by disclination formation was identified as a crucial mechanism for grain coarsening and structural improvement during the initial stage of film growth (phases 2–3 in Figure 20.19) [161]. The subsequent continuous decrease in dislocation density over millimeters of film thickness is attributed to the mutual interaction between dislocations resulting in annihilation or fusion reactions [162].

20.3.5.4 Multilayer Substrates for Scaling to Wafer Size

For all research experiments, thin iridium layers deposited by e-beam evaporation predominantly on oxide single crystals were used instead of bulk single crystals. These comprised MgO [102], $SrTiO_3$ [163], and Al_2O_3 [164]. Compared with diamond, oxides are characterized by high CTE values which results in high compressive stress in the diamond films grown on top. Figure 20.21 shows the

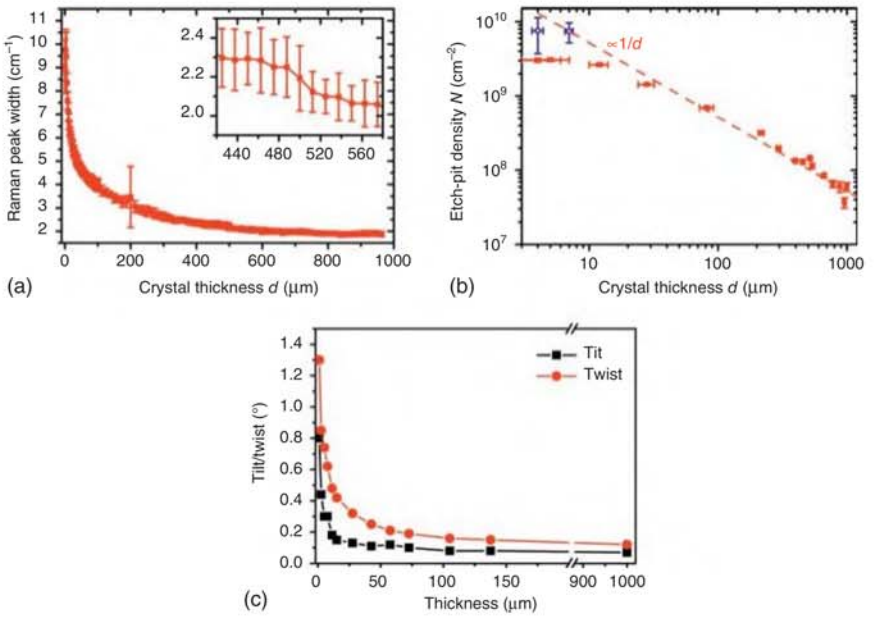

Figure 20.20 Variation of (a) Raman line width and (b) etch pit density (EPD) with thickness for a heteroepitaxial diamond film grown on Ir/YSZ/Si(001). The off-axis angle of the Si(001) wafer was 6° toward [110]. At a thickness of ≈500 μm, the initial nitrogen addition in the gas phase was reduced to zero (see step-like decrease in Raman line width in the inset). For the lowest thickness two data points (blue) of dislocation density measurements derived alternatively by TEM were added to the graph. (c) Mosaic spread of a heteroepitaxial diamond sample which was grown in a sequence of deposition steps without any nitrogen using a Si(001) substrate with an off-angle of 4°. Source: (a, b) Reprinted with permission from [160]. © 2013 AIP Publishing. (c) Graph courtesy of Dr. Martin Fischer, Augsburg Diamond Technology GmbH.

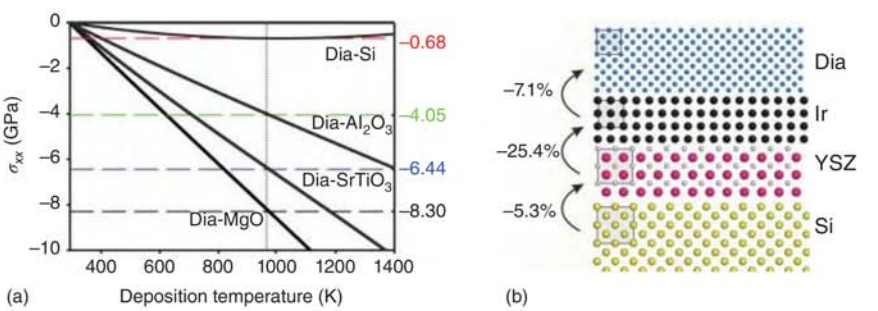

Figure 20.21 (a) Thermal stress σ_{xx} in diamond layers on different substrates vs. deposition temperature (the iridium interlayer can be ignored due to its low thickness). (b) Schematic representation of the epitaxial multilayer structure Dia/Ir/YSZ/Si(001).

compressive thermal stress that develops during cool down from deposition to room temperature for various multilayer substrates. Even for moderate temperatures of 700 °C, the values are very high, e.g. −8.3 GPa for diamond on MgO (the thin iridium interlayer is neglected in these considerations). Delamination and uncontrolled crack formation are usually a consequence. In contrast, silicon shows a minor misfit and the stress even decreases for higher deposition temperature. Silicon would also be a preferred option in terms of wafer quality, size, and price.

Since chemical reactivity and the formation of silicides with low melting point prevent direct growth of Ir on Si, a further inert interlayer between Ir and Si was necessary to facilitate growth of Ir on silicon wafers. Figure 20.21b shows the multilayer structure diamond/Ir/YSZ/Si(001) with YSZ = yttria stabilized zirconia [165]. Basically, YSZ of different stoichiometry resulting in tetragonal or cubic crystal structure can be chosen to grow oxide buffer layers by pulsed laser deposition (PLD) for the subsequent deposition of single crystal iridium [166]. With $SrTiO_3$ buffer layers grown by molecular beam epitaxy (MBE), the multilayer system diamond/Ir/$SrTiO_3$/Si(001) has been established as a promising alternative [167, 168].

A peculiarity of the heteroepitaxy of iridium on oxide buffers should be highlighted: as indicated in Figure 20.21b, the lattice misfit between YSZ and Ir is huge (25.4%). Moreover, the oxide layers grown by PLD have a typical mosaic spread of ≈1–2°. Both aspects are normally considered highly counterproductive for the growth of high-quality single crystal layers. However, this general rule is void for Ir on oxide buffer layers when an appropriate two-step deposition process with an ultralow rate in the first step is applied so that iridium with a mosaic spread of ≈0.1° can be realized on oxides with a mosaic spread of 1–2°. In the crucial first step, the metal islands reorient each other mutually during coalescence so that an angular spread lower than the growth substrate can be obtained [169]. This mechanism also works for various other metals [170]. In addition, the concept can be transferred to oxide layers with even higher mosaic spread like biaxially textured MgO produced by ion beam-assisted deposition (IBAD). Since biaxially textured oxide films can virtually be deposited on every substrate including amorphous or polycrystalline solids, the approach provides an additional degree of freedom for the selection of appropriate substrates [169].

20.3.5.5 The State of the Art in Scaling and Mosaic Spread

Scaling of the single crystal iridium wafers to a diameter of 4 in. [171] and in the following also of the diamond layers (see Figure 20.22a) [151] was achieved in the past years.

Wafers, as shown in Figure 20.22, can routinely be grown in the meantime. The mosaic spread has been further improved to $\Delta\omega = 0.03°$ and $\Delta\varphi = 0.05°$ with minimum dislocations densities of 7×10^6 cm^{-2} at a thickness of 2.2 mm [172].

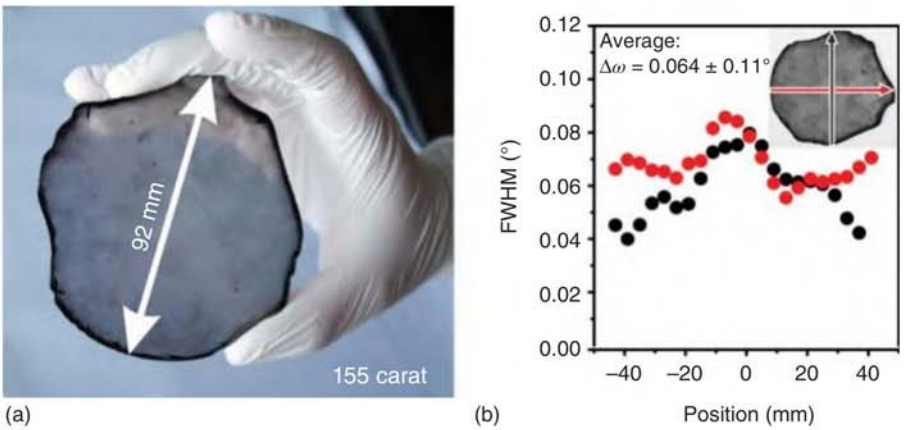

Figure 20.22 (a) Free-standing unpolished single crystal diamond wafer with a thickness of 1.6 ± 0.25 mm grown heteroepitaxially on Ir/YSZ/Si(001). (b) Width of rocking curve measured along two perpendicular lines across the wafer. The corresponding average azimuthal width (dia(311) reflection) was $0.12 \pm 0.04°$ and the Raman line width $1.75 \pm 0.07\ cm^{-1}$. Source: Schreck et al. [151].

20.3.5.6 Intrinsic Stress and Its Correlation with Dislocations

While extrinsic stress due to differences in CTEs between substrate and layer develops at the end of the deposition process during cool down to room temperature, intrinsic (growth) stress already appears during the deposition at constant temperature. Various former homoepitaxy experiments had already revealed that intrinsic stress can be a major problem for the growth of structurally intact films. Specifically on (111) surfaces tensile stress and pronounced crack formation in homoepitaxial layers were observed [173]. During heteroepitaxial diamond growth, these problems appeared even more drastically. It was finally found that the appearance of intrinsic stress is intimately related to the presence of dislocations and "effective climb of dislocations" was identified as the relevant mechanism [174]. The pronounced temperature dependence of stress formation is different for {001} and {111} growth sectors and varies from compressive at low to tensile at high deposition temperatures (see Figure 20.23). High dislocation densities promote stress formation and drastically narrow the temperature window for the growth of crack-free layers [162].

20.3.5.7 Heteroepitaxy on (111)-Oriented Substrates

The benefits of the (111)-orientation for in situ doping or for the incorporation of aligned NV centers are strong arguments for heteroepitaxial wafers with this orientation. After demonstration of the basic proof of concept [175], heteroepitaxial growth on Ir/YSZ/Si(111) has been studied in detail. It turned out that the structural improvement progresses even faster with increasing film thickness than for (001) samples. As a consequence, minimum values of 0.08° for the azimuthal mosaic spread, $4 \times 10^7\ cm^{-2}$ for the dislocation density, and $1.8\ cm^{-1}$ for the Raman line

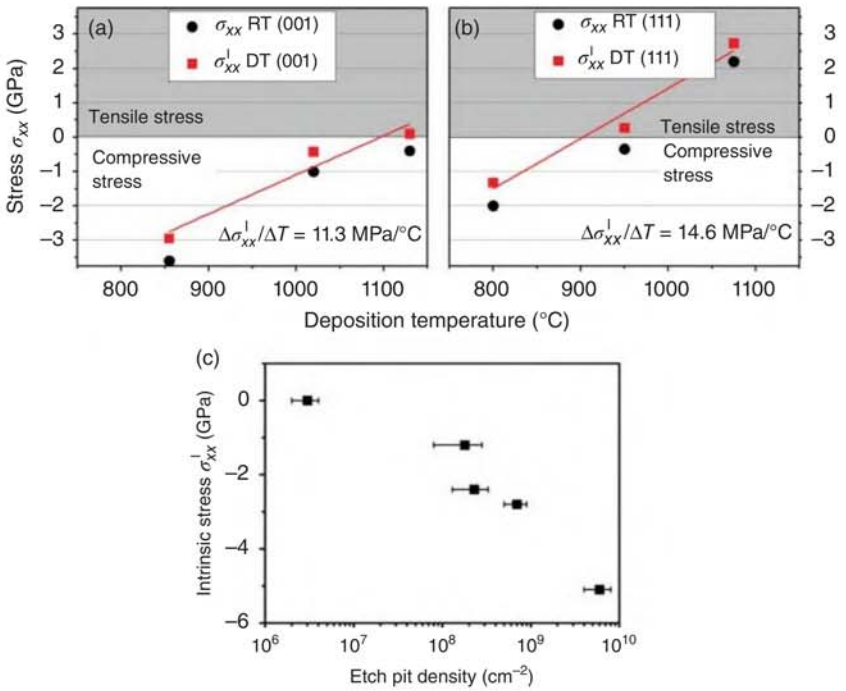

Figure 20.23 Variation of in-plane stress with deposition temperature for growth on (a) (001)- and (b) (111)-oriented substrates [174]. The RT values were measured by XRD at room temperature. The DT values at deposition temperature, which represent the intrinsic stress, were then calculated using the corresponding CTE values. (c) Variation of intrinsic stress with dislocation density for epitaxial growth on a series of (001)-oriented substrates which contained different dislocation densities [162]. The lowest density was obtained by a short bias-assisted growth treatment on an HPHT crystal before the homoepitaxial layer was grown. All samples were grown at 850 °C, 200 mbar, with 8% CH_4/H_2, i.e., under conditions which favor the development of compressive stress. Source: (a, b) Reprinted with permission from Fischer et al. [174]. © 2012 AIP Publishing. (c) Reprinted with permission from Schreck et al. [162]. © 2016 Wiley-VCH.

width have been obtained at comparatively low thickness [176]. All types of twins could be avoided by the use of off-axis substrates. However, growth rates were limited to ≈1 μm/h so that layers up to 330 μm in thickness required technologically unacceptable process times. One reason are the complex stress formation processes [177, 178] that drastically narrow the parameter window of useful deposition temperatures.

20.3.5.8 The Microneedle Approach

To cope with the thermal incompatibility of diamond on Ir/oxide substrates, Japanese groups developed the microneedle approach [179–181] (see Figure 20.24). It comprises first the standard procedures for heteroepitaxial growth of diamond on Ir/MgO substrates followed by patterning of the thin diamond film to form microneedles which are finally overgrown with a thick bulk layer. This bulk

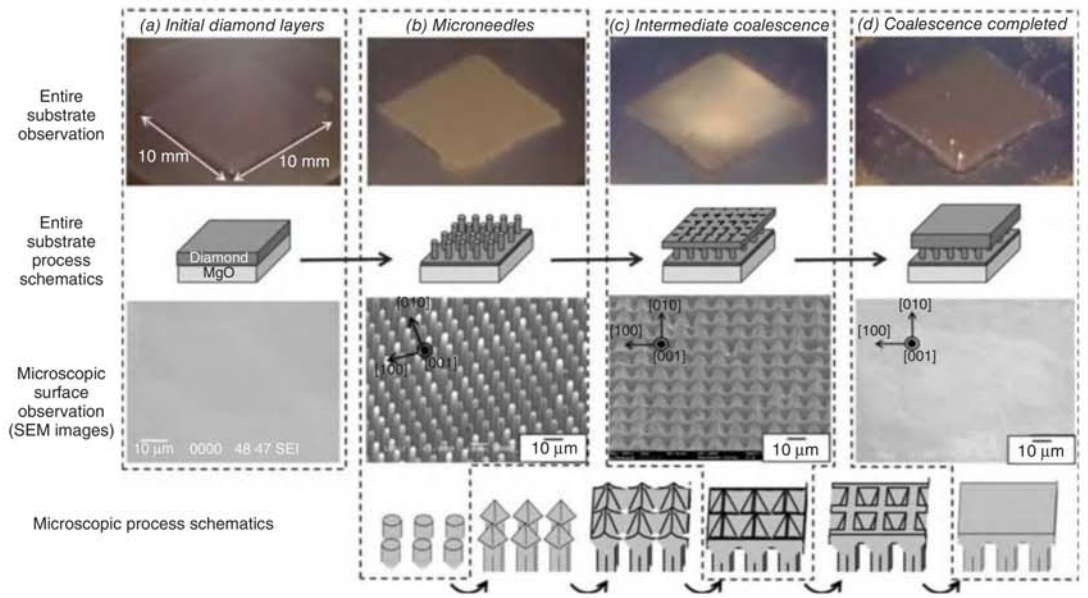

Figure 20.24 Sequence of process steps of the microneedle concept. (a) Thin heteroepitaxial diamond on Ir/MgO(001). (b) Formation of diamond microneedles via Ni masks using the thermochemical reaction of diamond with Ni in a high temperature hydrogen environment. (c, d) Two different stages of overgrowth of the needle structure with final formation of a closed bulk diamond layer after removal of the Ni. Source: Reprinted with permission from Aida et al. [180]. © 2017 Elsevier.

diamond layer splits off due to the thermal stress and bending of the whole multilayer structure during cool down from deposition temperature. The microneedle layer forms the weak link that initiates a well-defined separation. Up to 2-in. diamond wafers manufactured with this technique have recently been reported [182].

20.3.6 Advanced Concepts for Structural Improvement

The observation of the dislocation density decreasing inversely to the thickness d means that every additional order of magnitude in defect reduction requires an identical increase in thickness provided the correlation continues to be valid. Thus, refined approaches are necessary instead of simply growing thicker layers.

20.3.6.1 Epitaxial Lateral Overgrowth

ELO is a common technique for dislocation density reduction, e.g. in group-III nitride layers [183]. Several attempts have also been made in the field of diamond heteroepitaxy either by patterning directly the BEN layer [184, 185] or by the use of gold masks [186]. A very detailed study with a systematic variation of the grid spacing and fill factor (FF) has been published recently (see Figure 20.25). In this work, first BEN was performed on Ir/MgO(001) substrates. The thin carbon layer containing the nuclei was then covered by a photoresist which was patterned by photolithography. In the next step, the pattern with a defined grid spacing was transferred to the nucleation layer by Ar ion bombardment. Outside the 3-µm- wide lines, all the nuclei were destroyed. After removal of the photoresist, the pattern was overgrown (partial overgrowth is shown in Figure 20.25a) until a closed diamond layer was formed. At 60-µm thickness, etch pits were generated, and the dislocation density was derived. As shown in Figure 20.25b, the patterned overgrowth with various grid spacings reduced the dislocation density from 2×10^8 cm^{-2} for standard growth without patterning to a surface averaged value of 9×10^6 cm^{-2} (locally 5×10^6 cm^{-2}) for the 100-µm spacing. At the same time, the FWHM values for tilt

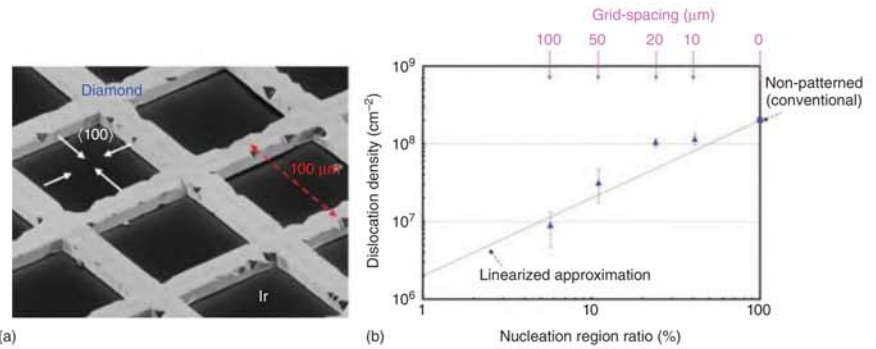

Figure 20.25 (a) Heteroepitaxial diamond layer after 2-hour growth (partial overgrowth) on an Ir/MgO(001) sample patterned with 100-µm grid spacing after BEN. (b) Average dislocation density after complete overgrowth vs. the ratio of the nucleation region in which the diamond nuclei were not destroyed by the patterning procedure. Source: Reprinted with permission from Ichikawa et al. [187]. © 2019 Elsevier.

and twist decreased from 0.17° and 0.51° (value measured at 60-µm thickness) to 0.064° and 0.043° (at 100-µm thickness), respectively.

The ELO technique described before is based on the destruction of diamond nuclei. Classically, a mask material is used as a stopping layer like for the liftoff concept with SiO_2 masks described in Chapter 20.3.4.2 or the gold masks in [186]. Besides this, the microneedle approach in Chapter 20.3.5.8 or the lateral growth over a macroscopic hole as reported by Tallaire et al. [188] represent a kind of air-bridged [189] or maskless [190] ELO. Both are known from GaN growth. Bridging the gap between neighboring needles or the macroscopic hole by lateral growth without generation of new dislocations can reduce the local dislocation density in the former gap regions and the average value after film closure. Actually, growth over the macroscopic hole manufactured in a Ib substrate (with a typical dislocation density of 10^4–10^6 cm^{-2}) resulted in a local value of 2×10^3 cm^{-2} [188].

20.3.6.2 Dislocation Stopping by W or Ta Atoms

A novel approach for a very efficient reduction in dislocation density has recently been reported. It is based on the metal-assisted termination (MAT) of dislocations by W or Ta atoms which are incorporated into the diamond crystal during a short hot filament growth step with high filament temperature >2400 K [191, 192]. Typical W concentrations are ≈10 ppm. Afterward, growth is continued metal free by MWPCVD. On single crystal substrates, incorporation of W atoms reduced the dislocation density from 2×10^6 cm^{-2} to 3×10^4 cm^{-2} (Figure 20.26) and also on heteroepitaxial substrates impressing improvements in crystal quality have been obtained. In both cases, the structural changes also translated into improved device characteristics of Schottky barrier diodes fabricated with these substrates.

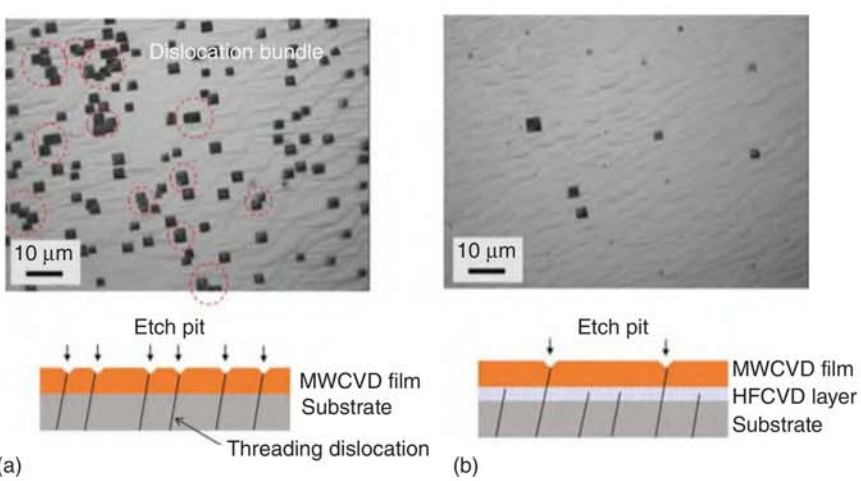

Figure 20.26 Etch pits generated to reveal densities of threading dislocations for MWPCVD layers grown (a) without and (b) with a few-micron-thick HFCVD interlayer on single crystal substrates with initial dislocation densities of $\approx 2 \times 10^6$ cm^{-2}.
Source: Reprinted with permission from Ohmagari et al. [191]. © 2018 AIP Publishing.

20.4 State of the Art and Outlook

During the last few years, appreciable progress has been achieved in the field of HPHT as well as CVD growth. Most prominent is the increase in single crystal size of HPHT crystals making available $15 \times 15\,mm^2$ single crystal plates and the 92-mm-wafer grown by CVD on the heteroepitaxy substrate Ir/YSZ/Si. HPHT crystals free of dislocations in limited regions have been shown. These would provide the ideal substrates for exploring the limits of diamond-based electronic devices. Systematically increasing the size of low dislocation density seeds is one approach toward electronic-grade wafer material. On the other hand, the heteroepitaxy concepts profit from the simultaneous nucleation over a large area. The coalescence of $\approx 2 \times 10^{13}$ nuclei that are typically formed during BEN on a 4-in. diameter wafer surface results in initial dislocation densities $>10^{10}\ cm^{-2}$. By simple growth of several millimeter thick crystals or by ELO, this value can be reduced to $<10^{7}\ cm^{-2}$. Future work has to show whether the different ELO concepts have the potential for significant further improvement. The intriguing novel MAT approach provides a simple and very efficient method to reduce dislocation densities. Exploring its potential, limits, and the underlying mechanisms deserve increased interest of the scientific community.

In conclusion, the progress in crystal growth is increasingly removing one former bottleneck in the development of diamond electronics by establishing a base for the supply of wafer-size high-quality substrates to manufacture competitive electronic devices.

Acknowledgments

The work in the author's laboratory was continuously supported by the former and current chair holder (Professors B. Stritzker and M. Albrecht) and by various funding agencies (DFG, BMBF, EC, Bayerische Forschungsstiftung, GSI in Darmstadt, ILL in Grenoble, FRMII in Munich, and HZB in Berlin). I would also like to express my great gratitude to all the motivated students over many years who placed their trust in me by joining the diamond group specifically S. Gsell and M. Fischer, cofounders of Augsburg Diamond Technology GmbH.

References

1 Gheeraert, E. (2018). Power electronic devices performances based on diamond properties. In: *Power Electronics Device Applications of Diamond Semiconductors* (eds. S. Koizumi, H. Umezawa, J. Pernot and M. Suzuki), 191–200. Duxford: Woodhead Publishing.

2 Evans, T. (1979). Changes produced by high temperature treatment of diamond. In: *The Properties of Diamond* (ed. J.E. Field), 403–424. London: Academic Press.

3 Wilks, J. and Wilks, E. (1991). *Properties and Applications of Diamond*. Oxford: Butterworth-Heinemann Ltd.

4 Palyanov, Y.N., Kupriyanov, I.N., Khokhryakov, A.F., and Ralchenko, V.G. (2015). Crystal growth of diamond. In: *Bulk Crystal Growth: Basic Techniques*, Part A, vol. II (eds. T. Nishinga and P. Rudolph), 671–713. Amsterdam: Elsevier.

5 Bundy, F.P. (1963). Direct conversion of graphite to diamond in static pressure apparatus. *J. Chem. Phys.* 38: 631–643.

6 Irifune, T., Kurio, A., Sakamoto, S. et al. (2003). Ultrahard polycrystalline diamond from graphite. *Nature* 421: 599–600.

7 Bundy, F.P., Bovenkerk, H.P., Strong, H.M., and Wentorf, R.H. (1961). Diamond-graphite equilibrium line from growth and graphitization of diamond. *J. Chem. Phys.* 35: 383–391.

8 Lysakovskyi, V.V., Novikov, N.V., Ivakhnenko, S.A. et al. (2018). Growth of structurally perfect diamond single crystals at high pressures and temperatures. Review. *J. Superhard Materials* 40: 315–324.

9 D'Haenens-Johansson, U.F.S., Katrusha, A., Moe, K.S. et al. (2015). Large colorless HPHT synthetic diamonds from New Diamond Technology. *Gems Gemol.* 51: 260–279.

10 Wedlake, R.J. (1979). Technology of diamond growth. In: *The Properties of Diamond* (ed. J.E. Field), 501–535. London: Academic Press.

11 Nassau, K. and Nassau, J. (1979). The history and present status of synthetic diamond. *J. Cryst. Growth* 46: 157–172.

12 Kanda, H. and Jia, X. (2001). Change of luminescence character of Ib diamonds with HPHT treatment. *Diamond Relat. Mater.* 10: 1665–1669.

13 Hazen, R.M. (1999). *The Diamond Makers – A Compelling Drama of Scientific Discovery*. Cambridge University Press.

14 Bovenkerk, H.P., Bundy, F.P., Hall, H.T. et al. (1959). Preparation of diamond. *Nature* 184: 1094–1098.

15 Abbaschian, R., Zhu, H., and Clarke, C. (2005). High pressure–high temperature growth of diamond crystals using split sphere apparatus. *Diamond Relat. Mater.* 14: 1916–1919.

16 Choudhary, D. and Bellare, J. (2000). Manufacture of gem quality diamonds: a review. *Ceram. Int.* 26: 73–85.

17 Katrusha, A. (2017). Fabrication and properties of ultra large (<100 carat) type IIa colorless synthetic diamonds. Invited talk INV11 at 28th International Conference on Diamond and Carbon Materials, Gothenburg, Sweden (3–7 September 2017).

18 Palyanov, Y.N., Borzdov, Y.M., Khokhryakov, A.F. et al. (2010). Effect of nitrogen impurity on diamond crystal growth processes. *Cryst. Growth Des.* 10: 3169–3175.

19 Han, Q.-G., Liu, B., Hu, M.-h. et al. (2011). Design an effective solution for commercial production and scientific research on gem-quality, large, single-crystal diamond by high pressure and high temperature. *Cryst. Growth Des.* 11: 1000–1005.

20 Angus, J.C. and Hayman, C.C. (1988). Low-pressure, metastable growth of diamond and "diamondlike" phases. *Science* 241: 913–921.

21 Zaitsev, A.M. (1998). Optical properties. In: *Handbook of Industrial Diamonds and Diamond Films* (eds. M.A. Prelas, G. Popovici and L.K. Bigelow), 227–376. New York: Marcel Dekker.

22 Aharonovich, I. and Neu, E. (2014). Diamond nanophotonics. *Adv. Opt. Mater.* 2: 911–928.

23 Dobrinets, I.A., Vins, V.G., and Zaitsev, A.M. (2013). *HPHT-Treated Diamonds: Diamonds Forever*. Berlin: Springer.

24 Dischler, B. (2012). *Handbook of Spectral Lines in Diamond: Tables and Interpretations*, vol. 1. Berlin: Springer-Verlag.

25 Woods, G.S. (1994). The "type" terminology for diamond. In: *Properties and Growth of Diamond*, EMIS Datareviews Series No. 9 (ed. G. Davies), 83–84. London: Inspec.

26 Bustarret, E., Achatz, P., Sacépé, B. et al. (2008). Metal-to-insulator transition and superconductivity in boron-doped diamond. *Philos. Trans. R. Soc. London, Ser. A* 366: 267–279.

27 Sumiya, H. and Satoh, S. (1996). High-pressure synthesis of high-purity diamond crystal. *Diamond Relat. Mater.* 5: 1359–1365.

28 Sumiya, H. and Tamasaku, K. (2012). Large defect-free synthetic type IIa diamond crystals synthesized via high pressure and high temperature. *Jpn. J. Appl. Phys.* 51: 090102.

29 Strong, H.M. and Wentorf, R.H. (1972). The growth of large diamond crystals. *Naturwissenschaften* 59: 1–7.

30 Palyanov, Y.N., Khokhryakov, A.F., Borzdov, Y.M., and Kupriyanov, I.N. (2013). Diamond growth and morphology under the influence of impurity adsorption. *Cryst. Growth Des.* 13: 5411–5419.

31 Shigley, J.E., Fritsch, E., Reinitz, I., and Moon, M. (1992). An update on Sumitomo gem-quality synthetic diamonds. *Notes and New Techniques, Gem&Gemology*, Summer 1992, p. 116.

32 Koivula, J.I., Kammerling, R.C., and Fritsch, E. (eds.) (1993). GemNews in *Gem&Gemology*, Summer 1993, p. 130.

33 Tallaire, A., Mille, V., Brinza, O. et al. (2017). Thick CVD diamond films grown on high-quality type IIa HPHT diamond substrates from New Diamond Technology. *Diamond Relat. Mater.* 77: 146–152.

34 Wentorf, R.H. and Bovenkerk, H.P. (1962). Preparation of semiconducting diamonds. *J. Chem. Phys.* 36: 1987–1990.

35 Koizumi, S., Kamo, M., Sato, Y. et al. (1997). Growth and characterization of phosphorous doped {111} homoepitaxial diamond thin films. *Appl. Phys. Lett.* 71: 1065–1067.

36 Nadolinny, V., Komarovskikh, A., Palyanov, Y., and Sokol, A. (2015). EPR of synthetic diamond heavily doped with phosphorus. *Phys. Status Solidi A* 212: 2568–2571.

37 Ekimov, E.A., Sidorov, V.A., Maslakov, K.I. et al. (2018). Influence of growth medium composition on the incorporation of boron in HPHT diamond. *Diamond Relat. Mater.* 89: 101–107.

38 Ekimov, E.A., Sidorov, V.A., Bauer, E.D. et al. (2004). Superconductivity in diamond. *Nature* 428: 542–545.

39 Blank, V.D., Kuznetsov, M.S., Nosukhin, S.A. et al. (2007). The influence of crystallization temperature and boron concentration in growth environment on its distribution in growth sectors of type IIb diamond. *Diamond Relat. Mater.* 16: 800–804.

40 Burns, R.C., Cvetkovic, V., Dodge, C.N. et al. (1990). Growth-sector dependence of optical features in large synthetic diamonds. *J. Cryst. Growth* 104: 257–279.

41 Tarelkin, S., Bormashov, V., Buga, S. et al. (2015). Power diamond vertical Schottky barrier diode with 10 A forward current. *Phys. Status Solidi A* 212: 2621–2627.

42 Saremi, M., Hathwar, R., Dutta, M. et al. (2017). Analysis of the reverse I–V characteristics of diamond-based PIN diodes. *Appl. Phys. Lett.* 111: 043507.

43 Butler, J.E. and Woodin, R.L. (1993). Thin film diamond growth mechanisms. *Philos. Trans. R. Soc. London, Ser. A* 342: 209–224.

44 Butler, J.E. and Woodin, R.L. (1994). Thin film diamond growth mechanisms. In: *Thin Film Diamond* (eds. A. Lettington and J.W. Steeds), 15–30. London: Chapman & Hall.

45 Butler, J.E., Mankelevich, Y.A., Cheesman, A. et al. (2009). Understanding the chemical vapor deposition of diamond: recent progress. *J. Phys. Condens. Matter* 21: 364201.

46 Lombardi, G., Hassouni, K., Stancu, G.-D. et al. (2005). Modeling of microwave discharges of H_2 admixed with CH_4 for diamond deposition. *J. Appl. Phys.* 98: 053303.

47 Hassouni, K., Silva, F., and Gicquel, A. (2010). Modelling of diamond deposition microwave cavity generated plasmas. *J. Phys. D: Appl. Phys.* 43: 153001.

48 Goodwin, D.G. and Butler, J.E. (1998). Theory of diamond chemical vapor deposition. In: *Handbook of Industrial Diamonds and Diamond Films* (eds. M.A. Prelas, G. Popovici and L.K. Bigelow), 527–581. New York: Marcel Dekker.

49 Harris, S.J. and Goodwin, D.G. (1993). Growth on the reconstructed diamond (001) surface. *J. Phys. Chem.* 97: 23–28.

50 Goodwin, D.G. (1993). Scaling laws for diamond chemical-vapor deposition. I. Diamond surface chemistry. *J. Appl. Phys.* 74: 6888–6894.

51 Silva, F., Achard, J., Brinza, O. et al. (2009). High quality, large surface area, homoepitaxial MPACVD diamond growth. *Diamond Relat. Mater.* 18: 683–697.

52 Asmann, M., Heberlein, J., and Pfender, E. (1999). A review of diamond CVD utilizing halogenated precursors. *Diamond Relat. Mater.* 8: 1–16.

53 Zhou, D., Gruen, D.M., Quin, L.C. et al. (1998). Control of diamond film microstructure by Ar additions to CH_4/H_2 microwave plasmas. *J. Appl. Phys.* 84: 1981–1989.

54 Zhou, D., McCauley, T.G., Quin, L.C. et al. (1998). Synthesis of nanocrystalline diamond thin films from an Ar-CH_4 plasma. *J. Appl. Phys.* 83: 540–543.

55 Tallaire, A., Rond, C., Bénédic, F. et al. (2011). Effect of argon addition on the growth of thick single crystal diamond by high-power plasma CVD. *Phys. Status Solidi A* 208: 2028–2032.

56 Bachmann, P.K., Leers, D., and Lydtin, H. (1991). Towards a general concept of diamond chemical vapor deposition. *Diamond Relat. Mater.* 1: 1–12.

57 Bachmann, P.K., Hademann, H.J., Lade, H. et al. (1994). Diamond chemical vapor deposition: gas compositions and film properties. *Mater. Res. Soc. Symp. Proc.* 339: 267–278.

58 Bauer, T., Schreck, M., and Stritzker, B. (2006). Homoepitaxial diamond layers on off-axis Ib HPHT substrates: growth of thick films and characterization by high-resolution X-ray diffraction. *Diamond Relat. Mater.* 15: 472–478.

59 Müller-Sebert, W., Wörner, E., Fuchs, F. et al. (1996). Nitrogen induced increase of the growth rate in chemical vapor deposition of diamond. *Appl. Phys. Lett.* 68: 759–760.

60 Kalayci, A. (2017). Defekteinbau beim Diamantwachstum mit Stickstoff. Bachelor thesis. University of Augsburg.

61 Gao, G.Z., Schermer, J.J., van Enckevort, W.J.P. et al. (1996). Growth of {100} textured diamond films by the addition of nitrogen. *J. Appl. Phys.* 79: 1357–1364.

62 Locher, R., Wild, C., Herres, N. et al. (1994). Nitrogen stabilized ⟨100⟩ texture in chemical vapor deposited diamond films. *Appl. Phys. Lett.* 65: 34–36.

63 Bohr, S., Haubner, R., and Lux, B. (1996). Influence of nitrogen additions on hot-filament chemical vapor deposition of diamond. *Appl. Phys. Lett.* 68: 1075–1077.

64 Dunst, S., Sternschulte, H., and Schreck, M. (2009). Growth rate enhancement by nitrogen in diamond chemical vapor deposition – a catalytic effect. *Appl. Phys. Lett.* 94: 224101.

65 Sartori, A.F. and Schreck, M. (2014). Mutual interaction of N, B, and O during heteroepitaxial diamond growth: triggering the nitrogen induced growth acceleration. *Phys. Status Solidi A* 211: 2290–2295.

66 Bachmann, P.K. (1994). Plasma CVD techniques for low pressure synthesis of diamond: an overview. In: *Properties and Growth of Diamond*, EMIS Datareviews Series No. 9 (ed. G. Davies), 349–353. London: Inspec.

67 Argoitia, A., Kovach, C.S., and Angus, J.C. (1998). Hot Filament CVD methods. In: *Handbook of Industrial Diamonds and Diamond Films* (eds. M.A. Prelas, G. Popovici and L.K. Bigelow), 797–819. New York: Marcel Dekker.

68 Li, D.M., Mäntylä, T., Hernberg, R., and Levoska, J. (1996). Diamond deposition by coiled and grid filaments using high methane concentrations. *Diamond Relat. Mater.* 5: 350–353.

69 Klages, C.-P. and Schäfer, L. (1998). Hot-filament deposition of diamond. In: *Low-Pressure Synthetic Diamond: Manufacturing and Applications* (eds. B. Dischler and C. Wild), 85–101. Berlin: Springer-Verlag.

70 Schäfer, L., Höfer, M., and Kröger, R. (2006). The versatility of hot-filament activated chemical vapor deposition. *Thin Solid Films* 515: 1017–1024.

71 Sawabe, A. and Inuzuka, T. (1985). Growth of diamond thin films by electron assisted chemical vapor deposition. *Appl. Phys. Lett.* 46: 146–147.

72 Sawabe, A., Yasuda, H., Inuzuka, T., and Suzuki, K. (1988). Growth of diamond thin films in a DC discharge plasma. *Appl. Surf. Sci.* 33/34: 539–545.

73 Bachmann, P.K. (1994). Plasma CVD synthesis of diamond. In: *Properties and Growth of Diamond*, EMIS Datareviews Series No. 9 (ed. G. Davies), 354–363. London: Inspec.

74 Chae, K.-W., Baik, Y.-J., Park, J.-K., and Lee, W.-S. (2010). The 8-inch free-standing CVD diamond wafer fabricated by DC-PACVD. *Diamond Relat. Mater.* 19: 1168–1171.

75 Ohtake, N. and Yoshikawa, M. (1990). Diamond film preparation by arc-discharge plasma-jet chemical vapor-deposition in methane atmosphere. *J. Electrochem. Soc.* 137: 717–722.

76 Lu, F.X., Tang, W.Z., Huang, T.B. et al. (2001). Large area high quality diamond film deposition by high power DC arc plasma jet operating at gas recycling mode. *Diamond Relat. Mater.* 10: 1551–1558.

77 Cappelli, M.A. and Owano, T.G. (1998). Plasma-jet deposition of diamond. In: *Low Pressure Synthetic Diamond: Manufacturing and Applications* (eds. B. Dischler and C. Wild), 59–84. Berlin: Springer-Verlag.

78 Kamo, M., Sato, Y., Matsumoto, S., and Setaka, N. (1983). Diamond synthesis from gas-phase in microwave plasma. *J. Cryst. Growth* 62: 642–644.

79 Sevillano, E. (1998). Microwave-plasma deposition of diamond. In: *Low Pressure Synthetic Diamond: Manufacturing and Applications* (eds. B. Dischler and C. Wild), 11–39. Berlin: Springer-Verlag.

80 Liang, Q., Chin, C.Y., Lai, J. et al. (2009). Enhanced growth of high quality single crystal diamond by microwave plasma assisted chemical vapor deposition at high gas pressures. *Appl. Phys. Lett.* 94: 024103.

81 Füner, M., Wild, C., and Koidl, P. (1998). Novel microwave plasma reactor for diamond synthesis. *Appl. Phys. Lett.* 72: 1149–1151.

82 Silva, F., Hassouni, K., Bonnin, X., and Gicquel, A. (2009). Microwave engineering of plasma-assisted CVD reactors for diamond deposition. *J. Phys. Condens. Matter* 21: 364202.

83 Vikharev, A.L., Gorbachev, A.M., Kozlov, A.V. et al. (2006). Diamond films grown by millimeter wave plasma-assisted CVD reactor. *Diamond Relat. Mater.* 15: 502–507.

84 Vikharev, A.L., Gorbachev, A.M., and Radishev, D.B. (2019). Physics and applications of gas discharge in millimeter wave beams. *J. Phys. D: Appl. Phys.* 52: 014001.

85 Wolden, C.A., Sitar, Z., and Davis, R.F. (1998). Combustion flame deposition of diamond. In: *Low Pressure Synthetic Diamond: Manufacturing and Applications* (eds. B. Dischler and C. Wild), 41–58. Berlin: Springer-Verlag.

86 Konov, V.I., Prokhorov, A.M., Uglov, S.A. et al. (1998). CO_2 laser-induced plasma CVD synthesis of diamond. *Appl. Phys. A: Mater.* 66: 575–578.

87 Metev, S., Brecht, H., Schwarz, J., and Sepold, G. (2002). New technology for high rate synthesis of PC-diamond coatings in air with photon plasmatron. *Diamond Relat. Mater.* 11: 472–477.

88 Gu, Y.J., Lu, J., Grotjohn, T. et al. (2012). Microwave plasma reactor design for high pressure and high power density diamond synthesis. *Diamond Relat. Mater.* 24: 210–214.

89 Schreck, M., Asmussen, J., Shikata, S. et al. (2014). Large-area high-quality single crystal diamond. *MRS Bull.* 39: 504–510.

90 Koizumi, S., Murakami, T., Inuzuka, T., and Suzuki, K. (1990). Epitaxial growth of diamond thin films on cubic boron nitride {111} surfaces by dc plasma chemical vapor deposition. *Appl. Phys. Lett.* 57: 563–565.

91 Jiang, X. and Klages, C.-P. (1993). Heteroepitaxial diamond growth on (100) silicon. *Diamond Relat. Mater.* 2: 1112–1113.

92 Iijima, S., Aikawa, Y., and Baba, K. (1990). Early formation of chemical vapor deposition diamond films. *Appl. Phys. Lett.* 57: 2646–2648.

93 Williams, O.A., Douhéret, O., Daenen, M. et al. (2007). Enhanced diamond nucleation on monodispersed nanocrystalline diamond. *Chem. Phys. Lett.* 445: 255–258.

94 Yugo, S., Kanai, T., Kimura, T., and Muto, T. (1991). Generation of diamond nuclei by electric field in plasma chemical vapor-deposition. *Appl. Phys. Lett.* 58: 1036–1038.

95 Stoner, B.R., Ma, G.H.M., Wolter, S.D., and Glass, J.T. (1992). Characterization of bias-enhanced nucleation of diamond on silicon by in vacuo surface-analysis and transmission electron microscopy. *Phys. Rev. B* 45: 11067–11084.

96 Stoner, B.R. and Glass, J.T. (1992). Textured diamond growth on (100) beta-SiC via microwave plasma chemical vapor deposition. *Appl. Phys. Lett.* 60: 698–700.

97 Wolter, S.D., McClure, M.T., Glass, J.T., and Stoner, B.R. (1995). Bias-enhanced nucleation of highly oriented diamond on titanium carbide (111) substrates. *Appl. Phys. Lett.* 66: 2810–1812.

98 Reinke, P. and Oelhafen, P. (1998). Bias-enhanced nucleation of diamond on molybdenum: a photoelectron spectroscopy study of the initial stages of the growth process. *J. Appl. Phys.* 84: 2612–2617.

99 Tucker, D.A., Seo, D.-K., Whangbo, M.-H. et al. (1995). Comparison of silicon, nickel, and nickel silicide (Ni_3Si) as substrates for epitaxial diamond growth. *Surf. Sci.* 334: 179–194.

100 Hayashi, Y., Shiraokawa, N., and Nishino, S. (2000). Effect of bias-enhancement in diamond nucleation and growth on nickel. *Thin Solid Films* 374: 268–273.

101 Bauer, T., Schreck, M., Gsell, S. et al. (2003). Epitaxial rhenium buffer layers on $Al_2O_3(0001)$: a substrate for the deposition of (111)-oriented heteroepitaxial diamond films. *Phys. Status Solidi A* 199: 19–26.

102 Ohtsuka, K., Suzuki, K., Sawabe, A., and Inuzuka, T. (1996). Epitaxial growth of diamond on iridium. *Jpn. J. Appl. Phys.* 35: L1072–L1074.

103 Zhu, W., Sivazlian, F.R., Stoner, B.R., and Glass, J.T. (1995). Nucleation and selected-area deposition of diamond by biased hot-filament chemical-vapor-deposition. *J. Mater. Res.* 10: 425–430.

104 Katoh, M., Aoki, M., and Kawarada, H. (1994). Plasma-enhanced diamond nucleation on Si. *Jpn. J. Appl. Phys.* 33: L194–L196.

105 Schreck, M. and Stritzker, B. (1996). Nucleation and growth of heteroepitaxial diamond films on silicon. *Phys. Status Solidi A* 154: 197–217.

106 Schreck, M. (2014). Single crystal diamond growth on iridium. In: *Comprehensive Hard Materials Volume 3 Superhard Materials* (eds. V.K. Sarin and C.E. Nebel), 269–304. Amsterdam: Elsevier.

107 Raizer, Y.P. (1991). *Gas Discharge Physics*. Berlin: Springer-Verlag.

108 Schreck, M., Baur, T., and Stritzker, B. (1995). Optical characterization of the cathode plasma sheath during the biasing step for diamond nucleation on silicon. *Diamond Relat. Mater.* 4: 553–558.

109 Kátai, S., Kováts, A., Maros, I., and Deák, P. (2000). Ion energy distributions and their evolution during bias-enhanced nucleation of chemical vapor deposition of diamond. *Diamond Relat. Mater.* 9: 317–321.

110 Jiang, X., Schiffmann, K., and Klages, C.-P. (1994). Nucleation and initial growth phase of diamond thin films on (100) silicon. *Phys. Rev. B* 50: 8402–8410.

111 Jiang, X., Zhang, W.J., Paul, M., and Klages, C.-P. (1996). Diamond film orientation by ion bombardment during deposition. *Appl. Phys. Lett.* 68: 1927–1929.

112 Zhang, W.J. and Jiang, X. (1996). The growth characteristics of (001) oriented diamond layers on (111) diamond face via bias-assisted chemical vapor deposition. *Appl. Phys. Lett.* 68: 2195–2197.

113 Thürer, K.-H., Schreck, M., and Stritzker, B. (1998). Limiting processes for diamond epitaxial alignment on silicon. *Phys. Rev. B* 57: 15454–15464.

114 Gu, C.Z. and Jiang, X. (2000). Deposition and characterization of nanocrystalline diamond films prepared by ion bombardment-assisted method. *J. Appl. Phys.* 88: 1788–1793.

115 Wild, C., Koidl, P., Müller-Sebert, W. et al. (1993). Chemical vapour deposition and characterization of smooth {100}-faceted diamond films. *Diamond Relat. Mater.* 2: 158–168.

116 Wild, C., Herres, N., and Koidl, P. (1990). Texture formation in polycrystalline diamond films. *J. Appl. Phys.* 68: 973–978.

117 Silva, F., Bénédic, F., Bruno, P., and Gicquel, A. (2005). Formation of ⟨110⟩ texture during nanocrystalline diamond growth: an X-ray diffraction study. *Diamond Relat. Mater.* 14: 398–403.

118 Van der Drift, A. (1967). Evolutionary selection, a principle governing growth orientation in vapour-deposited layers. *Philips Res. Rep.* 22: 267–288.

119 Wild, C., Kohl, R., Herres, N. et al. (1994). Oriented CVD diamond films: twin formation, structure and morphology. *Diamond Relat. Mater.* 3: 373–381.

120 Silva, F., Bonnin, X., Achard, J. et al. (2008). Geometric modeling of homoepitaxial CVD diamond growth: I. the {100}{111}{110}{113} system. *J. Cryst. Growth* 310: 187–203.

121 Silva, F., Achard, J., Bonnin, X. et al. (2006). 3D crystal growth model for understanding the role of plasma pre-treatment on CVD diamond crystal shape. *Phys. Status Solidi A* 203: 3049–3055.

122 Nebel, C.E. (2003). Transport and defect properties of intrinsic and boron-doped diamond. In: *Thin-Film Diamond I* (eds. C.E. Nebel and J. Ristein), 261–324. Amsterdam: Elsevier.

123 Isberg, J., Hammersberg, J., Bernhoff, H. et al. (2004). Charge collection distance measurements in single and polycrystalline CVD diamond. *Diamond Relat. Mater.* 13: 872–875.

124 Isberg, J., Hammersberg, J., Johansson, E. et al. (2002). High carrier mobility in single-crystal plasma-deposited diamond. *Science* 297: 1670–1672.

125 Nesladek, M., Bogdan, A., Deferme, W. et al. (2008). Charge transport in high mobility single crystal diamond. *Diamond Relat. Mater.* 17: 1235–1240.

126 Berdermann, E., Pomorski, M., de Boer, W. et al. (2010). Diamond detectors for hadron physics research. *Diamond Relat. Mater.* 19: 358–367.

127 Kamo, M., Yurimoto, H., and Sato, Y. (1988). Epitaxial growth of diamond on diamond substrate by plasma assisted CVD. *Appl. Surf. Sci.* 33/34: 553–560.

128 Badzian, A. and Badzian, T. (1993). Diamond homoepitaxy by chemical vapor deposition. *Diamond Relat. Mater.* 2: 147–157.

129 Hetherington, A.V., Wort, C.J.H., and Southworth, P. (1990). Crystalline perfection of chemical vapor-deposited diamond films. *J. Mater. Res.* 5: 1591–1594.

130 Achard, J. and Tallaire, A. (2018). Growth of thick CVD diamond films on different crystalline orientations: defects and doping. In: *Power Electronics Device Applications of Diamond Semiconductors* (eds. S. Koizumi, H. Umezawa, J. Pernot and M. Suzuki), 1–27. Duxford: Woodhead Publishing.

131 Bauer, T., Schreck, M., Sternschulte, H., and Stritzker, B. (2005). High growth rate homoepitaxial diamond deposition on off-axis substrates. *Diamond Relat. Mater.* 14: 266–271.

132 Bauer, T. (2007). Homoepitaktische Abscheidung von Diamant auf off-axis Substraten. Dissertation. Universität Augsburg.

133 Muehle, M., Becker, M.F., Schuelke, T., and Asmussen, J. (2014). Substrate crystal recovery for homoepitaxial diamond synthesis. *Diamond Relat. Mater.* 42: 8–14.

134 Couty, P., Wagner, F.R., and Hoffmann, P.W. (2005). Laser coupling with a multimode water-jet waveguide. *Opt. Eng.* 44: 068001.

135 Parikh, N.R., Hunn, J.D., McGucken, E. et al. (1992). Single-crystal diamond plate liftoff achieved by ion implantation and subsequent annealing. *Appl. Phys. Lett.* 61: 3124–3126.

136 Mokuno, Y., Chayahara, A., and Yamada, H. (2008). Synthesis of large single crystal diamond plates by high rate homoepitaxial growth using microwave plasma CVD and lift-off process. *Diamond Relat. Mater.* 17: 415–418.

137 Yamada, H., Chayahara, A., Mokuno, Y. et al. (2010). Fabrication of 1 inch mosaic crystal diamond wafers. *Appl. Phys Express* 3: 051301.

138 Schreck, M., Mayr, M., Weinl, M. et al. (2020). Liftoff of single crystal diamond by epitaxial lateral overgrowth using SiO_2 masks. *Diamond Relat. Mater.* 101: 107606.

139 Mokuno, Y., Chayahara, A., Soda, Y. et al. (2006). High rate homoepitaxial growth of diamond by microwave plasma CVD with nitrogen addition. *Diamond Relat. Mater.* 15: 455–459.

140 Nad, S., Charris, A., and Asmussen, J. (2016). MPACVD growth of single crystalline diamond substrates with PCD rimless and expanding surfaces. *Appl. Phys. Lett.* 109: 162103.

141 Mokuno, Y., Chayahara, A., Yamada, H., and Tsubouchi, N. (2009). Improving purity and size of single-crystal diamond plates produced by high-rate CVD growth and lift-off using ion implantation. *Diamond Relat. Mater.* 18: 1258–1261.

142 Yamada, H., Chayahara, A., Umezawa, H. et al. (2012). Fabrication and fundamental characterizations of tiled clones of single-crystal diamond with 1-inch size. *Diamond Relat. Mater.* 24: 29–33.

143 Yamada, H., Chayahara, A., Mokuno, Y. et al. (2014). A 2-in. mosaic wafer of a single-crystal diamond. *Appl. Phys. Lett.* 104: 102110.

144 Schreck, M. (2009). Heteroepitaxial growth. In: *CVD Diamond for Electronic Devices and Sensors* (ed. R.S. Sussmann), 125–161. Chichester: Wiley.

145 Koizumi, S. and Inuzuka, T. (1993). Initial growth process of epitaxial diamond thin films on cBN single crystals. *Jpn. J. Appl. Phys.* 32: 3920–3927.

146 Yoshimoto, M., Yoshida, K., Maruta, H. et al. (1999). Epitaxial diamond growth on sapphire in an oxidizing environment. *Nature* 399: 340–342.

147 Zhu, W., Yang, P.C., and Glass, J.T. (1993). Oriented diamond films grown on nickel substrates. *Appl. Phys. Lett.* 63: 1640–1642.

148 Tachibana, T., Yokota, Y., Nishimura, K. et al. (1996). Heteroepitaxial diamond growth on platinum (111) by the Shintani process. *Diamond Relat. Mater.* 5: 197–199.

149 Schreck, M., Thürer, K.-H., and Stritzker, B. (1997). Limitations of the process time window for the bias enhanced nucleation of heteroepitaxial diamond films on silicon in the time domain. *J. Appl. Phys.* 81: 3092–3095.

150 Schreck, M., Bauer, T., Gsell, S. et al. (2003). Domain formation in diamond nucleation on iridium. *Diamond Relat. Mater.* 12: 262–267.

151 Schreck, M., Gsell, S., Brescia, R., and Fischer, M. (2017). Ion bombardment induced buried lateral growth: the key mechanism for the synthesis of single crystal diamond wafers. *Sci. Rep.* 7: 44462.

152 Gsell, S., Berner, S., Brugger, T. et al. (2008). Comparative electron diffraction study of the diamond nucleation layer on Ir(001). *Diamond Relat. Mater.* 17: 1029–1034.

153 Bernhard, P., Ziethen, C., Schoenhense, G. et al. (2006). Structural properties of the diamond nucleation layer on iridium analyzed by laterally resolved X-ray absorption spectroscopy. *Jpn. J. Appl. Phys.* 45: L984–L986.

154 Brescia, R., Schreck, M., Gsell, S. et al. (2008). Transmission electron microscopy study of the very early stages of diamond growth on iridium. *Diamond Relat. Mater.* 17: 1045–1050.

155 Lifshitz, Y., Köhler, T., Frauenheim, T. et al. (2002). The mechanism of diamond nucleation from energetic species. *Science* 297: 1531–1533.

156 Banhart, F. and Ajayan, P.M. (1996). Carbon onions as nanoscopic pressure cells for diamond formation. *Nature* 382: 433–435.

157 Wesolowski, P., Lyutovich, Y., Banhart, F. et al. (1997). Formation of diamond in carbon onions under MeV ion irradiation. *Appl. Phys. Lett.* 71: 1948–1950.

158 Lyutovic, Y. and Banhart, F. (1999). Low-pressure transformation of graphite to diamond under irradiation. *Appl. Phys. Lett.* 74: 659–660.

159 Zaiser, M., Lyutovich, Y., and Banhart, F. (2000). Irradiation-induced transformation of graphite to diamond: a quantitative study. *Phys. Rev. B* 62: 3058–3064.

160 Stehl, C., Fischer, M., Gsell, S. et al. (2013). Efficiency of dislocation density reduction during heteroepitaxial diamond for detector applications. *Appl. Phys. Lett.* 103: 151905.

161 Schreck, M., Schury, A., Hörmann, F. et al. (2002). Mosaicity reduction during growth of heteroepitaxial diamond films on iridium buffer layers: experimental results and numerical simulations. *J. Appl. Phys.* 91: 676–685.

162 Schreck, M., Mayr, M., Klein, O. et al. (2016). Multiple role of dislocations in the heteroepitaxial growth of diamond: a brief review. *Phys. Status Solidi A* 213: 2028–2035.

163 Schreck, M., Roll, H., and Stritzker, B. (1999). Diamond/Ir/$SrTiO_3$: a material combination for improved heteroepitaxial diamond films. *Appl. Phys. Lett.* 74: 650–652.

164 Dai, Z., Bednarski-Meinke, C., Loloee, R., and Golding, B. (2003). Epitaxial (100) iridium on A-plane sapphire: a system for wafer-scale diamond heteroepitaxy. *Appl. Phys. Lett.* 82: 3847–3849.

165 Gsell, S., Bauer, T., Goldfuss, J. et al. (2004). A route to diamond wafers by epitaxial deposition on silicon via iridium/yttria-stabilized zirconia buffer layers. *Appl. Phys. Lett.* 84: 4541–4543.

166 Gsell, S., Fischer, M., Bauer, T. et al. (2006). Yttria-stabilized zirconia films of different composition as buffer layers for the deposition of epitaxial diamond/Ir on Si(001). *Diamond Relat. Mater.* 15: 479–485.

167 Bauer, T., Gsell, S., Schreck, M. et al. (2005). Growth of epitaxial diamond on silicon via iridium/$SrTiO_3$ buffer layers. *Diamond Relat. Mater.* 14: 314–317.

168 Lee, K.H., Saada, S., Arnault, J.-C. et al. (2016). Epitaxy of iridium on $SrTiO_3$/Si(001): a promising scalable substrate for diamond heteroepitaxy. *Diamond Relat. Mater.* 66: 67–76.

169 Gsell, S., Schreck, M., Brescia, R. et al. (2008). Iridium on biaxially textured oxide templates: a concept to grow single crystals on arbitrary substrates. *Jpn. J. Appl. Phys.* 47: 8925–8927.

170 Gsell, S., Fischer, M., Schreck, M., and Stritzker, B. (2009). Epitaxial films of metals from the platinum group (Ir, Rh, Pt and Ru) on YSZ-buffered Si(111). *J. Cryst. Growth* 311: 3731–3736.

171 Fischer, M., Gsell, S., Schreck, M. et al. (2008). Preparation of 4-inch Ir/YSZ/Si(001) substrates for the large-area deposition of single-crystal diamond. *Diamond Relat. Mater.* 17: 1035–1038.

172 Schreck, M., Ščajev, P., Träger, M. et al. (2020). Charge carrier trapping by dislocations in single crystal diamond. *J. Appl. Phys.* 127: 125102.

173 Mermoux, M., Marcus, B., Crisci, A. et al. (2005). Micro-Raman scattering from undoped and phosphorous-doped (111) homoepitaxial diamond films: stress imaging of cracks. *J. Appl. Phys.* 97: 043530.

174 Fischer, M., Gsell, S., Schreck, M., and Bergmaier, A. (2012). Growth sector dependence and mechanism of stress formation in epitaxial diamond growth. *Appl. Phys. Lett.* 100: 041906.

175 Fischer, M., Brescia, R., Gsell, S. et al. (2008). Growth of twin-free hetero-epitaxial diamond on Ir/YSZ/Si(111). *J. Appl. Phys.* 104: 123531.

176 Gallheber, B.-C., Fischer, M., Mayr, M. et al. (2018). Growth, stress and defects of heteroepitaxial diamond on Ir/YSZ/Si(111). *J. Appl. Phys.* 123: 225302.

177 Gallheber, B.-C., Fischer, M., Klein, O., and Schreck, M. (2016). Formation of huge in-plane anisotropy of intrinsic stress by off-axis growth of diamond. *Appl. Phys. Lett.* 109: 141907.

178 Gallheber, B.-C., Klein, O., Fischer, M., and Schreck, M. (2017). Propagation of threading dislocations in heteroepitaxial diamond films with (111) orientation and their role in the formation of intrinsic stress. *J. Appl. Phys.* 121: 225301.

179 Aida, H., Kim, S.-W., Ikejiri, K. et al. (2016). Fabrication of freestanding hetero-epitaxial diamond substrate via micropatterns and microneedles. *Appl. Phys Express* 9: 035504.

180 Aida, H., Kim, S.-W., Ikejiri, K. et al. (2017). Microneedle growth method as an innovative approach for growing freestanding single crystal diamond substrate: detailed study on the growth scheme of continuous diamond layers on diamond microneedles. *Diamond Relat. Mater.* 75: 34–38.

181 Aida, H., Ikejiri, K., Kim, S.-W. et al. (2016). Overgrowth of diamond layers on diamond microneedles: new concept for freestanding diamond substrate by heteroepitaxy. *Diamond Relat. Mater.* 66: 77–82.

182 Kim, S.-W., Kawamata, Y., Chandra, S.N. et al. (2019). Electrical properties of 2-inch heteroepitaxial diamond substrate. *Poster presentation 5.82. at the Hasselt Diamond Workshop 2019 SBDD XXIV*, Hasselt, Belgium (13–15 March 2019).

183 Hiramatsu, K. (2001). Epitaxial lateral overgrowth techniques used in group III nitride epitaxy. *J. Phys. Condens. Matter* 13: 6961–6975.

184 Washiyama, S., Mita, S., Suzuki, K., and Sawabe, A. (2011). Coalescence of epitaxial lateral overgrowth-diamond on stripe-patterned nucleation on Ir/MgO(001). *Appl. Phys Express* 4: 095502.

185 Ando, Y., Kamano, T., Suzuki, K., and Sawabe, A. (2012). Epitaxial lateral over-growth of diamonds on iridium by patterned nucleation and growth method. *Jpn. J. Appl. Phys.* 51: 090101.

186 Tang, Y.-H. and Golding, B. (2016). Stress engineering of high-quality single crystal diamond by heteroepitaxial lateral overgrowth. *Appl. Phys. Lett.* 108: 052101.

187 Ichikawa, K., Kurone, K., Kodama, H. et al. (2019). High crystalline quality heteroepitaxial diamond using grid-patterned nucleation and growth on Ir. *Diamond Relat. Mater.* 94: 92–100.

188 Tallaire, A., Brinza, O., Mille, V. et al. (2017). Reduction of dislocations in single crystal diamond by lateral growth over a macroscopic hole. *Adv. Mater.* 29: 1604823.

189 Kidoguchi, I., Ishibashi, A., Sugahara, G., and Ban, Y. (2000). Air-bridged lateral epitaxial overgrowth of GaN thin films. *Appl. Phys. Lett.* 76: 3768–3770.

190 Strittmatter, A., Rodt, S., Reißmann, L. et al. (2001). Maskless epitaxial lateral overgrowth of GaN layers on structured Si(111) substrates. *Appl. Phys. Lett.* 78: 727–729.

191 Ohmagari, S., Yamada, H., Tsubouchi, N. et al. (2018). Large reduction of threading dislocations in diamond by hot-filament chemical vapor deposition accompanying W incorporations. *Appl. Phys. Lett.* 113: 032108.

192 Ohmagari, S., Yamada, H., Tsubouchi, N. et al. (2019). Toward high-performance diamond electronics: control and annihilation of dislocation propagation by metal-assisted termination. *Phys. Status Solidi A* 216: 1900498.

21

Diamond Wafer Technology, Epitaxial Growth, and Device Processing

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21.1 Diamond Epitaxial Growth and Wafers

Several material constants of diamond are superior to those of other materials [1–3]. Owing to its high reflectivity and variety of light absorption characteristics, which are attributed to the many types of color centers, diamond is one of the most famous gemstones. Diamond has also been commercialized in industry in mechanical tools and heat spreaders [4]. In addition, the electrical and thermal characteristics of diamond are superior to those of other materials, as summarized in Figure 21.1 [1]. These characteristics are considered attractive for realization of high-performance power devices.

Although most commercialized diamond is obtained by mining, recently, some artificial diamond has been commercialized [4–11]. The production of artificial diamond using the high-pressure high-temperature (HPHT) method was first reported in the 1950s [5]. Since then, this method has been adopted worldwide to produce mechanical tools, heat spreaders, and dies in industry. In this method, diamond crystals are grown in its stable phase in a finite region inside the apparatus [12]. This method produces bulk crystal with the highest crystal quality, meaning the lowest dislocation density and lowest impurity content [13]. Currently, diamond substrates produced using the HPHT method, with edge lengths that are typically 2–3 and 10 mm at most, are available for use in experiments in electronics and spintronics. Recently, a diamond "block" with an almost 1-in. diameter was reported by a Russian company; however, its internal features were unclear [14]. Using this method, it is extremely difficult to realize a several-inch-size wafer because of practical difficulties. Chemical vapor deposition (CVD) is another technique used to grow diamond crystal artificially [15]. Artificial diamond grown using microwave (MW) plasma CVD was first reported as CVD-grown diamond in the 1980s [15]. Since then, several CVD methods have been used to grow diamond, including

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

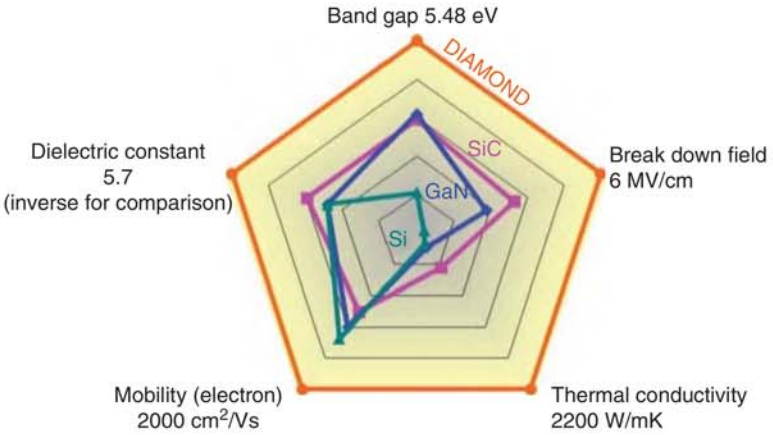


Figure 21.1 Electrical and thermal characteristics of diamond and other semiconductor materials. Source: Koizumi et al. [1]. © 2008, John Wiley & Sons.

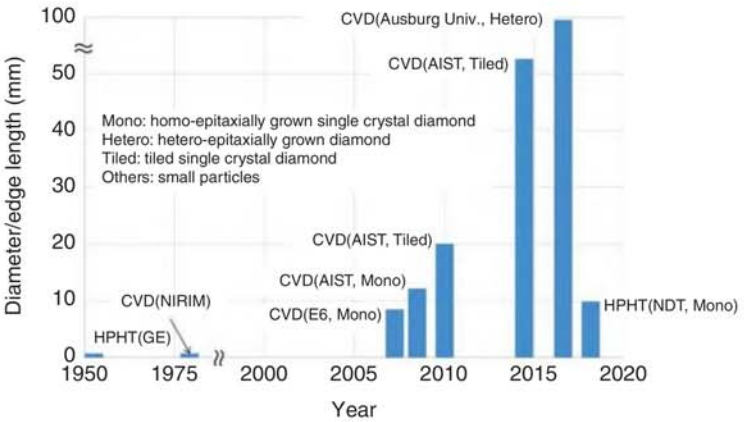


Figure 21.2 Progress made in the development of artificial diamond. Source: Element six [6]; Light Box Jewelry Inc [10]; Haruta et al. [17]; Ohtake and Yoshikawa [18]; Matsui et al. [19]; SP3 diamond technologies [20]; Ohmagari et al. [21] and Mokuno et al. [22]. GE, NIRIM, E6, AIST, and NDT represent General Electric Company in the US, the National Institute for Research in Inorganic Materials in Japan, Element Six in the UK, National Institute of Advanced Industrial Science and Technology in Japan, and New Diamond Technology in Russia, respectively.

(pulse-) direct current (DC) plasma, inductively coupled plasma (ICP), plasma-jet, flame, and hot-filament (HF) CVD [16–21]. In these methods, the vapor phase for the crystal growth is filled with the source gas mixture, which typically consists of hydrogen and methane. Then, this source gas mixture is dissociated into radicals; this process is promoted by plasma or highly heated filaments. These radicals react, and diamond crystals grow on the substrate. Figure 21.2 summarizes the progress made in the sizes of reported and commercialized artificial diamond.

As described above, the HPHT method can be used to synthesize crystals with the highest quality because the growth mode, in which the crystal grows three

dimensionally, is well established [13]. Because the dislocations extend from the seed crystal almost vertically to the top surface of the seed substrate, one may extract crystal from extended regions where dislocations are suppressed. This high-quality region is then re-used as the seed crystal to obtain a reduced dislocation density. However, such a three-dimensional growth mode is not well established for CVD [22–24]. An HPHT-made single-crystal diamond is typically adopted as the seed substrate for CVD growth. Therefore, the size and quality of CVD-made diamond is limited by the characteristics of the HPHT-made diamond, which is one of the major issues for the preparation of wafers with large area and sufficient quality. This issue must be solved for realization of industrial use, especially for electronics.

To increase the size of the seed substrate, one may attempt to repeat the growth on several {001} surfaces [25]. Using a substrate with 7–8-mm edge lengths, a half-inch-size substrate was demonstrated. However, it is not easy to grow diamond with thicknesses larger than several millimeters [22, 25, 26] because of the generation of undesired miscellaneous crystals and the thermally non-equilibrium environment of the growth [26–29]. In addition to the growth on the substrate, undesired miscellaneous crystals grow on the holder as well as the edges of the substrate. Such miscellaneous crystals act as antennas, leading to undesired concentration of the plasma for plasma CVD; therefore, the growth may need to be stopped to prevent drifting of the growth condition before the generation of these undesired miscellaneous crystals. To prepare a millimeter-thick crystal, one may thus repeat the growth with thicknesses of 0.1 mm or less [30]. The introduction of oxygen has been shown to reduce the appearance of these miscellaneous crystals [31]. Although the growth rate is also reduced in this case, the total growth thickness for a batch is increased. The thermally non-equilibrium environment is attributed to the locally concentrated plasma distribution with high temperature (approximately 3000 K) [27–29]. The hottest region is approximately 10 mm above the top substrate, where the temperature is maintained at approximately 1000–1300 K. Therefore, a steep temperature gradient of several 1000 K exists around the substrate, which may induce the generation of large internal stress inside the substrate. The use of pulse-mode discharge has been shown to reduce the gas temperature to some extent [32]. Optimization of the substrate holder shape is also effective for reducing the temperature gradation inside the substrate. These techniques enable several-millimeter-thick bulk crystal to be obtained, as shown in Figure 21.3.

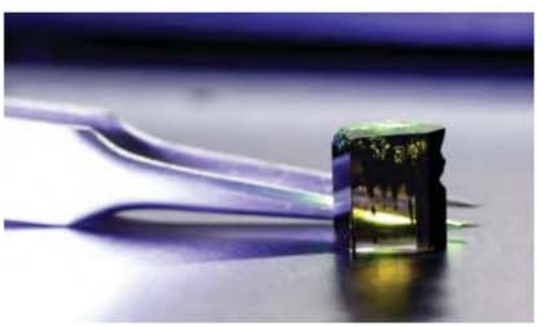


Figure 21.3 Example of bulk crystal with 10-mm thickness grown on 10 mm^2 square seed substrate using microwave plasma CVD.

Figure 21.4 Tiled clone with 20-mm edge, where four single-crystal diamond substrates with 10-mm edges were connected with each other.

Other approaches to obtain a diamond substrate with large area are tiling and hetero-epitaxial growth [33–36]. The concept of tiling was proposed in the 1990s for diamond; however, it is difficult to obtain a smooth boundary without cracking and/or non-epitaxial components [37]. It was observed that freestanding substrates made from identical seed substrate could be connected with each other smoothly [38]. In this case, although dislocations and stressed regions are still present near the boundaries, the boundaries could be made very smoothly, and such so-called "tiled-clones" could also be used for the seed substrate to obtain wafers with the same area and even to connect them to enlarge the area. Figure 21.4 shows an example of a tiled clone, where four single-crystalline diamond substrates with 10-mm edges were connected.

Another approach is to use hetero-epitaxial diamond. In this case, diamond is grown on another material, such as yttrium-stabilized zirconia (YSZ) or iridium [35]. Bias-enhanced nucleation (BEN) is used to promote nucleation before the growth. The dislocation density is therefore higher than that of homo-epitaxial single-crystalline diamond. This value can be reduced if a diamond layer of several 100 μm is grown [39].

Several attempts to improve the crystal quality of CVD-made diamond have been made [40–42]. Dislocations, which are present in the seed crystal, extend into the CVD-grown layers grown on the seed. The direction of the dislocations can be controlled by the off-angle of the top surface of the substrate [40]. However, the direction is limited to almost the same angle with the off-angle, and therefore, it is almost impossible to eliminate the dislocations. Lateral growth is a promising method to avoid the extension of the dislocations [41]. One may fabricate a specific structure to promote the lateral growth in a limited area on the top surface of the substrate. Furthermore, metal nanoparticles can be placed just above the locations of dislocations [42]. In these two cases, the regions just above the structure and nanoparticles can act as the origins of the dislocations. Another option to improve the crystal quality is growth into several {001} surfaces [25, 43].

For CVD, oxygen and nitrogen are sometimes introduced into the source gas mixture in addition to hydrogen and methane [18, 38, 43–48]. In the beginning of the study of the CVD growth of diamond, the "Bachmann diagram" was proposed,

where the fractions of hydrogen, methane, and oxygen are indicated for diamond growth [46]. Oxygen is known to have the effects of etching and improvement of the crystal quality [18, 45]. Therefore, this gas is sometimes adopted for pre-processing of the growth and even introduced during the growth [49]. Nitrogen is known to enhance the growth rate and promote preferential growth in ⟨001⟩ directions [38, 47, 48]. Frequently, substrates with {001} surfaces are adopted to grow diamond crystals because twin crystals are easily generated on {111} surfaces and the growth rate of {111} is usually lower than that of {001} surfaces. Therefore, especially to obtain bulk crystals using CVD, a small amount, on the order of ppm, of nitrogen is introduced. Nitrogen generates deep-level impurities (≈1.7 eV), which makes the crystal semi-insulating. Other impurities, such as boron and phosphine are also introduced to yield p- and n-type conductivity, whose impurity levels are 0.37 eV above the valence band maximum and 0.57 eV below the conduction band minimum, respectively [50–52]. Increasing these impurities is known to reduce the resistivity and generate soot inside the vacuum vessel for microwave plasma CVD [50]. Recently, HFCVD has been used to grow single-crystal diamond films with high-density boron without soot formation; however, metals of the wire were also incorporated. In addition to the low resistivity, some effects that reduce killer defects have been observed with the use of HFCVD [51]. For HPHT, carbon sources are supplied throughout catalytic metals, such as Ni, onto a seed crystal, because of the temperature gradient inside the apparatus, where an environment for achieving a diamond stable phase is realized. Therefore, catalytic metals can be incorporated into the crystals.

The growth mechanism of CVD diamond crystals has been studied from the viewpoint of gas phase analyses as well as surface reactions [53, 54]. CH_3 is considered one of the most important precursors that directly contributes to the crystal growth [53–56]. The models proposed in these preceding works suggest that the growth rate is proportional to the concentration of CH_3 near the top surface of the substrate. Some agreement with experimentally obtained growth rates was observed; however, the agreement was limited to the central region of the substrate [57]. Usually, the growth rate has a convex profile in the horizontal direction in experiments [57, 58]. However, the distribution of CH_3 near the top surface of the substrate has concave profiles [18, 27, 29]. To understand this gap between theoretical predictions and experimental results in terms of the distribution of the growth rate, the contributions from other radicals with large numbers of lone pair electrons and the non-uniformity of the substrate temperature may need to be considered [29, 57]. Understanding of the fundamental reaction processes of the impurities mentioned above in addition to those of hydrocarbon radicals require rather extensive work [53, 54].

Once a diamond crystal is obtained, further processing may be required, for example, to prepare freestanding wafers and/or a specific structure. One promising processing technique is laser irradiation. A pulsed laser with nano-second frequency is utilized, in which the transformation from the diamond structure into graphite is realized by local absorption of the incident laser and its thermal activation [59]. Use of a pico- and femto-second pulsed laser is considered to result in a gentler cutting process because its transformation mechanism is based on electronic excitation

[60, 61]. Using this method, one may be able to separate the CVD-grown layers from the seed substrate. However, because of the incident angle and finite diameter of the beam waist, the separation process from the substrate with larger size requires larger kerf loss. It is also possible to separate the CVD-grown layers by preparing patterned notches between the substrate and CVD layers before the growth [36, 62]. Use of high-speed ion implantation is another option to prepare freestanding wafers [25, 63]. This method can be applied for inch-size wafers [33, 38]. In addition to cutting and slicing, polishing is also necessary; diamond is one of the hardest and most fragile materials. One of the most conventional polishing techniques is scaif polishing [64–67]. This mechanical polishing process, in which iron plates with diamond particles are used as polishing plates, is known to damage the surfaces. SiO_2 plates are also adopted as polishing plates, and the redox reaction is expected to contribute to polishing of the surface [68]. Chemical reactions, ultra violet (UV) light, and plasma are also known to promote polishing of diamond surfaces [69–71]. Atomically flat surfaces have been achieved using photon–phonon etching [72]. A method to process the as-grown surface into such a super fine structure within a realistic time for inch-size substrates remains to be established.

The current state of the art of diamond epitaxial-growth and wafers has been summarized. In this decade, substrates with several millimeters in edge length and even inch-size substrates have become commercially available. To realize this achievement, techniques to prepare bulk crystals, including both growth techniques and processing techniques, have been developed. Many works studying the internal plasma chemical reactions both numerically and experimentally have elucidated part of the mechanism of the crystal growth. However, the fundamental concepts of growth apparatuses that are currently commercially available were proposed more than 10 years ago. A detailed understanding of the growth mechanisms may result in further development to help overcome the current status. This apparatus development would also enable the preparation of seed substrates of larger size and sufficient quality.

21.2 n-Type Doping and Processing

n-Type conductivity control by impurity doping has been one of the great challenges for CVD diamond, which tends to be an essentially p-type semiconductor, such as the natural gemstone "Blue Diamond." The introduction of n-type conductivity is theoretically possible by doping with group V impurities as well as silicon, whereas the incorporation of impurity atoms into substitutional sites of the diamond lattice is limited because of the toughness and dense covalent bond length of carbons. Nitrogen is one potential candidate owing to its similar covalent bond length (0.77 Å) to diamond (0.74 Å). However, the donor level of substitutional nitrogen is extremely deep at ~1.7 eV, below the bottom of the conduction band minimum, because of its structural distortion from the substitutional site. Therefore, improvement of the electrical conductivity at room temperature cannot be expected with nitrogen doping. However, the covalent bond length of phosphorus is approximately

1.1 Å, which is approximately 1.5 times larger than that of carbon. Phosphorus can be experimentally incorporated into the substitutional sites of the diamond lattice and forms a donor level at ~0.57 eV, which is currently the shallowest donor level in diamond semiconductors.

Phosphorus-doped diamond films have been homo-epitaxially grown by plasma-enhanced chemical vapor deposition (PECVD) using microwaves of 2.45 GHz [73, 74]. The source gas used is a mixture of pure hydrogen and methane, and n-type doping is achieved by introducing a phosphorus-based gas into the gas mixture. Phosphine, PH_3, used in general semiconductor processes is mainly used as a phosphorus dopant; phosphorus doping can also be achieved using an organic phosphorus-based gas, e.g. trimethyl-phosphine or tertiary-butyl-phosphine [75]. Typical gas flow rates of CH_4/H_2 are approximately 0.05–1%, and the ratio of PH_3/CH_4 varies from 1 ppm to 50% to cover wider phosphorus doping levels from 10^{15} to 10^{20} cm^{-3}. The total gas flow, substrate temperature, pressure, and microwave power are 1000 sccm, ~900 °C, 150 Torr, and 3600 W, respectively. Figure 21.5 shows typical process windows for phosphorus and boron doping of CVD diamond. For boron doping, the concentrations given by the open circles and triangles monotonically increase with increasing B_2H_5/CH_4 gas flow ratio during CVD growth without any restriction of (001) and (111) crystal orientations. For (111) phosphorus doping, marked by closed triangles, a similar tendency is observed in the low-concentration region; however, saturation starts in the region with concentrations exceeding 10^{19} cm^{-3}. For the (001) phosphorus doping, indicated by closed circles, the incorporation itself is extremely difficult compared with that for (111) doping, and the incorporation efficiency is two orders of magnitude lower than that for (111) phosphorus doping. This strong orientational dependence and the saturation tendency in the heavily doped region are typical for phosphorus doping and are caused by the steric barrier resulting from the large difference in the covalent bond length between phosphorus and carbon atoms. According to first-principles calculation, the formation energy of phosphorus atoms on the diamond surface is much lower than that in the bulk, indicating that phosphorus tends to segregate on the diamond surface during growth. This trend is stronger for phosphorus than for boron and stronger on (001)-oriented surfaces than on (111)-oriented surfaces [76].

Conductivity control by impurity doping is a fundamental component of the device fabrication process. From the viewpoint of the device active layer, higher carrier mobility achieved through light doping is preferable, whereas heavy doping is preferable for lower resistance including ohmic contact. In a general compensated semiconductor, the p-type or n-type character is determined by the relationship between the donor and acceptor densities (N_D and N_A, respectively) in the semiconductor. $N_D > N_A$ indicates n-type conductivity, and vice versa. Therefore, suppression of N_A is essential for light n-type doping as well as N_D control. N_A is the density of electron capture states, including boron acceptors, vacancy defects, and their complexes. To realize light n-type control, a metal CVD reactor compatible with ultra-high vacuum equipped with a load–lock system was developed to suppress the unintentional incorporation of other impurities. The plasma condition was modified for efficient dissociation of source gas mixtures

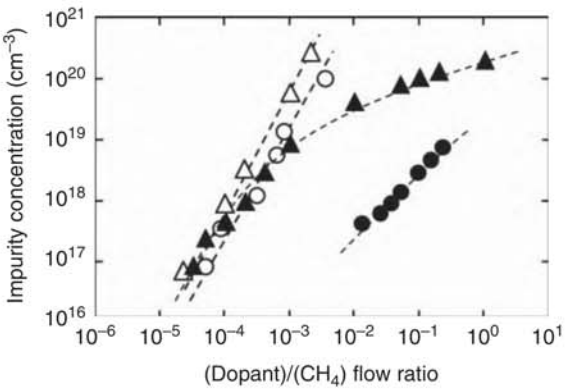


Figure 21.5 Typical process windows for phosphorus and boron doping of CVD diamond. The open and closed markers are data for boron and phosphorus doping, respectively. The circles and triangles represent (001) and (111) crystal orientations, respectively.

and radical generation for growth precursor. The off angle and direction of the initial substrate were also optimized to enhance the step-flow growth. These comprehensive parameter controls have enabled stable n-type doping even for lower phosphorus concentrations down to 10^{15} cm^{-3} [52].

Figure 21.6 shows the typical temperature dependence of the carrier concentration and mobility for a lightly n-type diamond film with phosphorus concentration of 3×10^{15} cm^{-3}. A negative Hall coefficient was measured in the entire temperature range, indicating thermally activated band conduction due to donor electrons. Through least-squares fitting using the theoretical formula accounting for carrier compensation, a donor level of ~0.57 eV due to the substitutional phosphorus was clearly achieved with N_D of approximately 3×10^{15} cm^{-3}, which is almost equal to the phosphorus concentration estimated by secondary ion mass spectrometry (SIMS). Most of the phosphorus atoms were incorporated into diamond substitutional sites and acted as donors. The electron mobility depends on the measurement temperature with a combination of electron scattering mechanisms, including those

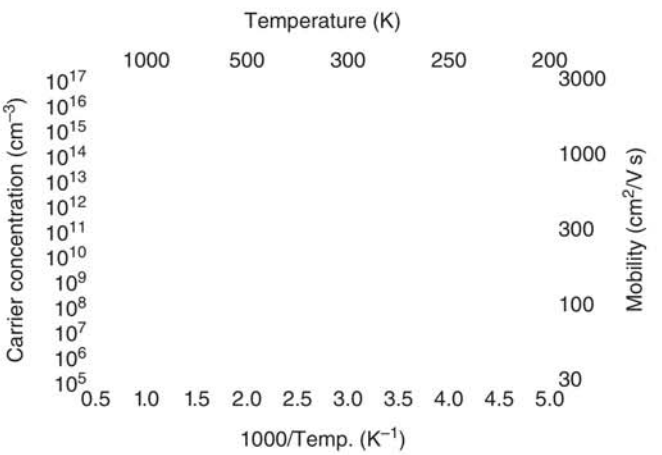


Figure 21.6 Typical temperature dependence of carrier concentration and mobility for lightly n-type diamond film with phosphorus concentration of 3×10^{15} cm^{-3}.

of acoustic phonons, valley phonons, ionized impurities, and neutral impurities [77]. For a phosphorus concentration of approximately $10^{18}\,cm^{-3}$, electron scattering due to ionization and/or neutral impurities is dominant, whereas for light phosphorus doping of approximately $10^{15}\,cm^{-3}$, the effect of these impurities is suppressed and acoustic phonon scattering is dominant. As observed in Figure 21.6, the electron mobility monotonically increases with decreasing measurement temperature with a $T^{-3/2}$ relationship, with the highest electron mobilities recorded at room temperature and 220 K of 1060 and $1500\,cm^2/(V\,s)$, respectively.

Heavy phosphorus doping is also important for device fabrication processes. Because of its deep dopant level of approximately 0.57 eV, only a low free-carrier concentration of approximately 10^9–$10^{11}\,cm^{-3}$ is thermally generated from the dopants at room temperature, resulting in a high specific resistance of approximately $10^6\,\Omega\,cm$. For a deep dopant such as diamond, when the doping concentration increases, the carrier transport mechanism changes from band conduction to hopping conduction through dense donor states, and this hopping conduction can easily result in lower resistivity. The specific resistance at room temperature becomes lower than $10^2\,\Omega\,cm$ through nearest-neighborhood-hopping conduction when the phosphorus concentration exceeds $10^{20}\,cm^{-3}$. In addition, another issue for n-type diamond is that ideal Ohmic contact has not yet been realized because of a deep pinning level around E_C-4.3 eV at the phosphorus-doped diamond/metal interface [78]. A realistic solution is to improve the injection efficiency by narrowing the barrier width through heavy doping [79]. Figure 21.7 shows changes of the barrier width of a semiconductor/metal interface and the contact resistance as a function of phosphorus concentration. The barrier width was calculated from the space-charge-layer width assuming a Schottky barrier height of 4.3 eV. The contact resistance was estimated using the transfer-length method based on circular-type transfer length method (TLM) pattern electrodes. With increasing phosphorus concentration, the barrier width drastically decreases down to the order of a few nanometers, and the contact resistance decreases accordingly by orders of

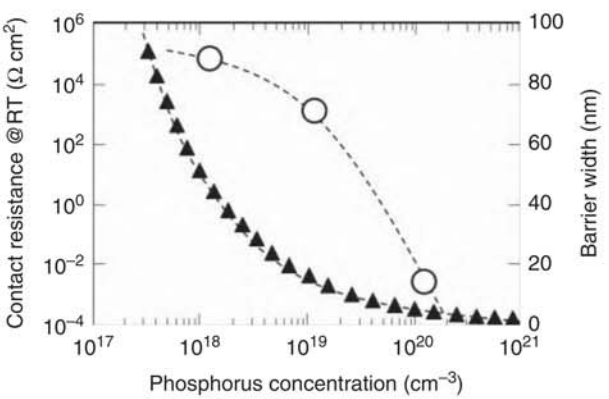


Figure 21.7 Changes of the barrier width of semiconductor/metal interface and the contact resistance as a function of phosphorus concentration. The open circles and closed triangles represent data for contact resistance and barrier width, respectively.

magnitude. The barrier width would be narrow enough for tunneling through the barrier to occur with heavy phosphorus doping.

The control of n-type conduction is an important subject for diamond semiconductors. Although issues remain to be solved, such as lower resistance and ideal ohmic contact, n-type control has finally been realized through phosphorus doping using microwave plasma CVD. This technical innovation based on n-type doping has led to the development of diamond electronic devices, such as high-blocking-voltage PIN diodes [80, 81], inversion channel metal oxide semiconductor field-effect transistors (MOSFETs) [82], and quantum applications based on nitrogen-vacancy complexes [83, 84].

21.3 p-Type Doping and Processing

Boron (B) is the most reliable and widely used element for controlling p-type conduction in diamond. Substitutionally incorporating B atoms into the diamond lattice produces the shallowest known acceptor level of 0.37 eV above the valence-band maximum. As compared with other semiconducting materials (e.g. Si, SiC, GaN, and Ga_2O_3), the activation energy is rather high, limiting the hole ionization at room temperature: the carrier concentration is limited to ~1% of the doping concentration. Full ionization of B for a lightly doped epilayer can be realized above 450 K [85]. High-temperature operation is one effective solution to exploit the full potential of diamond electronics. Superior device performance at elevated temperature has been demonstrated for Schottky barrier diodes (SBDs) [86] and metal–semiconductor field-effect transistors [87].

To control the doping concentration, in situ doping can be applied. Neither the thermal diffusion process nor the ion-implantation technique are well established for diamond. The former process is limited by the negligible diffusion coefficient in a realistic temperature range, and the latter technique is hampered by the lattice damage introduced by the highly energetic ions. Ion implantation is only applicable for the p^+ contact region and junction termination extension (JTE) structure, which requires a high doping concentration $>10^{19}\,cm^{-3}$ in a selective area. To realize an optimum doping profile with p-type conduction, a B-containing source gas (diborane: B_2H_6 or trimethylboron: $B(CH_3)_3$) is introduced during CVD growth.

Figure 21.8 shows the relationship between the film resistivity (ρ) and effective doping concentration (N_A–N_D) at room temperature [88]. ρ is modified widely from 10^5 to $10^{-3}\,\Omega$ cm by controlling the doping concentration from 10^{15} to $10^{21}\,cm^{-3}$. In the low-doping-concentration regime, ρ is largely affected by donor-like impurities (N_D). Reduction of background impurities, e.g. H, Si, N, O, is important to realize an optimum resistivity. Hole mobilities exceeding $2000\,cm^2/(V\,s)$ were confirmed by Hall effect measurements at room temperature; these values are larger than those of typical semiconducting materials. Polycrystalline films exhibit rather high ρ compared with that of single-crystal films because of the reduced mobility, which is mainly caused by carrier scattering by the grain boundaries. With increasing N_A–N_D, the carrier transport properties change from band

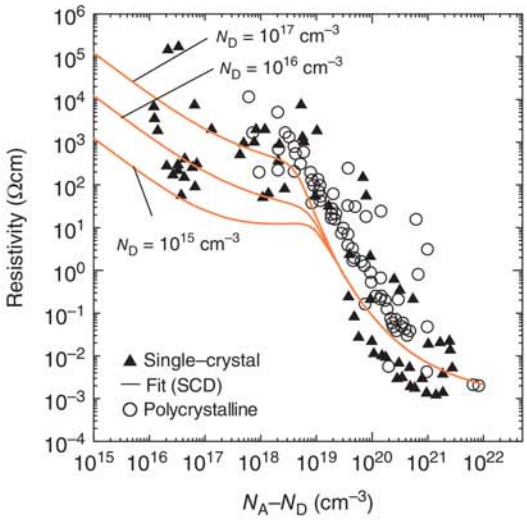


Figure 21.8 Resistivity as a function of effective B doping concentration (N_A–N_D). Source: The original version of this figure is presented in Werner et al. [88].

transport to nearest-neighbor-hopping conduction, which effectively decreases the apparent activation energy. This phenomenon is apparently observable for N_A–N_D $>10^{19}$ cm^{-3}. Above the metal–insulator-transition doping level (3×10^{20} cm^{-3}), the apparent activation energy becomes zero (degenerate semiconductors). Superconducting properties have been reported from such films [89].

To realize high-performance diamond electronics, reduction of electrically active killer defects is crucial. Threading dislocations (TDs) are major defects in CVD-grown diamond, and they are generally taken over from a substrate to an epitaxial layer or even proliferated from its interface [63]. Therefore, sophisticated surface treatment is a prerequisite [90]. UV-assisted ultra-flattening surface polishing can effectively suppress the dislocation emergence at the interface; however, existing dislocations in the substrate are all propagated during epitaxial growth. For III–V semiconductors such as gallium nitride (GaN), dislocation-reduction techniques, as represented by epitaxial lateral overgrowth (ELO), have been widely adopted [91]. This process requires a stripe mask pattern, which effectively terminates dislocations below the mask and only allows their propagation from opening windows. Their effectiveness has also been verified in heteroepitaxial diamond growth [92]. However, this method is only applicable for high dislocation densities ranging from 10^{10} to 10^6 cm^{-2}, and achieving further reduction of the dislocation density remains challenging.

Naamoun et al. proposed a technique to prevent TDs from propagating from the substrate to the CVD epitaxial layer using metal nanoparticles [42]. This concept is based on the selective revealing of dislocations by H_2/O_2 plasma etching followed by Pt nanoparticle self-assembly (island growth) in the etch-pit positions. After the subsequent CVD overgrowth, some of the TDs are annihilated by the metal nanoparticles. However, the overall dislocation density remains high ($\sim10^6$ cm^{-2}). Optimization of metal incorporation without introducing self-defects is therefore crucial. New dislocations emerging from the metal nanoparticles is another

problem that remains to be overcome. Ohmagari et al. proposed a technique called metal-assisted termination (MAT) to annihilate TD propagation through the incorporation of atomic-scale metal impurities [93]. In MAT, metal impurities that possess larger covalent radii than that of carbon atoms are randomly incorporated during epitaxial growth by CVD, suppressing TD propagation. This strategy was accomplished using hot-filament (HF) CVD with heated W wires. W ($\sim 10^{18}$ cm^{-3}) was incorporated as an impurity during epitaxial growth. After growth of a film with a thickness of several micrometers, the dislocation density decreased substantially from 10^6 cm^{-2} in the substrate to 10^4 cm^{-2} in the epilayer.

To investigate the effect of dislocation reduction, SBDs were fabricated. The thickness and B concentration of the drift layer were 3 μm and 1×10^{16} cm^{-3}, respectively. Two different device configurations were compared: Diode A (conventional SBDs without buffer layer) and Diode B (with MAT buffer layer). Mo/Au Schottky and Ti/Mo/Au Ohmic electrodes were prepared on an oxygen-terminated diamond surface. A total of 65 diodes (Schottky diameters of 100 μm) were fabricated on identical substrates, and the electrical characteristics were measured using a semiconductor parameter analyzer (Agilent Technologies Inc., B1505A). Figure 21.9a shows the typical J–V characteristics of Diode A. The diode properties were categorized into three groups depending on the leakage-current level at a reverse voltage of 5 V: (i) low leakage (below the detection limit), (ii) high leakage, or (iii) Ohmic-like (rectification ratio less than 10). The following results were reported for Diode A: 23 low-leakage diodes (35%), 39 high-leakage diodes (60%), and 3 Ohmic-like diodes (5%). The large leakage current may have originated from the high dislocation density of $\sim 10^6$ cm^{-2}. Breakdown behavior was observed at a reverse voltage of 50 V. In contrast, for Diode B, all 65 diodes exhibited low leakage, as observed in Figure 21.9b. The J–V curves of the examined diodes are superimposed, revealing their high uniformity. Breakdown was not observed up to 750 V, which was the limit of the apparatus.

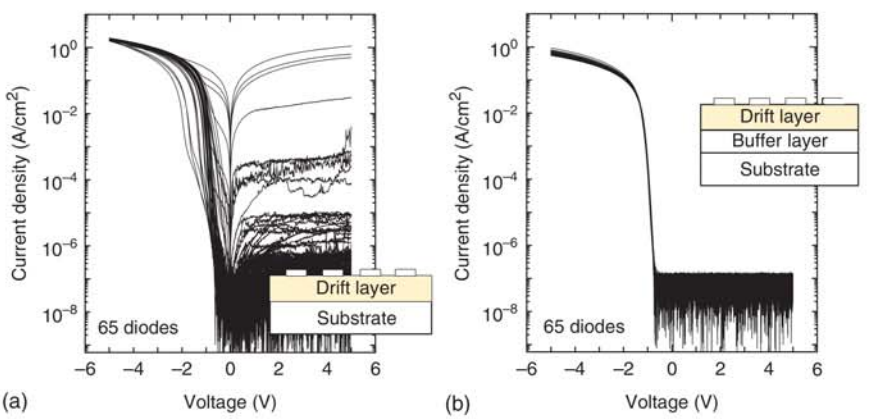


Figure 21.9 Electrical properties of diamond Schottky barrier diodes: (a) Diode A (normal epitaxy) and (b) Diode B (after insertion of buffer layer). A total of 65 Schottky contacts with diameters of 100 μm were fabricated on identical substrates, and their in-plane uniformity was evaluated.

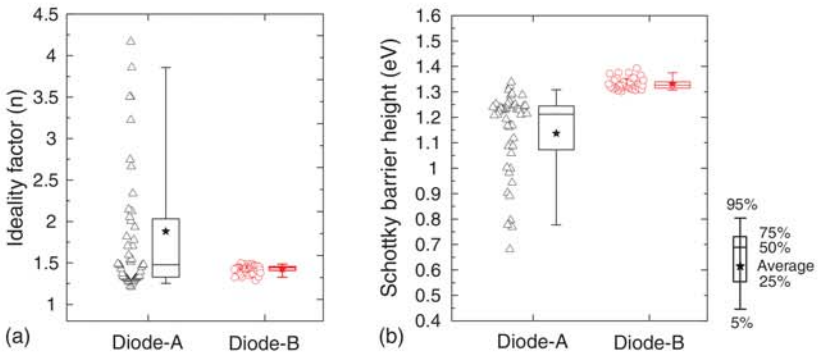


Figure 21.10 Distribution of SBD parameters of Diode A (normal epitaxy) and Diode B (after insertion of buffer layer): (a) Ideality factor and (b) Schottky barrier height.

Figure 21.10 presents the histogram analysis of the n and ϕ_B plots. Diode A showed discrete n and ϕ_B values: $n = 1.88$ (standard deviation 0.93) and $\phi_B = 1.14$ eV (standard deviation 0.17 eV). This tendency is often observed for diamond SBDs. The metal–semiconductor interface (i.e. oxygen termination) may have degraded because of the presence of defects [94]. Device B exhibited uniform forward characteristics: $n = 1.43$ (standard deviation 0.05) and $\phi_B = 1.33$ eV (standard deviation 0.02 eV). It was considered that highly uniform and stable oxygen termination was realized after the dislocation reduction.

The growth and physical properties of B-doped p-type diamond epilayers were briefly summarized. The film resistivity is widely controllable from 10^5 to 10^{-3} Ω cm with increasing B concentration from 10^{15} to 10^{21} cm^{-3}. To realize high-performance diamond electronics, a low-dislocation-density high-quality B-doped epilayer is indispensable. The electrical properties of a SBD with a p-type drift layer were non-uniform: good rectifying actions were observable; however, some diodes exhibited high leakage current. Highly uniform electrical properties were recently demonstrated after the insertion of a metal-containing buffer layer. Crystalline uniformity of the epilayer is important for handling high current with a large electrode.

21.4 Devices

Owing to its excellent material properties, diamond is the so-called "ultimate semiconductor" and is expected to reduce the power consumption and increase the operation frequency of circuits. A figure of merit (FOM) is a measure used to compare materials and how much devices can be improved. For power devices, Baliga introduced the following two important FOMs, Baliga's FOM (BFOM) and Baliga's high frequency FOM (BHFOM) [95]:

$$\text{BFOM} = \varepsilon\mu E_G^3 \cong {}^{V_{max}^2}/_{R_{on}A}$$

$$\text{BHFOM} = \mu E_B^2$$

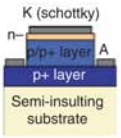
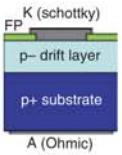
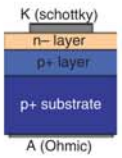
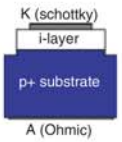
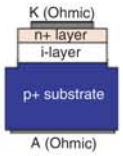
here, ε, μ, E_G, V_{max}, $R_{on}A$, and E_B are the dielectric constant, carrier mobility, bandgap energy, breakdown voltage, specific on-resistance, and avalanche breakdown field, respectively. The BFOM estimates the trade-off limit between conduction loss and the breakdown voltage of a unipolar device, and the BHFOM includes the switching loss of the gate capacitance of field-effect transistors (FETs). For both FOMs, diamond has advantages [96]. Huang also introduced FOMs such as the high-temperature FOM (HTFOM) and chip-area FOM (HCAFOM), which consider the actual switching behavior and estimated high temperature operation capability and reduction of chip area [97] (further details are provided in [96, 98]). As the FOMs of diamond are higher than those of other wide-bandgap semiconductors, the reported performance of experimentally fabricated diamond devices is not as high as that expected from the FOMs [98].

One of the major issues facing diamond is its low conductivity at room temperature, especially in the channel region and drift layer [96]. Only less than 5% of boron acceptors are activated at room temperature because of the large activation energies of impurity boron; accordingly, the resistivity becomes high. On the other hand, $R_{on}A$ of diamond becomes lower than that of SiC and GaN, and the advantage of using diamond is obvious when the operation temperature is higher than 100 °C. Another challenge is the poor device processing. Processing technology established for silicon devices, especially ion implantation and oxidation, are not applicable to diamond. Accordingly, edge-termination techniques, such as JTE, which can reduce the high electrical field peak at the edge of the electrode, cannot currently be applied for diamond [96]. The small size of a single-crystal diamond wafer (<4 mm) results in low reproducibility of the fabrication process. New device processing techniques need to be developed to increase the device performance up to the material limit.

To date, both unipolar and bipolar diodes, including p-type–intrinsic-n-type diodes (PiNDs), SBDs, junction barrier Schottky diodes (JBSDs), metal–intrinsic-p-type diodes (MiPDs), and Schottky pn diodes (SPNDs), have been experimentally reported. The cross-sectional structures and a summary of the device performances are presented in Table 21.1. The highest V_{max} (>11.5 kV) was achieved for a PiND without a mesa structure. The breakdown voltage decreased because the leakage current increased when a mesa structure was utilized. The decrease in the breakdown voltage is considered to result from structural effects at the mesa edges. The forward current density for bipolar diamond devices is low because of the short minority carrier lifetime.

The pseudo-vertical SBD (pVSBD) structure is well utilized for diamond diodes because of the high crystal quality and the ability to use a low-cost semi-insulating substrate. A heavily boron-doped p^+ type layer with 1–3 μm thickness is first grown on the semi-insulating substrate before the deposition of a lightly boron-doped p^- layer. Ohmic contacts are directly formed on the p^+ layer after selective etching of the p^- drift layer. In this structure, the depletion layer expands vertically through the drift layer and the forward current flows laterally in the p^+ layer [98]. The highest

Table 21.1 Diamond diodes.

Type	Unipolar				Bipolar
Device	**pVSBD**	**VSBD**	**SPND**	**MiPD**	**PiN**
Structure					
V_{max}	2.5 kV	1.8 kV	<100 V	2.5 kV	>10 kV
E_{max}	*>7 MV/cm*	*2.7 MV/cm*	*3.4 MV/cm*	*4.2 MV/cm*	3.4 MV/cm
I_{max}	0.5 A	20 A	<100 mA	<100 mA	<100 mA
J_{max}	*>4.5 kA/cm²*	*>1 kA/cm²*	*>60 kA/cm²*	*7.5 kA/cm²*	
Remarks	Stable interface @ 400 °C and X-ray	Fast turn-off @ 250 °C t_{rr} < 20 ns	No trade-off between $R_{on}S$ vs. V_{br}	Small temperature coefficient of R_{on}	Highest V_{max}
Challenge	Edge-termination current capability	Edge-termination defects	Low n-doping with low compensation	High current capability	Long lifetime of electron high n+ doping

Values of Emax and Jmax are italic.

reported BFOM is 244 MW/cm² on pVSBD using ozone surface oxidation [99]. For this device, no breakdown behavior was confirmed because of the measurement limit of the test equipment. A maximum breakdown field of 7.7 MV/cm was estimated from the doping concentrations in the p^- layer. $R_{on}A$ of pVSBD increased with increasing contact area because the lateral resistance of the p^+ layer limits the maximum current. Accordingly, VSBD is needed for high-current (>5 A) applications. Figure 21.11 shows the typical forward and reverse current–voltage characteristics of a VSBD [98]. The maximum reverse electrical field was 2.1 MV/cm, which is poorer than the ideal value of diamond, >10 MV/cm. The leakage current of diamond SBDs can be explained using a thermionic-field emission model considering the barrier lowering effect. This model agrees well with the measured leakage current even at elevated temperatures [99, 100].

One of the reasons for the premature breakdown at low electrical field is the breakdown at the edge of the electrode where the potential distribution becomes steep [98]. Field enhancement at the edge of the electrode can be experimentally visualized using electron-beam-induced current (EBIC) (for more details on the measurement mechanisms, refer to [101]). Figure 21.12a shows an EBIC image under biased

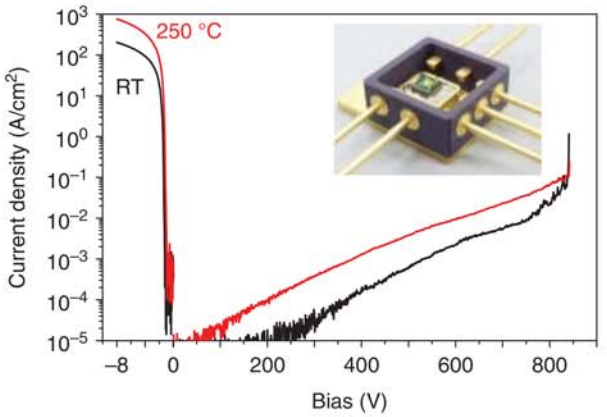


Figure 21.11 IV characteristics of diamond Schottky barrier diode and packaged device.

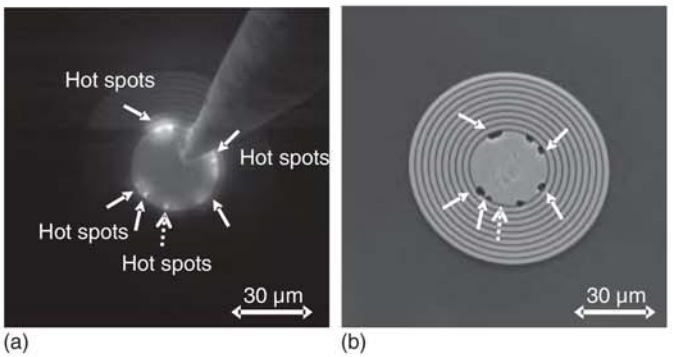


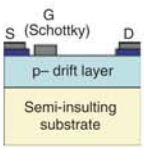
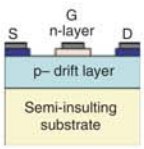
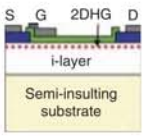
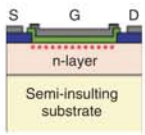
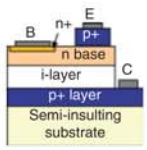
Figure 21.12 (a) EBIC image of diamond pVSBD with floating metal guard rings under biased condition, and (B) top view of the pVSBD after hard breakdown [102].

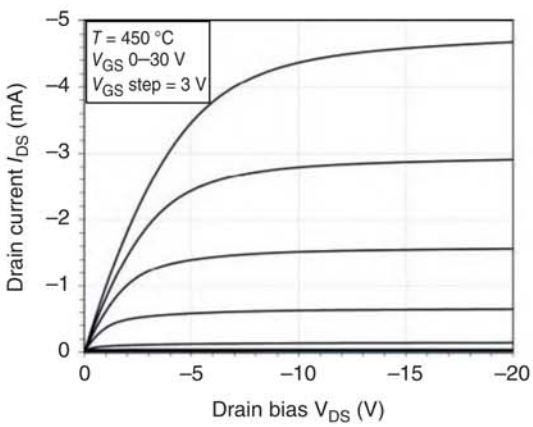
condition, and Figure 21.12b shows a top view after the hard breakdown of pVSBD with floating metal guard rings. As observed in these figures, hot spots appeared at the periphery of the main contact, and hard breakdown occurred at the spots [103]. One possible source of the hot spots is structural defects originating from the fabrication process, particularly the lithography and lift-off processes [101].

For switching devices, metal–semiconductor field-effect transistors (MESFETs), metal–insulator–semiconductor FETs (MISFETs) [104], junction FETs (JFETs) [105], hydrogen-terminated surface channel FETs (H-FETs), inversion-channel metal–oxide–semiconductor (MOS) FETs [82], and bipolar transistors have been realized. The typical device structures and a summary of the performances reported to date are provided in Table 21.2.

The first kV-class diamond FETs were realized on MESFETs [87]. Figure 21.13 shows the typical current–voltage characteristics of a MESFET operated at 450 °C

Table 21.2 Diamond switching devices.

Type	Unipolar				Bipolar
Device	**MESFET**	**JFET**	**H-FET**	**MOSFET**	**BJT**
Structure					
V_{max}	2.2 kV	>600 V	2 kV	<50 V	<50 V
E_{max}	2.1 MV/cm	*>6 MV/cm*	*3.6 MV/cm*		
I_{max}	1 A@250C	*450 A/cm²*	*12 kA/cm²*	<1 mA	<1 mA
J_{max}	*<3 mA/mm@250C*	*(bipolar mode)*			
Remarks	Stable operation @ 500 °C & after 10 MGy X-rays	Normally off high *T* Bipolar mode	Shallow channel $f_{max} > 100$ GHz Normally-on/off vertical structure	Inversion channel (normally-off)	
Challenge	Vertical structure	Vertical structure High n+ doping	Reliability Doping control	High Vr Vertical structure Mobility	Long lifetime of electron low n+ layer resistivity



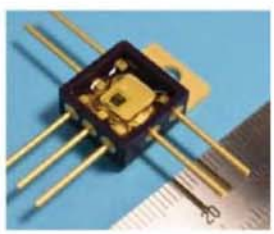


Figure 21.13 IDS-VDS characteristics of diamond MESFET operated at 450 °C and packaged device. Source: Koizumi et al., [96]. copyright 2018, Elsevier.

[87] and of a discrete FET mounted on a metal–ceramics package. Increasing the gate–drain distance (L_{GD}) allows wide expansion of the depletion layer from the gate to the drain; accordingly, V_{max} can be increased from 700 to 1500 V when L_{GD} is increased from 5 to 30 μm. Without considering field spikes at the drain edge of the gate electrode, E_{max} was estimated to be 2.15 MV/cm. The MESFET works with low gate leakage current even at high temperature owing to its high Schottky barrier height.

The highest current density of diamond FETs (>12 kA/cm^2) was achieved on a surface channel diamond FET [106] using vertical configuration. The FET uses a p-type 2D channel formed by surface hydrogen termination [107]. Similar to a MESFET, V_{max} of hydrogen-terminated surface channel FETs can be increased to 2 kV by increasing L_{GD} to 24 μm.

An inversion-type p-MOSFET has been realized utilizing OH termination on (111) diamond [82]. A phosphorous-doped n-type layer was used for the body, and Al_2O_3 deposited by atomic layer deposition was used as the gate insulator. The inversion mobility was limited to 20 cm^2/(V s) because of the high interface state density (1×10^{13}/[cm^2 eV]).

References

1 Koizumi, S., Nebel, C.E., and Nesladek, M. (eds.) (2008). *Physics and Applications of CVD Daimond*. Weinheim: Wiley-VCH.

2 Fujimori, N. and Shikata, S. (eds.) (2008). *Frontier of Diamond for Electronics Applications*. CMC Publishing Co., Ltd. (in Japanese).

3 Yoshikawa, M., Suzuki, K., Ohtake, N. et al. (eds.) (2007). *Comprehensive Bibliography of Diamond Technology*. Tokyo: NGT Ltd. (in Japanese).

4 Olson, D.W. (2016). *Diamond, Industrial. U.S. Geological Survey Minerals Yearbook 2016*, 21.1–21.12. U.S. Geological Survey.

5 Sumitomo Electric Industries, Ltd. www.sumitool.com/en/products/diamond-cbn/ (accessed 31 January 2020).

6 Element six, a member of the De Beers Group of Companies. e6cvd.com/us/application/all.html (accessed 31 January 2020).

7 EDP Corp. www.d-edp.jp (accessed 30 December 2019).

8 New Diamond Technology. ndtcompany.com/ (accessed 31 January 2020).

9 Augsburg Diamond Technology GmbH. www.audiatec.de/index.html (accessed 31 January 2020).

10 Light Box Jewelry Inc. lightboxjewelry.com/ (accessed 30 December 2019).

11 Bundy, F.P., Hall, H.T., Strong, H.M., and Wentorf, R.H. Jr., (1955). Man-made diamonds. *Nature* 176: 51–55.

12 D'Haenens-Johansson, U.F.S., Katrusha, A., Moe, K.S. et al. (2015). Large colorless HPHT synthetic diamonds from new diamond technology. *Gems Gemol.* 51 (3): 1–16.

13 Sumiya, H. and Tamasaku, K. (2012). Large defect-free synthetic Type IIa diamond crystals synthesized via high pressure and high temperature. *Jpn. J. Appl. Phys.* 51: 090102 (4pages).

14 Katrusha, A. (2017). Fabrication and properties of ultra-large (<100 carat) Type IIa colorless synthetic diamonds. *Invited talk at the International Conference on Diamond and Carbon Materials (ICDCM) in Gothenbrg*, Sweden (6 September 2017).

15 Kamo, M., Sato, Y., and Matsumoto, S. (1983). Diamond synthesis from gas phase in microwave plasma. *J. Cryst. Growth* 62 (3): 642–644.

16 Chae, K.-W., Baik, Y.-J., Park, J.-K., and Lee, W.-S. (2010). The 8-inch free-standing CVD diamond wafer fabricated by DC-PACVD. *Diamond Relat. Mater.* 19: 1168–1171.

17 Haruta, Y., Fujimoto, K., Horita, S. et al. (2013). Time evolution in radiation intensities of C_2 and H spectra in $Ar/CH_4/H_2$ pulse modulated induction thermal plasmas for diamond film deposition. *J. Phys. Conf. Ser.* 441: 012017.

18 Ohtake, N. and Yoshikawa, M. (1993). Effects of oxygen addition on growth of diamond film by Arc discharge plasma jet chemical vapor deposition. *Jpn. J. Appl. Phys.* 32: 2067–2073.

19 Matsui, Y., Yuuki, A., Sahara, M., and Hirose, Y. (1989). Flame structure and diamond growth mechanism of acetylene torch. *Jpn. J. Appl. Phys.* 28: 1718–1724.

20 SP3 Diamond Technologies. www.sp3diamondtech.com/ (accessed 1 January 2020).

21 Ohmagari, S., Yamada, H., Tsubouchi, N. et al. (2019). Toward high-performance diamond electronics: control and annihilation of dislocation propagation by metal-assisted termination. *Phys. Status Solidi A* 216 (21): 1900498.

22 Mokuno, Y., Chayahara, A., Yamada, H., and Tsubouchi, N. (2010). Improvements of crystallinity of single crystal diamond plates produced by lift-off process using ion implantation. *Diamond Relat. Mater.* 19: 128–130.

23 Muehle, M., Asmussen, J., Beckera, M.F., and Schuelke, T. (2017). Extending microwave plasma assisted CVD SCD growth to pressures of 400 Torr. *Diamond Relat. Mater.* 79: 150–163.

24 Silva, F., Achard, J., Bonnin, X. et al. (2008). Single crystal CVD diamond growth strategy by the use of a 3D geometrical model: growth on (113) oriented substrates. *Diamond Relat. Mater.* 17: 1067–1075.

25 Mokuno, Y., Chayahara, A., Yamada, H., and Tsubouchi, N. (2009). Improving purity and size of single-crystal diamond plates produced by high-rate CVD growth and lift-off process using ion implantation. *Diamond Relat. Mater.* 18: 1258–1261.

26 Nad, S., Gu, Y., and Asmussen, J. (2015). Growth strategies for large and high quality single crystal diamond substrates. *Diamond Relat. Mater.* 60: 26–34.

27 Lombardi, G., Hassouni, K., Stancu, G.-D. et al. (2005). Modeling of microwave discharges of H_2 admixed with CH_4 for diamond deposition. *J. Appl. Phys.* 98: 053303.

28 Yamada, H. (2012). Numerical simulations to study growth of single-crystal diamond by using microwave plasma chemical vapor deposition with reactive (H, C, N) species. *Jpn. J. Appl. Phys.* 51: 090105.

29 Yamada, H., Chayahara, A., and Mokuno, Y. (2018). Effect of Ar addition on uniformity of diamond growth by using microwave plasma chemical vapor deposition. *Diamond Relat. Mater.* 87: 143–148.

30 Feng, Z.B., Chayahara, A., Mokuno, Y. et al. (2010). Raman spectra of a cross section of a large single crystal diamond synthesized by using microwave plasma CVD. *Diamond Relat. Mater.* 19: 171–173.

31 Yamada, H., Chayahara, A., and Mokuno, Y. (2020). Method to increase the thickness and quality of diamond layers using plasma chemical vapor deposition under (H, C, N, O) system. *Diamond Relat. Mater.* 101: 107652.

32 Yamada, H., Chayahara, A., and Mokuno, Y. (2016). Short-pulse excitation of microwave plasma for efficient diamond growth. *Appl. Phys. Lett.* 109: 092102.

33 Yamada, H., Chayahara, A., Mokuno, Y. et al. (2010). Fabrication of 1 inch mosaic crystal diamond wafers. *Appl. Phys Express* 3: 051301.

34 Yamada, H., Chayahara, A., Mokuno, Y. et al. (2014). A 2-in. mosaic wafer made of a single-crystal diamond. *Appl. Phys. Lett.* 104: 102110.

35 Schreck, M., Gsell, S., Brescia, R., and Fischer, M. (2017). Ion bombardment induced buried lateral growth: the key mechanism for the synthesis of single crystal diamond wafers. *Sci. Rep.* 7: 44462.

36 Aida, H., Kim, S.-W., Ikejiri, K. et al. (2017). Microneedle growth method as an innovative approach for growing freestanding single crystal diamond substrate: detailed study on the growth scheme of continuous diamond layers on diamond microneedles. *Diamond Relat. Mater.* 75: 34–38.

37 Efremow, N.N., Susalka, R., Twichell, J.C. et al. (1994). Mosaic diamond substrates approaching single-crystal quality using cube-shaped diamond seeds. *Diamond Relat. Mater.* 4: 76–82.

38 Yamada, H., Chayahara, A., Umezawa, H. et al. (2012). Fabrication and fundamental characterizations of tiled clones of single-crystal diamond with 1-inch size. *Diamond Relat. Mater.* 24: 29–33.

39 Gallheber, B.-C., Fischer, M., Mayr, M. et al. (2018). Growth, stress, and defects of heteroepitaxial diamond on Ir/YSZ/Si(111). *J. Appl. Phys.* 123: 225302.

40 Davis, N., Khan, R., Martineau, P. et al. (2011). Effect of off-axis growth on dislocations in CVD diamond grown on {001} substrates. *J. Phys. Conf. Ser.* 281: 012026.

41 Tallaire, A., Brinza, O., Mille, V. et al. (2017). Reduction of dislocations in single crystal diamond by lateral growth over a macroscopic hole. *Adv. Mater.* 29: 1604823.

42 Naamoun, M., Tallaire, A., Doppelt, P. et al. (2015). Reduction of dislocation densities in single crystal CVD diamond by using self-assembled metallic masks. *Diamond Relat. Mater.* 58: 62–68.

43 Friel, I., Clewes, S.L., Dhillon, H.K. et al. (2009). Control of surface and bulk crystalline quality in single crystal diamond grown by chemical vapour deposition. *Diamond Relat. Mater.* 18: 808–815.

44 Bachman, P., Leers, D., and Lydtin, H. (1991). Towards a general concept of diamond chemical vapor depositions. *Diamond Relat. Mater.* 1: 1–12.

45 Teraji, T. (2015). High-quality and high-purity homoepitaxial diamond (100) film growth under high oxygen concentration condition. *J. Appl. Phys.* 118: 4929962.

46 Bogdanov, S.A., Vikharev, A.L., Drozdov, M.N., and Radishev, D.B. (2017). Synthesis of thick and high-quality homoepitaxial diamond with high boron doping level: oxygen effect. *Diamond Relat. Mater.* 74: 59–64.

47 Yan, C.-S., Vohra, Y.-K., Mao, H.-K., and Hemley, R.J. (2002). Very high growth rate chemical vapor deposition of single-crystal diamond. *Proc. Natl. Acad. Sci. U.S.A.* 99 (22): 12523–12525.

48 Achard, J., Silva, F., Tallaire, A. et al. (2007). High quality MPACVD diamond single crystal growth: high microwave power density regime. *J. Phys. D: Appl. Phys.* 40: 6175–6188.

49 Tallaire, A., Achard, J., Boussadi, A. et al. (2014). High quality thick CVD diamond films homoepitaxially grown on (111)-oriented substrates. *Diamond Relat. Mater.* 41: 34–40.

50 Tokuda, N., Umezawa, H., Saito, T. et al. (2007). Surface roughening of diamond (001) films during homoepitaxial growth in heavy boron doping. *Diamond Relat. Mater.* 16: 767–770.

51 Ohmagari, S., Yamada, H., Umezawa, H. et al. (2018). Growth and characterization of freestanding p+ diamond (100) substrates prepared by hot-filament chemical vapor deposition. *Diamond Relat. Mater.* 81: 33–37.

52 Kato, H., Ogura, M., Makino, T. et al. (2016). N-type control of single-crystal diamond films by ultra-lightly phosphorus doping. *Appl. Phys. Lett.* 109: 142102.

53 Ashold, M.N.R., Mahoney, J.D., Mushtaq, S. et al. (2017). What [plasma used for growing] diamond can shine like flame? *Chem. Commun.* 53: 10482.

54 Butler, J.E., Mankelevich, Y.A., Cheesman, A. et al. (2009). Understanding the chemical vapor deposition of diamond: recent progress. *J. Phys. Condens. Matter* 2: 364201.

55 Goodwin, D.G. (1993). Scaling laws for diamond chemicalvapor deposition. I. Diamond surface chemistry. *J. Appl. Phys.* 74: 6888.

56 Mankelevich, Y.A. and May, P.W. (2008). New insights into the mechanism of CVD diamond growth: single crystal diamond in MW PECVD reactors. *Diamond Relat. Mater.* 17: 10201–11028.

57 Yamada, H., Chayahara, A., Ohmagari, S., and Mokuno, Y. (2016). Factors to control uniformity of single crystal diamond growth by using microwave plasma CVD. *Diamond Relat. Mater.* 63: 17–20.

58 Weng, J., Xiong, L.W., Dai, S.Y. et al. (2012). Investigation of depositing large area uniform diamond films in multi-mode MPCVD chamber. *Diamond Relat. Mater.* 30: 15–19.

59 Kononenko, T.V., Ralchenko, V.G., Vlasov, I.I. et al. (1998). Ablation of CVD diamond with nanosecond laser pulses of UV–IR range. *Diamond Relat. Mater.* 7: 1623–1627.

60 Pimenov, S.M., Vlasov, I.I., Khomich, A.A. et al. (2011). Picosecond-laser-induced structural modifications in the bulk of single-crystal diamond. *Appl. Phys. A* 105: 673–677.

61 Shimizu, M., Shimotsuma, Y., Sakakura, M. et al. (2009). Periodic metallo-dielectric structure in diamond. *Opt. Express* 17 (1): 46–54.

62 Schreck, M., Mayr, M., Weinl, M. et al. (2020). Liftoff of single crystal diamond by epitaxial lateral overgrowth using SiO_2. *Diamond Relat. Mater.* 101: 107606.

63 Mokuno, Y., Kato, Y., Tsubouchi, N. et al. (2014). A nitrogen doped low-dislocation density free-standing single crystal diamond plate fabricated by a lift-off process. *Appl. Phys. Lett.* 104: 252109.

64 Kraus, E.H. and Slawson, C.B. (1939). Variation of hardness in the diamond. *J. Mineral. Soc. Am.* 24 (1): 661–676.

65 Hird, J.R. and Field, J.E. (2005). A wear mechanism map for the diamond polishing process. *Wear* 258: 18–25.

66 Schuelke, T. and Grotjohn, T.A. (2013). Diamond polishing. *Diamond Relat. Mater.* 32: 17–26.

67 Bussone, G., Lafford, T.A., Masiello, F. et al. (2011). Investigation of surface and sub-surface damage in high quality synthetic diamonds by X-ray reflectivity and grazing incidence in-plane diffraction. *Phys. Status Solidi A* 208 (11): 2612–2618.

68 Tatsumi, N., Maruoka, K., Harano, K. et al. (2018). Crystalline quality distributions of the Type IIa diamond substrate and the CVD diamond layer processed by chemical mechanical polishing using a SiO_2 wheel. *Jpn. J. Appl. Phys.* 57: 105503.

69 Kubota, A., Nagase, S., and Touge, M. (2016). Improvement of material removal rate of single-crystal diamond by polishing using H_2O_2 solution. *Diamond Relat. Mater.* 70: 39–45.

70 Kubota, A., Fukuyama, S., Ichimori, Y., and Touge, M. (2012). Surface smoothing of single-crystal diamond (100) substrate by polishing technique. *Diamond Relat. Mater.* 24: 59–62.

71 Yamamura, K., Emori, K., Sun, R. et al. (2018). Damage-free highly efficient polishing of single-crystal diamond wafer by plasma-assisted polishing. *CIRP Ann.* 67: 353–356.

72 Yatsui, T., Nomura, W., Naruise, M., and Ohtsu, M. (2012). Realization of an atomically flat surface of diamond using dressed photon–phonon etching. *J. Phys. D: Appl. Phys.* 45: 475302.

73 Koizumi, S., Kamo, M., Sato, Y. et al. (1997). Growth and characterization of phosphorous doped {111} homoepitaxial diamond thin films. *Appl. Phys. Lett.* 71: 1065–1067.

74 Kato, H., Yamasaki, S., and Okushi, H. (2005). n-type doping of (001)-oriented single-crystalline diamond by phosphorus. *Appl. Phys. Lett.* 86 (22): 222111.

75 Kato, H., Yamasaki, S., and Okushi, H. (2005). Growth and characterization of phosphorus-doped diamond using organophosphorus gases. *Phys. Status Solidi A* 202: 2122–2128.

76 Miyazaki, T., Kato, H., Ri, S.G. et al. (2006). Energetics of dopant atoms in subsurface positions of diamond semiconductor. *Superlattices Microstruct.* 40: 574–579.

77 Pernot, J. and Koizumi, S. (2008). Electron mobility in phosphorous doped {111} homoepitaxial diamond. *Appl. Phys. Lett.* 93 (5): 052105.

78 Suzuki, M., Yoshida, H., Sakuma, N. et al. (2004). Electrical characterization of phosphorus-doped n-type homoepitaxial diamond layers by Schottky barrier diodes. *Appl. Phys. Lett.* 84: 2349–2351.

79 Kato, H., Umezawa, H., Tokuda, N. et al. (2008). Low specific contact resistance of heavily phosphorus-doped diamond film. *Appl. Phys. Lett.* 93: 202103.

80 Suzuki, M., Sakai, T., Makino, T. et al. (2013). Electrical characterization of diamond PiN diodes for high voltage applications. *Phys. Status Solidi A* 210: 2035–2039.

81 Makino, T., Kato, H., Takeuchi, D. et al. (2012). Device design of diamond Schottky-pn diode for low-loss power electronics. *Jpn. J. Appl. Phys.* 51: 090116.

82 Matsumoto, T., Kato, H., Oyama, K. et al. (2016). Inversion channel diamond metal-oxide-semiconductor field-effect transistor with normally off characteristics. *Sci. Rep.* 6: 31585.

83 Doi, Y., Fukui, T., Kato, H. et al. (2016). Pure negatively charged state of the NV center in n-type diamond. *Phys. Rev. B* 93: 081203.

84 Herbschleb, E.D., Kato, H., Maruyama, Y. et al. (2019). Ultra-long coherence times amongst room-temperature solid-state spins. *Nat. Commun.* 10: 3766.

85 Chicot, G., Eon, D., and Rouger, N. (2016). Optimal drift region for diamond power devices. *Diamond Relat. Mater.* 69: 68–73.

86 Tarelkin, S., Bormashov, V., Buga, S. et al. (2015). Power diamond vertical Schottky barrier diode with 10 A forward current. *Phys. Status Solidi A* 212 (11): 2621–2627.

87 Umezawa, H., Matsumoto, T., and Shikata, S.-I. (2014). Diamond metal–semiconductor field-effect transistor with breakdown voltage over 1.5 kV. *IEEE Electron Device Lett.* 35 (11): 1112–1114.

88 Werner, M., Locher, R., Kohly, W. et al. (1997). The diamond Irvin curve. *Diamond Relat. Mater.* 6 (2–4): 308–313.

89 Ekimov, E.A., Sidorov, V.A., Bauer, E.D. et al. (2004). Superconductivity in diamond. *Nature* 428 (6982): 542–545.

90 Achard, J., Tallaire, A., Mille, V. et al. (2014). Improvement of dislocation density in thick CVD single crystal diamond films by coupling H_2/O_2 plasma

etching and chemo-mechanical or ICP treatment of HPHT substrates. *Phys. Status Solidi A* 211 (10): 2264–2267.

91 Usui, A., Sunakawa, H., Sakai, A., and Atsushi, A.Y. (1997). Thick GaN epitaxial growth with low dislocation density by hydride vapor phase epitaxy. *Jpn. J. Appl. Phys.* 36 (7B): L899–L902.

92 Ichikawa, K., Kodama, H., Suzuki, K., and Sawabe, A. (2017). Effect of stripe orientation on dislocation propagation in epitaxial lateral overgrowth diamond on Ir. *Diamond Relat. Mater.* 72: 114–118.

93 Ohmagari, S., Yamada, H., Tsubouchi, N. et al. (2018). Large reduction of threading dislocations in diamond by hot-filament chemical vapor deposition accompanying W incorporations. *Appl. Phys. Lett.* 113 (3): 032108.

94 Teraji, T., Fiori, A., Kiritani, N. et al. (2017). Mechanism of reverse current increase of vertical-type diamond Schottky diodes. *J. Appl. Phys.* 122 (13): 135304.

95 Baliga, B.J. (1989). Power semiconductor-device figure of merit for high-frequency applications. *IEEE Electron Device Lett.* 10: 455–457.

96 Koizumi, S., Umezawa, H., Pernot, J., and Suzuki, M. (eds.) (2018). *Power Electronics Device Applications of Diamond Semiconductors*. Elsevier.

97 Huang, A.Q. (2004). New unipolar switching power device figures of merit. *IEEE Electron Device Lett.* 25: 298–301.

98 Umezawa, H. (2018). Recent advances in diamond power semiconductor devices. *Mater. Sci. Semicond. Process.* 78: 147–156.

99 Eon, D., Traoré, A., Pernot, J., and Gheeraert, E. (2016). Recent progress on diamond Schottky diode. *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*.

100 Umezawa, H., Saito, T., Tokuda, N. et al. (2007). Leakage current analysis of diamond Schottky barrier diode. *Appl. Phys. Lett.* 90: 073506.

101 Umezawa, H., Gima, H., Driche, K. et al. (2017). Defect and field-enhancement characterization through electron-beam-induced current analysis. *Appl. Phys. Lett.* 110: 182103.

102 Driche, K. (2018) Diamond unipolar devices: towards impact ionization coefficients extraction, Ph.D Thesis, Université Grenoble Alpes, Grenoble, France.

103 Driche, K., Rugen, S., Kaminski, N. et al. (2018). Electric field distribution using floating metal guard rings edge-termination for Schottky diodes. *Diamond Relat. Mater.* 82: 160–164.

104 Pham, T.T., Pernot, J., Perez, G. et al. (2017). Deep-depletion mode boron-doped monocrystalline diamond metal oxide semiconductor field effect transistor. *IEEE Electron Device Lett.* 38: 1571–1574.

105 Iwasaki, T., Hoshino, Y., Tsuzuki, K. et al. (2013). High-temperature operation of diamond junction field-effect transistors with lateral p-n junctions. *IEEE Electron Device Lett.* 34: 1175–1177.

106 Iwataki, M., Oi, N., Horikawa, K. et al. (2020). Over 12000 A/cm^2 and 3.2 m omega cm^2 miniaturized vertical-type two-dimensional hole gas diamond MOSFET. *IEEE Electron Device Lett.* 41: 111–114.

107 Kawarada, H. (1996). Hydrogen-terminated diamond surfaces and interfaces. *Surf. Sci. Rep.* 26: 205–259.

22

Gallium Oxide: Material Properties and Devices

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22.1 Introduction

At present, the majority of power switching devices are made by Si. However, it is difficult to keep continuous improvements of Si device performance for a long time in the future from the viewpoint of its intrinsic material properties ruled by a small bandgap energy (E_g) of 1.1 eV. Given these circumstances, silicon carbide (SiC) and gallium nitride (GaN) are expected to be principal candidates for next-generation power devices from their physical properties such as larger E_g of 3.3–3.4 eV, greater breakdown electric fields (E_{br}), and larger Baliga's figures of merit (FOMs) than those of Si [1, 2]. However, these materials have the same fundamental drawback that melt-grown bulk single crystals are hardly available.

Gallium oxide (Ga_2O_3) is one of the oxide semiconductors having an extremely large E_g of over 4.5 eV [3–5] and an expected E_{br} of larger than 7 MV/cm. Availability of melt-grown bulk single crystals is another important feature, especially for future industrialization and mass production of Ga_2O_3 power devices. From these advantages over the competitors, Ga_2O_3 has recently been attracting much attention as a promising material for next-generation power electronics. Furthermore, Ga_2O_3 is recognized as a representative among emerging ultrawide bandgap semiconductors, which correspond to semiconductor materials with E_g significantly exceeding those of SiC and GaN [6].

First, this chapter introduces material properties, and melt bulk and epitaxial thin-film growth techniques of Ga_2O_3 based on the comprehensive survey of published literatures. Primitive developments of Ga_2O_3 Schottky barrier diodes (SBDs) and field-effect transistors (FETs) are then discussed, with a particular focus on devices developed in the author's group.

Wide Bandgap Semiconductors for Power Electronics: Materials, Devices, Applications,
First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

22.2 Physical Properties of Ga_2O_3

22.2.1 Polymorphs

From the first report in 1952, it has been believed that Ga_2O_3 has five types of polymorphs that are labeled as α, β, γ, δ, and ε [7]. In addition to the five polymorphs, a new phase of κ-Ga_2O_3, which has a very similar crystal structure to ε-Ga_2O_3, was recently discovered [8, 9]. Research efforts have mostly been devoted to β-Ga_2O_3 until now because its bulk single crystals can be synthesized by melt growth methods. β-Ga_2O_3 has a unique crystal structure called "β-gallia structure," which is the thermodynamically stable form that belongs to the C2/m space group with lattice constants of $a = 12.2$ Å, $b = 3.0$ Å, and $c = 5.8$ Å, as illustrated in Figure 22.1. It is a monoclinic structure with an angle between the a and c axes of 104°. The unit cell of β-Ga_2O_3 contains two inequivalent Ga sites and three inequivalent O sites. Ga(I) and Ga(II) are tetrahedrally and octahedrally coordinated with O, respectively. O(I) and O(II) have threefold Ga coordination, while O(III) has fourfold one.

The other polymorphs (α, γ, δ, ε, and κ) correspond to metastable phases. It is impossible to synthesize bulk single crystals of the metastable phases from melt; only thin films are available by low-temperature heteroepitaxial growth on foreign substrates. Corundum α-Ga_2O_3 is the second most investigated phase behind β-Ga_2O_3 because of its ease of epitaxial growth on sapphire substrates having the same corundum structure. γ-, δ-, ε-, and κ-Ga_2O_3 crystallize into defective spinel, cubic bixbyite-like, hexagonal, and orthorhombic structures, respectively. ε- and κ-Ga_2O_3 are expected to exhibit large spontaneous polarization and ferroelectric properties. Note that the metastable Ga_2O_3 thin films change into the most stable β-Ga_2O_3 by high-temperature annealing processes and that device process temperature is restricted to be relatively low to avoid the transformation. Throughout this chapter, most of the topics will be focused on β-Ga_2O_3.

22.2.2 Material Properties of β-Ga_2O_3

Table 22.1 summarizes important material properties of major semiconductors and β-Ga_2O_3 for power switching devices. The E_g of β-Ga_2O_3 was estimated to be

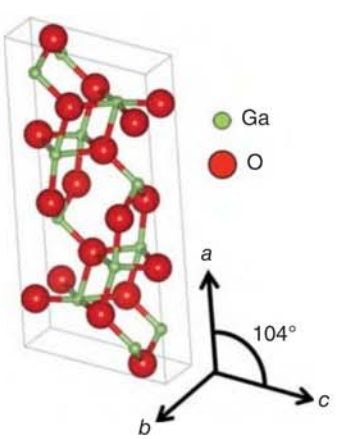


Figure 22.1 Atomic unit cell of β-Ga_2O_3.

Table 22.1 Comparison of material properties between Si, SiC, GaN, and β-Ga_2O_3.

	Si	4H-SiC	GaN	β-Ga_2O_3
Bandgap (eV)	1.1	3.3	3.4	4.5
Mobility (μ) ($cm^2/V\,s$)	1400	1000	1200	~200
Breakdown electric field (E_{br}) (MV/cm)	0.3	2.5	3.3	7–8
Dielectric constant (ε)	11.8	9.7	9.0	10–12
Baliga's FOM ($\varepsilon\mu E_{br}^3$)	1	340	870	>1500
Thermal conductivity (W/cm K)	1.5	2.7	2.1	0.27

4.4–4.9 eV from optical absorption spectra [3–5]. Furthermore, there have been arguments about whether β-Ga_2O_3 is a direct or an indirect bandgap semiconductor. Onuma et al. investigated polarized transmittance and reflectance spectra of β-Ga_2O_3 bulk single crystals and found out that β-Ga_2O_3 is an indirect semiconductor with an E_g of 4.43 eV at room temperature [5]. On the other hand, the direct E_g corresponding to band-to-band transition at the Γ point was estimated to be 4.48 eV, which is larger than the indirect E_g by only 50 meV. The optical E_g of α-Ga_2O_3 was extracted to be 5.3 eV from the optical transmittance spectrum [10]. It can be considered that the large E_g leads to the expected high E_{br}. In fact, the peak E_{br} of β-Ga_2O_3 at catastrophic breakdown event happening at a gate dielectric of an FET or an anode electrode edge of a SBD has been simulated to be >5 MV/cm [11–13], which is approximately double those of SiC and GaN and leads to the Baliga's FOM much larger than those of SiC and GaN as shown in Table 22.1.

Si, germanium, and tin (Sn) are often used as donor dopants of β-Ga_2O_3. These group IV elements form shallow donor states in Ga_2O_3. The electron density (n) in β-Ga_2O_3 can be controlled in the wide range of 10^{15}–10^{20} cm^{-3} by using the donor dopants. The electron effective mass was calculated to be 0.23–0.34 m_0 (m_0: the free electron mass) [14–16], which agree well with experimental data [17–19] and are nearly equal to those of SiC and GaN. β-Ga_2O_3 has multiple phonon modes in the low-energy range due to its unique band structure determined by the low-symmetric crystal structure [20, 21], and the room-temperature electron mobility in β-Ga_2O_3 is expected to be up to 200 $cm^2/V\,s$ due to the polar optical phonon scatterings in the lowest energy branch [22, 23]. The saturation electron velocity was theoretically calculated to be about 2×10^7 cm/s [24], which is comparable with the values for other compound semiconductors such as GaAs and GaN and thus sufficiently high for various radio-frequency (RF) device applications.

Two fundamental properties of Ga_2O_3 are often pointed out as serious drawbacks for power device applications. One is a lack of p-type material, and the other is poor heat dissipation capacity due to its low thermal conductivity.

In contrast to the n-type doping, there has been no report on successful p-type doping with effective hole conduction. In general, it is difficult for single-crystal oxide semiconductors to realize shallow acceptor doping because their valence band states are derived mainly from the O 2p orbitals with strong bonding. There are

some proposed candidates for deep acceptors of Ga_2O_3 such as magnesium (Mg), zinc, beryllium, and nitrogen (N); however, theoretical studies have predicted that all these impurities would exhibit extremely large activation energies of over 1 eV [25–27]. Another expected factor that limits hole conductivity in Ga_2O_3 is the very low mobility owing to the heavy hole effective mass originated from the valence band structure with small energy dispersion [14, 15, 28]. Furthermore, it has also been predicted by first-principles calculations that holes tend to form localized small polarons by the self-trapping effect due to local lattice distortions and that this phenomenon prohibits effective hole conduction under low electric field or by diffusion [27, 29]. From the three factors, hole-conductive p-Ga_2O_3 seems to be hardly realized. However, the deep acceptor p-Ga_2O_3 is sufficiently useful to form a large energy barrier (>3 eV) in n-Ga_2O_3 by utilizing the built-in potential of the p–n junction.

Performance of Ga_2O_3 devices operated at high-voltage and large current conditions is limited by its low thermal conductivity because self-heating under high-power operation is inevitable even in high-efficiency power devices, and the resistance of the drift layer increases with rising operation temperature due to the decrease in electron mobility [30–34]. Therefore, the low thermal conductivity of Ga_2O_3 in the range of 0.1–0.3 W/cm K at room temperature [35–39], which is more than an order of magnitude smaller than those of Si, SiC, and GaN, is a serious potential weakness of Ga_2O_3 power devices. The thermal management will be one of the important and challenging research topics for Ga_2O_3 device technologies. Direct wafer bonding to a foreign substrate with good thermal and electrical conductivities is considered to be one of the effective methods to improve the heat dissipation [40, 41].

22.3 Melt Bulk Growth

The most important feature of β-Ga_2O_3 from the viewpoint of device commercialization is that bulk single crystals can be synthesized by melt growth methods. Various techniques such as floating zone [42, 43], Czochralski [44, 45], vertical Bridgman [46], and edge-defined film-fed growth (EFG) [47, 48] have been utilized for Ga_2O_3 bulk growth. High-quality, large-size wafers can be produced from melt-grown bulk ingots as is the case with Si, GaAs, and sapphire. This merit can offer Ga_2O_3 a significant advantage in material quality and production cost over SiC and GaN, whose bulk crystals can be produced only by alternative techniques requiring high pressure and/or temperature. Six-inch-diameter single-crystal Ga_2O_3 wafers have already been fabricated from an EFG bulk. n-type conductivity of Ga_2O_3 bulk crystals has been controlled by shallow donor doping of Si or Sn, and semi-insulating bulk crystals are also available by deep acceptor/trap doping with iron (Fe) or Mg [48].

22.4 Epitaxial Growth

As is the case with other compound semiconductors, various epitaxial growth technologies have been developed for Ga_2O_3, such as molecular beam epitaxy (MBE),

halide vapor phase epitaxy (HVPE), and metalorganic chemical vapor deposition (MOCVD). For Ga_2O_3, there is another unique and popular technique called mist chemical vapor deposition (CVD), which was mainly designed for oxide semiconductors and has often been utilized for growth of the metastable phases.

22.4.1 MBE

In the early stage of development, epitaxial growth of Ga_2O_3 thin films was mostly explored by MBE. A conventional gas source MBE machine is used for Ga_2O_3 growth, as schematically illustrated in Figure 22.2. There are two types of oxygen sources used for Ga_2O_3 MBE. One is ozone, and the other is oxygen (O) radicals that are produced by decomposing O_2 gas with an RF plasma cell. Purity of Ga_2O_3 epitaxial films grown by ozone MBE is typically better than those grown by plasma-assisted molecular beam epitaxy (PAMBE). High-density Si and N impurities are unintentionally doped (UID) in Ga_2O_3 films grown by PAMBE [49]; on the other hand, densities of both impurities in UID films grown by ozone MBE are below detection limits of secondary ion mass spectrometry. The Si atoms in the PAMBE-grown films are probably supplied from a plasma bulb made by quartz in the plasma cell. The source of N atoms is still unclear; however, it is likely the N_2 impurity gas incorporated in the high-purity O_2 source gas. Due to the short lifetime of ozone in vacuum, a nozzle head of the ozone inlet tube has to be set in a very short distance of <5 cm from a substrate. This configuration leads to poor in-plane thickness uniformity of the ozone MBE-grown films. In case of PAMBE, good thickness uniformity can be obtained since enough long distance is kept between a plasma cell and a substrate.

There is a unique technical issue for in situ donor doping during oxide MBE growth. Normally, the donor metal source is installed in a Knudsen cell and thermally evaporated or sublimated to generate the dopant flux. However, under

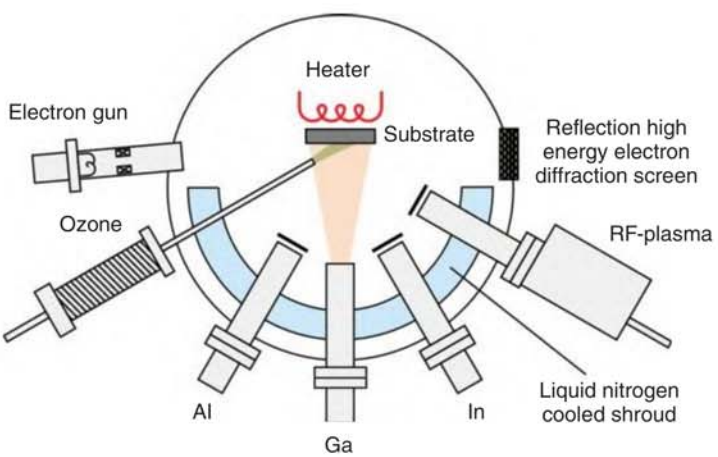


Figure 22.2 Schematic of ozone/RF-plasma MBE system illustrating Ga_2O_3 thin film growth using ozone as O source.

the typical vacuum pressure of 10^{-6}–10^{-4} Torr in the growth chamber, which is determined primarily by the background O_2 pressure during growth, the surface of the heated dopant metal is readily oxidized, and volatile compounds are formed. As a result, the donor dopant flux is limited by the formation of volatile metal oxides rather than the vapor pressure of the donor metal itself [50]. In consequence, the large increase in the dopant flux supplied to the growth surface makes it very difficult to precisely control the low-level donor doping on the order of 10^{15}–10^{16} cm^{-3}. This is a common issue for both ozone MBE and PAMBE.

22.4.2 HVPE

Successful development of Ga_2O_3 HVPE growth technology in 2014 initiated current worldwide development trend of vertical Ga_2O_3 transistors and SBDs [51, 52]. An atmospheric-pressure horizontal hot-wall HVPE system for Ga_2O_3 thin-film growth is schematically illustrated in Figure 22.3. GaCl generated by reaction of high-purity Ga metal with Cl_2 gas is used as a Ga source, and O_2 gas is an O source. $SiCl_4$ gas is used for donor doping to grow n-Ga_2O_3 films. The growth rate can be increased to ~20 μm/h without any degradation of the crystal quality.

UID β-Ga_2O_3 thin films grown by HVPE on Ga_2O_3 substrates possess excellent structural and electrical properties, which were confirmed by an extremely low residual n of less than 1×10^{13} cm^{-3} [52]. The n-type conductivity of Ga_2O_3 films can be controlled by Si doping in the wide range of $n = 10^{15}$–10^{19} cm^{-3}. The peak room- and low-temperature electron mobilities of Si-doped n-Ga_2O_3 films were estimated to be ~150 and ~5000 $cm^2/V\,s$, respectively [53].

Now, HVPE-grown β-Ga_2O_3 epitaxial wafers are commercially available, and many universities and research institutes have started developments of vertical Ga_2O_3 devices by using the commercial HVPE wafers.

22.4.3 MOCVD

MOCVD has been an epitaxial growth technique widely used for mass production of optical and electrical compound semiconductor devices. For Ga_2O_3, development of MOCVD was a little behind those of MBE and HVPE; however, crystal qualities of MOCVD-grown Ga_2O_3 films have improved rapidly over the past few years.

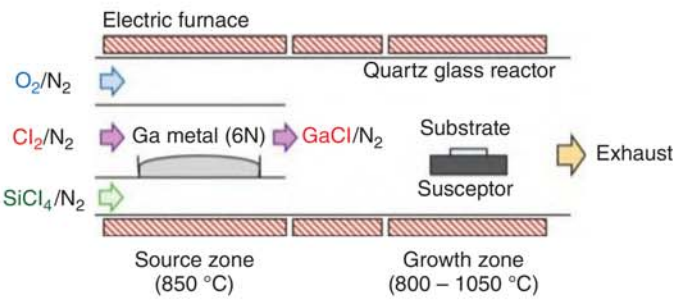


Figure 22.3 Schematic of atmospheric-pressure HVPE system for Ga_2O_3 growth.

Traditional Ga precursors, such as trimethylgallium and triethylgallium, and O_2 gas are used for Ga_2O_3 growth [54]. Growth temperatures are typically set at 800–900 °C, which is 100–200 °C lower than that for GaN MOCVD. Si can be doped in an epitaxial film during growth by simultaneously supplying Si-containing precursors such as silane and tetraethyl orthosilicate. The growth rate is typically in the range of 0.1 to a few μm/h.

The residual n at a low level of less than 1×10^{16} cm^{-3} in MOCVD-grown UID Ga_2O_3 films has been reported recently [55, 56]. The peak electron mobilities of Si-doped n-Ga_2O_3 films were ~180 and ~5000 cm^2/V s at room temperature and 45 K, respectively [56]. These electrical properties are comparable with those of HVPE-grown films. High-quality $(AlGa)_2O_3$ epitaxial films have also been grown by MOCVD [57].

22.4.4 Mist CVD

Mist CVD was developed as a technique mainly focusing on oxide semiconductors. Especially, mist CVD has shown its strength on heteroepitaxial growth of metastable Ga_2O_3 films with α- [10, 58], γ- [59], and ε-phases [60] on foreign substrates. In the mist CVD process, mist atomized from Ga precursors dissolved in water is generated by ultrasonic transducers and then transferred by carrier gas to a growth chamber. Then, epitaxial growth of Ga_2O_3 films happens on a substrate kept at growth temperature. High-quality Ga_2O_3 films can be obtained, even though it is a simple technique.

22.5 Vertical Diodes

At this time, there have been much more reports on SBDs compared with those on FETs owing to their simple structures and commercially available HVPE-grown epitaxial wafers. Ga_2O_3 SBDs have already shown their promising performance such as a breakdown voltage (V_{br}) of over 2 kV [61, 62], a large forward on-current of over 10 A [63], and high-temperature operation up to 500 °C [64]. In this section, the primitive SBD developments conducted by the author's group are first discussed. Then, state-of-the-art Ga_2O_3 SBDs and heterojunction p–n diodes using amorphous p-type oxides are described.

22.5.1 SBD with HVPE-Grown Drift Layer

We first fabricated simple SBD structures on 7-μm-thick n-Ga_2O_3 drift layers with a Si doping concentration on the order of low-10^{16} cm^{-3} grown on n$^+$-Ga_2O_3(001) substrates by HVPE to mainly characterize basic material properties of the drift layers and Schottky contacts [65]. A cross-sectional schematic illustration of the SBD structure is shown in Figure 22.4. The backside ohmic cathode and circular Schottky anode electrodes were fabricated by Ti/Au and Pt/Ti/Au stacks, respectively.

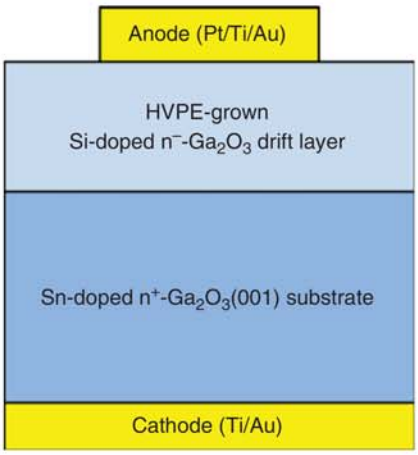


Figure 22.4 Schematic cross section of vertical Ga_2O_3 SBD structure.

From linear fits to the forward current density–voltage (J–V) curves within the range of J = 100–200 A/cm^2, the specific on-resistances (R_{on}) were estimated to be 3.0 mΩ cm^2 for the device with a net donor concentration ($N_d - N_a$) of 1.4×10^{16} cm^{-3} in the drift layer and 2.4 mΩ cm^2 for the one with $N_d - N_a = 2.0 \times 10^{16}$ cm^{-3}. Excellent ideality factors of 1.02 ± 0.01 were also obtained for the SBDs. The reverse J–V characteristics revealed a V_{br} of ~500 V for both SBDs.

In an operating temperature range from 21 to 200 °C, the Pt/Ga_2O_3(001) Schottky contact exhibited a zero-bias barrier height of 1.09–1.15 eV with a constant near-unity ideality factor. The J–V characteristics of the SBDs were well fitted by the thermionic emission model in the forward regime and the thermionic field emission model in the reverse regime over the entire temperature range, indicating the high-quality Schottky interface.

22.5.2 Field-Plated SBD

A field plate (FP) is a metal–oxide overlap structure that has mitigating effect of electric field concentration at an anode electrode edge when a SBD is reverse-biased. It is often utilized for the electric field termination to enhance V_{br} of SBDs and FETs. Based on the simple SBD structures, Ga_2O_3 FP-SBDs as shown in Figure 22.5 were fabricated to enhance V_{br} [12]. The R_{on} of the typical Ga_2O_3 FP-SBD was estimated to be 5.1 mΩ cm^2. Successful FP engineering led to a large enhancement of V_{br} from ~500 V for the non-FP devices to 1076 V. This was the first demonstration of V_{br} over 1 KV for any Ga_2O_3 transistors and diodes. At the breakdown condition, the simulated maximum electric field under the anode foot edge reached to 5.1 MV/cm, which is much larger than theoretical limits for SiC and GaN.

22.5.3 Field-Plated SBD with Guard Ring Formed by Nitrogen-Ion Implantation

To further improve V_{br}, Ga_2O_3 SBDs having a N-ion-implanted guard ring (GR) in a drift layer and a dielectric FP formed on the GR were developed [66]. Note that N is a

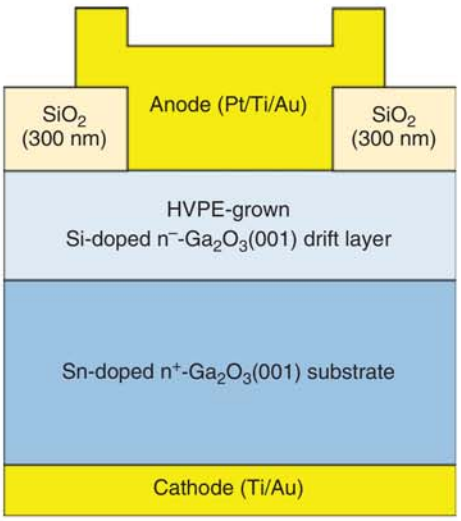


Figure 22.5 Schematic cross section of vertical Ga_2O_3 FP-SBD structure.

deep acceptor in Ga_2O_3 and that N-doped Ga_2O_3 acts as a current blocker in n-Ga_2O_3 by the built-in potential of the p–n junction [67]. N ions were implanted into an HVPE-grown drift layer at multiple energies to form a 0.8-μm-deep box profile with a doping concentration of 1.0×10^{17} cm^{-3}, followed by thermal annealing at 1100 °C for recovering implantation damage of the crystal and activating the implanted N atoms. Excellent device characteristics such as an R_{on} of 4.7 mΩ cm^2 and a V_{br} of 1.43 kV were obtained for the typical SBD due to the effects of the FP and GR.

22.5.4 Trench SBD

Employment of a trench SBD structure is another standard technique for vertical semiconductor devices to enhance V_{br}. This structure could be especially useful for Ga_2O_3 devices because Ga_2O_3 lacks of hole-conductive p-type. Li et al. reported vertical trench Ga_2O_3 SBDs with a fin channel width of a few micrometer as shown in Figure 22.6 [62, 68]. The V_{br} monotonically increased with decreasing the fin width and reached 2.44 kV. The electric field concentration at the anode edge can be effectively suppressed by depletion regions from the fin sidewalls.

22.5.5 α-Ga_2O_3 SBD

FLOSFIA Inc., which is a spin-off company from Kyoto University, demonstrated SBDs using α-Ga_2O_3 films grown on sapphire substrates by mist CVD [69]. It can be pointed out as a key feature in the device process of the α-Ga_2O_3 SBDs that an epitaxial lift-off technology was employed. The free-standing n-Ga_2O_3 film was peeled from the sapphire wafer, and anode and cathode metal electrodes were directly deposited on the front and back surfaces, respectively. It can be considered that the device structure is effective to improve R_{on} and heat dissipation.

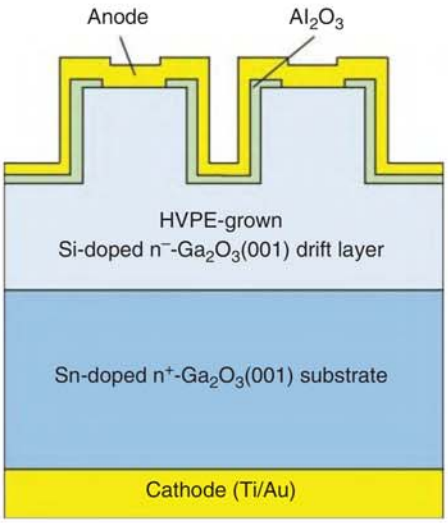


Figure 22.6 Schematic cross section of vertical Ga_2O_3 fin-channel SBD structure.

22.5.6 Heterojunction p-Amorphous Oxide/n-Ga_2O_3 Diode

A heterojunction between different oxide materials usually provides relatively good interface properties in contrast to the other compound semiconductors, even though they are not lattice matched. By using the benefit, there have been some reports on heterojunction p–n diodes depositing amorphous p-type oxides on n-Ga_2O_3. A p-Cu_2O/n-Ga_2O_3 diode demonstrated decent device characteristics such as a forward J of more than 100 A/cm^2, an R_{on} of 8.2 mΩ cm^2, and a large V_{br} of 1.49 kV. The V_{br} was twice larger than that of a normal SBD simultaneously fabricated on the same wafer. [70]

22.6 Lateral FETs

In the primitive development stage of Ga_2O_3 FETs, as other semiconductors, there have been many challenges for developing lateral devices prior to vertical ones because it is typically easier and simpler to fabricate lateral geometry than vertical one. Many fundamental process technologies for Ga_2O_3 devices have been developed in the efforts.

22.6.1 MESFET

Transistor action for single-crystal Ga_2O_3 devices was first demonstrated using simple metal-semiconductor field-effect transistors (MESFETs) fabricated by the author of this chapter and collaborators in 2011 [71]. Figure 22.7a shows a schematic cross section of the MESFET structure. The MESFET having a circular geometry as shown in Figure 22.7b showed decent device characteristics as the first FET, such as effective modulation of drain current (I_d) by gate voltage (V_g) swing, a three-terminal

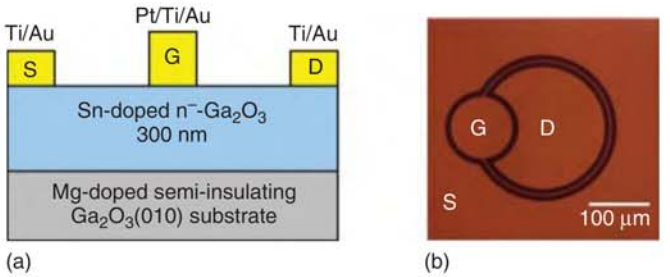
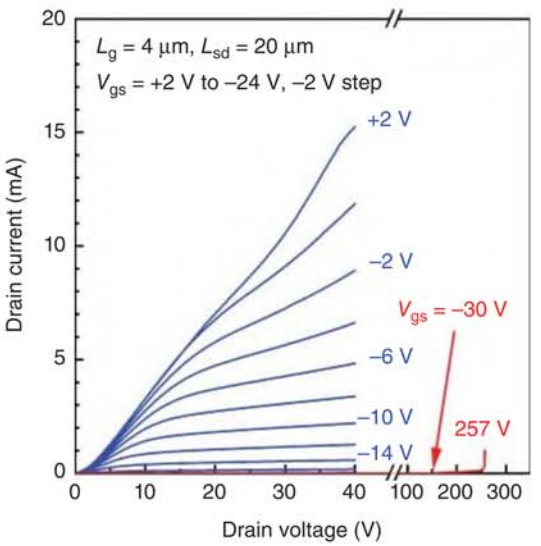


Figure 22.7 (a) Schematic cross section and (b) optical micrograph of Ga_2O_3 MESFET structure.

Figure 22.8 DC output characteristics of Ga_2O_3 MESFET.



destructive V_{br} of over 250 V, and an I_d on/off ratio of 4 orders of magnitude. DC output characteristics of the circular MESFET are shown in Figure 22.8. The non-linear turn-on and poor saturation I_d characteristics as a function of drain voltage (V_d) were caused by poor ohmic characteristics of the source and drain electrodes.

It is worth noting that the community of Ga_2O_3 researchers and engineers rapidly grew after the report of the MESFET demonstration. Therefore, this accomplishment has been considered as the most important breakthrough for Ga_2O_3 technologies.

22.6.2 Depletion-Mode MOSFET

The Ga_2O_3 MESFETs exhibited good device characteristics as a first trial. However, the devices also revealed two clear issues of a large ohmic contact resistance of source and drain electrodes and a small current leakage through the Ga_2O_3 surface. To overcome the drawback of ohmic contact, Si-ion implantation doping technology was developed [72]. Implanted Si atoms in Ga_2O_3 are well activated by thermal annealing at 900–1000 °C. Selective-area high-density Si-ion implantation doping under the

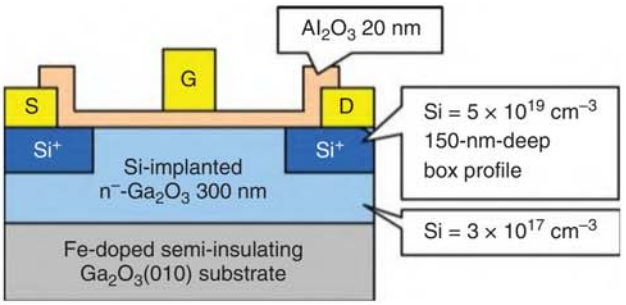


Figure 22.9 Schematic cross section of D-mode Ga_2O_3 MOSFET structure fabricated by Si-ion implantation doping.

source and drain electrode areas can provide a specific contact resistance of less than $1 \times 10^{-5}\,\Omega\,cm^2$; this is an enough low value for various Ga_2O_3 device applications. The other issue of the surface leakage was drastically suppressed by Al_2O_3 surface passivation.

By employing the new device processes, depletion-mode (D-mode) Ga_2O_3 metal oxide-semiconductor field-effect transistors (MOSFETs) as schematically depicted in Figure 22.9 were fabricated [73]. A UID Ga_2O_3 layer was grown on an Fe-doped semi-insulating Ga_2O_3(010) substrate by ozone MBE. A channel, and source and drain ohmic regions were fabricated by Si-ion implantations with densities of 3×10^{17} and $5 \times 10^{19}\,cm^{-3}$, respectively. The Al_2O_3 gate dielectric and passivation layer was formed by plasma atomic layer deposition.

Figure 22.10 shows I_d–V_d output characteristics of the representative D-mode MOSFET. The turn-on linearity and saturation of I_d were drastically improved from the characteristics of the MESFET. The maximum I_d was 65 mA/mm at $V_g = +6$ V, which was more than twice as large as that of the MESFET. The three-terminal

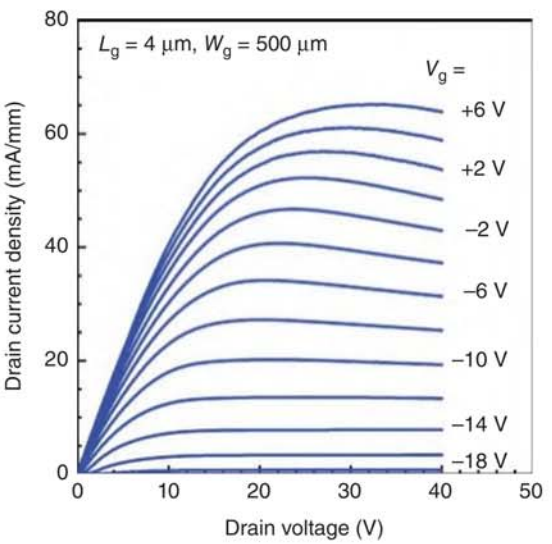


Figure 22.10 DC output characteristics of D-mode Ga_2O_3 MOSFET.

off-state V_{br} was enhanced to 400 V, and the off-state leakage was drastically decreased to less than the lower limit of a measurement instrument. Due to the large decrease in leakage current, the I_d on/off ratio was increased to over 10 orders of magnitude. High-temperature stable operation up to 300 °C was also demonstrated without permanent degradation in electrical device characteristics.

This device has been a base structure for following developments of lateral Ga_2O_3 FETs conducted all over the world.

22.6.3 Field-Plated MOSFET

An FP is commonly used as an edge termination structure for lateral FETs to enhance V_{br} by preventing the electric field concentration at a drain side edge portion of a gate metal. Figure 22.11 shows a cross-sectional schematic of a Ga_2O_3 MOSFET structure with a gate-connected FP [74]. The FP contributed to a large enhancement of V_{br} from ~400 to ~750 V without any degradation of on-state device characteristics from those of the D-mode MOSFET without an FP. The device also exhibited no DC-RF dispersion due to the effect of the thick SiO_2 passivation. As a result of continuing development, the V_{br} of lateral Ga_2O_3 FP-MOSFETs has been enhanced to over 2 kV [75, 76].

22.6.4 Modulation-Doped FET

$(AlGa)_2O_3/Ga_2O_3$ modulation-doped field-effect transistors (MODFETs), which are analogous to AlGaAs/GaAs MODFETs, were developed [77, 78]. Either Si or Ge

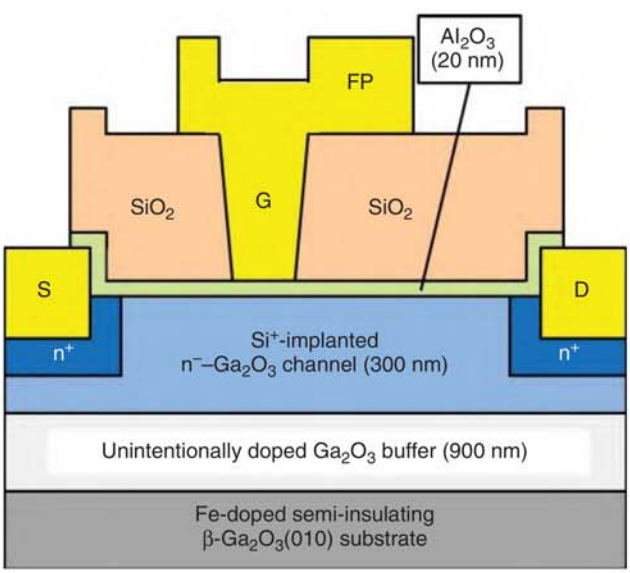


Figure 22.11 Schematic cross section of Ga_2O_3 FP-MOSFET structure.

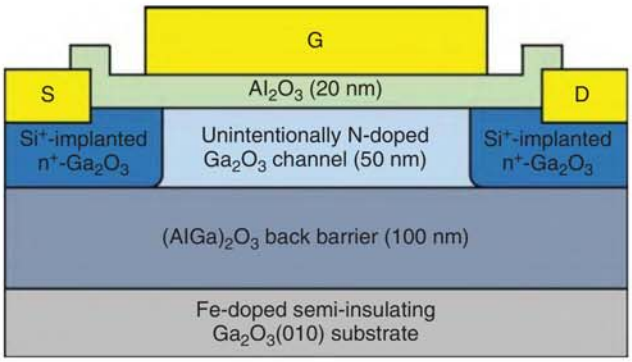


Figure 22.12 Schematic cross section of Ga_2O_3 MOSFET structure with N-doped channel layer.

was doped in the $(AlGa)_2O_3$ barrier layer as a donor, and two-dimensional electron gas (2DEG) with a sheet charge density of low $10^{12}\,cm^{-2}$ was formed at the interface. Zhang et al. succeeded in not only confirming 2DEG formation at the interface but also estimating the electron effective mass of $0.313 \pm 0.015\,m_0$ in Ga_2O_3 from Shubnikov–de Haas oscillations of the $(AlGa)_2O_3/Ga_2O_3$ MODFET [19]. A high V_{br} of 1.37 kV and a large average E_{br} of 3.9 MV/cm have also been demonstrated [79]. The MODFETs are expected to be useful especially for high-frequency applications.

22.6.5 Normally Off FET

Planar enhancement-mode (E-mode) Ga_2O_3 MOSFETs realizing normally off operation were fabricated by decreasing a thickness and/or a doping concentration of a channel layer to enable full depletion under a gate at $V_g = 0$ V. Early E-mode operations were demonstrated for wrap-gate FETs [80], nanomembrane FETs [31], MOSFETs with a UID channel layer [81], and MOSFETs with a recessed gate [82].

Recently, the author's group achieved normally off operation for Ga_2O_3 MOSFETs with an unintentionally N-doped Ga_2O_3 channel layer grown by PAMBE, as illustrated in Figure 22.12 [49]. The channel layer had N and Si concentrations of 1×10^{18} and $2 \times 10^{17}\,cm^{-3}$, respectively, indicating that it should be a p-type material with $N_a > N_d$, if both N and Si atoms were highly activated. The MOSFETs demonstrated a turn-on threshold V_g of larger than +8 V, implying formation of an inversion channel at an interface between an Al_2O_3 gate dielectric and the N-doped Ga_2O_3 layer.

22.7 Vertical FETs

As of the time of this writing, to the best of the author's knowledge, there have been a few groups developing vertical Ga_2O_3 transistors in the world. The following section will discuss two representative developments of vertical Ga_2O_3 FETs.

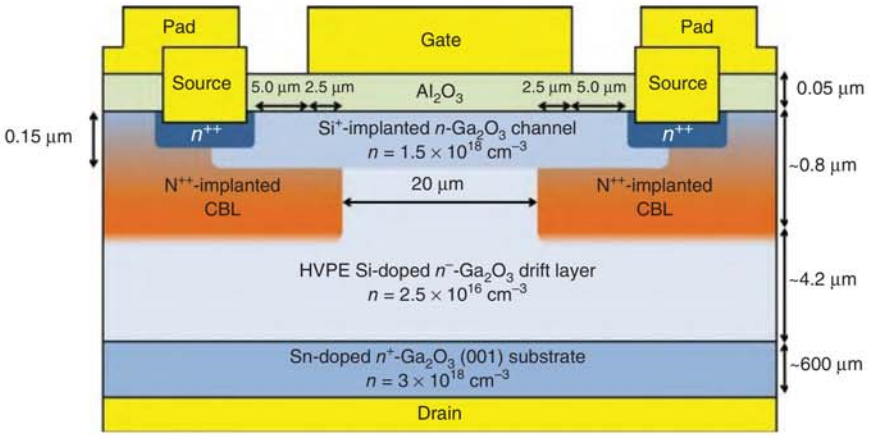


Figure 22.13 Schematic cross section of vertical D-mode Ga_2O_3 MOSFET structure with current aperture.

22.7.1 Current Aperture FET

Vertical FETs with a current aperture were often selected as a first structure in the history of vertical transistor developments due to its simple structure. Figure 22.13 shows a schematic cross section of a vertical D-mode Ga_2O_3 MOSFET with a current aperture that was bounded laterally by N-implanted current blocking layers (CBLs) [83]. It should be noted that three ion implantations were performed to form the N-doped p-Ga_2O_3 CBLs, a Si-doped n-Ga_2O_3 channel, and heavily Si-doped n^{++}-Ga_2O_3 source ohmic contact regions. Decent device characteristics such as a maximum I_d of 0.42 kA/cm^2 and a specific R_{on} of 31.5 mΩ cm^2 were demonstrated. The I_d on/off ratio recorded more than 8 orders of magnitude. The three-terminal off-state V_{br} was limited to <30 V owing to large electric field in the Al_2O_3 gate dielectric due to the high Si doping density of the channel.

E-mode operation of vertical Ga_2O_3 MOSFETs was also demonstrated [84]. The device fabrication process and structure of the E-mode MOSFETs were almost the same as those of the D-mode devices. There were two modifications from the D-mode structure. One was a decrease in the Si doping density of the channel from 1.5×10^{18} to 5.0×10^{17} cm^{-3}. The other was the formation of an n^{++}-region–gate overlap to avoid full channel depletion in the gate–source access region at thermal equilibrium. A turn-on threshold V_g of larger than +3 V and an I_d on/off ratio of more than 6 orders of magnitude were demonstrated, which are sufficiently large values for practical switching applications. Furthermore, the off-state V_{br} was largely improved to ~250 V due to the reduction of the Si density in the channel.

22.7.2 Fin Channel FET

Trench structures are also effective for vertical transistors on electric field management. The same group of Cornell University that developed the trench SBDs reported vertical Ga_2O_3 transistors with a sub-micrometer fin channel [85]. E-mode operation

was achieved for the devices due to full depletion from the sidewalls at $V_g = 0$ V. The fin FETs revealed excellent device characteristics such as a large I_d of 1 kA/cm^2, a specific R_{on} of 10–20 mΩ cm^2, an I_d on/off ratio of 8 orders of magnitude, and an off-state V_{br} of ~1 kV.

22.8 Summary

This chapter presents an overview of current status of research and development on Ga_2O_3 power devices, which covers material properties, melt bulk growth, epitaxial thin-film growth, and device technologies. The extremely large Baliga's FOM and availability of high-quality, large-diameter single-crystal wafers produced from melt-grown bulks are especially appealing to the semiconductor power device community. Over the past 10 years, significant progress in all the aspects of Ga_2O_3 material and device technologies has been made and several milestones on the way to industrialization and commercialization of Ga_2O_3 power transistors and diodes have already been achieved. However, there is no room for doubt that the current Ga_2O_3 power device technologies are still immature and that we still have a long way to start to introduce them to practical markets. Future intense efforts are indispensable to develop advanced device structures to further improve device characteristics. Overcoming the two drawbacks related to fundamental material properties, which are the absence of hole-conductive p-Ga_2O_3 and the poor thermal conductivity, should be tough challenges. However, the author believes that potential of Ga_2O_3 power devices is sufficiently deserved for the efforts.

References

1 Baliga, B.J. (1982). Semiconductors for high voltage, vertical channel field effect transistors. *J. Appl. Phys.* 53 (3): 1759–1764.
2 Baliga, B.J. (1989). Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Lett.* 10 (10): 455–457.
3 Tippins, H.H. (1965). Optical absorption and photoconductivity in the band edge of β-Ga_2O_3. *Phys. Rev. A* 140 (1A): 316–319.
4 Orita, M., Ohta, H., Hirano, M., and Hosono, H. (2000). Deep-ultraviolet transparent conductive β-Ga_2O_3 thin films. *Appl. Phys. Lett.* 77 (25): 4166–4168.
5 Onuma, T., Saito, S., Sasaki, K. et al. (2015). Valence band ordering in β-Ga_2O_3 studied by polarized transmittance and reflectance spectroscopy. *Jpn. J. Appl. Phys.* 54: 112601.
6 Tsao, J.Y., Chowdhury, S., Hollis, M.A. et al. (2018). Ultrawide-bandgap semiconductors: research opportunities and challenges. *Adv. Electron. Mater.* 4: 1600501.
7 Roy, R., Hill, V.G., and Osborn, E.F. (1952). Polymorphism of Ga_2O_3 and the system Ga_2O_3–H_2O. *J. Am. Chem. Soc.* 74 (3): 719–722.
8 Cora, I., Mezzadri, F., Boschi, F. et al. (2017). The real structure of ε-Ga_2O_3 and its relation to κ-phase. *CrystEngComm* 19: 1509–1516.

9 Kneiß, M., Hassa, A., Splith, D. et al. (2019). Tin-assisted heteroepitaxial PLD-growth of κ-Ga_2O_3 thin films with high crystalline quality. *APL Mater.* 7: 022516.

10 Shinohara, D. and Fujita, S. (2008). Heteroepitaxy of corundum-structured α-Ga_2O_3 thin films on α-Al_2O_3 substrates by ultrasonic mist chemical vapor deposition. *Jpn. J. Appl. Phys.* 47 (9): 7311–7313.

11 Green, A.J., Chabak, K.D., Heller, E.R. et al. (2016). 3.8-MV/cm breakdown strength of MOVPE-grown Sn-doped β-Ga_2O_3 MOSFETs. *IEEE Electron Device Lett.* 37 (7): 902–905.

12 Konishi, K., Goto, K., Murakami, H. et al. (2017). 1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes. *Appl. Phys. Lett.* 110: 103506.

13 Yan, X., Esqueda, I.S., Ma, J. et al. (2018). High breakdown electric field in β-Ga_2O_3/graphene vertical barristor heterostructure. *Appl. Phys. Lett.* 112: 032101.

14 He, H., Orlando, R., Blanco, M.A. et al. (2006). First-principles study of the structural, electronic, and optical properties of Ga_2O_3 in its monoclinic and hexagonal phases. *Phys. Rev. B* 74: 195123.

15 Peelaers, H. and Van de Walle, C.G. (2015). Brillouin zone and band structure of β-Ga_2O_3. *Phys. Status Solidi B* 252 (4): 828–832.

16 Furthmüller, J. and Bechstedt, F. (2016). Quasiparticle bands and spectra of Ga_2O_3 polymorphs. *Phys. Rev. B* 93: 115204.

17 Mohamed, M., Janowitz, C., Unger, I. et al. (2010). The electronic structure of β-Ga_2O_3. *Appl. Phys. Lett.* 97: 211903.

18 Mock, A., Korlacki, R., Briley, C. et al. (2017). Band-to-band transitions, selection rules, effective mass, and excitonic contributions in monoclinic β-Ga_2O_3. *Phys. Rev. B* 96: 245205.

19 Zhang, Y., Neal, A., Xia, Z. et al. (2018). Demonstration of high mobility and quantum transport in modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructures. *Appl. Phys. Lett.* 112: 173502.

20 Onuma, T., Saito, S., Sasaki, K. et al. (2016). Temperature-dependent exciton resonance energies and their correlation with IR-active optical phonon modes in β-Ga_2O_3 single crystals. *Appl. Phys. Lett.* 108: 101904.

21 Schubert, M., Korlacki, R., Knight, S. et al. (2016). Anisotropy, phonon modes, and free charge carrier parameters in monoclinic β-gallium oxide single crystals. *Phys. Rev. B* 93: 125209.

22 Ma, N., Tanen, N., Verma, A. et al. (2016). Intrinsic electron mobility limits in β-Ga_2O_3. *Appl. Phys. Lett.* 109: 212101.

23 Ghosh, K. and Singisetti, U. (2016). *Ab initio* calculation of electron–phonon coupling in monoclinic β-Ga_2O_3 crystal. *Appl. Phys. Lett.* 109: 072102.

24 Ghosh, K. and Singisetti, U. (2017). *Ab initio* velocity-field curves in monoclinic β-Ga_2O_3. *J. Appl. Phys.* 122: 035702.

25 Lyons, J.L. (2018). A survey of acceptor dopants for β-Ga_2O_3. *Semicond. Sci. Technol.* 33: 05LT02.

26 Peelaers, H., Lyons, J.L., Varley, J.B., and Van de Walle, C.G. (2019). Deep acceptors and their diffusion in Ga_2O_3. *APL Mater* 7: 022519.

27 Gake, T., Kumagai, Y., and Oba, F. (2019). First-principles study of self-trapped holes and acceptor impurities in Ga_2O_3 polymorphs. *Phys. Rev. Mater.* 3: 044603.

28 Varley, J.B., Weber, J.R., Janotti, A., and Van de Walle, C.G. (2010). Oxygen vacancies and donor impurities in β-Ga_2O_3. *Appl. Phys. Lett.* 97: 142106.

29 Varley, J.B., Janotti, A., Franchini, C., and Van de Walle, C.G. (2012). Role of self-trapping in luminescence and p-type conductivity of wide-band-gap oxides. *Phys. Rev. B* 85: 081109(R).

30 Wong, M.H., Morikawa, Y., Sasaki, K. et al. (2016). Characterization of channel temperature in Ga_2O_3 metal-oxide-semiconductor field effect transistors by electrical measurements and thermal modeling. *Appl. Phys. Lett.* 109: 193503.

31 Zhou, H., Maize, K., Qiu, G. et al. (2017). β-Ga_2O_3 on insulator field-effect transistors with drain currents exceeding 1.5 a/mm and their self-heating effect. *Appl. Phys. Lett.* 111: 092102.

32 Singh, M., Casbon, M.A., Uren, M.J. et al. (2018). Pulsed large signal RF performance of field-plated Ga_2O_3 MOSFETs. *IEEE Electron Device Lett.* 39 (10): 1572–1575.

33 Pomeroy, J.W., Middleton, C., Singh, M. et al. (2019). Raman thermography of peak channel temperature in β-Ga_2O_3 MOSFETs. *IEEE Electron Device Lett.* 40 (2): 189–192.

34 Mahajan, B.K., Chen, Y.-P., Noh, J. et al. (2019). Electrothermal performance limit of β-Ga_2O_3 field-effect transistors. *Appl. Phys. Lett.* 115: 173508.

35 Handwerg, M., Mitdank, R., Galazka, Z., and Fischer, S.F. (2015). Temperature-dependent thermal conductivity in Mg-doped and undoped β-Ga_2O_3 bulk-crystals. *Semicond. Sci. Technol.* 30: 024006.

36 Guo, Z., Verma, A., Wu, X. et al. (2015). Anisotropic thermal conductivity in single crystal β-gallium oxide. *Appl. Phys. Lett.* 106: 111909.

37 Santia, M.D., Tandon, N., and Albrecht, J.D. (2015). Lattice thermal conductivity in β-Ga_2O_3 from first principles. *Appl. Phys. Lett.* 107: 041907.

38 Slomski, M., Blumenschein, N., Paskov, P.P. et al. (2017). Anisotropic thermal conductivity of β-Ga_2O_3 at elevated temperatures: effect of Sn and Fe dopants. *J. Appl. Phys.* 121: 235104.

39 Jiang, P., Qian, X., Li, X., and Yang, R. (2018). Three-dimensional anisotropic thermal conductivity tensor of single crystalline β-Ga_2O_3. *Appl. Phys. Lett.* 113: 232105.

40 Lin, C.-H., Hatta, N., Konishi, K. et al. (2019). Single-crystal-Ga_2O_3/polycrystalline-SiC bonded substrate with low thermal and electrical resistances at the heterointerface. *Appl. Phys. Lett.* 114: 032103.

41 Xu, Y., Mu, F., Wang, Y. et al. (2019). Direct wafer bonding of Ga_2O_3–SiC at room temperature. *Ceram. Int.* 45 (5): 6552–6555.

42 Víllora, E.G., Shimamura, K., Yoshikawa, Y. et al. (2004). Large-size β-Ga_2O_3 single crystals and wafers. *J. Cryst. Growth* 270: 420–426.

43 Suzuki, N., Ohira, S., Tanaka, M. et al. (2007). Fabrication and characterization of transparent conductive Sn-doped β-Ga_2O_3 single crystal. *Phys. Status Solidi C* 4 (7): 2310–2313.

44 Tomm, Y., Reiche, P., Klimm, D., and Fukuda, T. (2000). Czochralski grown Ga_2O_3 crystals. *J. Cryst. Growth* 220: 510–514.

45 Galazka, Z., Uecker, R., Klimm, D. et al. (2017). Scaling-up of bulk β-Ga_2O_3 single crystals by the Czochralski method. *ECS J. Solid State Sci. Technol.* 6 (2): Q3007–Q3011.

46 Hoshikawa, K., Ohba, E., Kobayashi, T. et al. (2016). Growth of β-Ga_2O_3 single crystals using vertical Bridgman method in ambient air. *J. Cryst. Growth* 447: 36–41.

47 Aida, H., Nishiguchi, K., Takeda, H. et al. (2008). Growth of β-Ga_2O_3 single crystals by the edge-defined, film fed growth method. *Jpn. J. Appl. Phys.* 47 (11): 8506–8509.

48 Kuramata, A., Koshi, K., Watanabe, S. et al. (2016). High-quality β-Ga_2O_3 single crystals grown by edge-defined film-fed growth. *Jpn. J. Appl. Phys.* 55: 1202A2.

49 Kamimura, T., Nakata, Y., Wong, M.H., and Higashiwaki, M. (2019). Normally-off Ga_2O_3 MOSFETs with unintentionally nitrogen-doped channel layer grown by plasma-assisted molecular beam epitaxy. *IEEE Electron Device Lett.* 40 (7): 1064–1067.

50 Kalarickal, N.K., Xia, Z., McGlone, J. et al. (2019). Mechanism of Si doping in plasma assisted MBE growth of β-Ga_2O_3. *Appl. Phys. Lett.* 115: 152106.

51 Nomura, K., Goto, K., Togashi, R. et al. (2014). Thermodynamic study of β-Ga_2O_3 growth by halide vapor phase epitaxy. *J. Cryst. Growth* 405: 19–22.

52 Murakami, H., Nomura, K., Goto, K. et al. (2015). Homoepitaxial growth of β-Ga_2O_3 layers by halide vapor phase epitaxy. *Appl. Phys. Express* 8: 015503.

53 Goto, K., Konishi, K., Murakami, H. et al. (2018). Halide vapor phase epitaxy of Si doped β-Ga_2O_3 and its electrical properties. *Thin Solid Films* 666: 182–184.

54 Wagner, G., Baldini, M., Gogova, D. et al. (2014). Homoepitaxial growth of β-Ga_2O_3 layers by metal-organic vapor phase epitaxy. *Phys. Status Solidi A* 211 (1): 27–33.

55 Zhang, Y., Alema, F., Mauze, A. et al. (2019). MOCVD grown epitaxial β-Ga_2O_3 thin film with an electron mobility of 176 $cm^2/V\,s$ at room temperature. *APL Mater.* 7: 022506.

56 Feng, Z., Bhuiyan, A.F.M.A.U., Karim, M.R., and Zhao, H. (2019). MOCVD homoepitaxy of Si-doped (010) β-Ga_2O_3 thin films with superior transport properties. *Appl. Phys. Lett.* 114: 250601.

57 Bhuiyan, A.F.M.A.U., Feng, Z., Johnson, J.M. et al. (2019). MOCVD epitaxy of β-$(Al_xGa_{1-x})_2O_3$ thin films on (010) Ga_2O_3 substrates and N-type doping. *Appl. Phys. Lett.* 115: 120602.

58 Kawaharamura, T., Dang, G.T., and Furuta, M. (2012). Successful growth of conductive highly crystalline Sn-doped α-Ga_2O_3 thin films by fine-channel mist chemical vapor deposition. *Jpn. J. Appl. Phys.* 51: 040207.

59 Oshima, T., Nakazono, T., Mukai, A., and Ohtomo, A. (2012). Epitaxial growth of γ-Ga_2O_3 films by mist chemical vapor deposition. *J. Cryst. Growth* 359: 60–63.

60 Tahara, D., Nishinaka, H., Morimoto, S., and Yoshimoto, M. (2017). Stoichiometric control for heteroepitaxial growth of smooth ε-Ga_2O_3 thin films on c-plane AlN templates by mist chemical vapor deposition. *Jpn. J. Appl. Phys.* 56: 078004.

61 Yang, J., Ren, F., Tadjer, M. et al. (2018). 2300V reverse breakdown voltage Ga_2O_3 Schottky rectifiers. *ECS J. Solid State Sci. Technol.* 7 (5): Q92–Q96.

62 Li, W., Hu, Z., Nomoto, K. et al. (2018). 2.44 kV Ga_2O_3 vertical trench Schottky barrier diodes with very low reverse leakage current. *Proceedings of the International Electron Device Meeting*, San Francisco, CA, USA (3–5 December 2018). IEEE Xplore.

63 Sasaki, K., Takatsuka, A., Otsuka, F. et al. (2019). Demonstration of over 10-A Ga_2O_3 Schottky barrier diodes fabricated by using high-quality β-Ga_2O_3 homoepitaxial films. *Abstract of 3rd International Workshop on Gallium Oxide and Related Materials*, Columbus, OH, USA (12–15 August 2019).

64 Fares, C., Ren, F., and Pearton, S.J. (2019). Temperature-dependent electrical characteristics of β-Ga_2O_3 diodes with W Schottky contacts up to 500°C. *ECS J. Solid State Sci. Technol.* 8 (7): Q3007–Q3012.

65 Higashiwaki, M., Konishi, K., Sasaki, K. et al. (2016). Temperature-dependent capacitance–voltage and current–voltage characteristics of Pt/Ga_2O_3(001) Schottky barrier diodes fabricated on n^-–Ga_2O_3 drift layers grown by halide vapor phase epitaxy. *Appl. Phys. Lett.* 108: 133503.

66 Lin, C.-H., Yuda, Y., Wong, M.H. et al. (2019). Vertical Ga_2O_3 Schottky barrier diodes with guard ring formed by nitrogen-ion implantation. *IEEE Electron Device Lett.* 40 (9): 1487–1490.

67 Wong, M.H., Lin, C.-H., Kuramata, A. et al. (2018). Acceptor doping of β-Ga_2O_3 by Mg and N ion implantations. *Appl. Phys. Lett.* 113: 102103.

68 Li, W., Nomoto, K., Hu, Z. et al. (2019). Fin-channel orientation dependence of forward conduction in kV-class Ga_2O_3 trench Schottky barrier diodes. *Appl. Phys. Express* 12: 061007.

69 Oda, M., Tokuda, R., Kambara, H. et al. (2016). Schottky barrier diodes of corundum-structured gallium oxide showing on-resistance of 0.1 $m\Omega\,cm^2$ grown by MIST EPITAXY®. *Appl. Phys. Express* 9: 021101.

70 Watahiki, T., Yuda, Y., Furukawa, A. et al. (2017). Heterojunction p-Cu_2O/n-Ga_2O_3 diode with high breakdown voltage. *Appl. Phys. Lett.* 111: 222104.

71 Higashiwaki, M., Sasaki, K., Kuramata, A. et al. (2012). Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3(010) substrates. *Appl. Phys. Lett.* 100: 013504.

72 Sasaki, K., Higashiwaki, M., Kuramata, A. et al. (2013). Si-ion implantation doping in β-Ga_2O_3 and its application to fabrication of low-resistance ohmic contacts. *Appl. Phys. Express* 6: 086502.

73 Higashiwaki, M., Sasaki, K., Kamimura, T. et al. (2013). Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors on β-Ga_2O_3(010) substrates and temperature dependence of their device characteristics. *Appl. Phys. Lett.* 103: 123511.

74 Wong, M.H., Sasaki, K., Kuramata, A. et al. (2016). Field-plated Ga_2O_3 MOSFETs with a breakdown voltage of over 750 V. *IEEE Electron Device Lett.* 37 (2): 212–215.

75 Mun, J.K., Cho, K., Chang, W. et al. (2019). 2.32 kV breakdown voltage lateral β-Ga_2O_3 MOSFETs with source-connected field plate. *ECS J. Solid State Sci. Technol.* 8 (7): Q3079–Q3082.

76 Zeng, K., Vaidya, A., and Singisetti, U. (2019). A field-plated Ga_2O_3 MOSFET with near 2-kV breakdown voltage and 520 mΩ·cm^2 on-resistance. *Appl. Phys. Express* 12: 081003.

77 Ahmadi, E., Koksaldi, O.S., Zheng, X. et al. (2017). Demonstration of β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 modulation doped field-effect transistors with Ge as dopant grown via plasma-assisted molecular beam epitaxy. *Appl. Phys. Express* 10: 071101.

78 Krishnamoorthy, S., Xia, Z., Joishi, C. et al. (2017). Modulation-doped β-$(Al_{0.2}Ga_{0.8})_2O_3$/Ga_2O_3 field-effect transistor. *Appl. Phys. Lett.* 111: 023502.

79 Joishi, C., Zhang, Y., Xia, Z. et al. (2019). Breakdown characteristics of β-$(Al_{0.22}Ga_{0.78})_2O_3$/$Ga_2O_3$ field-plated modulation-doped field-effect transistors. *IEEE Electron Device Lett.* 40 (8): 1241–1244.

80 Chabak, K.D., Moser, N., Green, A.J. et al. (2016). Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate with high breakdown voltage. *Appl. Phys. Lett.* 109: 213501.

81 Wong, M.H., Nakata, Y., Kuramata, A. et al. (2017). Enhancement-mode Ga_2O_3 MOSFETs with Si-ion-implanted source and drain. *Appl. Phys. Express* 10: 041101.

82 Chabak, K.D., McCandless, J.P., Moser, N.A. et al. (2018). Recessed-gate enhancement-mode β-Ga_2O_3 MOSFETs. *IEEE Electron Device Lett.* 39 (1): 67–70.

83 Wong, M.H., Goto, K., Murakami, H. et al. (2019). Current aperture vertical β-Ga_2O_3 MOSFETs fabricated by N- and Si-ion implantation doping. *IEEE Electron Device Lett.* 40 (3): 431–434.

84 Wong, M.H., Murakami, H., Kumagai, Y., and Higashiwaki, M. (2019). Enhancement-mode current aperture vertical Ga_2O_3 MOSFETs. *Abstract of 77th Device Research Conference*, Ann Arbor, MI, USA (23–26 June 2019).

85 Hu, Z., Nomoto, K., Li, W. et al. (2018). Enhancement-mode Ga_2O_3 vertical transistors with breakdown voltage >1 kV. *IEEE Electron Device Lett.* 39 (6): 869–872.

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First Edition. Edited by Peter Wellmann, Noboru Ohtani, and Roland Rupp.

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