# 7

# Optical Receiver Front-End Integrated Circuit Design

In the intensity-modulation/direct-detection (IM-DD) system, the intensity modulation means that information is carried only by the intensity or power of the transmitted lightwave, not by its frequency or phase. The term direct detection refers to the receiver configuration, where the received signal is applied directly to a photodetector (PD). The optical receiver is a combination of the optical detector, electronic preamplifier, and the electronic processing elements that recover information sent on the optical signal. The role of an optical receiver is to convert the optical signal back into electrical form and recover the data transmitted through the lightwave system. It should have high sensitivity, fast response, low noise, low cost, and high reliability. Its size should be compatible with the fiber-core size. The most important part in an optical receiver is the front-end circuit, which consists of a PD and transimpedance preamplifier. Figure 7.1 shows the signal transmission in an optical front-end circuit. An attenuated optical signal modulated with an electrical pulse signal (bit rate is $1/T_b$) is the input of the optical receiver and the optical signal will be transformed to an electric signal current by a photodiode and then amplified by a transimpedance preamplifer before passing through electronic processing elements for regeneration.

The optical receivers have key roles in high-speed optical fiber communications, in high-speed chip-to-chip interconnections in computers, efficient networking between computers, and in other diverse areas such as medical imaging. Recent trends in optical fiber communication systems experimentation have been towards a 10–40 Gb/s channel bandwidth. This has increased the emphasis on receiver performance. Particular requirements include ultra-wide bandwidth, high sensitivity, and a large dynamic range for use with unbounded line codes [1, 2, 3, 4, 5, 6, 7, 8]. Ultra-wide bandwidth optical receivers are critical components for multi-gigabit/s direct detection transmission systems, as well as for future subcarrier-multiplexed or coherent

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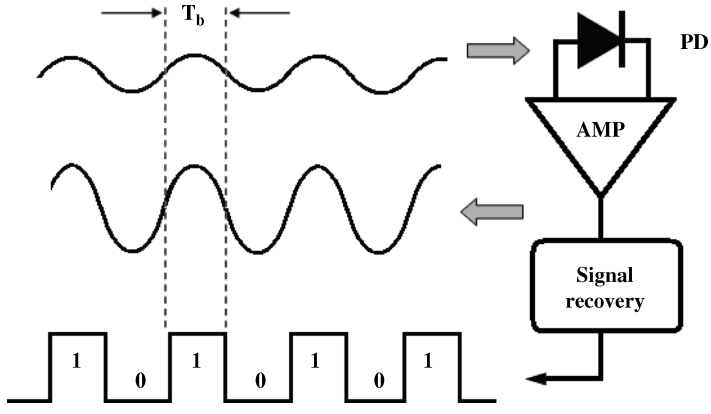



**Figure 7.1** Signal transmission in an optical front-end circuit.

communications systems. One of the most critical building blocks in an optical link system is the front end, which consists of a photodiode (PD) and a preamplifier. The performance of such a receiver is determined to a large extent by the front-end circuit. An integrated front-end photoreceiver consists of a photodetector and an amplifier fabricated on a single chip.

In this chapter, we will introduce the basic concept of a high-speed receiver, the integrated circuit (IC) technique of the front-end. Subsequently, passive peaking techniques for a preamplifier are described.

## 7.1 Basic Concepts of the Optical Receiver

This section introduces basic concepts such as signal-to-noise ratio (SNR), bit error ratio (BER), sensitivity, bandwidth, and dynamic range. To understand these figures of merit is very useful for designing an optimum front-end optical receiver.

### *7.1.1 Signal-to-Noise Ratio*

In optical communication systems, the SNR of the receiver is a measure of signal strength relative to background noise at the input port, expressed as a simple arithmetic ratio or in decibels:

$$SNR = \frac{\text{Signal power at the input port}}{\text{Noise power at the input port}} = \frac{I_p^2}{\langle N^2 \rangle} \tag{7.1}$$

where $I_p^2$ is the average power of the photocurrent and $\langle N^2 \rangle$ is the average power of the equivalent input noise current for the optical receiver. $\langle N^2 \rangle$ consists of the shot

noise generated by PD $\langle N_{PD}^2 \rangle$ and preamplifier noise $\langle N_A^2 \rangle$, and can be expressed as follows:

$$\langle N^2 \rangle = \langle N_{PD}^2 \rangle + \langle N_A^2 \rangle \tag{7.2}$$

Based on the PIN PD and APD PD noise model described in Chapter NaN, the shot noise generated by PD $\langle N_{PD}^2 \rangle$ can be expressed as:

$$\langle N_{PD}^2 \rangle = 2q(I_p + I_{dark})\Delta f \qquad \text{for PIN PD} \tag{7.3}$$

$$\langle N_{PD}^2 \rangle = 2qM^2F(M)(I_p + I_{dark})\Delta f \qquad \text{for APD PD} \tag{7.4}$$

where $\Delta f$ is the noise-effective bandwidth and can in turn be determined by the transfer function of the receiver:

$$B = \frac{1}{|H(0)|^2}\int_0^\infty |H(f)|^2 \mathrm{d}f \tag{7.5}$$

where $H(0)$ is the asymptotic value of the transfer function $H(f)$ at low frequencies.

The previously described receiver noise can introduce serious degradations in the system bit error ratio and must be strongly suppressed in high-speed optical systems.

### 7.1.2 Bit Error Ratio

The goal of any digital transmission system is to deliver error-free information reliably and economically from one location to another. Therefore, the quality of transmission systems can be evaluated using the bit error ratio (BER). A digital receiver must take a weak optical signal and convert it into an electrical signal, and the decision circuit determines if a bit is a zero or a one by comparing the output voltage to the threshold voltage, which is located at the midpoint between zero and one, and finally generate an electronically compatible voltage representative of the logic state. The performance criterion for digital receivers is governed by the BER, defined as the number of bits received in error divided by the number of bits transmitted, which equals the error count in a measurement period divided by the product of the bit rate and the measurement period. The BER can be expressed as follows:

$$BER = \frac{N_e}{N_t} = \frac{N_e}{Bt} = \frac{T_b N_e}{t} \tag{7.6}$$

where $N_e$ is the bits of incorrect identification, $N_t$ is the total transmission bits, $B$ is the bit rate, and $T_b = 1/B$ is the pulse width. A commonly used criterion for digital optical

receivers requires the BER to be below $10^{-9}$, corresponding to an average of 1 error per billion bits.

Figure 7.2 shows the probability density curves for a logical 1 and a logical 0. The total probability of making an error is the sum of the probability of deciding 0 when 1 is received and the probability of deciding 1 when 0 is received; therefore, the BER can be expressed as follows:

$$BER = P(1)P(0/1) + P(0)P(1/0) \tag{7.7}$$

where $P(1)$ and $P(0)$ are the probabilities of receiving bits 1 and 0, respectively, $P(0/1)$ is the probability of deciding 0 when 1 is received, and $P(0/1)$ is the probability of deciding 1 when 0 is received [1].

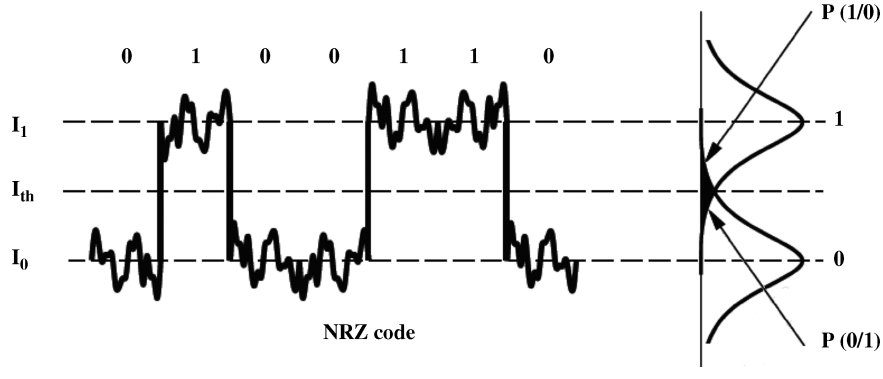



**Figure 7.2** Probability density curves for a logical 1 and a logical 0.

When average and variance values are $I_1$ and $\langle N_1 \rangle$ for 1 and average and variance values are $I_0$ and $\langle N_0 \rangle$ for 0, the BER can be expressed in terms of $I_1$, $I_0$, $\langle N_1 \rangle$, and $\langle N_0 \rangle$ as follows:

$$BER = \frac{1}{2}\text{erfc}\left(\frac{Q}{\sqrt{2}}\right) \approx \frac{\exp(-Q^2/2)}{Q/\sqrt{2\pi}} \tag{7.8}$$

with

$$Q = \frac{I_1 - I_0}{\langle N_1 \rangle + \langle N_0 \rangle}$$

where the complementary error function is defined as

$$\text{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty \exp(-y^2)\text{d}y \tag{7.9}$$

Table 7.1 shows how the BER varies with the $Q$ parameter; it can be found that the requirement of $Q$ is more than 6 for BER less than $10^{-9}$. When $\langle N_1 \rangle = \langle N_0 \rangle$, $I_{th} = (I_1 + I_0)/2$, which corresponds to setting the decision threshold in the middle. The BER can be simplified as follows [2]:

$$BER = \frac{1}{2}\text{erfc}\left(\frac{I_1}{2\sqrt{2}\langle N_1 \rangle}\right) = \frac{1}{2}\text{erfc}\left(\frac{\sqrt{SNR}}{2\sqrt{2}}\right) \tag{7.10}$$

**Table 7.1** BER versus $Q$.

| $Q$ | BER | $Q$ | BER |
|---|---|---|---|
| 0.0 | 0.5 | 5.998 | $10^{-9}$ |
| 3.090 | $10^{-3}$ | 6.361 | $10^{-10}$ |
| 3.719 | $10^{-4}$ | 6.706 | $10^{-11}$ |
| 4.265 | $10^{-5}$ | 7.035 | $10^{-12}$ |
| 4.753 | $10^{-6}$ | 7.349 | $10^{-13}$ |
| 5.199 | $10^{-7}$ | 7.651 | $10^{-14}$ |
| 5.612 | $10^{-8}$ | 7.942 | $10^{-15}$ |

### *7.1.3 Sensitivity*

An important performance measure for optical receivers is receiver sensitivity. To allow large repeater separations in an optical communication system, therefore, receivers have been designed to have good sensitivity, that is to require only a very low level of mean received optical power while operating within the maximum specified BER necessary to achieve a BER of $10^{-9}$. In addition to direct measurement of the sensitivity through BER measurements, the sensitivity of a photoreceiver can be estimated from the analog noise performance. A simple analysis that considers only noise and finite bandwidth contributions to BER results is given in the following expression for the sensitivity:

$$\overline{P} = \frac{h\upsilon}{\eta q} SNR_{\min} \sqrt{\overline{i_{in}^2}} \tag{7.11}$$

where

$\eta$ = photodiode external quantum efficient
$\upsilon$ = frequency of the incident light
$h$ = Planck's constant
$q$ = electronic charge

$SNR_{\min}$ = minimum signal-to-noise ratio required to achieve the desired bit error ratio
$\overline{i_{in}^2}$ = mean square noise current at the input of the receiver

This expression assumes that the detector bandwidth is sufficiently large so that the detector responsivity can be assumed to be constant for the frequencies of interest and that the amplifier exhibits a single-pole low-pass frequency response. Receiver sensitivity is determined by the SNR and the noise current at the input to the decision circuit in the regenerator. Optical receivers that employ an APD generally provide a higher SNR for the same incident optical power. The improvement is due to the internal gain, which increases the photocurrent by a multiplication factor $M$. Table 7.2 shows the comparison of typical PIN and APD receiver sensitivity. It can be found that sensitivity of the APD receiver is higher by 10 dB than the PIN receiver when the multiplication factor $M$ is 10.

**Table 7.2** Typical PIN/APD receiver sensitivity.

| Bit rate | 2.5 Gb/s | 10 Gb/s |
|---|---|---|
| Noise current of preamplifier | 400 nA | 1.2 μA |
| PIN receiver | −24.3 dBm | −19.5 dBm |
| APD receiver | −34.3 dBm | −29.5 dBm |

### *7.1.4 Eye Diagram*

High-speed optical transmission systems often suffer serious impairment due to low-probability phenomena such as modulation fluctuation and spectrum fluctuation of lasers. Degradation of quality occurs in each process: modulation, transmission, and detection. The eye pattern of the receiving amplifier output contains all the information concerning the degradation of quality. Therefore, the analysis of the eye pattern is important in analyzing the degradation mechanism. The eye diagram can be applied to many types of investigation, for example modulation characteristics and transmission characteristics of laser diodes, analysis of noise, jitter, intersymbol interference, and estimation of eye margin [3, 4, 9].

The eye diagram is formed by superposing 2–3 bit-long electrical sequences in the bit stream on top of each other. The resulting pattern is called an eye diagram because of its appearance. The best sampling time corresponds to maximum opening of the eye. Eye patterns can be observed using an oscilloscope. The oscilloscope is synchronized so that the pulses overlap on the screen. Since the bit pattern is random, if we consider a 4-bit pattern, the combinations can be only the following:

0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111,
1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111

Since 0 represents no light pulse and 1 represents the presence of a light pulse, an overlap of all the pulses is shown in Figure 7.3. The figure formed by the overlapping pulses is the eye diagram and the center is called the *eye*.

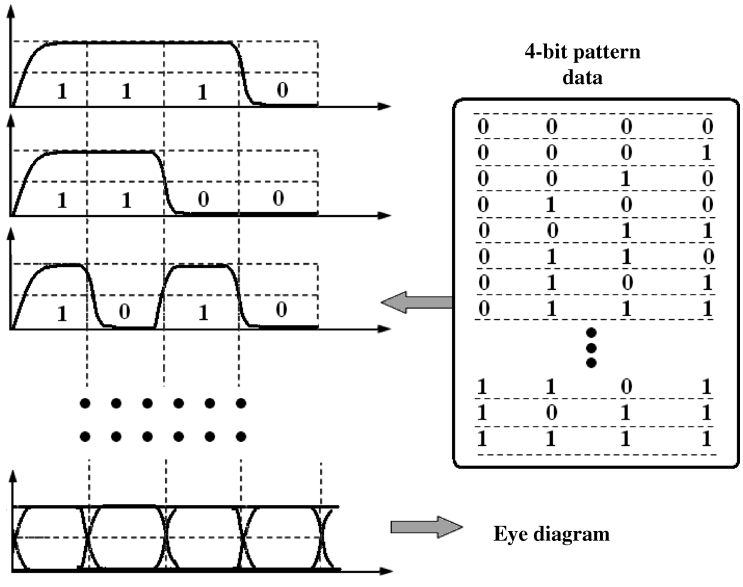



**Figure 7.3** Eye pattern formed by overlapping the random pulse sequence. In this case the eye is open.

The resulting eye diagram contains a number of easily observed information about the digital transmission characteristics of the optical receiver (as shown in Figure 7.4):

1. Rise time and fall time of bit transition. The rise/fall time (20–80 %) is an analog parameter of fundamental importance in a high-speed optical receiver, since it is a measure of the ability of a circuit to respond to fast input signals.
2. Extinction ratio. The extinction ratio is an important specified test parameter for high-speed transmission systems and is typically defined as:

$$ER = 10 \log \frac{\overline{P_1}}{\overline{P_0}} \tag{7.12}$$

   where $\overline{P_1}$ and $\overline{P_0}$ are the mean or average optical power level of the logic 1 level and logic 0 level, respectively.
3. Jitter at the transition point. As shown in Figure 7.4, jitter can be measured in the eye diagram by computing a histogram of the time points when the signal crosses a

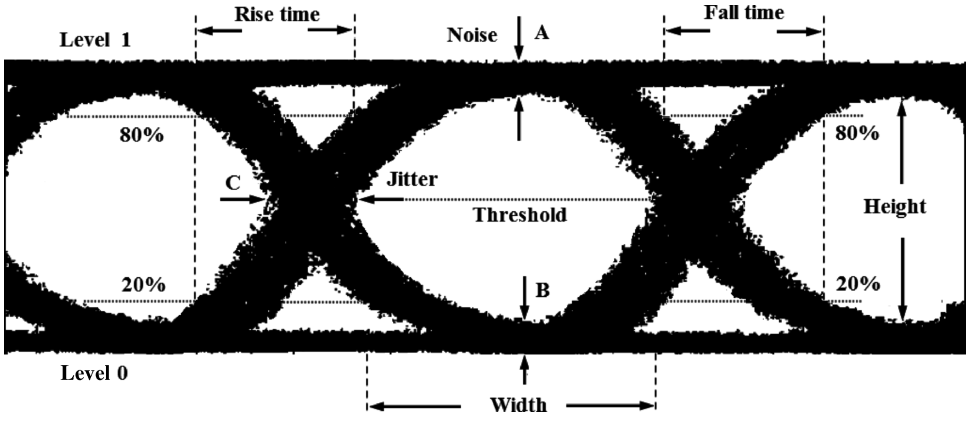



**Figure 7.4** Representative eye diagram.

reference voltage, that is the width of the threshold crossing ('C' on the figure). This voltage is set to the eye crossing point where the histogram has the tightest distribution. Many sampling oscilloscopes have the capability to calculate and display such histograms. From Figure 7.4, it can be found that the eye pattern when the pulses have suffered dispersion and have some jitter (that is the time interval between adjacent pulses does not remain constant but keeps changing randomly). The timing jitter is defined as (in %)

$$\text{Timing jitter}(\text{in }\%) = \frac{\Delta t}{T_b} \times 100\,\% \tag{7.13}$$

where $T_b$ is the bit spacing in the data stream. This jitter is an indication of the timing accuracy of received pulse as modified by the receiver.

4. Eye opening height. This height is a measure of the amplitude distortion of the signal; the extinction ratio increases with the increase of eye opening height.
5. Eye opening width. This width gives the optimum sampling time interval for the received signal to be sampled without error from intersymbol interference.
6. Noise level. The noise level of the output signal of the receiver can be determined from the spacing of 'A' and 'B' on the figure.

### *7.1.5 Signal Bandwidth*

In this section, we will introduce how to determine the optimum signal bandwidth of the receiver. Figure 7.5 shows the normalized spectrum of the NRZ code. It is obvious that the signal bandwidth of the receiver should be equal to the bit rate in order to cover the frequency occupied by the NRZ code. However, due to the fact that most frequency spectrums (more than 90 %) concentrate on the frequency 0–0.8$B$, it is usually

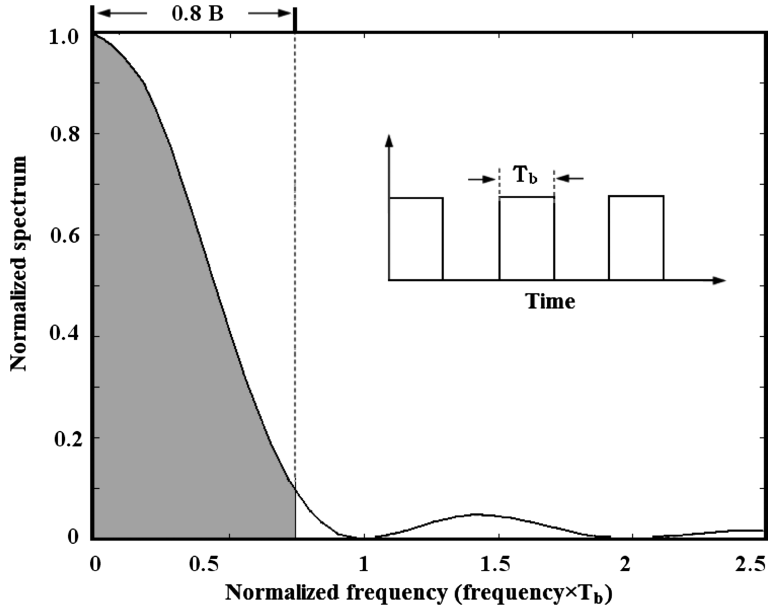



**Figure 7.5** Normalized spectrum of the NRZ code.

common to design the receiver, with a bandwidth of 80 % of the data rate. This means that

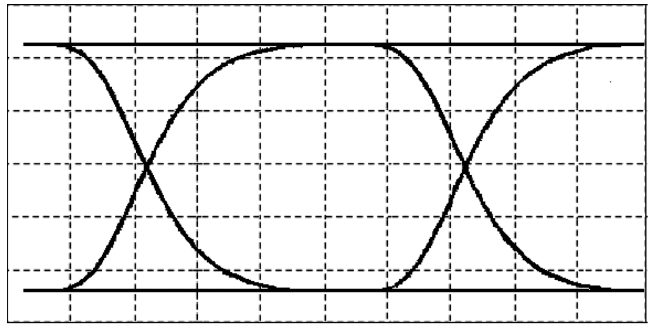
$$BW_R \geq 0.8B = \frac{0.8}{T_b} \tag{7.14}$$

Therefore, the bandwidth requirement of the high-speed optical receiver is 80 % of the required bit rate; that is, for a 10 Gb/s optical receiver design, an 8 GHz signal bandwidth is enough. Similarly, a 32 GHz signal bandwidth is enough for a 40 Gb/s optical receiver design. Figure 7.6 shows the eye diagram of the output signal with different bandwidths of the optical receiver [7], where it can be seen that the rise/fall times and noise level increase with the decrease of the bandwidth.

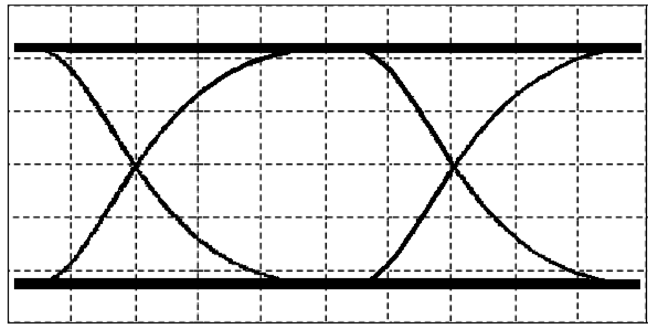
### *7.1.6 Dynamic Range*

Dynamic range is defined as the difference between the maximum and minimum signal levels that the system can accommodate. The maximum and minimum levels are sometimes defined rather arbitrarily; the minimum signal level is often defined as the sensitivity. The *dynamic range* of the receiver can be expressed as

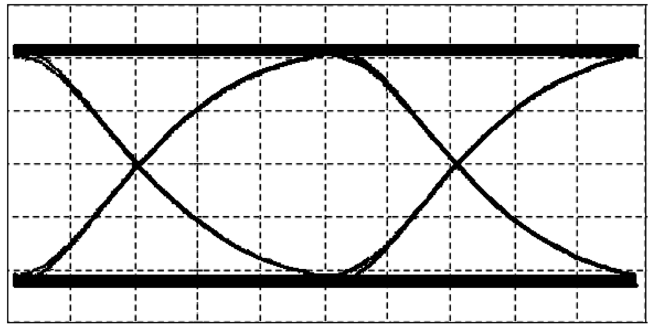
$$\text{Dynamic range} = P_{\max} - \overline{P} \tag{7.15}$$



(a) $BW_R = B$



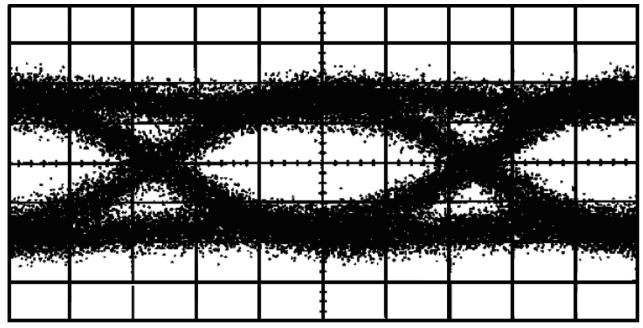
(b) $BW_R = 0.7B$



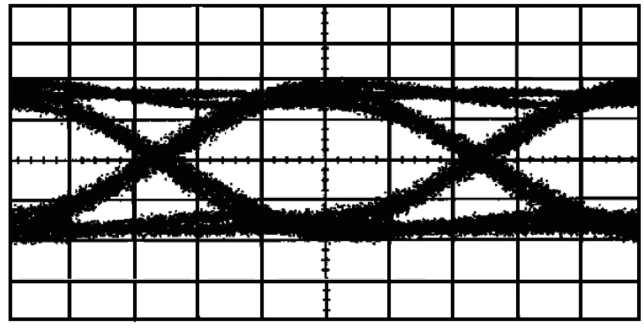
(c) $BW_R = 0.5B$

**Figure 7.6** Eye diagram of the output signal with different bandwidths of the optical receiver: (a) $BW_R = B$; (b) $BW_R = 0.7B$; and (c) $BW_R = 0.5B$.

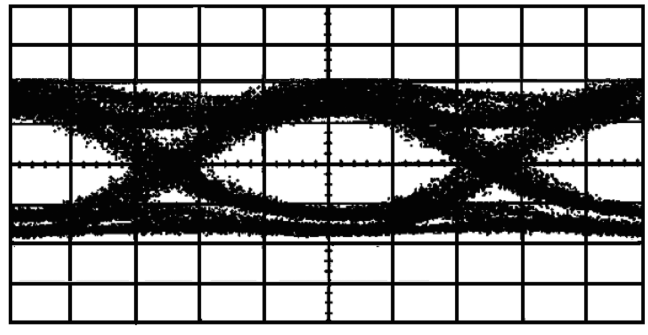
Figure 7.7 shows the eye diagram of the output signal with different input power of a 10 Gb/s optical receiver [10]. It is seen that well-opened eye diagrams are obtained for a wide input dynamic range.



(a) $P_{in} = -20\,\text{dBm}$



(b) $P_{in} = -10\,\text{dBm}$



(c) $P_{in} = 0\,\text{dBm}$

**Figure 7.7** Eye diagram of the output signal with different input power of the optical receiver: (a) $P_{in} = -20\,\text{dBm}$; (b) $P_{in} = -10\,\text{dBm}$; and (c) $P_{in} = 0\,\text{dBm}$.

## 7.2 Front-End Circuit Design

An integrated lightwave receiver front-end is made of two basic elements: the PD and the electronic amplifier. The choice of optical device technology for the PD and electronic device technology are based on three criteria: performance (sensitivity,

frequency response, and noise), ease of monolithic integration, and maturity of technology. The noise performance of the electronic devices is important at high bit rates, because the device noise dominates the input equivalent noise of the receiver.

### *7.2.1 Hybrid and Monolithic OEIC*

The monolithic optoelectronic integrated circuits (MOEICs) and hybrid optoelectronic integrated circuits (HOEICs) are two kinds of technologies for integrating optoelectronic devices and electronic circuitry. High-performance PDs commonly used for high-speed optical fiber communication are the avalanche photodiode (APD), PIN, or metal–semiconductor–metal (MSM) PD. While APDs are attractive for high-sensitivity applications, the other two photodetectors are more suitable for OEICs. The state-of-the-art active devices for very high-speed amplifiers are heterojunction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs). Figure 7.8 shows the commonly used hybrid optoelectronic integrated optical receivers, where a matching network is normally necessary between the PD and preamplifier.

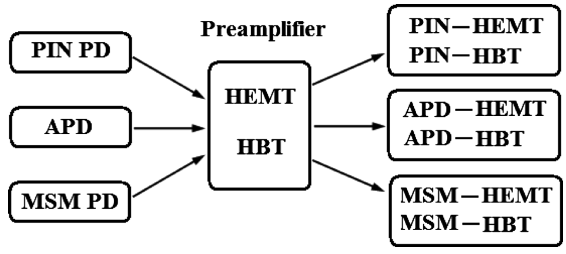



**Figure 7.8** Hybrid optoelectronic integrated optical receivers.

In order to maximize the speed of a photoreceiver front end, minimization and careful control of the interconnect parasitics between the PD and the electrical amplifier is essential. One attractive approach for reducing these interconnect parasitic elements is to integrate the PD monolithically with active electrical devices on a common substrate. Among the MSM- and PIN-based integrated photoreceivers, MSM-HEMT and PIN-HBT are two popular choices of system designers because of its mature technology (as shown in Figure 7.9):

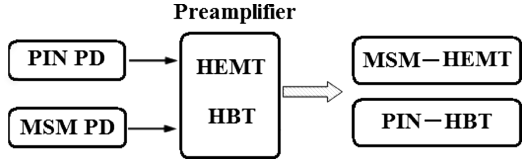



**Figure 7.9** Monolithic optoelectronic integrated optical receivers.

1. In the shared-layer integration scheme for PIN/HBT photoreceivers, the PIN layers are grown simultaneously with the growth of the epitaxial layers of HBTs. This type of integration has the advantages of one-step epitaxy, simplicity of fabrication, and possibly higher reliability.
2. Most of the beneficial properties of the MSM PD stem from its lateral planar geometry and compatibility with high-performance field-effect transistor technology and MSM PD is easily integrable with HEMT. The MSM PD and HEMT devices are integrated vertically in a stacked-layer structure. The HEMT epilayers were grown first, followed by a barrier layer of semi-insulating ferrous-doped InP. The growth of the MSM PD structure completes the growth sequence.

The design of the receiver is much more demanding than the design of the transmitter. The sensitivity of the receiver is dominated by the noise sources at the front-end and hence the design of a low-noise preamplifier is very important. The preamplifier has the following basic requirements:

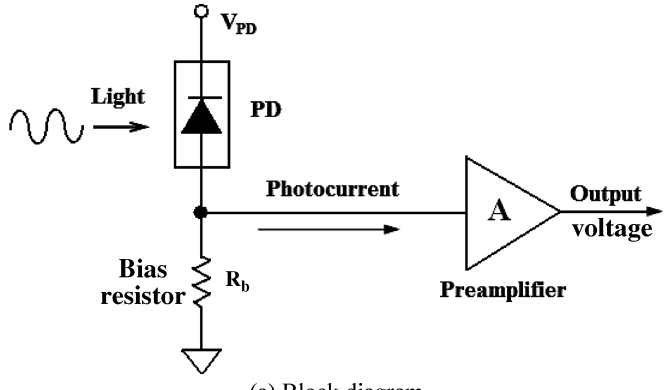
1. The transimpedance gain is high enough to override the noise of subsequent circuits.
2. Wide frequency band.
3. Low noise.
4. The input impedance is low enough to avoid degrading the frequency band with photodiode capacitance.
5. Wide dynamic range.

The two basic front-end topologies commonly used for integrated photoreceivers are: (1) the high-impedance (HZ) design and (2) the transimpedance (TZ) design [11, 12].

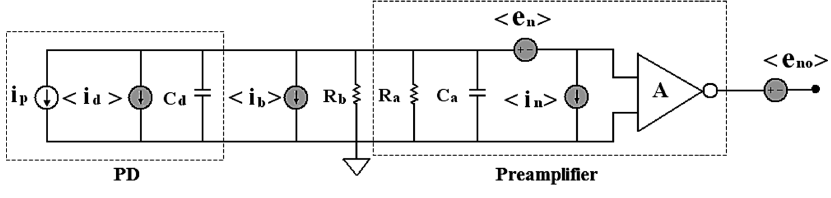
### *7.2.2 High-Impedance Front-End*

Figure 7.10(a) shows the block diagram of the HZ front-end. The HZ amplifier design achieves low noise by using a large detector biasing resistor $R_b$. The input admittance of the amplifier is therefore dominated by the total input capacitance, and the input signal tends to be integrated by this capacitance. The HZ amplifier is used in combination with an equalizer to compensate for the distortion caused by the limited bandwidth of the high input admittance.

Figure 7.10(b) shows the equivalent circuit model of the HZ front-end, where the HZ preamplifier is modeled by an arbitrarily large, noiseless, fixed gain $A$. The PD is modeled by a shunt current source for the signal current $i_p$ and a shunt capacitance $C_d$. The input impedance of the amplifier is modeled by the parallel combination of resistance $R_a$ and capacitance $C_a$. An equivalent series voltage noise source $e_n$ and an




(a) Block diagram




(b) Equivalent circuit model

**Figure 7.10** Block diagram and equivalent circuit model of the HZ front-end: (a) block diagram; (b) equivalent circuit model.

equivalent shunt current noise source $i_n$ are used to model the noisy two-port network of the preamplifier. The front-end also includes the input bias resistor $R_b$ with its equivalent thermal noise current $i_b$.

The signal transfer function for the HZ front end is

$$H_{HZ}(\omega) = \frac{v_o}{i_p} = \frac{AR_T}{1 + \omega R_T C_T} \tag{7.16}$$

The corresponding 3 dB bandwith of the signal transfer function can be determined directly from Equation (7.16):

$$BW_{HZ} = \frac{1}{2\pi R_T C_T} \tag{7.17}$$

where

$$C_T = C_d + C_a, R_T = R_a//R_b = \frac{R_a R_b}{R_a + R_b}$$

The mean square of equivalent input circuit current can be expressed as follows:

$$\frac{\mathrm{d}\langle i_{HZ}^2\rangle}{\mathrm{d}f} = \frac{\mathrm{d}\langle i_d^2\rangle}{\mathrm{d}f} + \frac{\mathrm{d}\langle i_b^2\rangle}{\mathrm{d}f} + \frac{\mathrm{d}\langle i_n^2\rangle}{\mathrm{d}f} + \left(\frac{\mathrm{d}\langle e_n^2\rangle}{\mathrm{d}f} + \frac{\mathrm{d}\langle e_{no}^2\rangle}{A^2}\right)\left[\frac{1}{R_T^2} + (\omega C_T^2)\right] \tag{7.18}$$

where $\langle e_{no}\rangle$ is the noise voltage contributed by the succeeding circuit after the preamplifier.

Although the HZ amplifier is capable of giving the absolute minimum noise and has demonstrated exceptional bandwidth, it suffers from several shortcomings. First, the amplifiers may have to be individually equalized due to their sensitivity to device and temperature variations. Furthermore, the HZ front-end reduces the dynamic range of the amplifier compared to the TZ front-end.

### *7.2.3 Transimpedance Front-End*

The TZ amplifier or shunt feedback amplifier is the most commonly used design in OEIC receivers due to its wide bandwidth and dynamic range compared to the HZ front-end. The amplifier consists of an inverting voltage amplifier with resistive feedback from output to input. In practice, the noise performance of the TZ amplifier is not as good as that achieved with the HZ amplifier, but at high bit rates, this noise performance gap decreases. With proper design the TZ amplifier can almost match the noise performance of the HZ amplifier.

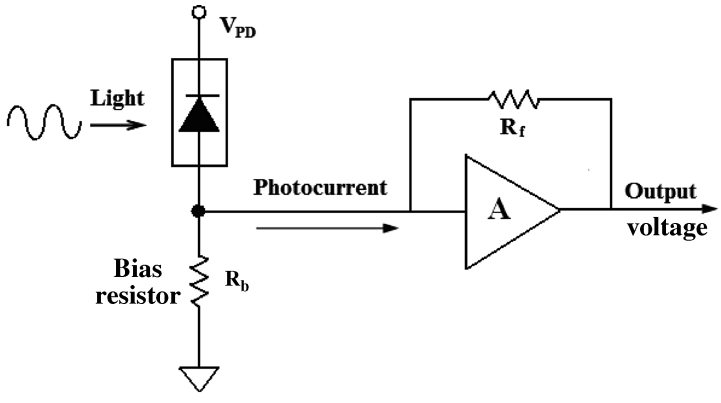
Figure 7.11(a) shows the block diagram of the TZ front-end and Figure 7.11(b) shows the corresponding equivalent circuit model, where the noise current $\langle i_f\rangle$ is generated by feedback resistance $R_f$. The signal transfer function for the TZ front-end can be expressed as follows:

$$H_{TZ}(\omega) = \frac{R_f}{1 + 1/A + R_f/(AR_T) + \mathrm{j}\omega R_f C_T/A} \tag{7.19}$$

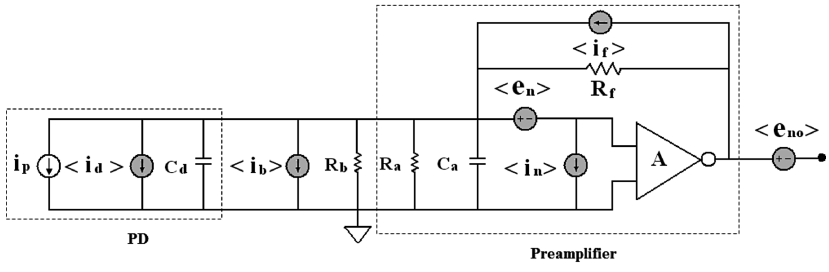
Note that

$$\lim_{A\to\infty} H_{TZ}(\omega) = R_f \tag{7.20}$$

As shown in Equations (7.19) and (7.20), the feedback resistance determines the transimpedance, and thus the sensitivity of the amplifier. Larger feedback resistances increase the sensitivity of the amplifier, but simultaneously reduce the amplifier bandwidth.




(a) Block diagram




(b) Equivalent circuit model

**Figure 7.11** Block diagram and equivalent circuit model of the TZ front-end: (a) block diagram; (b) equivalent circuit model.

The corresponding 3 dB bandwidth of the signal transfer function can be determined directly from Equation (7.19):

$$BW_{TZ} = \frac{1 + R_f/(1+A)/R_T}{2\pi C_T R_f/(1+A)} \approx \frac{1}{2\pi C_T R_f/(1+A)} \tag{7.21}$$

The mean square of equivalent input circuit current can be expressed as follows:

$$\begin{aligned} \frac{\mathrm{d}\langle i_{TZ}^2 \rangle}{\mathrm{d}f} = {} & \frac{\mathrm{d}\langle i_d^2 \rangle}{\mathrm{d}f} + \frac{\mathrm{d}\langle i_b^2 \rangle}{\mathrm{d}f} + \frac{\mathrm{d}\langle i_n^2 \rangle}{\mathrm{d}f} + \frac{\mathrm{d}\left\langle i_f^2 \right\rangle}{\mathrm{d}f} \\ & + \left( \frac{\mathrm{d}\langle e_n^2 \rangle}{\mathrm{d}f} + \frac{\mathrm{d}\langle e_{no}^2 \rangle}{A^2} \right) \left[ \frac{A^2}{R_f^2} + (\omega C_T^2) \right] \end{aligned} \tag{7.22}$$

with

$$\frac{\mathrm{d}\left\langle i_f^2 \right\rangle}{\mathrm{d}f} = \frac{4kT}{R_f}$$

Figure 7.12 shows the frequency response of the HZ and TZ front-ends, where it is obvious that the TZ front-end has a lower gain of transfer function and wide bandwidth. The ratio of gains of the HZ and TZ front-ends and the ratio of bandwidths of the HZ and TZ front-ends can be expressed as follows:

$$R_{gain} = \lim_{\omega \to 0} \frac{H_{HZ}(\omega)}{H_{TZ}(\omega)} = A\frac{R_T}{R_f} \gg 1 \tag{7.23}$$

$$R_{BW} = \frac{BW_{TZ}(\omega)}{BW_{HZ}(\omega)} = \frac{(1+A)R_T}{R_f} \gg 1 \tag{7.24}$$

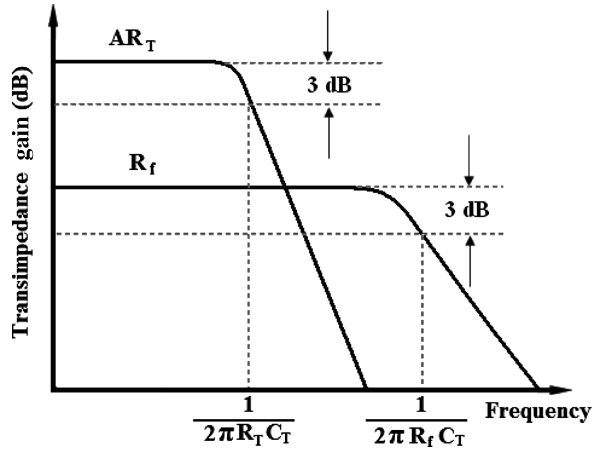



**Figure 7.12** Frequency response of the HZ and TZ front-ends.

The difference of equivalent input noise current densities of the TZ and HZ front-ends can be expressed as

$$\frac{\mathrm{d}\left\langle i_{TZ}^2 \right\rangle}{\mathrm{d}f} - \frac{\mathrm{d}\left\langle i_{HZ}^2 \right\rangle}{\mathrm{d}f} = \frac{4kT}{R_f} + \frac{\mathrm{d}\left\langle e_{no}^2 \right\rangle}{A^2}\left[\frac{A^2}{R_f^2} - \frac{1}{R_T^2}\right] \approx \frac{4kT}{R_f} \tag{7.25}$$

Table 7.3 summarizes the comparison of the HZ and TZ front-ends, showing that there is a trade-off between the bandwidth and the noise (speed versus sensitivity) of a

**Table 7.3** Comparison of optical HZ and TZ front-ends.

| Front-end | HZ | TZ | Result |
|---|---|---|---|
| Gain at low frequencies | $AR_T$ | $R_f$ | HZ |
| Bandwidth | $\dfrac{1}{2\pi R_T C_T}$ | $\dfrac{1}{2\pi C_T R_f/(1+A)}$ | TZ |
| Input impedance | $\dfrac{R_T}{1+\mathrm{j}\omega R_T C_T}$ | $\dfrac{R_f}{1+A+\mathrm{j}\omega R_f C_T}$ | TZ |
| Input noise current | $\dfrac{\mathrm{d}\langle i_{HZ}^2\rangle}{\mathrm{d}f}$ | $\dfrac{\mathrm{d}\langle i_{HZ}^2\rangle}{\mathrm{d}f}+\dfrac{\mathrm{d}\langle i_f^2\rangle}{\mathrm{d}f}$ | HZ |

TZ front-end. Additionally, the dynamic range of the TZ front-end is greater than that of the HZ front-end; for a given preamplifier, the improvement in dynamic range will be approximately the ratio of the open- and closed-loop gains.

## 7.3 Transimpedance Gain and Equivalent Input Noise Current

The major design goals of the front-ends are the transimpedance gain and equivalent input noise current density. The transimpedance gain of front-ends must be large enough to overcome the noise of the subsequent stage, typically a 50Ω driver or a limiting amplifier. The equivalent input noise current density determines the minimum input current that yields a given bit error ratio, directly impacting the link budget. Unfortunately the transimpedance gain and equivalent input noise current density cannot be measured directly from microwave and noise equipments, while the *S* parameters and noise figure of front-ends can be measured from a vector network analyzer (VNA) and noise figure meter in a straightforward manner. Therefore a fast transformation between *S* parameters/noise figure and transimpedance gain/equivalent input noise current density is needed. Although analytical expressions for transimpedance gain and equivalent input noise current of optical receivers have been derived in reference [13], simple expressions for the relationship between the transimpedance gain and *Z* parameters is given in reference [14]. However, the expressions mentioned above are not universally valid, and the transimpedance gain and equivalent input noise current density cannot be accurately calculated directly from *S* parameters and noise figure measurement data. A simple but efficient transformation technique for front-ends will be introduced in this section, and the analytical expressions for the relationships between the transimpedance gain and S parameters, equivalent input noise current density and the noise figure for high-speed optical transimpedance preamplifier design are derived. This technique is based on the signal-and-noise equivalent circuit model of the optical receiver front-end.

Compared with previous publications, this method has the following advantages:

1. The transimpedance gain can be directly derived from *S* parameters for arbitrary source and load impedance, and simplified expressions for two special cases (source impedances are zero and 50 Ω) are also given.
2. The equivalent input noise current density can be determined from the noise figure measurement without four noise parameters (minimum noise figure, noise resistance, and optimum source reflection coefficient) of the transimpedance amplifier (TIA) in 50 Ω and non-50 Ω systems.

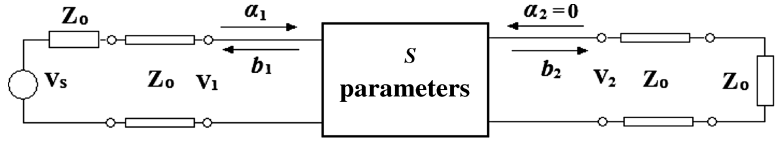
### *7.3.1 S Parameters of a Two-Port Network*

The *S* parameter characterization of two-port networks are based on exciting the network by the incident waves at the input port and output port. In this case $a_1$ and $a_2$ are the independent variables and $b_1$ and $b_2$ are the dependent variables. The network operation can be described by two equations:

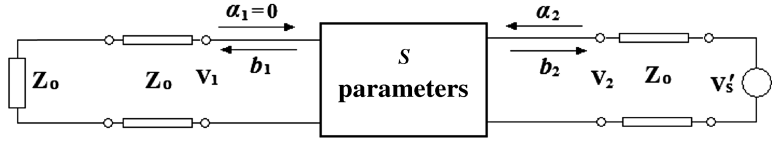
$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{7.26}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{7.27}$$

where $[S]$ is called the scattering matrix of a two-port network. $S_{ij}(i,j = 1,2)$ are known as the scattering parameters of the two-port network. Since the units of the incident and reflected waves are the same, scattering parameters must be dimensionless. As already mentioned above, the *S* parameters can only be determined under conditions of perfect matching on the input or output side. For instance, in order to record $S_{11}$ and $S_{21}$ we have to ensure that on the output side the line impedance $Z_o$ is matched for $a_2 = 0$ to be enforced. Figure 7.13 shows the block diagram for




(a) Block diagram for calculation of $S_{11}$ and $S_{21}$




(b) Block diagram for calculation of $S_{12}$ and $S_{22}$

**Figure 7.13** Block diagram for calculation of *S* parameters: (a) block diagram for calculation of $S_{11}$ and $S_{21}$; (b) block diagram for calculation of $S_{12}$ and $S_{22}$.

calculation of $S_{11}$ and $S_{21}$ (as shown in Figure 7.13(a)) and the block diagram for calculation of $S_{12}$ and $S_{22}$(as shown in Figure 7.13(b)) [15]. The definition equations and physical meaning of the $S$ parameters are summarized in Table 7.4 [16].

**Table 7.4** Definition of $S$ parameters.

| Parameters | Definition equation | Physical meaning |
|---|---|---|
| $S_{11}$ | $\left.\frac{b_1}{a_1}\right\|_{a_2=0} = \frac{2V_1}{V_S} - 1$ | Input reflection coefficient when output port is terminated in a matched load |
| $S_{21}$ | $\left.\frac{b_2}{a_1}\right\|_{a_2=0} = \frac{2V_2}{V_S}$ | Forward transmission coefficient when output port is terminated in a matched load |
| $S_{12}$ | $\left.\frac{b_1}{a_2}\right\|_{a_1=0} = \frac{2V_1}{V_S'}$ | Reverse transmission coefficient when input port is terminated in a matched load |
| $S_{22}$ | $\left.\frac{b_2}{a_2}\right\|_{a_1=0} = \frac{2V_2}{V_S'}$ | Output reflection coefficient when input port is terminated in a matched load |

## 7.3.2 Noise Figure of a Two-Port Network

The noise figure (or noise factor) is a figure of merit quantitatively specifying how noisy a component or system is. The most basic definition of the noise figure $F$ is the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output, as shown in Figure 7.14:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_i/N_i}{S_o/N_o} \tag{7.28}$$

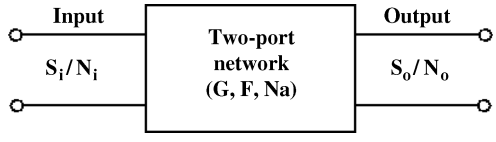



**Figure 7.14** Noise figure of a two-port network.

where $SNR_{in}$ and $SNR_{out}$ are the available signal-to-noise ratios at the input and output ports, respectively, $S_i$ and $N_i$ are the available signal and noise power at the input port, respectively, and $S_o$ and $N_o$ are the available signal and noise power at the output port, respectively.

Assuming the available signal and noise power of the two-port network are $G$ and $N_a$, the available noise power at the output port can be expressed as follows:

$$N_o = N_a + GN_i \tag{7.29}$$

With Equation (7.29) substituted in Equation (7.28), we have

$$F = \frac{S_i/N_i}{S_o/N_o} = \frac{N_o}{GN_i} = \frac{S_i/N_i}{GS_i/(N_a + GN_i)} = \frac{N_a + GN_i}{GN_i} \tag{7.30}$$

or

$$F = 1 + \frac{N_a}{kT_0BG} \tag{7.31}$$

### 7.3.3 Transimpedance Gain

The schematic of the optical receiver front-end circuit is shown in Figure 7.15, where $Y_S$ is the photodiode (PD) input admittance. Typically this will be that of the PIN/APD and is almost completely capacitive (that is $Y_S = \pi\omega C_{pd}$). $Y_L$ is the load admittance, which is generated mainly by input admittance of the next stage (typically the admittance should be 20 mS for an impedance of 50 Ω, that is $Y_L = Y_o = 20$ mS).

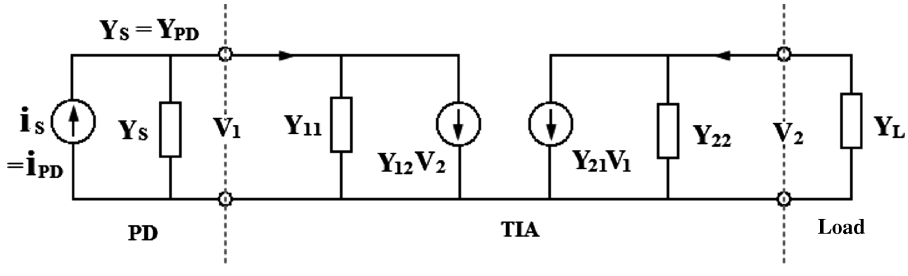



**Figure 7.15** Simplified model of the optical receiver front-end.

The transimpedance is defined as the magnitude of the ratio of output voltage $V_2$ at a load impedance and photocurrent through the photodiode $i_s$. Based on the small-signal circuit model analysis for an optical receiver front-end in Figure 7.15 and applying Kirchhoff's current law, the transimpedance gain of the optical receiver front-end can be expressed as

$$Z_T = \frac{V_2}{i_s} = -\frac{Y_{21}}{(Y_S + Y_{11})(Y_L + Y_{22}) - Y_{21}Y_{12}} \tag{7.32}$$

The relationship between the $S$ parameters and $Y$ parameters can be expressed as

$$Y_{11} = Y_o \frac{(1+S_{22})(1-S_{11})+S_{12}S_{21}}{(1+S_{22})(1+S_{11})-S_{12}S_{21}} \tag{7.33}$$

$$Y_{12} = Y_o \frac{-2S_{12}}{(1+S_{22})(1+S_{11})-S_{12}S_{21}} \tag{7.34}$$

$$Y_{21} = Y_o \frac{-2S_{21}}{(1+S_{22})(1+S_{11})-S_{12}S_{21}} \tag{7.35}$$

$$Y_{22} = Y_o \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{22})(1+S_{11})-S_{12}S_{21}} \tag{7.36}$$

where $Y_o (= 20\,\text{mS})$ is the characteristic admittance of the system.

Substituting Equations (7.33) through (7.36) into Equation (7.32), we have

$$Z_T = \frac{V_2}{i_s} = \frac{2S_{21}}{Y_o A + Y_L B + Y_S C + Y_S Y_L D/Y_o} \tag{7.37}$$

with

$$\begin{aligned} A &= (1-S_{11})(1-S_{22}) - S_{12}S_{21} \\ B &= (1-S_{11})(1+S_{22}) + S_{12}S_{21} \\ C &= (1+S_{11})(1-S_{22}) + S_{12}S_{21} \\ D &= (1+S_{22})(1+S_{11}) - S_{12}S_{21} \end{aligned}$$

If source impedance is infinite (that is $Y_S = 0$) and the output end of the TIA is connected to a matched load (that is $Y_L = Y_o = 20\,\text{mS}$), the corresponding transimpedence gain of the receiver front-end can be simplified as follows:

$$Z_T^T = \frac{S_{21}}{Y_o(1-S_{11})} \tag{7.38}$$

When the TIA is operated in a $50\,\Omega$ system (that is $Y_L = Y_S = Y_o = 20\,\text{mS}$), the transimpedence gain can be written as

$$Z_T^{50} = \frac{S_{21}}{2Y_o} \tag{7.39}$$

The transimpedance gain versus $Y_S$ and $Y_L$ are summarized in Table 7.5 [17], where it can be observed that the transimpedance 3 dB bandwidth can be determined from the

**Table 7.5** Transimpedance gain versus $Y_S$ and $Y_L$.

| Source and load impedances | Transimpedance gain | Physical meaning |
|---|---|---|
| Arbitrary $Y_S$ and $Y_L$ | $Z_T$ | Receiver front-end (PD + TIA) |
| $Y_L = Y_o, \quad Y_S = 0$ | $Z_T^T$ | TIA only |
| $Y_L = Y_S = Y_o$ | $Z_T^{50}$ | Power gain $S_{21}$ of TIA |

forward transmission coefficient $S_{21}$ only when the input and output ports are terminated in the matched loads. The physical meanings of the three transimpedance gains mentioned above are as follows: $Z_T$ is the transimpedance gain of the whole optical receiver front-end (PD + TIA), $Z_T^T$ is the transimpedance gain of the TIA, and $Z_T^{50}$ is proportional to the power gain $S_{21}$ of the TIA.

## 7.3.4 Equivalent Input Noise Current

### 7.3.4.1 Equivalent Input Noise Current Density of the TIA

Figure 7.16 shows the noise model of the noise figure measurement system for the optical preamplifier. It is noted that 50 Ω standard resistances have been used for the source and load impedances (that is $Z_S = Z_L = Z_o = 50\,\Omega$). $Z_i^T$ and $Z_o^T$ are the input and output impedances of the TIA, respectively, $\overline{v_{no}}$ is the total output noise voltage density, and $\overline{i_{in}^T}$ is the equivalent input noise current density of the TIA.

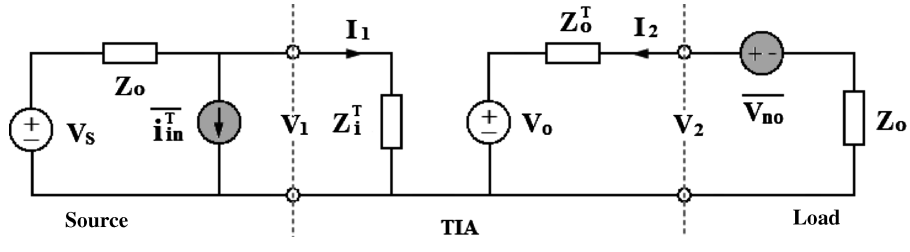



**Figure 7.16** Noise model of the 50 Ω noise figure measurement system for the optical preamplifier.

The noise figure of the TIA can be expressed as follows:

$$F_{50} = 1 + \frac{\overline{v_{no}^2}}{4kT\left|A_v^2\right|Z_o} \tag{7.40}$$

that is

$$\overline{v_{no}^2} = 4kT\left|A_v^2\right|Z_o(F_{50}-1) \tag{7.41}$$

where $A_v$ is the voltage gain and can be expressed as

$$A_v = \frac{V_2}{V_s} = \frac{S_{21}}{2} = \frac{Z_T^T}{Z_i^T + Z_o} \tag{7.42}$$

where $Z_T^T$ is the transimpedance gain of the TIA ($Z_T^T = V_2/I_1$). The corresponding equivalent input noise current density of the TIA $\overline{i_{in}^T}$ can be derived as follows:

$$\overline{i_{in}^T} = \frac{\overline{v_{no}}}{|Z_T^T|} = \frac{\sqrt{(F_{50}-1)4kT_0Z_o}}{|Z_o + Z_i^T|} \tag{7.43}$$

With $Z_i^T = Z_o(1 + S_{11})/(1 - S_{11})$ substituted in Equation (7.43), we have

$$\overline{i_{in}^T} = \frac{\overline{v_{no}}}{|Z_T^T|} = |1-S_{11}|\sqrt{\frac{(F_{50}-1)kT_0}{Z_o}} \tag{7.44}$$

### 7.3.4.2 Equivalent Input Noise Current Density of the Front-End

Figure 7.17 shows the noise model of a typical optical receiver front-end in a non-50 Ω system, where $\overline{i_{in}^R}$ is the total equivalent input noise current density and $\overline{v_{no}}$ is the total output noise voltage density of the receiver front-end. It is noted that the input port of the TIA is connected to the PD, not the matched load. Therefore the expression (7.44) is only valid for the TIA design, not the whole receiver front-end.

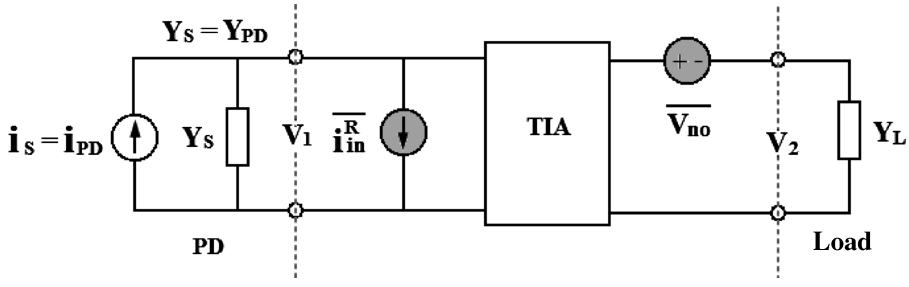



**Figure 7.17** Noise model of the optical receiver front-end.

Assuming that the total output noise voltage density $\overline{v_{no}}$ is composed mainly of the TIA (here the noise contribution of the PD is neglected), the equivalent input noise current density of the receiver front-end $\overline{i_{in}^R}$ can be expressed as follows:

$$\overline{i_{in}^R} = \frac{\overline{v_{no}}}{|Z_T|} = \frac{1}{2}|Y_oA + Y_LB + Y_SC + Y_SY_LD/Y_o|\sqrt{kT_oZ_o(F_{50}-1)} \tag{7.45}$$

Traditionally, the output end of the TIA is connected to a matched load (that is $Y_L = Y_o = 20\,\text{mS}$) and $\overline{i_{in}^R}$ can be rewritten as

$$\overline{i_{in}^R} = \frac{\overline{v_{no}}}{|Z_T|} = |1 - S_{11} + (1 + S_{11})Y_S/Y_o| \sqrt{\frac{kT_o(F_{50} - 1)}{Z_o}} \tag{7.46}$$

When the TIA is operated in a $50\,\Omega$ system (that is $Y_L = Y_S = Y_o = 20\,\text{mS}$), the equivalent input noise current density can be simplified to

$$\overline{i_{in}^{50}} = 2\sqrt{\frac{kT_o(F_{50} - 1)}{Z_o}} \tag{7.47}$$

It is noted that expression (7.47) is the conventional formula for predicting the equivalent input noise current density for the TIA IC, and the $\overline{i_{in}^{50}}$ is dependent on the noise figure only and independent of the $S$ parameters of the TIA. The equivalent input noise current density versus $Y_S$ and $Y_L$ are summarized in Table 7.6 [17].

**Table 7.6** Equivalent input noise current density versus $Y_S$ and $Y_L$.

| Source and load impedances | Input noise current density | Physical meaning |
|---|---|---|
| Arbitrary $Y_S$ and $Y_L$ | $\overline{i_{in}^R}$ | Receiver front-end (PD + TIA) |
| $Y_L = Y_o, Y_S = 0$ | $\overline{i_{in}^T}$ | TIA only |
| $Y_L = Y_S = Y_o$ | $\overline{i_{in}^{50}}$ | Only dependent on noise figure of TIA |

### 7.3.5 *Simulation and Measurement of Transimpedance Gain and Equivalent Input Noise Current*

In order to demonstrate the expressions derived in Sections 7.3.3 and 7.3.4 for the TIA, a HEMT-based TIA which operates at 10 Gb/s has been designed using a 0.2 μm PHEMT process [18]. Figure 7.18 shows a schematic of the developed TIA IC by using both enhancement- and depletion-mode (E–D) transistors. This IC consists of three parts: a parallel-feedback amplifier core, a source–follower buffer, and an output match stage. The source–follower buffer improves the flatness of the gain–frequency characteristics by separating the parallel-feedback loop from the large input capacitance of the output buffer (that is eliminates the Miller capacitance loading to the previous stages). The output stage is designed for a $50\,\Omega$ output impedance match. Figure 7.19 shows the experimental setup for $S$ parameters and noise figure measurement. All measurements were carried out on wafer using air-coplanar probes.

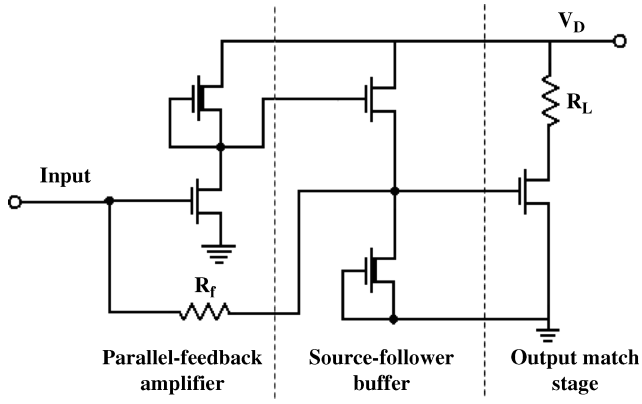



**Figure 7.18** Schematic of the 10 Gb/s HEMT-based TIA IC.

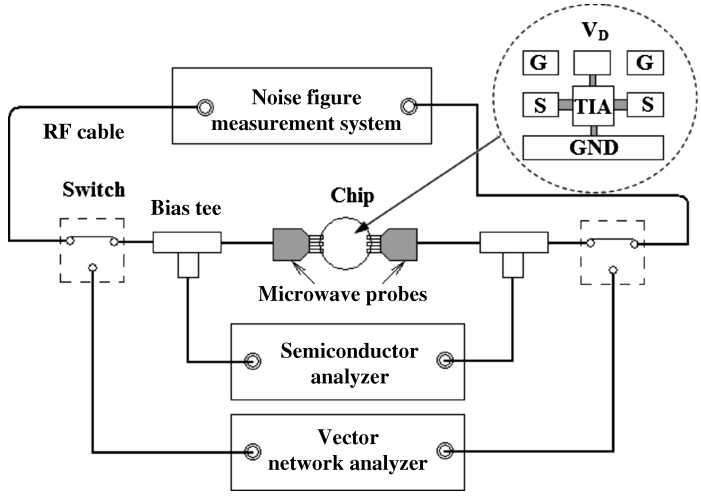
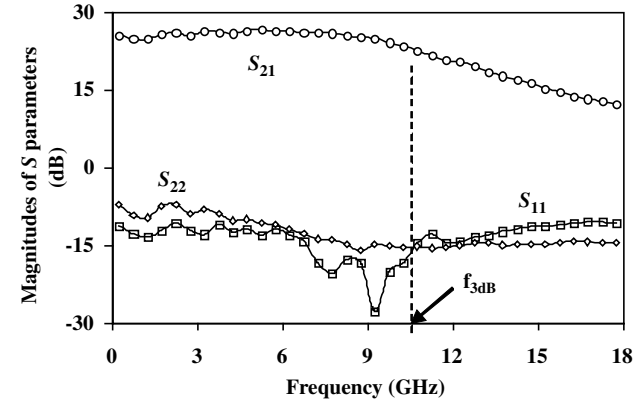


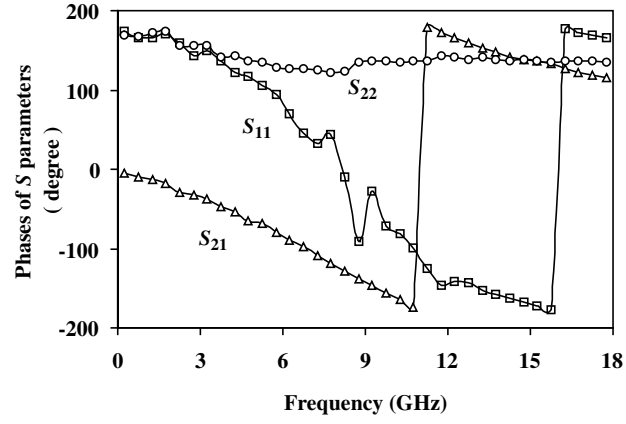

**Figure 7.19** Experimental setup for *S* parameters and noise figure measurement.

The wafer probes were calibrated using the line-reflect-match (LRM) calibration method for *S*-parameter measurement. The noise parameter measurement method here has been tested on wafer up to 26 GHz.

Figure 7.20 shows the measured magnitudes and phases of the *S* parameters of the TIA IC. A high gain $|S_{21}|$ of 25 dB and a broad 3 dB bandwidth over 10.8 GHz have been obtained. Good matching has also been achieved; $|S_{11}|$ is below $-10$ dB and $|S_{22}|$ is below $-7$ dB for the whole frequency range. The corresponding noise figure versus frequency is shown in Figure 7.21. The transimpedance gain (TG) and equivalent input noise current density (EINCD) can be obtained from AC and noise signal analysis by using commercial circuit design tools (such as SPICE), but it is difficult to measure




(a)




(b)

**Figure 7.20** *S* parameters of the 10 Gb/s HEMT-based TIA IC: (a) magnitudes; (b) phases.

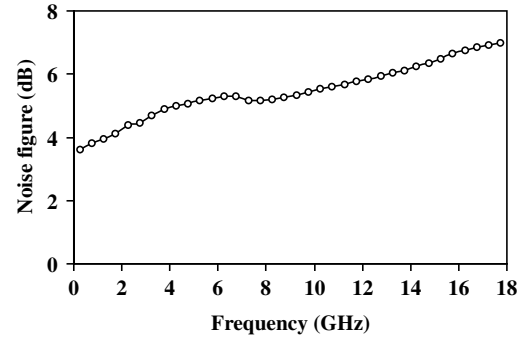



**Figure 7.21** Measured noise figure of the 10 Gb/s HEMT-based TIA IC.

directly using conversional microwave signal and noise measurement system. Alternatively, they can be calculated from *S* parameters and noise figure measurements by using the proposed transformation expressions.

Figure 7.22 shows the transimpedance gain that is derived from the measured *S* parameters of the 10 Gb/s TIA and the corresponding 3 dB bandwidth versus capacitance of the PD is shown in Figure 7.23. It can be found that a 3 dB bandwidth of TIA transimpedance gain is 11.5 GHz roughly, and the corresponding optical receiver front-end 3 dB bandwidth decreases with the increase of PD capacitance ($Y_S = j\omega C_{pd}$). As long as the capacitance of the PD is less than 0.6 pF (the 3 dB bandwidth is above 8 GHz), the proposed TIA can be operated at 10 Gb/s. Figure 7.24 shows the comparison of the predicted transimpedance gain for a 10 Gb/s TIA by using expressions (7.38) and (7.39). It is obvious that the gain and bandwidth predicted by Equation (7.38) is better than that of the TIA operating in a matching system. That means the transimpedance gain will be underestimated using the conventional formula.

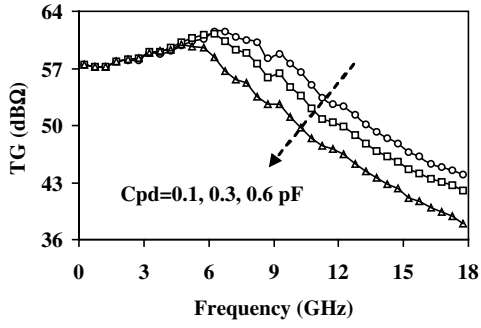



**Figure 7.22** Plot of transimpedance gain versus frequency for the 10 Gb/s TIA.

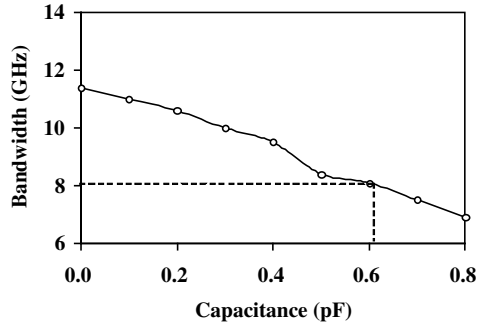



**Figure 7.23** The 3 dB bandwidth of transimpedance gain versus PD capacitance.

Figure 7.25 shows the equivalent input noise current density (EINCD) derived from the measured noise figure of the 10 Gb/s TIA and the corresponding average values

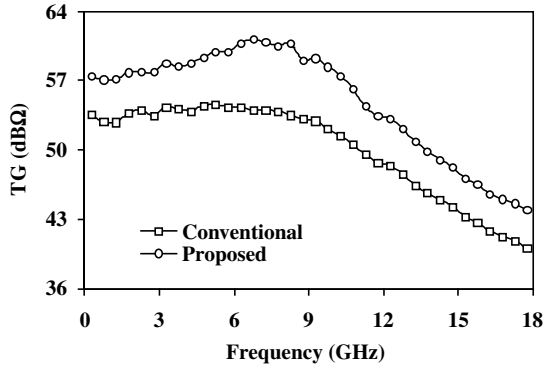



**Figure 7.24** Comparison of transimpedance gain for the 10 Gb/s TIA by using predicted data from Equations (7.38) and (7.39).

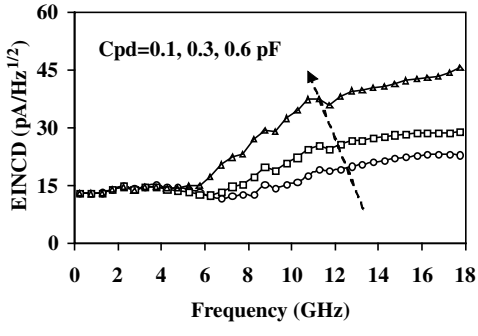



**Figure 7.25** Equivalent input noise current density (EINCD) versus frequency for the 10 Gb/s TIA.

versus PD capacitance is shown in Figure 7.26. It can be found that the equivalent input noise current density increases with the increase of PD capacitance ($Y_S = j\omega C_{pd}$). As long as the capacitance of the PD is less than 0.3 pF, the equivalent input noise current density of the TIA is below $20\,\text{pA}/\sqrt{\text{Hz}}$. Figure 7.27 shows the comparison of the

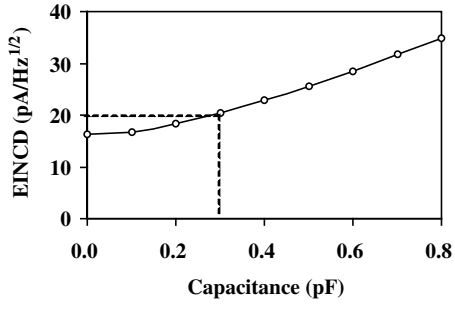



**Figure 7.26** Equivalent input noise current density (EINCD) versus PD capacitance.

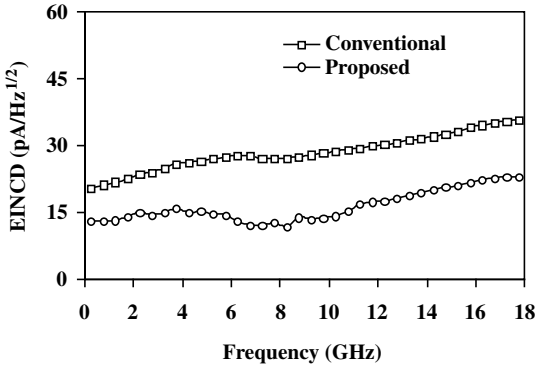



**Figure 7.27** Comparison of equivalent input noise current density (EINCD) for the 10 Gb/s TIA: predicted data from the proposed expression (7.44) and the conventional expression (7.47).

predicted equivalent input noise current density for the 10 Gb/s TIA. By using the proposed expressions (7.44) and the conventional formula (7.47), it is obvious that the equivalent input noise current density predicted by Equation (7.44) is better than that predicted by the conventional formula. This means that the equivalent input noise current density will be overestimated using the conventional formula.

## 7.4 Transimpedance Amplifier Circuit Design

In the receiver front-end of an optical fiber communication system, transimpedance amplifiers (TIAs) are widely used as the first active building block to convert the photodiode current to an amplified voltage for data recovery. Since the system specifications such as sensitivity, speed, and signal-to-noise ratio are strongly influenced by the TIA, tremendous design efforts are required in determining the circuit parameters for optimum performance. The high-speed TIAs can be fabricated by various semiconductor techniques, such as silicon, GaAs, and InP, and so on. The speed of a TIA based on a silicon BJT can be achieved up to 10 Gb/s. Based on GaAs MESFET, HEMT, and HBT devices, the TIA can be operated at 10–40 Gb/s. In order to achieve over 40 Gb/s, state-of-art InP HEMT and HBT should be used.

### *7.4.1 BJT-Based Circuit Design*

The basic elementary of a BJT-based TIA includes the common-emitter inverter stage and emitter followers mainly (as shown in Figure 7.28) [19, 20, 21, 22, 23, 24, 25]. The emitter followers are used for level shifting between the amplifier cells. Moreover, they are required for improving the mismatch between the amplifier stages (impedance transformation) and can be used for gain peaking at high frequencies.

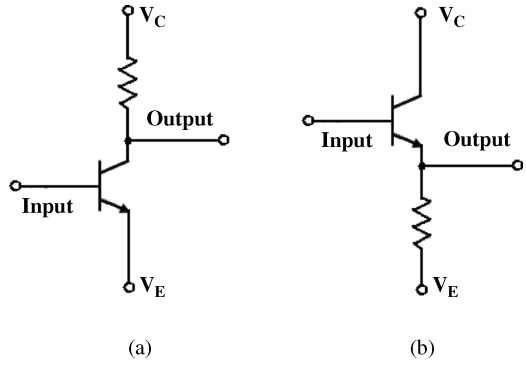



**Figure 7.28** Basic elements of a BJT-based TIA.

Traditionally, in BJT-based TIA circuit design, single-feedback and dual-feedback techniques are commonly used to improve bandwidth and noise performance. Figure 7.29 shows the single-feedback techniques in the BJT-based TIA, where the output signal can be fed back into the input port using either local stage feedback or feedback from succeeding buffer stage techniques.

Figure 7.30 shows the dual-feedback loop in a BJT-based TIA, where the gain stage design is based on a dual-feedback loop circuit having both current feedback $R_{F1}$ and voltage feedback $R_{F2}$ [22]. For the preamplifier, the input noise of the circuit is mainly due to thermal noise in the current feedback resistor $R_{F1}$. Increasing the resistance value of $R_{F1}$ is very effective for reducing input noise. However, a large resistance of $R_{F1}$ causes a bandwidth degradation. The dual-feedback configuration aids in producing a wide bandwidth amplifier with a large current feedback resistor $R_{F1}$ value. Table 7.7 summarizes the comparison of the performance of BJT-based TIAs.

### *7.4.2 HBT-Based Circuit Design*

Heterojunction transistors (HBTs) extend the advantages of a silicon bipolar transistor to significantly high frequencies. For high-speed applications requiring a high-current drive, high transconductance, high-voltage handing capability, low-noise oscillator, and uniform threshold voltage, HBTs have been a natural choice at frequencies from 1 to 100 GHz. Based on the substrate material, HBTs have three categories: GaAs HBT, InP HBT, and SiGe HBT. The SiGe base, adopting a Ge graded profile, reduces the base transit time due to the presence of a drift field. Therefore, the SiGe-base bipolar transistor provides a faster maximum cutoff frequency than a conventional Si-bipolar transistor. The commonly used HBT-based high-speed TIAs will be introduced in the following list [33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 45, 46, 47, 48, 49].

1. **Darlington feedback amplifier:** Darlington transistors contain two transistors connected in an emitter–follower configuration, while sharing the same collector

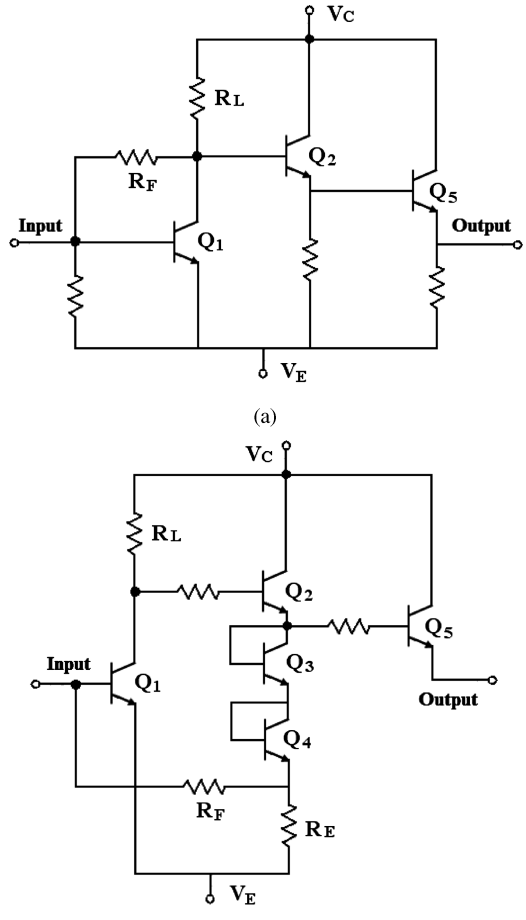



**Figure 7.29** Single feedback techniques in a BJT-based TIA: (a) feedback from the local stage; (b) feedback from the succeeding buffer stage.

contact. The key advantage of the Darlington configuration is that the total current gain of the circuit equals the product of the current gain of the two devices. The disadvantage is the larger saturation voltage.

Figure 7.31 shows the configuration of the Darlington feedback amplifier. This direct-coupled amplifier topology consists of two gain stages. The first stage is a common-emitter amplifier and the second stage is a feedback amplifier comprised of Darlington connected transistors, Q2 and Q3. The first stage acts as a low-noise common-emitter amplifier stage that determines the noise figure of the overall two-stage amplifier. The second-stage Darlington feedback amplifier provides wide-band gain and output drive capability. The feedback resistor $R_{f2}$ is used to control the noise figure as well as input return-loss performance.

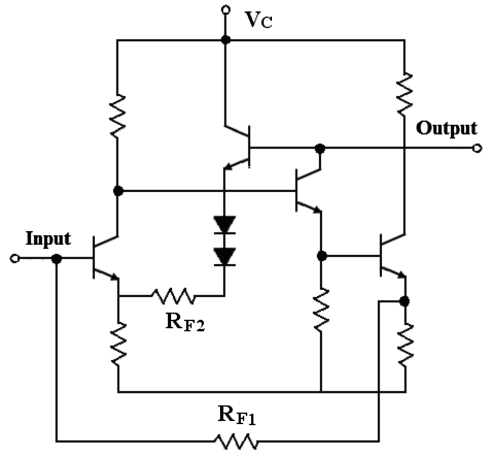



**Figure 7.30** Dual-feedback loop in a BJT-based TIA.

**Table 7.7** BJT-based TIA.

| $f_t$ (GHz) | Bandwidth (GHz) | TG (dB Ω) | EINCD (pA/$\sqrt{\text{Hz}}$) | Power (mW) | Ref. |
|---|---|---|---|---|---|
| 12 | 2.2 | 55 | 18 | — | [26] |
| 15 | 1.67 | 70 | 3.5 | 170 | [27] |
| 28 | 5.1 | 50 | 9.5 | — | [28] |
| 40 | 11.2 | 53 | — | — | [29] |
| — | 9 | 45 | — | 400 | [30] |
| 23 | 7.8 | 57 | 9 | 143 | [31] |
| 23 | 9 | 57 | 10 | 215 | [31] |
| 35 | 10.5 | 60 | 12 | 450 | [32] |

2. **Differential feedback amplifier:** Figure 7.32 shows the configuration of the differential feedback amplifier. The differential operation mode reduces noise problems, typical in amplifiers with high gain and operating speed. The amplifier consists of a differential TIA stage, followed by two emitter followers (2EF), a transadmittance stage (TAS), and a transimpedance stage (TIS) to give high bandwidth through the impedance mismatch. The negative-feedback resistor is only used in the first stage to extend the bandwidth and improve the dynamic range.
3. **Cascode feedback amplifier:** The cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer. Compared to a single amplifier stage, this combination may have one or more of the following advantages: higher input–output isolation, higher input impedance, higher output impedance, higher gain, or higher bandwidth.

   In the case of transistors, the gain device can be operated in common-emitter or common-collector modes, which utilize a second transistor in the common base

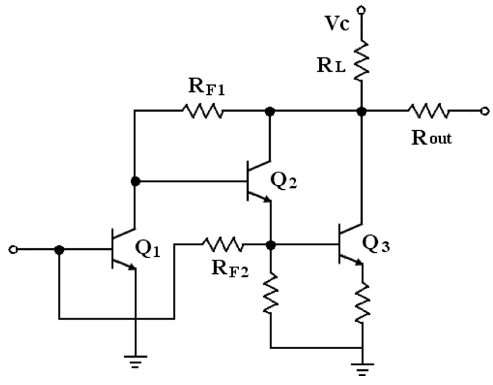



**Figure 7.31** Configuration of the Darlington feedback preamplifier.

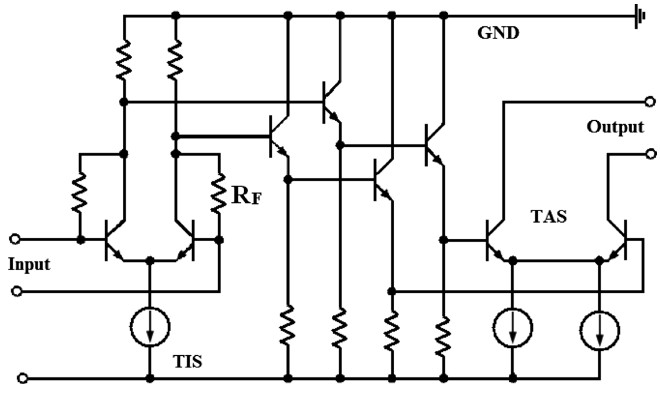



**Figure 7.32** Configuration of the differential feedback amplifier.

mode whose emitter is connected to the collector of the gain transistor. The cascode improves input–output isolation as there is no direct coupling from the output to input. This eliminates the Miller effect and thus contributes to a higher bandwidth.

Figure 7.33 shows the configuration of the cascode feedback amplifier. In order to reduce the capacitance and high shot noise current at the input due to the large DC base current of the transistor, the small emitter-area HBTs for the input cascoded-pair stage should be used, followed by a two-step emitter-follower involving one small and one large emitter-area HBT.

Tables 7.8 to 7.10 summarize the performance of GaAs-, InP-, and SiGe-based HBT TIAs. It is obvious that the transmission bit rate can be greatly improved compared with a BJT-based TIA.

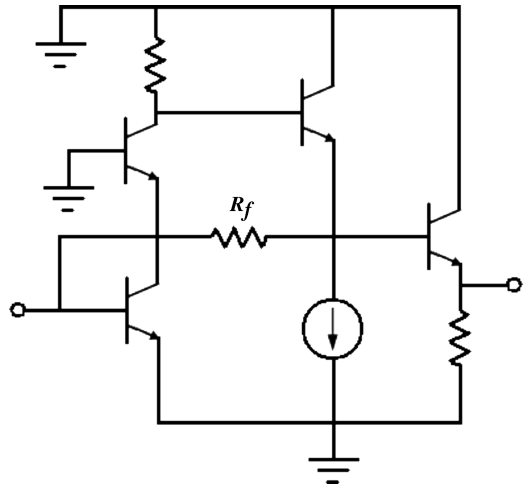



**Figure 7.33** Configuration of the cascode feedback amplifier.

**Table 7.8** GaAs HBT-based TIA.

| $f_t$ (GHz) | Bandwidth (GHz) | TG (dB Ω) | EINCD (pA/$\sqrt{\text{Hz}}$) | Power (mW) | Ref. |
|---|---|---|---|---|---|
| 24 | 9.1 | 53 | <12 | 53 | [33] |
| 41 | 12.7 | 50 | — | — | [34] |
| 70 | 27 | 53 | — | 102 | [35] |
| 70 | 40 | 50 | — | 280 | [35] |

**Table 7.9** InP HBT-based TIA.

| $f_t$ (GHz) | Bandwidth (GHz) | TG (dB Ω) | EINCD (pA/$\sqrt{\text{Hz}}$) | Power (mW) | Ref. |
|---|---|---|---|---|---|
| 54 | 10 | 40 | — | 84 | [39] |
| 67 | 14 | 45 | 10 | 34.3 | [40] |
| 80 | 32 | 32 | — | — | [41] |
| 125 | 40 | 45 | — | 130 | [42] |
| 160 | 47 | 56 | 35 | 457 | [43] |
| 120 | 26.7 | 48.9 | 25 | 26.5 | [44] |

**Table 7.10** SiGe HBT-based TIA.

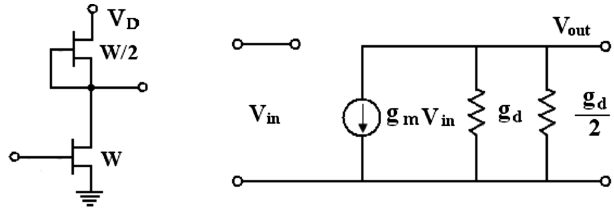
| $f_t$ (GHz) | Bandwidth (GHz) | TG (dB Ω) | EINCD (pA/$\sqrt{\text{Hz}}$) | Power (mW) | Ref. |
|---|---|---|---|---|---|
| 60 | 19 | 38 | — | 95 | [45] |
| 52 | 9 | 45 | | 77 | [46] |
| 18 | 5.5 | 43 | 20 | — | [47] |
| 200 | 50 | 49 | 30 | 200 | [48] |

### 7.4.3 FET-Based Circuit Design

Compared with HBT devices, the FET devices (including MESFET and HEMT) have the lowest noise performance; therefore, they are more suitable for optical preamplifier design. A common-source FET is chosen as the basic amplifying element since it provides voltage and current gain along with reverse isolation, a combination not available from common-gate or common-drain configurations. An active-load FET is used rather than a resistor load because it results in better large-signal performance for a given small-signal gain. With the active load it is possible to choose a quiescent operating point nearly half of the saturation current of the common-source FET. The circuit, which consists of a common-source FET and an active-load FET, is called an inverter, as a basic elementary cell for high-speed optical preamplifier design [58].

Figure 7.34 shows the inverter circuit and corresponding equivalent circuit model at low-frequency ranges. The gain of the inverter circuit can be calculated as follows:

$$A_V = \frac{g_m}{g_d + g_d/2} = \frac{2}{3}\frac{g_m}{g_d} \tag{7.48}$$




(a) Inverter circuit (b) Equivalent circuit model at low-frequency ranges

**Figure 7.34** (a) Inverter circuit and (b) equivalent circuit model at low-frequency ranges.

where $g_m$ and $g_d$ are the transconductance and output conductance of the common-source FET, respectively. The gain is independent of the inverter FET gate width, so long as the active-load FET remains half the width of the inverter FET, as assumed for this calculation. The inverter circuit of Figure 7.34(a) could be cascaded, with AC coupling, to produce a multistage amplifier with higher gain. However, the bandwidth would be reduced substantially due to the heavy capacitive loading of the succeeding stage's gate capacitance. Therefore, a buffer circuit is necessary to insert between the inverter circuits. The combination of an inverter and a buffer circuit will be referred to as a single amplifier stage, although they could, as well, be treated as two stages: common source followed by common drain.

The configurations of commonly used FET-based high-speed TIAs are shown in Figure 7.35. The resistive feedback, active feedback, and cascade are three popular

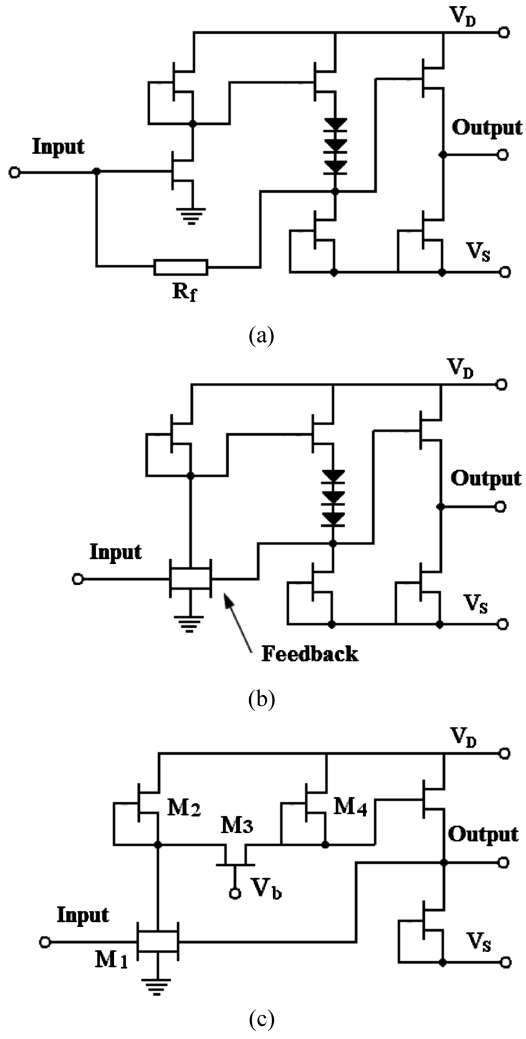



**Figure 7.35** Configurations of the commonly used FET-based TIAs: (a) passive feedback; (b) active feedback; and (c) cascade with active feedback.

choices for FET-based TIAs. Tables 7.11 and 7.12 summarize the performance of MESFET- and HEMT-based TIAs.

For the cascode configuration, it consists of a common-source stage $M_1/M_2$ (inverting), followed by a common-gate stage M3/M4 (noninverting). The total gain of an FET cascode circuit is approximately as follows [59]:

$$A_{cascode} = -\frac{g_{m1}}{g_{d4}} \frac{1}{1 + (1 + g_{d3}/g_{d4})(g_{d1} + g_{d2})/g_{m3}} \tag{7.49}$$

**Table 7.11** GaAs MESFET-based TIA.

| $f_t$ (GHz) | Bandwidth (GHz) | TG (dB Ω) | EINCD (pA/$\sqrt{\text{Hz}}$) | Power (mW) | Reference |
|---|---|---|---|---|---|
| -/0.3 | 8.6 | 55 | 20.9 | 95 | [49] |
| 40/- | 13 | 54 | 15 | — | [50] |
| -/- | 3.5 | 59 | 12 | 800 | [51] |
| 13/1.0 | 7.6 | 67 | — | — | [52] |
| -/0.5 | 12 | 44 | 12.6 | — | [53] |

**Table 7.12** GaAs/InP HEMT-based TIA.

| $f_t$ (GHz) | Bandwidth (GHz) | TG (dB Ω) | EINCD (pA/$\sqrt{\text{Hz}}$) | Power (mW) | Reference |
|---|---|---|---|---|---|
| 35 | 10 | 55 | 13.5 | — | [54] |
| 85 | 8.0 | 63.3 | 6.5 | 465 | [55] |
| 60 | 18 | 41.8 | 20 | — | [56] |
| 170 | 43 | 48.2 | 20 | 350 | [57] |

where $g_{m1}$ and $g_{m3}$ are the transconductances of FET M1 and M3, respectively; $g_{di}(i = 1,...,4)$ is the output conductance of FET $M_j$ $(j = 1,...,4)$.

### 7.4.4 MOSFET-Based Circuit Design

Due to the inherently high-speed and low-noise characteristics, III–V compound semiconductor devices have been dominantly utilized to realize such amplifiers. With the continuous scaling of transistor feature size, fully integrated TIA designs using submicrometer CMOS technologies have attracted great attention due to the low implementation cost and high integration level. Figure 7.36 shows the cutoff frequency

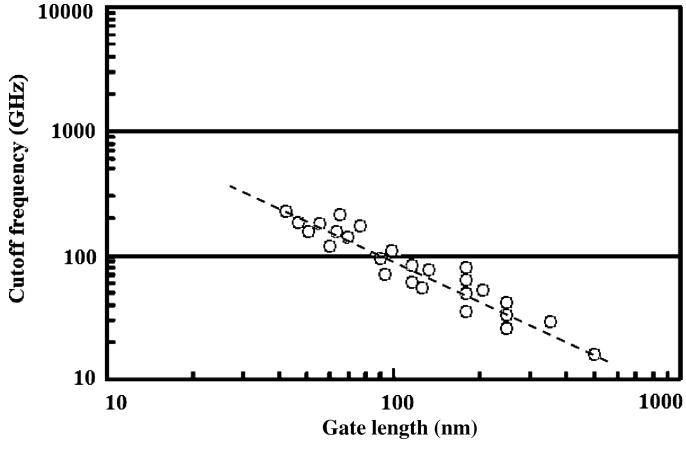



**Figure 7.36** Cutoff frequency versus gate length for MOSFET.

versus gate length for a MOSFET. It can be seen that as the CMOS technology is downscaled to gate lengths of 90 nm and less, current state-of-the art 70–45 nm CMOS devices have achieved performances similar to III–V devices or Si-Ge bipolar transistors, but at a lower cost [60, 61]. The peak transit frequency of an NMOS transistor is pushed to over 100 GHz. Therefore, the design of circuits in CMOS technology operating over 10 GHz should be straightforward.

Figure 7.37 shows the schematic of a conventional single-stage resistive shunt feedback TIA in the common-source configuration, and Table 7.13 summarizes the performance of MOSFET-based TIAs.

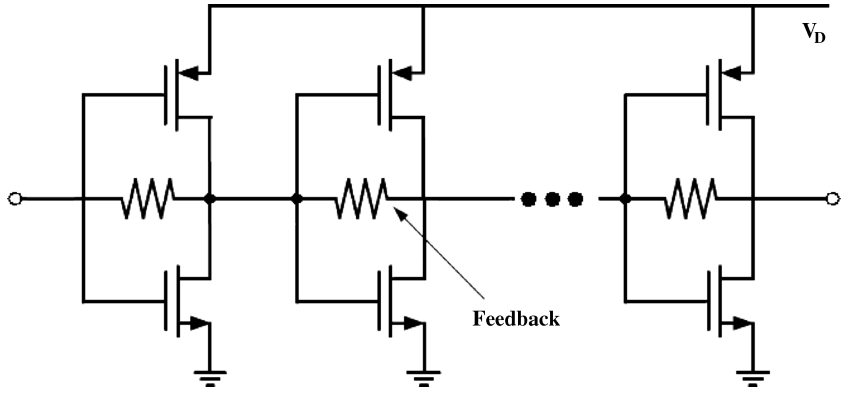



**Figure 7.37** Schematic of a conventional resistive shunt feedback TIA in the common-source configuration.

**Table 7.13** MOSFET-based TIA.

| Process (μm) | Bandwidth (GHz) | TG (dB Ω) | EINCD ($pA/\sqrt{Hz}$) | Power (mW) | Ref. |
|---|---|---|---|---|---|
| 0.08 | 19 | 45 | — | 6.5 | [62] |
| 0.08 | 20 | 52 | 50 | 2.2 | [63] |
| 0.18 | 6 | 53 | — | 88 | [64] |
| 0.18 | 7.2 | 61 | 8.2 | 70 | [65] |
| 0.18 | 7.6 | 52 | — | 34 | [66] |
| 0.18 | 7.9 | 90 | — | 199 | [67] |
| 0.18 | 8 | 53 | 18 | 25 | [67] |
| 0.18 | 9.2 | 54 | — | 55 | [68] |
| 0.25 | 9 | 55 | 9.5 | 140 | [69] |

### *7.4.5 Distributed Circuit Design*

In future optical transmission systems, data rates of more than 40 Gb/s are expected. Millimeter-wave wireless technology will be used in such future applications as

multimedia mobile access communication (MMAC) and intelligent transport systems (ITSs). A wide-bandwidth baseband amplifier is a key component for developing such systems. Baseband amplifiers are used as preamplifiers in optical receivers and as data signal amplifiers in optical communication systems. Distributed circuit-design amplifiers have been used in approaches to obtain bandwidths extending into the millimeter-wave frequency range [70, 71, 72, 73, 74, 75, 76, 77].

The schematic circuit of a conventional distributed amplifier is depicted in Figure 7.38. It has artificial input and output lines that are constructed with a series of transmission lines and the parasitic capacitances of the transistors. These lines have very high cutoff frequencies and cancel out the effects of parasitic capacitances. Thus, these amplifiers inherently have wideband characteristics.

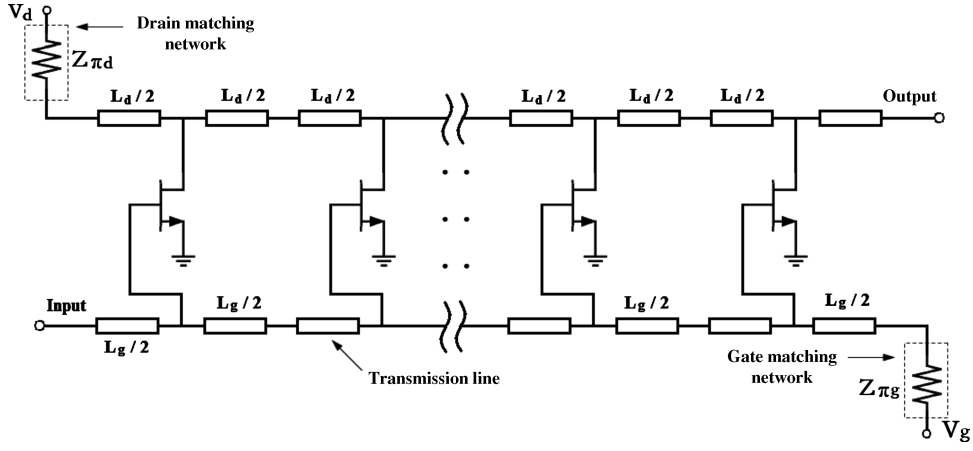



**Figure 7.38** Schematic circuit of a conventional distributed amplifier.

The gate extrinsic inductors $L_g$ and gate–source capacitance $C_{gs}$ of the gain cells (FET device) form an input artificial transmission line. The input line has impedance given by

$$Z_{\pi g} = \sqrt{L_g / C_{gs}} \tag{7.50}$$

The drain extrinsic inductors $L_d$ and drain–source capacitance $C_{ds}$ of the gain cells (FET device) form an input artificial transmission line. The output line has impedance given by

$$Z_{\pi d} = \sqrt{L_d / C_{ds}} \tag{7.51}$$

The gate and drain lines are matched with the terminating resistors, equal to $Z_{\pi g}$ and $Z_{\pi d}$, so that input and output impedances of the preamplifier remain constant over a

large frequency bandwidth. The magnitude of the transimpedance in the passband is given by

$$|Z_{Tf}| = \frac{n}{2} g_m Z_{\pi g} Z_{\pi d} \tag{7.52}$$

where $g_m$ is the transconductance of the FET and $n$ is the number of FETs in the distributed preamplifier structure.

Bandwidth is a high priority in transimpedance amplifiers. Unlike conventional microwave amplifiers, these amplifiers have to maintain an acceptable response down to very low frequencies and still perform satisfactorily at high frequencies. The low-frequency response must extend as close as possible to zero Hz. However, with conventional design techniques, gain and noise performance are low at relatively low frequencies. This makes it very difficult to produce a baseband amplifier for optical transmission systems. By using frequency-dependent drain termination and active gate termination, a 0 Hz-to-millimeter-wave bandwidth with a low noise figure is achieved (as shown in Figures 7.39 and 7.40). Table 7.14 summarizes the performance of the distributed circuit design amplifiers.

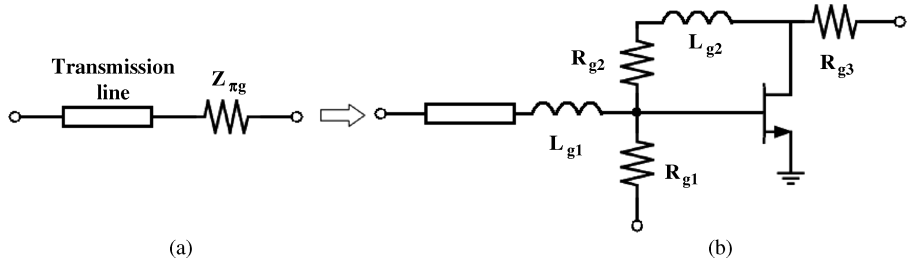



**Figure 7.39** Schematic gate termination circuits of distributed amplifiers: (a) resistor termination; (b) active termination.

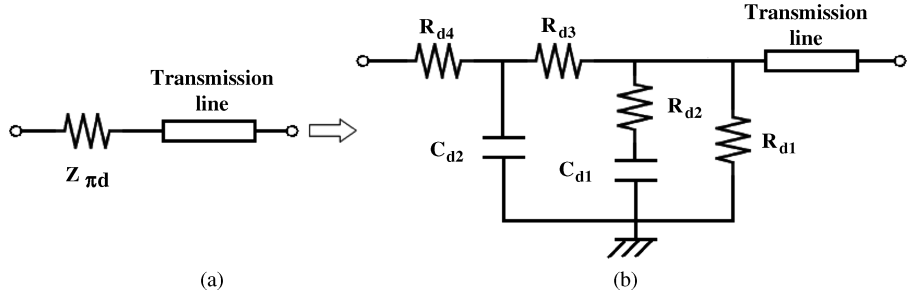



**Figure 7.40** Schematic drain termination circuits of distributed amplifiers: (a) conventional resistor termination; (b) frequency-dependent termination.

**Table 7.14** Distributed TIA.

| $f_t$ (GHz) | Bandwidth (GHz) | TG (dB Ω) | EINCD (pA/$\sqrt{\text{Hz}}$) | Power (mW) | Ref. |
|---|---|---|---|---|---|
| 43 (MESFET) | 0.5–30 | 41 | 30 | — | [70] |
| 20 (MESFET) | 0.5–8 | 45 | 8 | — | [71] |
| 40 (MESFET) | DC–36 | 41 | 20 | 1000 | [72] |
| 80 (HBT) | 0.055–55 | 38 | — | 82 | [73] |
| 147 (HBT) | 0.05–50 | 53 | — | 240 | [74] |
| 167 (HEMT) | 0.1–49 | 52 | — | 520 | [75] |

## 7.5 Passive Peaking Techniques

The bandwidth of a high-speed optical receiver front-end is normally determined by the cutoff frequency of the semiconductor device. In order to overcome the limitations of semiconductor technology (such as CMOS, FET, and HBT), the passive peaking techniques can be used to extend circuit bandwidth significantly without the penalty of power consumption. Meanwhile, it can have a relatively flat frequency response similar to LC-ladder filters.

### *7.5.1 Inductive Peaking Techniques*

Although inductors are commonly associated with narrowband circuits, they are useful in broadband circuits as well. There are many different methods of broadband amplifier design; one of the most extensively used is inductive peaking. This method involves placing inductors in strategic locations so that they resonate with parasitic capacitances and, consequently, broaden the bandwidth. Inductive peaking offers an advantage over conventional microwave design techniques in that it allows for an increase in bandwidth without sacrificing low-frequency gain [78, 79, 80, 81, 82, 83].

There are five types of inductive peaking techniques that are commonly used as follows:

a. Gate inductive peaking technique out of the feedback loop
b. Gate inductive peaking technique in the feedback loop
c. Drain inductive peaking technique out of the feedback loop
d. Drain inductive peaking technique in the feedback loop
e. Feedback inductive peaking technique.

Figure 7.41 shows the reduced circuit configurations of preamplifier with various inductive peaking techniques. Conventionally, the planar inductors are fabricated by forming a dielectric on a semiconductor substrate such as Si and GaAs, on printed circuit boards, and on hybrid integrated circuit substrates, and then depositing metal in a spiral geometry directly on the dielectric. To improve the performance of spiral

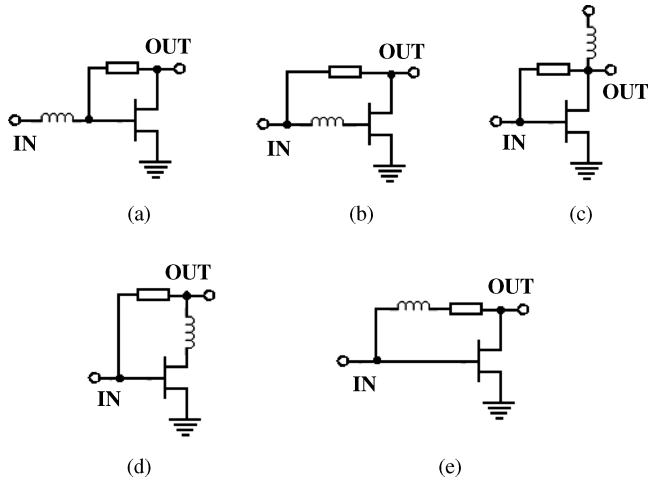



**Figure 7.41** Circuit configurations of a preamplifier with inductive peaking techniques.

inductors, airbridges, rather than a dielectric, can be used to separate the metal from the substrate. The nonidealities of on-chip inductors present several challenges for implementing monolithic gigahertz circuitry. In shunt-peaking applications, the biggest issue is the reduction in bandwidth improvement because of the additional parasitic capacitance introduced by the on-chip inductor. Figure 7.42 shows the configuration of a square spiral inductor with the corresponding equivalent circuit model.

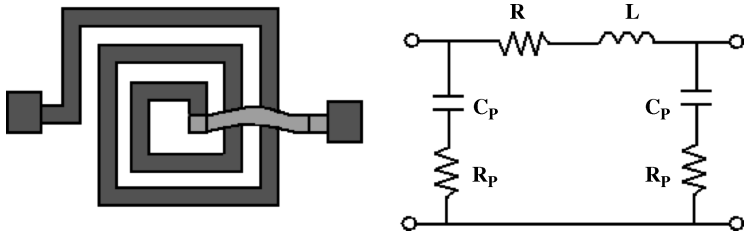



**Figure 7.42** Configuration of a square spiral inductor with an equivalent circuit model.

Figures 7.43 to 7.45 show the effects of gate (a and b), drain (c and d), and feedback inductor peaking on the 3 dB bandwidth, gain peaking, and equivalent input noise current density (EINCD). It can be seen that gate inductor peaking is especially useful for high bandwidths and EINCD, whereas drain inductor peaking is good for high bandwidths. Figures 7.46 and 7.47 show the typical FET-based TIA and MOSFET-based TIA designs using gate and drain peaking inductors. It is well known from circuit theory that excessive gain peaking can lead to system instability; therefore, the peaking inductor value is limited by the stability factor of the amplifier.

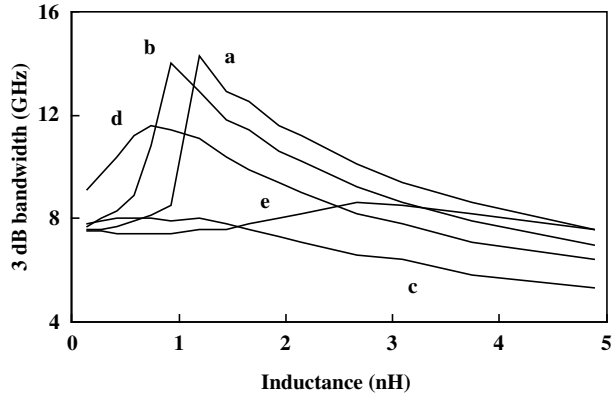



**Figure 7.43** 3 dB bandwidth of a TIA versus a peaking inductor.

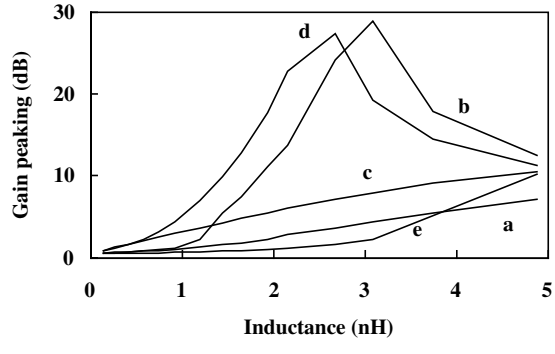



**Figure 7.44** Gain peaking of a TIA versus a peaking inductor.

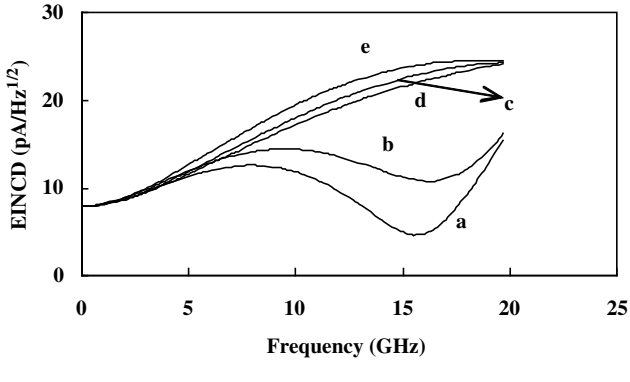



**Figure 7.45** EINCD of a TIA versus peaking inductor.

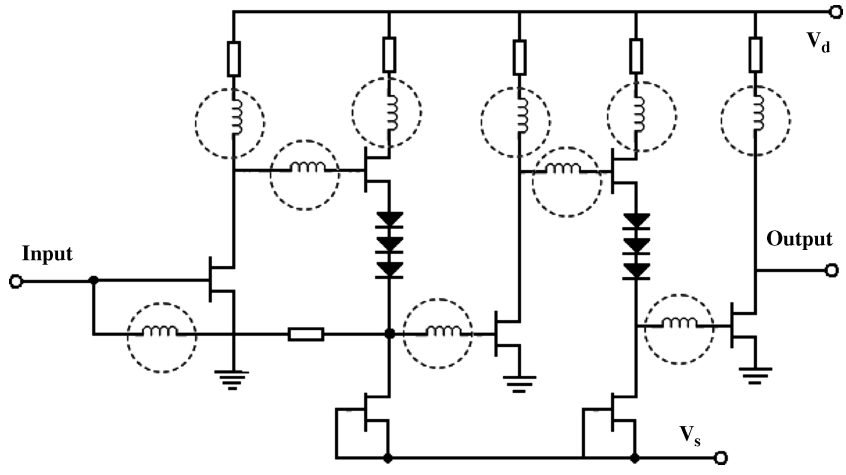



**Figure 7.46** Typical FET-based TIA design with gate and drain peaking inductors.

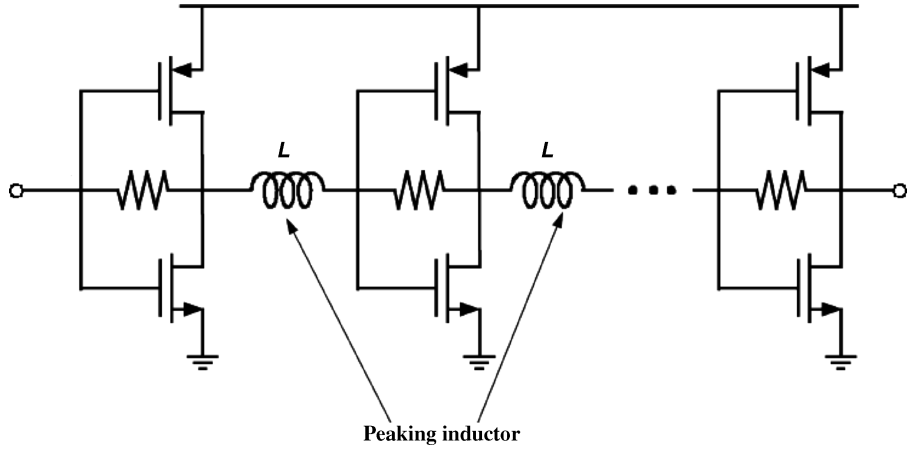



**Figure 7.47** Typical MOSFET-based TIA design with gate peaking inductors.

## *7.5.2 Capacitive Peaking Techniques*

As previous mentioned, the bandwidth and noise performance can be improved using inductive peaking techniques. This method usually places inductors in a strategic location of the amplifier circuit, resulting in a resonance with parasitic capacitances, which broadens the bandwidth of the amplifier. However, there are several issues that need to be overcome:

1. The stray capacitances of the inductor often cause a bandwidth degradation rather than an improvement. To overcome this problem, the size of the inductor must be as small as possible to reduce the stray capacitance effect.

2. It is difficult to fabricate the on-chip inductors with a high-quality factor on the silicon-based substrate, resulting in worse noise.
3. The area of the chip increases with the increase in the number of on-chip inductors, resulting in a larger die area and high cost.

Instead of inductive peaking, capacitive peaking can be used to increase the bandwidth of a TIA. Because the size of a capacitor is relatively smaller than an inductor, the parasitic effect can also be reduced. Figure 7.48 shows the typical FET-based TIA design with peaking capacitors, and the corresponding frequency response is shown in Figure 7.49 [84]. To deliver proper DC bias to the next stage, three-level shift diodes are inserted in the source follower. Diodes are attained by connecting the source and the drain of an FET produced using the conventional GaAs process. Resistance components of the diodes degrade the frequency performance of the SF. To overcome this problem, a capacitor is inserted in parallel with the diodes so that AC signals

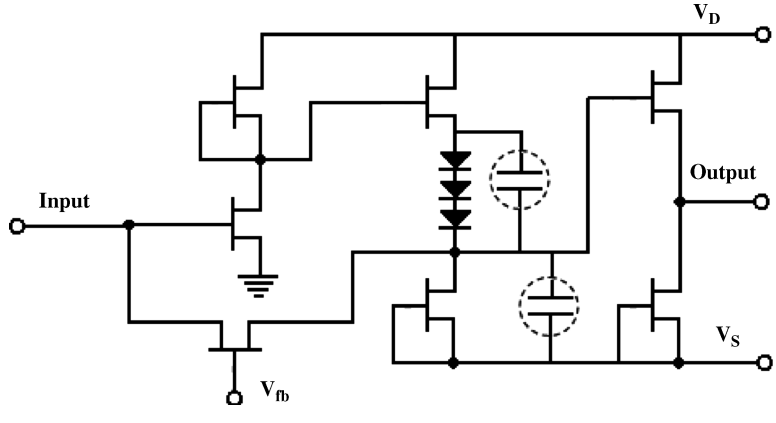



**Figure 7.48** Typical FET-based TIA design with peaking capacitors.

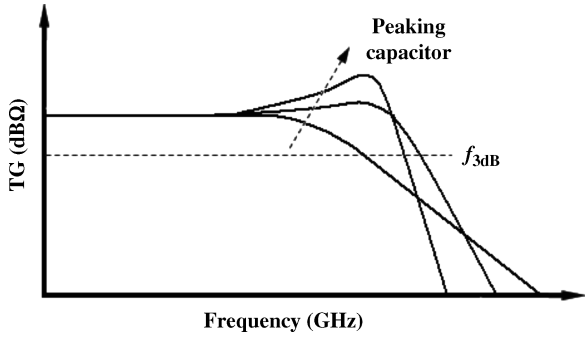



**Figure 7.49** Frequency response of TIA with peaking capacitor.

bypass the diodes. This arrangement permits an increase in high-frequency gain and expansion of the bandwidth.

## 7.6 Matching Techniques

Optical receivers for direct detection are required to operate at over several decades of frequency span with flat gain. However, conventional microwave design techniques are not generally applicable for operation from nearly DC to gigahertz frequencies. For this reason, wideband receiver front-ends are generally based on a mismatched TIA amplifier and PD configuration. Therefore, it is difficult to achieve the optimum noise and gain design for an ultra-wideband front-end using conventional microwave low-noise amplifier design rules. However, by inserting a matching network between the TIA amplifier and PD, the equivalent input noise current density can be minimized for a certain frequency range (passband). This kind of optical front-end is called a tuned front-end. The use of front-end tuning in optical receivers can provide a significant improvement in the noise performance of certain optical communication links. Schemes such as subcarrier multiplexing (SCM) particularly benefit as the information to be transmitted is frequency translated before optical modulation. The basic concept behind SCM is borrowed from microwave technology, which employs multiple microwave carriers for transmission of multiple channels over optical fiber. With such a modulation scheme the optical receiver only has to operate over a restricted bandwidth and as such allows tuned front-end techniques to be employed. A tuned front-end receiver not only provides the required passband response but minimizes the noise contribution of the receiver [85, 86].

The noise behavior of a linear noisy two-port network (TIA) can be characterized by the four noise parameters, $F_{\min}$, $R_n$, $G_{opt}$, and $B_{opt}$, as follows:

$$F = F_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right] \tag{7.53}$$

or

$$F = F_{\min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 \tag{7.54}$$

where $F$ is the noise figure, $Y_s = G_s + jB_s$ is the source admittance, $F_{\min}$ is the minimum noise figure, $R_n$ is the noise resistance, and $Y_{opt} = G_{opt} + jB_{opt}$ is the optimum source admittance. It is obvious that in order to obtain the optimum noise figure, it is necessary to match the source admittance of the TIA (looking into the output of the matching network) to the impedance of the optimum source admittance.

Figure 7.50 shows the configuration of a tuned optical front-end and Figure 7.51 shows the noise-equivalent circuit model of an FET-based tuned front-end. The two

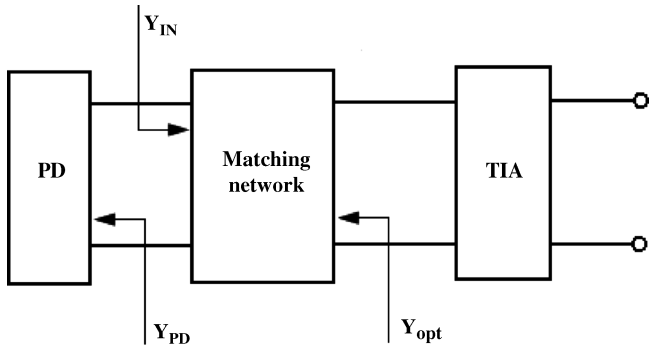



**Figure 7.50** Configuration of a tuned optical front-end.

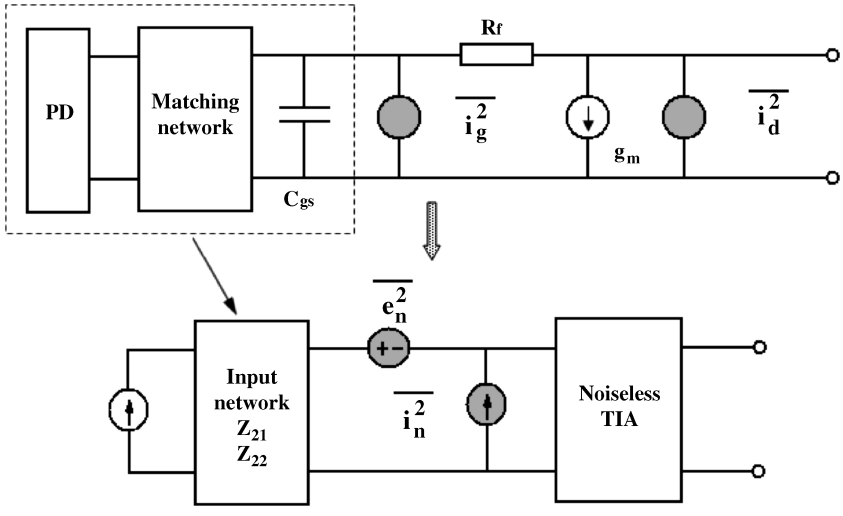



**Figure 7.51** Noise-equivalent circuit model of an FET-based tuned front-end.

current noise sources $\overline{i_g^2}$ and $\overline{i_g^2}$ represent the internal noises of the FET device; these noise sources are correlated. It is noted that two input noise voltages $\overline{e_n^2}$ and currents $\overline{i_n^2}$ are used to represent the noise property of the noisy two-port TIA.

The corresponding admittance noise correlation matrix of the FET can be expressed as

$$C_Y = 4kT \begin{bmatrix} (\omega C_{gs})^2 R/g_m & \mathrm{j}\omega C_{gs} C\sqrt{PR} \\ -\mathrm{j}\omega C_{gs} C\sqrt{PR} & g_m P \end{bmatrix} \tag{7.55}$$

where $g_m$ is the transconductance, $C_{gs}$ is the gate-to-source capacitance, $R$ and $P$ are the gate and drain noise model parameters, and $C$ is the correlation coefficient.

The input noise voltage $\overline{e_n^2}$ and current $\overline{i_n^2}$ can be determined by using noise matrix techniques:

$$\overline{e_n^2} = \frac{C_{Y22}}{|Y_{21}|^2} \tag{7.56}$$

$$\overline{e_n i_n^*} = -\frac{C_{Y21}}{Y_{21}} + C_{Y22}\frac{Y_{11}^*}{|Y_{21}|^2} \tag{7.57}$$

$$\overline{e_n^* i_n} = -\frac{C_{Y21}}{Y_{21}} + C_{Y22}\frac{Y_{11}^*}{|Y_{21}|^2} \tag{7.58}$$

$$\overline{i_n^2} = C_{Y11} - C_{Y21}\frac{Y_{11}}{Y_{21}} - C_{Y12}\frac{Y_{11}^*}{Y_{21}^*} + C_{Y22}\left|\frac{Y_{11}}{Y_{21}}\right|^2 \tag{7.59}$$

The equivalent input noise current density of the PD and TIA (without a tuned network) can be expressed in terms of the input noise voltage $\overline{e_n^2}$ and current $\overline{i_n^2}$:

$$\begin{aligned} \left\langle i_{in}^2 \right\rangle &= [e_n Y_{in}(\omega) + i_n]\,[e_n Y_{in}(\omega) + i_n]^* \\ &= \overline{e_n^2}|Y_{in}(\omega)|^2 + \overline{e_n i_n^*} Y_{in}(\omega) + \overline{e_n^* i_n} Y_{in}^*(\omega) + \overline{i_n^2} \end{aligned} \tag{7.60}$$

where $Y_{in}(\omega)$ is the input admittance of the TIA.

The equivalent input noise current density of the complete tuned front-end is given by

$$\left\langle i_{in}^2 \right\rangle = \frac{4KT}{g_m}\frac{\Gamma(Z_{22})}{|Z_{21}|^2} \tag{7.61}$$

where $k$ is the Boltzmann constant, $T$ is the absolute temperature (normally 290 K), $Z_{21}$ and $Z_{22}$ are the $Z$ parameters of the input network (as shown in Figure 7.51), and $\Gamma(Z_{22})$ is the noise factor of the front-end, given by

$$\Gamma(Z_{22}) = P + \left((\omega C_{gs})^2 R + \frac{g_m}{R_f}\right)|Z_{22}|^2 - 2C\sqrt{PR}(\omega C_{gs}\mathrm{Im}[Z_{22}]) + \frac{2(1+P)}{R_f}\mathrm{Re}[Z_{22}]$$

For the untuned case, it is obvious that the noise factor $\Gamma(Z_{22})$ is constant and that the correlation term is additive so that $\Gamma(Z_{22})$ is increased. For the tuned case, $\Gamma(Z_{22})$ in general becomes frequency dependent. In order to minimize the equivalent input noise

current density of the complete tuned front-end, two conditions should be satisfied for the $Z$ parameter of the input network:

1. The real part of $Z_{22}$ is zero, that is $\mathrm{Re}[Z_{22}] = 0$. The tuned network should be a lossless network.
2. The imaginary part of $Z_{22}$ should be larger than zero, that is $\mathrm{I}m[Z_{22}] > 0$. The noise factor $\Gamma(Z_{22})$ can be regarded as a quadratic polynomial; therefore optimum values can be determined from $\Gamma(Z_{22})$:

$$\mathrm{Im}[Z_{22}]_{opt} = \frac{C\sqrt{PR}(\omega C_{gs})}{(\omega C_{gs})^2 R + gm/R_f} \tag{7.62}$$

Substituting Equation (7.62) into (7.61), the optimum noise factor is given by

$$\Gamma(Z_{22})_{\min} = P\left[1 - \frac{(\omega C_{gs})^2 RC^2}{(\omega C_{gs})^2 R + gm/R_f}\right] \tag{7.63}$$

It is very common to use reactive components to achieve this impedance transformation, because they do not absorb any power or add noise. Thus, series or parallel inductance or capacitance can be added to the circuit to provide an impedance transformation. Figure 7.52 shows the typical narrowband inductor tuning networks: parallel tuning, T-type tuning, and Pi-type tuning. Figure 7.53 shows the gain and noise performance of a tuned receiver front-end using three typical narrowband inductor tuning networks. By using a single inductor tuning network, the noise factor of the front-end can be minimized at a single frequency point. When broader noise tuning bandwidths are required, multielement tuning networks that provide a noise match across the desired frequency band are required. For tuning bandwidths of around an octave, transformer tuning is a popular method used. The two equivalent circuit representations of a transformer, namely T-type and Pi-type, are used when analyzing and designing transformer tuned front-ends.

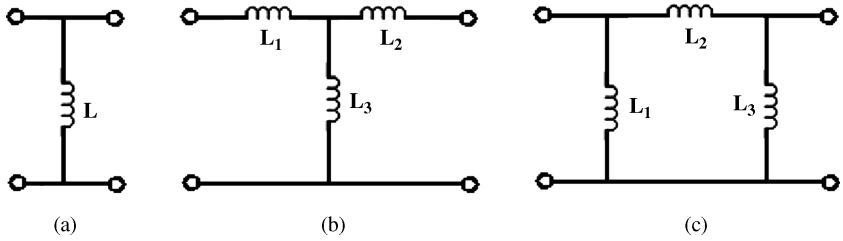
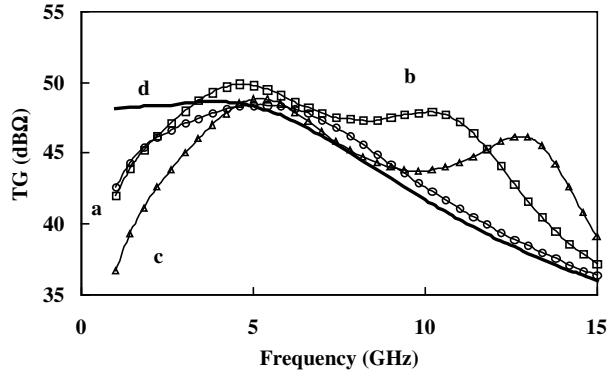
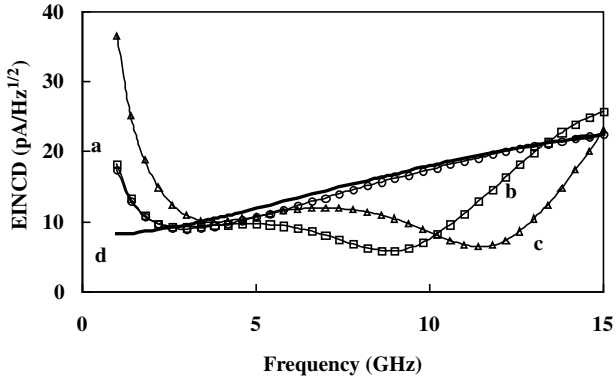



**Figure 7.52** Typical narrowband inductor tuning network: (a) parallel tuning; (b) T-type tuning; and (c) Pi-type tuning.




(a) Gain




(b) Noise

**Figure 7.53** (a) Gain and (b) noise performance of a tuned receiver front-end using the three typical narrowband inductor tuning networks.

Of course, the tuned optical receiver front-end using a narrowband inductor tuning network is suitable for an SCM system only. In the case of broadband optical receivers, the noise-matching network must be synthesized to satisfy the network requirements over a wide frequency range. The commonly used noise-matching network between

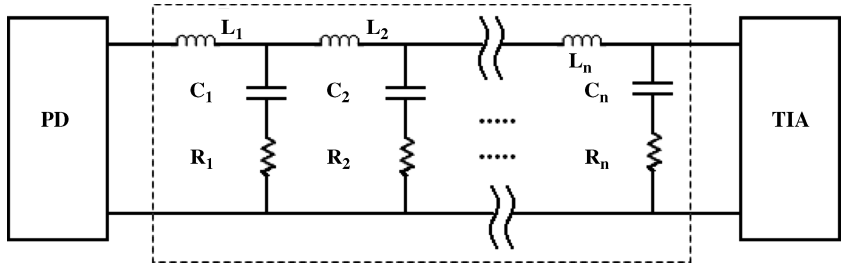



**Figure 7.54** Broadband noise-matching network.

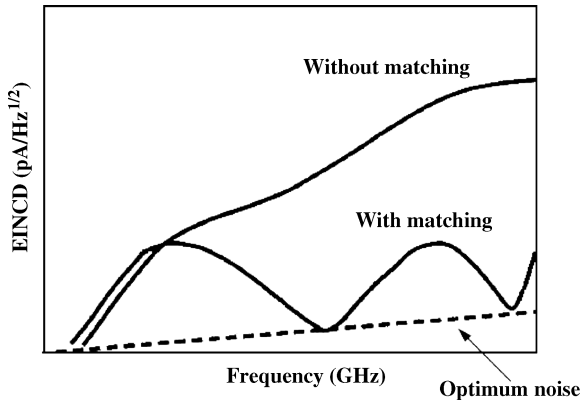



**Figure 7.55** Noise performance of a tuned receiver front-end using a broadband noise-matching network.

the PD and TIA is shown in Figure 7.54. By using a high-order low-pass filter-type network as the noise-matching network, the equivalent input noise current density of a completely tuned front-end can be reduced,as shown in Figure 7.55 [87, 88].

## 7.7 Summary

In this chapter, the basic concept of a high-speed receiver, the integrated circuit (IC) design technique of the front-end, has been introduced. The passive peaking techniques, which include inductance and capacitance techniques for extending bandwidth and minimizing the noise performance of transimpedance preamplifier designs, are described in more detail.

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