Copper Interconnect Technology

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Introduction to the Series

The Tutorial Texts series was initiated in 1989 as a way to make the material presented in SPIE short courses available to those who couldn't attend and to provide a reference book for those who could. Typically, short course notes are developed with the thought in mind that supporting material will be presented verbally to complement the notes, which are generally written in summary form, highlight key technical topics, and are not intended as stand-alone documents. Additionally, the figures, tables, and other graphically formatted information included with the notes require further explanation given in the instructor's lecture. As stand-alone documents, short course notes do not generally serve the student or reader well.

Many of the Tutorial Texts have thus started as short course notes subsequently expanded into books. The goal of the series is to provide readers with books that cover focused technical interest areas in a tutorial fashion. What separates the books in this series from other technical monographs and textbooks is the way in which the material is presented. Keeping in mind the tutorial nature of the series, many of the topics presented in these texts are followed by detailed examples that further explain the concepts presented. Many pictures and illustrations are included with each text, and where appropriate tabular reference data are also included.

To date, the texts published in this series have encompassed a wide range of topics, from geometrical optics to optical detectors to image processing. Each proposal is evaluated to determine the relevance of the proposed topic. This initial reviewing process has been very helpful to authors in identifying, early in the writing process, the need for additional material or other changes in approach that serve to strengthen the text. Once a manuscript is completed, it is peer reviewed to ensure that chapters communicate accurately the essential ingredients of the processes and technologies under discussion.

During the past nine years, my predecessor, Donald C. O'Shea, has done an excellent job in building the Tutorial Texts series, which now numbers nearly forty books. It has expanded to include not only texts developed by short course instructors but also those written by other topic experts. It is my goal to maintain the style and quality of books in the series, and to further expand the topic areas to include emerging as well as mature subjects in optics, photonics, and imaging.

Arthur R. Weeks, Jr.
Invivo Research Inc. and University of Central Florida

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INTRODUCTION

The semiconductor industry is continuing its quest to create ever more powerful CPU and memory chips.[1] These efforts are focused principally in two areas. On one hand, the speed of individual devices is increased through the continual reduction of the minimum size of device features. Along with this goes a corresponding increase in device density on the chip. On the other hand, in order to take advantage of increased device speeds, one needs to connect individual devices into circuits using increasingly complex interconnect schemes. These now involve multilayer structures made up of several levels of metal wiring separated by an interlayer dielectric (ILD). Efforts in both of these areas are supported by more and more sophisticated device and circuit design.

The exact nature of the trade-off between individual device and interconnect performance depends on details of the circuit architecture. However, it is now generally recognized that the overall circuit performance is going to be dominated by the efficiency with which devices are connected rather than by the speed of the individual devices. From the materials point of view, a better interconnect efficiency may be achieved with various new materials combinations for the metal and the interlayer dielectric (ILD). It is now becoming apparent that a major component of improved interconnect performance will consist in replacing aluminum, the previous metal of choice, with copper.

Several companies announced recently that they have been successful in fabricating ultralarge-scale integrated (ULSI) circuits using Cu.[2–5] IBM[2] was first to publish pictures showing interconnect structures with six levels of Cu metal (M1-M6, see Figs. 1 and 2). Some of the features of the announced Cu processes are given below. The IBM process has been described in detail in Ref. [3].

IBM:[4a]

CMOS process (Cu with SiO_2); M1 contacted pitch 0.63 μm, M2-M6 contacted pitch 0.91 μm, local tungsten interconnects, gate length 0.20 μm, SRAM cell size 6.8 μm^2.

Motorola:[5]

CMOS process (Cu with SiO_2); M1 pitch 0.63 μm, M6 pitch 1.62 μm, gate length 0.15 μm, SRAM cell size 7.6 μm^2.

Texas Instruments:[6]

Interconnect tests structures with 0.3 μm Cu lines embedded in xerogel, capped with silicon nitride and silicon oxide.

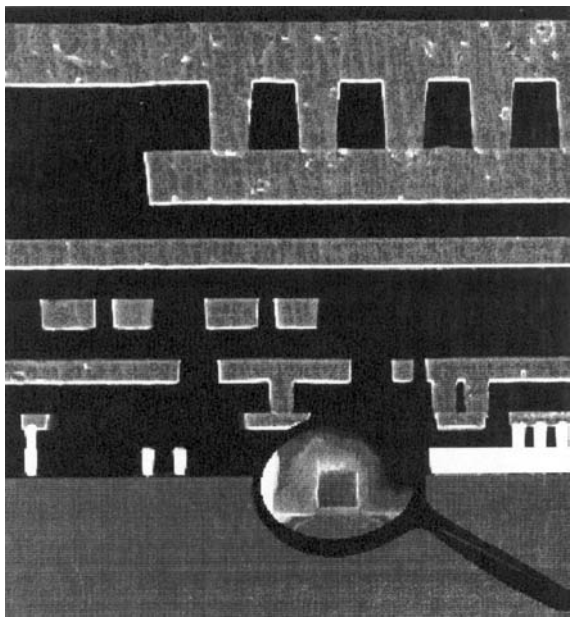

Figure 1 Scanning electron micrograph of IBM six-level Cu interconnect structure: cross section.

Very recently, IBM reported on two technologies involving Cu and an ILD with lower dielectric constant than silicon dioxide. In the first paper,[4b] the integration of fluorine-doped oxide with Cu for the 0.18-μm node has been described. In the second paper,[4c] the application of Cu and an organic material as the ILD for the 0.13-μm technology node has been demonstrated. (For further details see Sec. 7.)

The purpose of this book is to present a tutorial overview of the issues involved in implementing the use of copper in future interconnect technologies. We will attempt to give the reader an appreciation of the range of problems involved and the avenues along which solutions to these problems are being sought. With this focus in mind, we will not try to deal exhaustively with all the technical issues in every area covered. This would be beyond the scope of this book. Rather, we will provide representative examples of the most important technical approaches being pursued and references to more in-depth information elsewhere. In order to put our arguments in perspective, it will be worth taking note of Ref. [7], which contains an extensive discussion of previous, aluminum-based interconnect technologies as well as early work in copper technology.

The organization of the book is as follows: We start with a brief description of the status, major issues, and materials options for interconnect technologies. Next, we illustrate in general terms different approaches to the fabrication of mul-

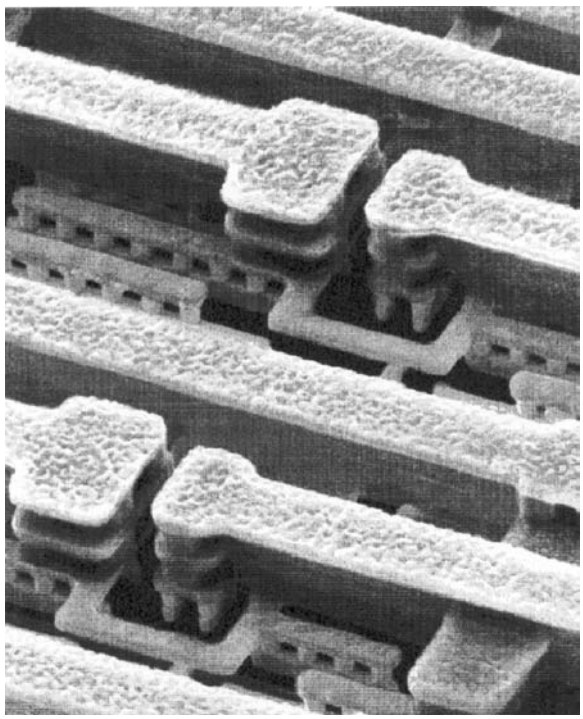

Figure 2 Scanning electron micrograph of IBM six-level Cu interconnect structure: perspective view.

tilayer interconnect structures, with particular emphasis on how to create patterned multilayers. This includes a comparison of subtractive patterning, as used with Al metallization, and damascene patterning, as used with Cu metallization. We then give a general discussion of Cu deposition and patterning, interlayer dielectrics, Cu diffusion barriers and passivation, and Cu/barrier/ILD issues, with a focus on scientific fundamentals, potential process alternatives, and future options. We conclude with a detailed description of the preferred approaches and technological practices being implemented at this time.

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2

INTERCONNECT ISSUES

2.1 OVERVIEW

Several factors contribute to the performance of a particular interconnect scheme, including its architecture and the properties of the materials involved. A basic figure of merit to such a scheme is its RC delay, which represents a measure of the time delay for signal propagation. R denotes the resistance of an interconnect metal line, and C denotes the effective capacitance between the line and its surroundings.

The estimated effect of various geometrical and materials parameters on the RC delay can be obtained by considering the test structure of Fig. 3, which is similar to the one used in Refs. [8] and [9]. The test structure employs a set of metal lines between two grounded metal planes, all embedded in the interlayer dielectric medium. Let us assume that the metal line width is W, the metal line thickness is T, the spacing between two lines is S, the metal line pitch is P (with $P = W + S$), and the thickness of the ILD between the top of the metal lines and the grounded planes is D. Also, let $L =$ length of a metal line and $\rho =$ metal resistivity. We will use the pitch P and the metal thickness T as basic parameters, so that we can set $W = aP$ and $D = bT$ where a and b are constants appropriate for the given geometry.

The resistance R of a metal line is then given by

$$R = \rho L/WT = \rho L/aPT. \tag{1}$$

If the ILD has an isotropic relative dielectric constant k and one neglects edge contributions from the metal lines as well as coupling of the metal line sidewalls to the ground planes, then one has

$$C_{LG} = k\varepsilon_o WL/D = k\varepsilon_o aPL/bT, \tag{2}$$

and

$$C_{LL} = k\varepsilon_o TL/S = k\varepsilon_o TL/(P - W) = k\varepsilon_o TL/(1 - a)P, \tag{3}$$

where ε_o is the permittivity of free space. In Eqs. (2) and (3), C_{LG} represents the "vertical" capacitance between a metal line and a ground plane above (or below),

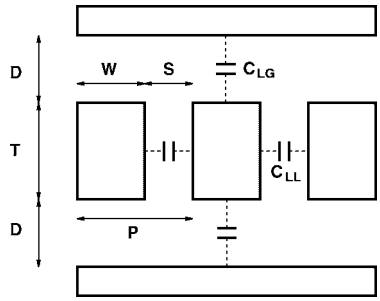


Figure 3 Simplified RC delay test structure.

and C_{LL} represents the "horizontal" capacitance between two neighboring lines. For the total capacitance C of a metal line relative to its surroundings one can write

$$C = 2(C_{LG} + C_{LL}) = 2k\varepsilon_o L[aP/bT + T/(1-a)P]. \tag{4}$$

For the RC time delay constant, it follows that

$$RC = 2R(C_{LG} + C_{LL}), \tag{5}$$

or, combining Eqs. (1), (4) and (5),

$$RC = 2\rho k\varepsilon_o L^2\big[1/bT^2 + 1/a(1-a)P^2\big]. \tag{6}$$

Equivalently one can write

$$RC = 2\rho k\varepsilon_o\big(L^2/P^2\big)\big[P^2/bT^2 + 1/a(1-a)\big]. \tag{7}$$

The right-hand side of Eq. (6) has a natural interpretation, in that the factors $2\rho k\varepsilon_o$ and $L^2(1/bT^2 + 1/a(1-a)P^2)$ represent the materials and architecture contributions to the interconnect time delay.

Equation (7) can be examined from a slightly different point of view if one defines the aspect ratio A of the metal lines as the ratio of line thickness to line width, $A = T/W$, or equivalently $A = T/aP$. In terms of A, Eq. (7) can be expressed as

$$RC = 2\rho k\varepsilon_o\big(L^2/P^2\big)\big(1/a^2bA^2 + 1/a(1-a)\big). \tag{8}$$

Keep in mind that the term $1/a^2bA^2$ in Eq. (8) represents the "vertical" and the term $1/a(1-a)$ the "horizontal" contribution to the total capacitance.

We conclude from Eqs. (7) and (8) that for fixed line length L and fixed aspect ratio A, the RC delay increases quadratically with decreasing feature size (decreasing pitch P). In addition, Eqs. (7) and (8) imply that for $A \ll 1$ the interlayer ("vertical") capacitance is more important to the RC delay than the intralayer ("horizontal") capacitance, whereas the opposite is true for $A \gg 1$. Also note that for the simplest geometry where $a = 0.5$ and $b = 1$ ($D = T$), Eq. (8) reduces to

$$RC = 8\rho k\varepsilon_o\left(L^2/P^2\right)\left(1/A^2 + 1\right). \tag{9}$$

Using the assumptions above, one can generalize Eqs. (7) and (8) to the case where the ILD is not isotropic. If the ILD has a "vertical" (between-layer) dielectric constant k_{LG} and a "horizontal" (between-lines) dielectric constant k_{LL}, then one obtains

$$RC = 2\rho\varepsilon_o\left(L^2/P^2\right)\left[k_{LG}/a^2bA^2 + k_{LL}/a(1-a)\right]. \tag{10}$$

Again, for the simplest geometry where $a = 0.5$ and $b = 1$ ($D = T$), Eq. (10) reduces to

$$RC = 8\rho\varepsilon_o\left(L^2/P^2\right)\left(k_{LG}/A^2 + k_{LL}\right). \tag{11}$$

For a semi-quantitative comparison, consider Eq. (11) with some Cu and Al interconnect structures. Let L, W, P, and D be fixed ($W = 0.5P$, $a = 0.5$). Let $T_{\mathrm{Cu}} = D$ ($b_{\mathrm{Cu}} = 1$), and let both metal lines have the same resistance, which requires that $T_{\mathrm{Al}} = 1.3T_{\mathrm{Cu}}$ ($\rho_{\mathrm{Al}} = 1.3\rho_{\mathrm{Cu}}$, $b_{\mathrm{Al}} = 1/1.3$). In other words, the geometries are the same except that the aspect ratio of the Al lines is 1.3 times the aspect ratio of the Cu lines. From Eq. (10) it follows that the expressions $(k_{LG}/A_{\mathrm{Cu}}^2 + k_{LL})$ for Cu and $(k_{LG}/A_{\mathrm{Cu}}^2 + 1.3k_{LL})$ for Al represent figures of merit, being proportional to the respective RC delays.

Numerical examples are listed below for $A_{\mathrm{Cu}} = 2$ and $A_{\mathrm{Cu}} = 2.6$. With Cu, an isotropic ILD is assumed, whereas with Al the spaces between lines are assumed to be filled with a material of lower k_{LL}.

Cu:	$k_{LG} = k_{LL} = 4.3$	$k_{LG}/A_{\mathrm{Cu}}^2 + k_{LL} = 5.4$
	3.9	4.9
	2.7	3.4
	2.0	2.5
Al:	$k_{LG} = 4.3$, $k_{LL} = 2.7$	$k_{LG}/A_{\mathrm{Cu}}^2 + 1.3k_{LL} = 4.6$
	2.0	3.7
	1.3	2.8
	$k_{LG} = 3.9$, $k_{LL} = 1.2$	2.5

The numbers for k_{LG} and k_{LL} are representative of normal oxide (4.3), F-doped oxide (3.9), a current low-k polymer (2.7), a lower-k future polymer or porous material (2.0), and a highly porous, or air-gap, material (1.3, 1.2). From these results one may conclude, for example, that Al with intralayer airgaps could be almost equivalent to Cu with an isotropic, teflon-like ILD. It should be pointed out, however, that the numerical comparison depends on the details of the ILD structure. If the entire geometry were the same for both Cu and Al (i.e., equal aspect ratios), the figure of merit for Al would also be represented by $k_{LG}/A_{\mathrm{Cu}}^2 + k_{LL}$, which would give slightly larger numerical values for Al.

The results above illustrate how important k_{LL} is, especially for high-aspect ratio structures, and that a high aspect ratio mitigates the influence of k_{LG}. In addition, note that the contribution proportional to $1/a(1-a)$ in Eqs. (8) and (10), due to the intralayer capacitance, is minimized when $a = 0.5$, that is when the metal line width W is equal one half of the pitch P.

In interpreting Eqs. (7) to (11) it is important to keep in mind that as devices and their interconnect dimensions are reduced in size, the ratio L/P does not stay constant but rather increases, because the metal line lengths L tend to scale less strongly than the metal pitch P.[9–11] That is, even as devices keep shrinking, they still contain some rather long lines.[242,243] For example, for a 4M-gate circuit block with 7 metal levels and using 260 nm design rules, several hundred metal line segments longer than 1 mm were found.[243] Modeling the wiring distribution in the Intel Pentium Klamath design shows that most wires are 1–10 μm long, yet there is also a not insignificant number of wires (of the order of 0.1%) as long as 1–10 mm.[12] At the same time, the aspect ratio A tends to increase because R needs to be kept as low as possible in order for electrical power dissipation to be minimized (see Fig. 1). When applied to Eqs. (7) to (11), these geometrical constraints lead to two conclusions: For a given set of interconnect materials (that is, for fixed ρ and k), as device dimensions are reduced,

(1) the RC delay will increase;
(2) the overall capacitance will be dominated by the intralayer capacitance, which will also give rise to increased line-to-line crosstalk.

As far as the relative importance of intrinsic and interconnect delays is concerned, it should be pointed out that the exact feature size at which the interconnect RC delay equals and then surpasses the intrinsic transistor delay depends on details of the circuit design. Moreover, the total overall time delay t_{int} is composed of four components and can be approximated by[243]

$$t_{int} = R_0 C + 0.4\left[(RC)^{1.6} + (tof)^{1.6}\right]^{1/1.6} + 0.7RC_{in}, \tag{12}$$

where R_0 is the output resistance of the driver device, *tof* the time of flight of the electromagnetic wave in the interconnect, and C_{in} the input capacitance of the device in the next gate. These four terms contribute differently to the overall delay depending on gate length and width, interconnect line length L, and other geometrical parameters.[1,3,10,11,243] In one case, the effect of various approaches to relaxing design rules in upper interconnect metal levels has been investigated.[243] Note that the upper levels of metallization are used for power distribution where electromigration is a major concern. However, all these results point to a minimum feature size of the order of 0.5 μm at which the interconnect RC delay starts to become more significant than the intrinsic transistor delay.[1,8–11] The consequences of interconnect length, scaling, and material properties on crosstalk between distributed RC lines have also been discussed.[244]

Equations (7) to (11) provide some general insight as to how the interconnect RC delay can be minimized. With respect to circuit architecture one can conclude that as the minimum feature size and thus the pitch P in the lower interconnect metal levels decrease, the line length L should be reduced as much as possible. This may ultimately require using block designs or repeaters. Conversely, for lines with large L the pitch P should be large. This means that long interconnect lines should only be used in the upper interconnect metal layers where there is room for increased pitch. Therefore, an interconnect scheme will involve a hierarchy of scales, with the smallest lines in the first metal layer and progressively fatter and longer lines in the upper layers. This type of approach also helps to improve other aspects of chip performance, such as coupled-noise induced delays and clock skew.[3]

On the interconnect materials side, it is evident that one should use the metal with the lowest possible resistivity ρ and the ILD with the lowest possible dielectric constant k. With regard to the metal, this means using copper. With regard to the ILD, it will be especially helpful to selectively reduce the k_{LL} between the metal lines. Some of of the benefits of this latter approach have already been demonstrated.[9]

It is also worth pointing out that the decrease in minimum feature size is predicted to be accompanied by an increase in the complexity of the interconnect structure itself, in particular by a rapid increase in the number of metal layers necessary to achieve clock frequency targets.[13] As the minimum feature size reaches the 0.1 μm range, this number may, in fact, become prohibitive from the point of view of being manufacturable, unless new designs involving smaller circuit blocks will be implemented.[13]

2.2 MATERIALS REQUIREMENTS

Since we will focus on materials issues related to optimizing interconnections, let us note that in the traditional interconnect technologies the metal of choice has been Al and the ILD has been SiO_2.[8] This materials system has some unique advantages compared to potential replacements, as we shall see in detail below, and it has also evolved into mature fabrication technology. As a point of reference for materials parameters, let us keep in mind that $\rho = 2.7\ \mu\Omega\,\text{cm}$ for pure Al and $k = 4.2$ for the type of SiO_2 typically used as an ILD. However, Al is often alloyed with Si and/or Cu for reasons of stability with respect to the interaction with Si and for improved electromigration resistance. With the introduction of salicided junctions, the need for Si addition to Al has been removed. Also, in Al technology contact to the underlying layer is usually made through vias filled with W plugs, which eliminates the need for Si alloying. Furthermore, in many applications a thin, higher resistivity layer is used as a barrier between the metal and the ILD or Si. These modifications result in an increased effective resistivity ρ_{eff} for the Al interconnect lines of typically about $3.3\ \mu\Omega\,\text{cm}$.[12]

We will deal with various materials requirements for the metal and the ILD in detail shortly, but at this point it is apparent already that for the metal, the only possible options in replacing Al are Cu, Ag, and Au, and the only practical option really is Cu. Not only do costs, manufacturability, and device reliability favor Cu, but in terms of improved resistivity the additional gain in going from Cu ($\rho_{bulk} = 1.7\ \mu\Omega\,\text{cm}$) to either Ag ($\rho_{bulk} = 1.6\ \mu\Omega\,\text{cm}$) or Au ($\rho_{bulk} = 1.5\ \mu\Omega\,\text{cm}$) would be quite minimal. Hence there are in principle two ways by which to migrate from the traditional Al/SiO_2 interconnect technology to an ultimate solution involving Cu/low-k ILD, depending on whether the metal or the ILD is replaced first (Fig. 4).

In contrast to the situation with the metals, the choices for the best ILD are much more open, and it is unclear at this point whether there will be a single winner in the end. Therefore, using a conservative but realistic ρ_{eff} for Cu of $2.6\ \mu\Omega\,\text{cm}$[12] and $k = 1$ for air as the ideal ILD, the RC delay could be improved by a factor of at best about 5.3 relative to Al/SiO_2. A more realistic estimate is probably a factor of about 2.8, corresponding to an ILD with k around 2, or a little lower than 2.

The particular requirements for Cu to replace Al fall into three categories: control of the microstructure, patterning for creating fine lines, and control of the metal/ILD interface. First, the microstructure of Cu determines its resistivity and resistance to electromigration and is a function of the deposition method, the deposition conditions, and the nature and topography of the substrate. The deposition methods being investigated primarily are physical vapor deposition (PVD), chemical vapor deposition (CVD), and electrochemical plating (ECP). Second, the optimal patterning method for Cu appears to be the damascene (inlaid) technique, whereby the desired patterns are actually formed in the ILD and then filled with

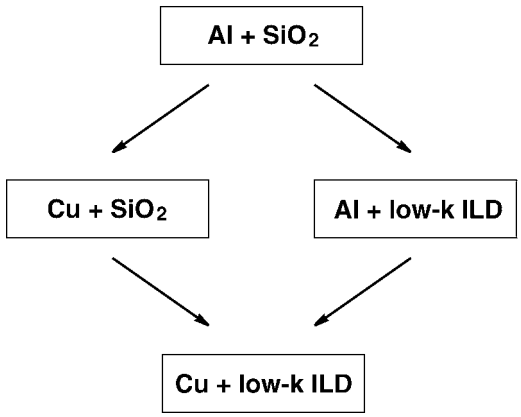


Figure 4 Materials options for migration from Al/SiO_2 to Cu/low-k interconnect technology.

the metal. The third important issue is the stability of the Cu/ILD interface. This is exemplified on the one hand by the rather weak adhesion of Cu to most ILD materials and the strong tendency of Cu to diffuse into and through the ILD, and on the other hand by the rapid oxidation of Cu in an oxidizing environment. (Thus Cu cannot be used without diffusion barriers and passivation layers.) All these issues have a significant bearing on the overall integration of Cu into a manufacturing process and eventually on the long-term reliability of Cu devices.

With regard to several of the issues just mentioned, it turns out that Al has significant advantages over Cu,[7] not the least of which is that Al technology has matured over a long period of time, and extensive experience has been accumulated with the material in the semiconductor industry. Let us note first that the deposition of Al is fairly straightforward, involving the PVD process of sputter deposition, often in combination with elevated substrate temperature. Neither the deposition method nor the temperature generally pose a problem since the ILD has been SiO_2 and the aspect ratios of features in the ILD that need to be filled with Al have been fairly small. However, with Cu the low-k ILD of the future may be a polymer, i.e., a material with much lower thermal stability than SiO_2. This will necessitate processing with a much lower thermal budget than before. Furthermore, physical deposition methods will most likely be inadequate to fill features with the more aggressive aspect ratios that will be required in future technologies.[1] Second, the fine-line patterning of Al is done by reactive ion etching in a chlorine-based plasma, i.e., by a subtractive method in which those parts of a blanket Al film which are not part of the desired wiring pattern are directly and selectively removed. It is much more difficult to apply the same type of process to the patterning of Cu for reasons that we will discuss further below. Third, Al reacts with

SiO_2 to form a strong interface, and the native oxide layer on Al also provides self-passivation with respect to further reaction. The only clear advantage Cu has over Al at the outset, except for its lower resistivity, is that it is much more stable toward electromigration[14,15] and stress migration failure.[3] In addition, it should be mentioned that electrochemical plating, the currently favored method for Cu deposition, allows for much lower processing temperatures, thus enabling the use of ILDs with lower temperature stability than SiO_2.

As we noted above, the options are more varied when it comes to the choice of an ILD, but so are the materials requirements placed on an ILD.[1,8,10] It may in fact turn out that several options will be implemented along the two paths illustrated in Fig. 4. A few examples of work reported along these lines include the use of Cu with a silica-based low-k ILD,[16] Cu in combination with a low-k polymer,[17] and Al with various low-k ILDs.[10,18,19] More details will be discussed below in Chapter 5 on interlayer dielectrics.

Some of the generic issues to be resolved in connection with the introduction of new ILD's are the following:

- *electrical*: low k overall, controlled anisotropy in k, low dissipation and leakage, high dielectric strength;
- *chemical*: chemical resistance, ability to be patterned, low moisture absorption, no metal corrosion;
- *mechanical*: adhesion (ILD-Cu, ILD-ILD), low stress, high strength (polishability);
- *thermal*: stability up to required temperature, low coefficient of thermal expansion (CTE), low thermal shrinkage, high thermal conductivity.

In terms of specific ILD materials characteristics, the following are desired, in the order of their importance:[8]

(1) Low k (< 3);
(2) Thermal stability: glass transition temperature $T_g > 400°C$; $< 1\%$ weight loss at $T < 425°C$ in N_2;
(3) Moisture absorption: $< 2\%$ at 100% humidity;
(4) Adhesion, ILD-metal and ILD-ILD: pass Scotch tape test; no peel after cycling to 450°C;
(5) CTE: < 50 ppm/°C at 200°C;
(6) Chemical resistance: ILD inert towards, acids, bases, and photoresist strippers;
(7) Patterning: adequate selectivity for ILD/metal and metal/ILD in plasma etch, processable in damascene technology.

The above is only a partial list, and additional desired characteristics have been identified.[8]

2.3 MATERIALS OPTIONS

On the basis of the arguments made above, interconnect materials options can be summarized briefly as follows: As far as the *metal* is concerned, Cu will clearly be the material of choice for future interconnect technologies. The open questions relate more to the optimal implementation of various aspects of the processing of Cu. On the other hand, it is not clear at this point which material will be used as an adhesion/diffusion barrier layer between Cu and a future low-*k* ILD, although it is evident that a barrier will be necessary. The specific choice of barrier material may well depend on the properties of the particular ILD that the barrier is intended to be combined with.

The candidates for future low-*k* ILDs fall into two classes of materials. The first one is comprised of a set of inorganic, *silica-based oxides*:

- doped SiO_2 (F-doped, with composition SiO_xF_y and abbreviated as FSG for fluorosilicate glass; or C-doped).
- hydrogen silsesquioxane (composition $HSiO_{3/2}$, abbreviated as HSQ). Related materials with composition $RSiO_{3/2}$, where R is a side group other than H, are also under investigation.
- xerogels (porous SiO_2).
- air gap structures (metal wiring where the spaces between metal lines are only partially filled with SiO_2, and thus contain voids).

The second class of prospective ILD's involves a variety of *organic polymers*, for example:

- non-fluorinated (benzocyclobutene, parylene-n, FLARE2.0, SiLK, Black Diamond, Coral, various polyimides, etc.).
- fluorinated (perfluorinated cyclobutene, parylene-f, FLARE1.0, teflon, fluorinated amorphous carbon, etc.).

In Chapters 3 to 6, we will discuss in detail issues pertinent to the deposition and patterning of Cu films, the formation and characterization of various ILD materials, and the integration of barrier materials with Cu and ILDs.

2.4 MULTILEVEL INTERCONNECT FABRICATION

In order to put the materials issues of Cu interconnect technology in perspective, it is useful to consider, in brief general terms, how multilevel interconnect structures can be fabricated. (Additional details will be provided below in the chapters on Cu and ILD processing.) Two complementary approaches can be distinguished. They have in common that they start from the same initial structure (in the figures below a Si wafer with active devices on it and covered by the first ILD layer), and they arrive at the same final wiring pattern, but in doing so they proceed differently.

The traditional approach (used with Al/SiO_2) is illustrated in Fig. 5. The metal is patterned directly by dry etching and the ILD deposited on top of the metal is planarized. For every new interconnect layer, the steps shown in Fig. 5 are repeated.

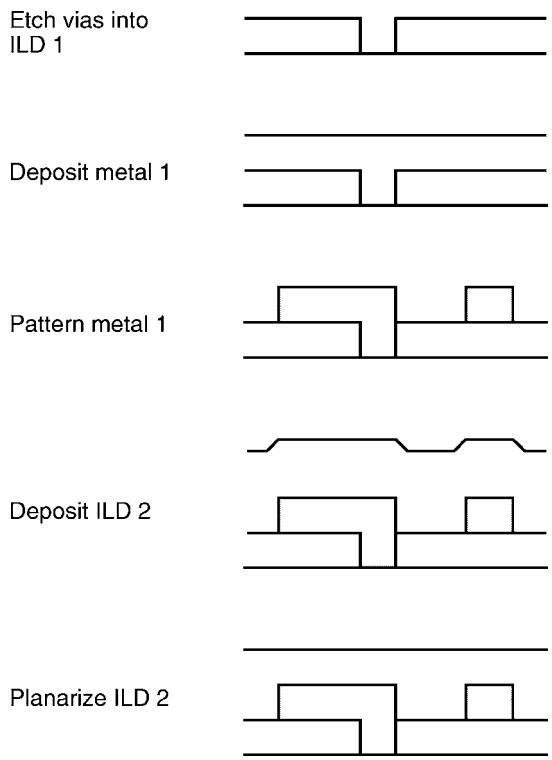


Figure 5 Schematic process of interconnect fabrication: traditional approach using subtractive metal patterning. The steps shown resemble a process employing Al plugs in the vias, as used in earlier microelectronics technology. Present Al technology uses W plugs, which are formed by blanket CVD of W, followed by removal of the extra W in the field regions by chemical-mechanical polishing.

The damascene approach (used with Cu/SiO_2 and most likely with Cu and low-*k* ILDs) is illustrated in Fig. 6. The entire wiring pattern is formed as an inlaid template in the ILD by dry etching. This pattern is then filled with metal, and finally the metal is planarized and the extra metal on top of the ILD is removed.

Note that in Figs. 5 and 6 all processing steps are not shown. Several lithography steps necessary to define the patterns in the metal and the ILD are missing, for example the steps for the definition of the via (contact hole) in the top panel of Fig. 5. Also note that both schemes require two dry, plasma etch steps to transfer the lithographically defined patterns into the underlying layer. In the traditional approach, these two steps are a dielectric etch and a metal etch. Both steps end on top of the layer underlying the material being etched, which facilitates etch end point detection. The dielectric etch of the ILD defines the vias, through which contact is made to the underlying layer, and the metal etch defines the wiring pattern connecting the vias. Together they serve to make up the structure of one interconnect

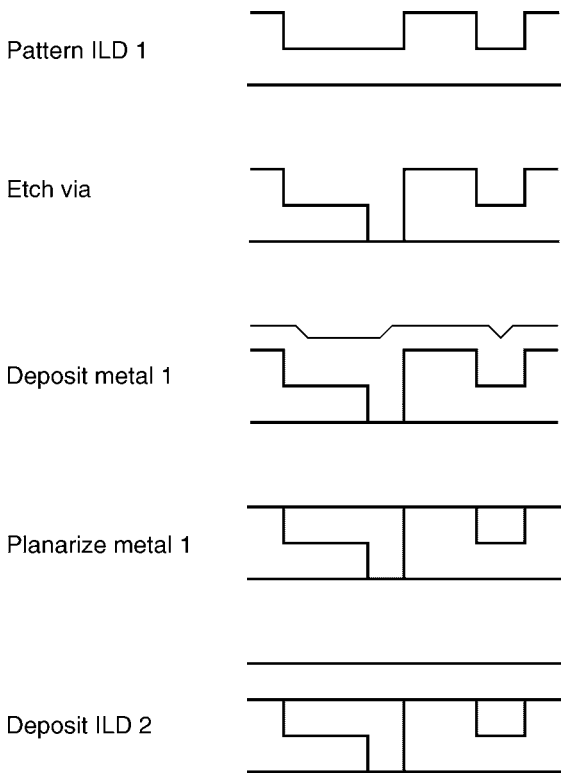


Figure 6 Schematic process of interconnect fabrication: damascene approach using inlaid, planarized metal.

level. In the damascene approach, the two etch steps are both in the ILD. One of them defines the vias and the other the actual wiring as an inlaid pattern in the ILD connecting the vias. Consequently, one of these etch steps must end in the middle of the ILD. This presents additional difficulties in terms of etch end point detection because the end point does not occur when the material has been cleared but rather when the proper etch depth has been reached. Therefore, the etch depth must be controlled precisely. In practice, this is often achieved using an intermediate etch stop such as SiN. However, the damascene approach does have one crucial advantage over the traditional approach; with damascene one can get around having to do a metal plasma etch step. In fact, the point that it is much more difficult to etch Cu than Al has turned out to be the major stumbling block in applying the traditional approach to Cu technology and has been the main driving force in the development of the damascene approach for Cu interconnect technology.

Three additional issues are worth pointing out in connection with the damascene approach. First, since two ILD patterning steps are required, the question is in which order to proceed. That is, should the vias or the trenches be formed first (Fig. 7)? If the vias are first, they could be formed halfway through the ILD, as shown in Fig. 7, or they could be formed completely down to the metal below. Each of these ways has advantages and disadvantages. Without going into details here, let us just mention that when the vias are formed first, the photoresist for

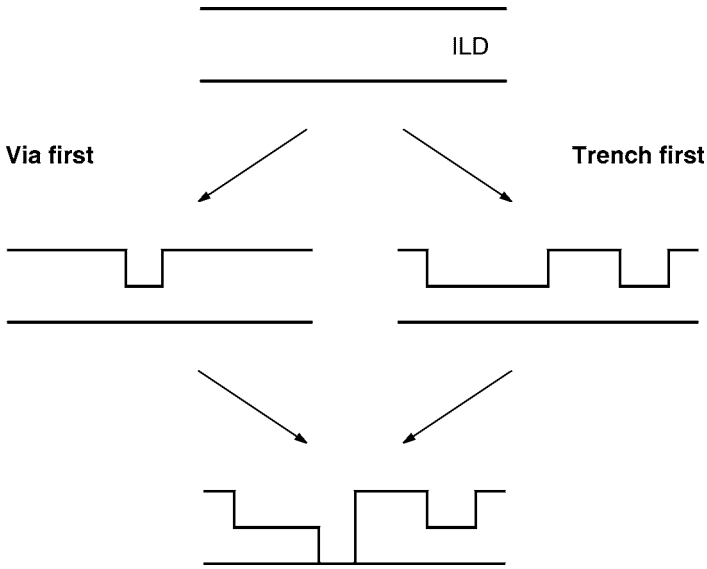


Figure 7 Damascene patterning: Via first, or trench first?

defining the second patterning step will fill the via hole and therefore be quite non-uniform in thickness across the wafer. Consequently, it will be difficult to expose the photoresist such that it clears everywhere properly. With the trenches formed first, the lithography for defining the vias must be done on an extra-thick layer of photoresist on top of a non-planar substrate. This makes it more difficult to maintain critical dimensions in that second step, which is precisely the one involving the features (vias) with the smallest dimensions (see also Sec. 5.4.3).

Second, the graphs in Figs. 5 and 6 give a simplified picture of the structure of real multilevel interconnects. With Cu there will have to be a barrier layer between the Cu and any ILD in contact with the Cu (Fig. 8), since Cu is a fast diffuser in practically all ILD materials investigated to date. In the planarization step, the metal is removed by chemical-mechanical polishing (CMP). In the final stage of this processing step, the Cu and the barrier layer 1 must be removed uniformly, even though these are materials with rather different chemical and mechanical properties, and the Cu surfaces must be left planar regardless of their size and pattern density. Before the next ILD layer is deposited, the barrier layer 2 has to be put down so that the top exposed Cu surfaces are also protected (Fig. 8). Moreover,

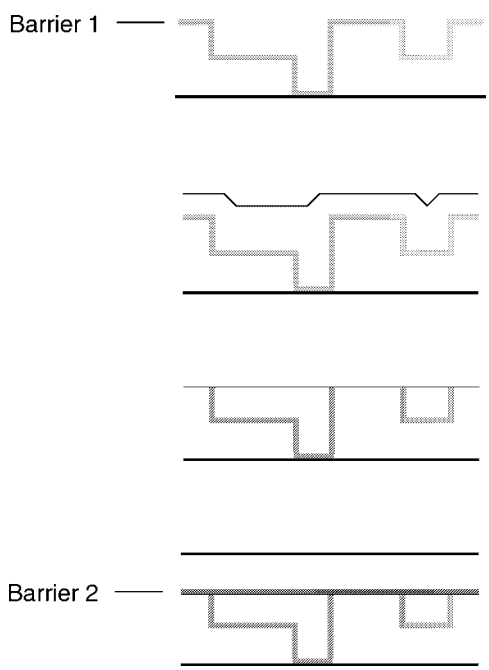


Figure 8 Damascene patterning and Cu planarization by chemical-mechanical polishing, showing top and bottom barriers barriers.

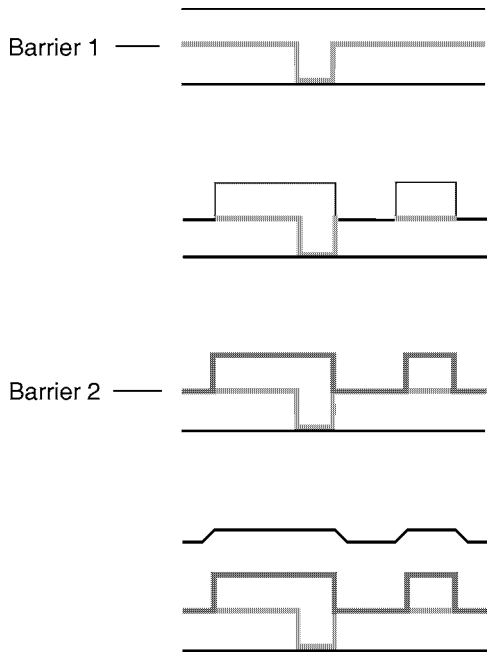


Figure 9 Barriers in subtractive metal patterning.

it should be noted that in the first metal layer, the vias are generally filled with W so that Cu is not in direct contact with the active devices.

Two barrier layers would also be necessary for Cu interconnect structures formed by the traditional approach (Fig. 9). In that case, the metal etch also has to remove the barrier 1 material between the metal lines. In both approaches, barrier 1 ends up covering just the lower portion of the metal pattern and thus can be an electrical conductor, whereas barrier 2 must be an insulator in order to maintain electrical isolation between metal lines (Figs. 8 and 9).

Third, when forming the vias in an ILD layer, it is important that the metal surface area at the bottom of the via can be cleaned properly so that eventually good electrical contact can be achieved between the upper and lower metal levels. Initially this requires that all vias are cleared in the course of the etching and no ILD is left in any of them. In order to insure complete via clearing everywhere, a certain amount of overetch is generally applied. This, in turn, tends to deposit polymeric residue, possibly containing metal, at the bottoms of some of the vias. Removal of this residue in cleaning the vias is often not a trivial task.

3

COPPER DEPOSITION

3.1 OVERVIEW

For the deposition and processing of copper films one may distinguish the following general requirements:

(1) It must be possible to deposit high-purity films for the lowest possible resistivity ρ. In addition, it will be desirable to be able to control the texture of the Cu films, since this is a determining factor for the electromigration resistance of the material.
(2) The deposition method chosen must allow for high deposition rates for adequate throughput.
(3) A chemical-mechanical polishing technique has to be developed that makes it feasible to planarize Cu and its associated barrier layer.
(4) Given that Cu will be used in conjunction with the damascene method for patterning, the deposition method must be able to completely fill trenches and vias with high aspect ratios.
(5) Since the use of Cu necessitates a diffusion barrier, it will be desirable to perform the metal/barrier depositions in an integrated cluster tool, so that the sample does not have to be exposed to the atmosphere between the two depositions.
(6) It must be possible to maintain a low-cost, high-reliability process for low cost of ownership.

In the next two sections we will describe various chemical and physical methods for the deposition of Cu. This will be followed by a section on approaches to the patterning of Cu, both subtractive and damascene.

3.2 CHEMICAL DEPOSITION METHODS FOR COPPER

This section deals with the two major chemical methods for depositing Cu films. These are chemical vapor deposition (CVD) and electrochemical plating (ECP). (For information on electroless plating, a third chemical method, the reader is referred to Ref. [19]. This method appears to be of less practical importance at the present time.) Since the CVD method generally involves organometallic precursor species, it is sometimes referred to as MOCVD. We use the term “chemical

method" in the sense that chemical reactions of molecular precursor species containing Cu atoms are an essential part of the deposition process.

3.2.1 Chemical vapor deposition (CVD)

The principle underlying any CVD method is the heterogeneous decomposition of a gaseous precursor, such that the desired atomic species are deposited on the substrate and the by-products remaining from the precursor molecules are carried away in the gas phase. The Cu films so formed must, of course, satisfy the requirements outlined above. This points immediately to two main issues in Cu CVD: (1) the availability of suitable precursor species, which means precursor species with adequate volatility, and (2) the purity (hence the electrical resistivity) of the deposited films, which may be limited by incorporation of by-products from the deposition reaction. In addition, the temperature required for Cu CVD may restrict the type of ILD that can be used in conjunction with the CVD process. On the other hand, one can anticipate that Cu CVD will give excellent results in regard to via filling, since it tends to form highly conformal deposits, as is common for CVD methods in the surface-reaction controlled regime.

A typical set-up for Cu CVD is displayed schematically in Fig. 10.[21] The reactor of Fig. 10 shows the usual gas introduction and pumping facilities. The Cu-containing species from the liquid precursor are carried into the chamber with the help of a carrier gas. The showerhead serves to direct a uniform flux of reactants over the wafer surface. Hydrogen represents an additional gas that may be made to react with the copper precursor to facilitate the deposition process. The reactor in Fig. 10 is a cold-wall reactor, in that only the substrate is heated. Alternatively, in a hot-wall reactor the entire chamber is heated. The major drawback of a hot-wall reactor is that unwanted Cu deposition may occur on the chamber walls.

In general, precursors are metallorganic Cu compounds, the most favored being ligand-stabilized Cu^{I} and Cu^{II} β-diketonates. Cu^{I} compounds are usually liquid and Cu^{II} solid at room temperature. The vapor pressures of both these types of compounds are such that adequate volatility can be achieved at reasonable temperatures. Solid precursors present somewhat more difficulties in maintaining controlled evaporation and consistent delivery to the substrate. Therefore, dissolution of the solid precursor in a solvent, followed by transport of the solvent into the reactor, has also been explored.[21] Generalized examples of Cu^{I} and Cu^{II} β-diketonate precursors are shown in Fig. 11.

The most common class of compounds involves $R = R' = CF_3$. In this case the diketonate is abbreviated as hfac (hexafluoroacetylacetonate), and the precursors are called $Cu^{II}(hfac)_2$ and $(hfac)Cu^{I}(L)$. A commercially available variety is CupraSelect,[22] which can be represented as $(hfac)Cu^{I}(tmvs)$ where tmvs stands for trimethylvinylsilane (Fig. 12). It is worth noting that the volatility of these

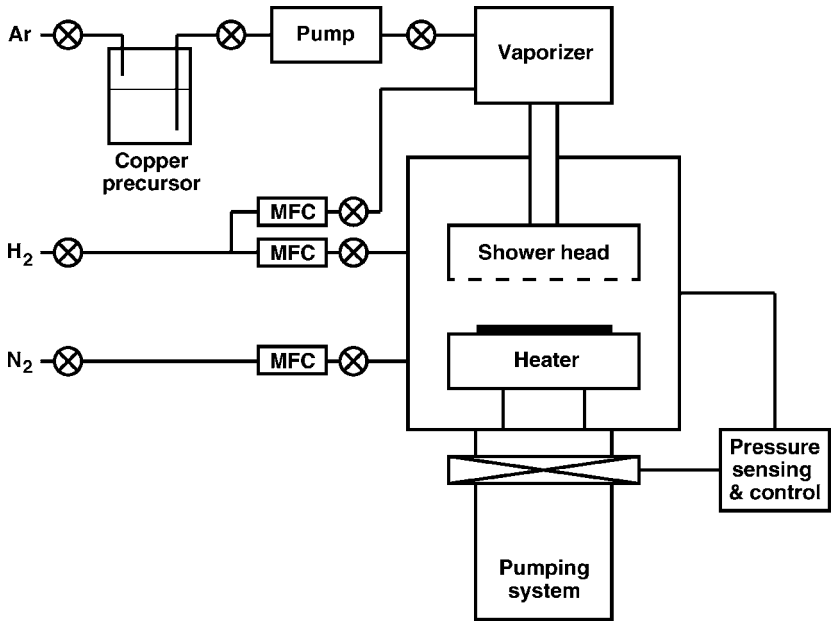


Figure 10 Cu chemical vapor deposition (CVD): schematic experimental setup.

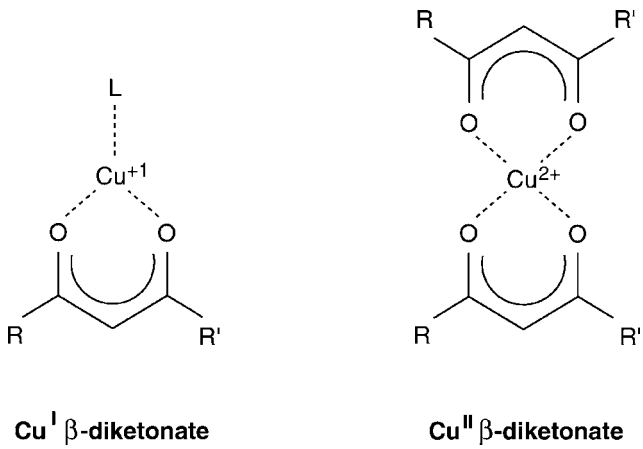


Figure 11 Examples of Cu^{I} and Cu^{II} precursors for Cu CVD.

compounds can be varied systematically by changing the size and the nature of the ligands R, R′, and L. The temperature stability also depends on the nature of the ligands. The suitability of many different compounds, obtained by substituting different ligands, has been investigated as precursors for Cu deposition.[23–27]

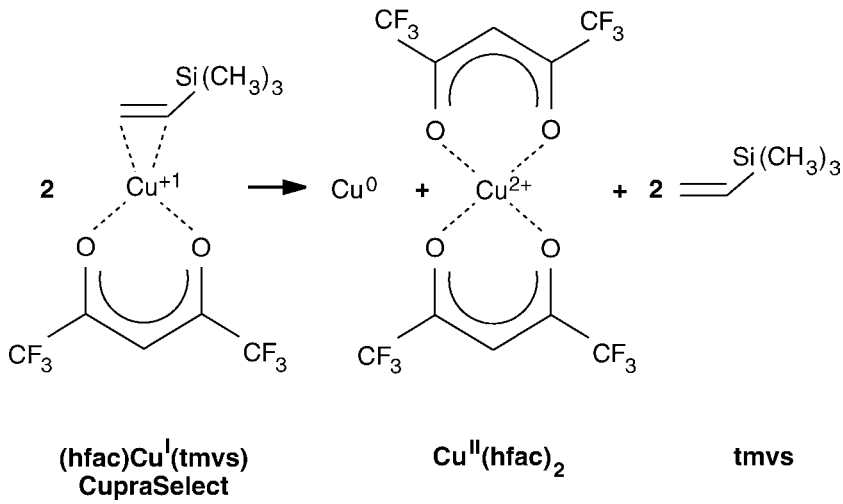


Figure 12 (hfac)Cu(tmvs) precursor and corresponding disproportionation reaction for CVD of Cu.

The two types of precursors produce Cu films through two different types of reactions. Deposition from Cu^{I} compounds occurs by a surface disproportionation reaction:

$$2(\text{hfac})\text{Cu}^{\text{I}}(\text{L}) \rightarrow \text{Cu}^{0}(\text{s}) + \text{Cu}^{\text{II}}(\text{hfac})_2 + 2\text{L}. \tag{13}$$

Note that one of the reaction products is a volatile Cu^{II} precursor, which implies that the yield of the reaction in Eq. (13) can be at best 50%. It has been argued recently that loss of the ligand L occurs to a significant extent in the gas phase and that the active precursor is really $(\text{hfac})\text{Cu}^{\text{I}}$.[28] Deposition from Cu^{II} compounds involves reduction by hydrogen:

$$\text{Cu}^{\text{II}}(\text{hfac})_2 + \text{H}_2 \rightarrow \text{Cu}^{0}(\text{s}) + (\text{COR})\text{CH}(\text{COR}'). \tag{14}$$

Various approaches have been explored to make the reactions described in Eqs. (13) and (14) more reliable and efficient, e.g., using chemical additives or a plasma enhancement. In the deposition from $(\text{hfac})\text{Cu}^{\text{I}}$(tmvs), the dissolution of the precursor in (tmvs), followed by direct liquid injection into the reaction chamber, mitigates premature disproportionation in the delivery system and gives a more stable delivery rate to the reactor.[22,29] Moreover, the addition of Hhfac ligand vapor into the reactor during deposition increases the deposition rate and improves film uniformity and smoothness.[22,29] The addition of water, either directly[30,31] or in the form of Hhfac-dihydride (Hhfac:$2H_2O$) also tends to increase the deposition

rate. Blends of CupraSelect with tmvs and Hhfac:$2H_2O$ are available commercially (e.g., 2504, with 2.5% tmvs and 0.4% Hhfac:$2H_2O$).

Introducing excitation of the reactants by a plasma has also been examined. The primary benefit of this process in the Cu^{II} reaction [Eq. (14)] is to provide a supply of free H atoms, and thus to increase the deposition rate,[21,32] since the thermal dissociation of H_2 at typical Cu deposition conditions is small and the reaction of H_2 with $Cu^{II}(hfac)_2$ is rather slow.[33] H atoms may also aid the Cu^{I} reaction [Eq. (13)] by yielding additional Cu from the secondary reaction of H with the primary reaction product $Cu^{II}(hfac)_2$. A potential side effect of too high a level of plasma excitation is the generation of fragments of the metallorganic precursor species, which may lead to the incorporation of undesirable impurities into the Cu film.[21]

For blanket Cu CVD films, fairly high deposition rates of the order of several hundred nm/min have been achieved. Because of the chemical nature of the process, precursor molecules impinge onto the substrate from all different directions. Therefore, the CVD of Cu in principal can be highly conformal. This requires, however, that the sticking coefficient of the precursor is small so that the reaction does not take place preferentially at the top of a feature. Alternatively, one may say that an adsorbed precursor molecule should have a large probability for re-emission. In addition, a large surface diffusion coefficient for adsorbed precursors is desirable. Experience has shown that in order to completely fill features with aggressive aspect ratios, the experimental conditions often have to be chosen such that the overall deposition rate is reduced considerably. Yet a process deemed manufacturable, giving a deposition rate of over 200 nm/min and capable of filling 0.3-μm vias with 2.7 aspect ratio, has been reported.[34] Further details and results regarding feature-scale deposition will be discussed in Sec. 7.4.

In the early stages of the development of copper technology, extensive efforts were being made to devise a method for selective CVD of copper.[21] The goal was to deposit Cu only onto metallic surfaces, not onto SiO_2, in order to be able to fill contact vias and trenches selectively and thus to reduce or even eliminate the use of chemical-mechanical polishing. For the Cu^{I} chemistry, the disproportionation reaction [Eq. (13)] requires transfer of an electron and was thought to be facilitated by a metal surface. The Cu^{II} reaction was believed to depend on dissociatively adsorbed hydrogen, which again would be greatly favored to occur on metals rather than on SiO_2. However, with these mechanisms in mind, a major difficulty is apparent immediately; any metal contamination on the SiO_2 surface will contravene the selective Cu deposition. Furthermore, SiO_2 surfaces are typically terminated with hydroxyl groups, which are primary sites for the adsorption of Cu precursors.[35] These sites can be passivated, and thus Cu nucleation can be suppressed, by reaction with suitable silylating agents.[31,36] Presently, selective copper deposition has not seen significant application in production because

of the successful development of the cheaper alternative of copper electroplating in combination with chemical-mechanical polishing. Moreover, it appears that Cu deposition by electroplating can lead to films with larger grains, thus alleviating electromigration concerns.

3.2.2 Electrochemical plating (ECP)

In the electrochemical plating of Cu, the reactants are provided as Cu^{+2} ions in solution, the substrate takes the role of the cathode in an electrochemical cell, and deposition occurs by the reduction of Cu^{+2} ions at the cathode. A corresponding oxidation reaction at the anode puts Cu^{+2} ions in solution and balances the electric current flow driven by the external power supply. A schematic view of an ECP reaction cell is given in Fig. 13.

If the applied potential is reversed, cathode and anode are reversed, and so are the locations where Cu deposition and dissolution occur. Alternating between deposition and dissolution, a process known as pulse plating, may be useful in order to improve the filling capability of a plated film.

The most common chemistry for the Cu ECP bath is based on $CuSO_4$ in H_2SO_4,[37,38] but other acidic baths are being investigated as well.[39] Alkaline baths

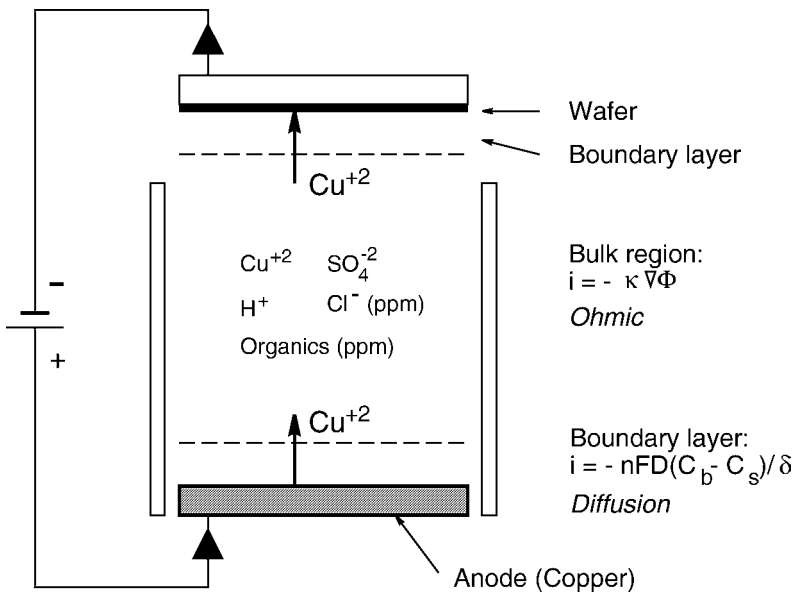


Figure 13 Schematic of electrochemical plating (ECP) cell for Cu deposition.

are also under development.[40,41] In commercial processes, proprietary organic additives to the plating solution are used in order to improve the filling of features.

ECP requires a closed loop for continuous electric current. Therefore, one cannot plate directly onto an insulator, such as SiO_2. In that case, an electrically conducting contact layer must be deposited first. This may be the eventual barrier layer, although thin barriers may have too high an electrical resistance. Otherwise a thin seed layer of Cu itself may be deposited, e.g., by CVD or by PVD. This initial conducting layer not only enables the plating to begin, but it also has a strong influence on the details of how the plated film nucleates and grows.

The ECP cell can be divided into three regions: two boundary layers near the electrodes, and a bulk region in between (Fig. 13). In the boundary layers, ion transport is governed by diffusion under the influence of a concentration gradient, whereas in the bulk region transport is essentially ohmic under the influence of the electric field. Ordinarily, conversion of Cu^{+2} ions to plated Cu atoms occurs with near 100% efficiency, so that the electric current density is a direct measure of the plating rate. Plating uniformity across a wafer is determined by ohmic effects, primarily by the current distribution.

The plating current density i is a function of the applied voltage V. A typical curve is shown in Fig. 14. When $\log(i)$ is plotted vs V, the resulting graph is referred to as a Tafel plot.[42] Three regions can be distinguished in the curve of Fig. 14. The region at low voltage, where i increases with V is the region used for ECP. At somewhat higher voltages, the current density reaches a limiting value, and at the highest voltages hydrogen evolution sets in. The potential, as the driving force behind the electrochemical reaction, governs the overall film deposition and morphology, and in particular determines the relative rates of film nucleation and growth.[37] The limiting current is a function of the mass transport in the system.

Important information regarding the nucleation and growth in ECP can be obtained from so-called chronoamperometry plots, in which a step function potential is applied to one of the electrodes and the resulting current is recorded against time. An example of such a plot is shown in Fig. 15 for the deposition of Cu onto Au(111) using a $K_2SO_4/CuSO_4$ plating bath at a fixed $pH = 4$.[38] After a brief initial delay to charge the double layer, the form of the current vs. time is determined by the competition between the formation of new nuclei and the growth of nuclei already formed. In a large number of systems, the overall process is controlled by mass transfer, which creates a growing ion-depleted diffusion zone around each nucleus, thus limiting both the formation of new nuclei and the further growth of nuclei present already. Note that the current I reaches a maximum I_m at a time t_m, depending on the applied potential (Fig. 15). Similar behavior is observed for a fixed potential step and variable pH of the plating solution.[38]

As long as diffusion zones do not overlap, nucleation normally follows a first-order rate law:

$$N = N_o[1 - \exp(-At)], \tag{15}$$

where N_o is the number of nucleation sites and A is the nucleation rate constant. Depending on the relative importance of the two reaction steps, two special cases can be distinguished.[37,43]

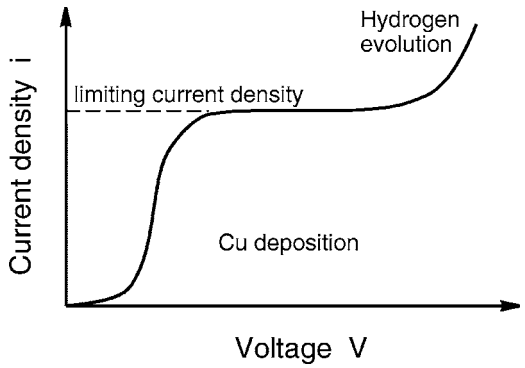


Figure 14 Typical current vs. voltage characteristic for ECP of Cu.

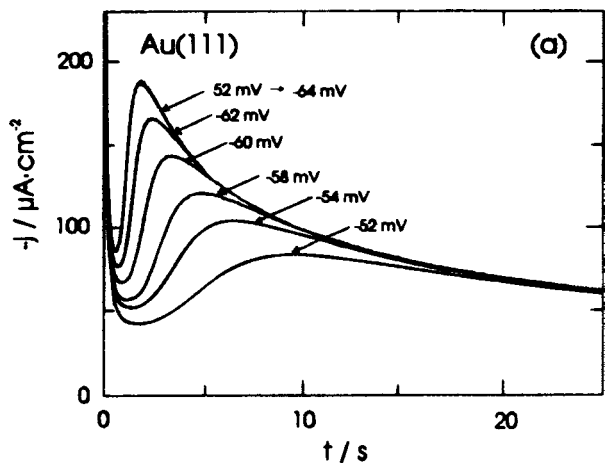


Figure 15 Typical ECP current vs. time, $I(t)$.[38]

(1) Instantaneous nucleation: $At \gg 1$, and thus $N = N_0$. Essentially all nuclei are formed at the very beginning of the process in terms of the time scale of the experiment.
(2) Progressive nucleation: $At \ll 1$, and thus $N = N_0 At \ll N_0$. Nuclei form continuously, and the number of nuclei initially increases as a linear function of time.

The growth phase depends on the shape of the diffusion zone and the growth morphology. The case of 3D hemispherical diffusion-controlled growth has been treated and modeled in detail.[43,44] Again, as long as the diffusion zones do not overlap, for instantaneous nucleation the current density is proportional to $t^{1/2}$, and for progressive nucleation the current density is proportional to $t^{3/2}$. Overlapping diffusion zones can be corrected for.[43] An example for Cu deposition on Au(111) is given in Fig. 16,[38] where the data from Fig. 15 for $(I/I_m)^2$ are plotted against t/t_m and compared to model predictions. Note that in terms of these dimensionless variables, the curve for progressive nucleation and growth is more peaked than the curve for instantaneous nucleation and growth. Hence one may conclude that in the example given the prevailing mechanism for Cu deposition is progressive nucleation. On the other hand, for a fixed potential step, the mechanism changes from progressive to instantaneous nucleation as the pH of the plating solution is decreased from 4 to 2. The mechanisms for ECP of Cu in microelectronic applications have not been characterized yet in great detail. However, there is one report of Cu deposition on TiN/n-Si(100) in an H_3BO_3/HBF_4 plating bath at pH = 1.4, which follows instantaneous nucleation and growth.[39]

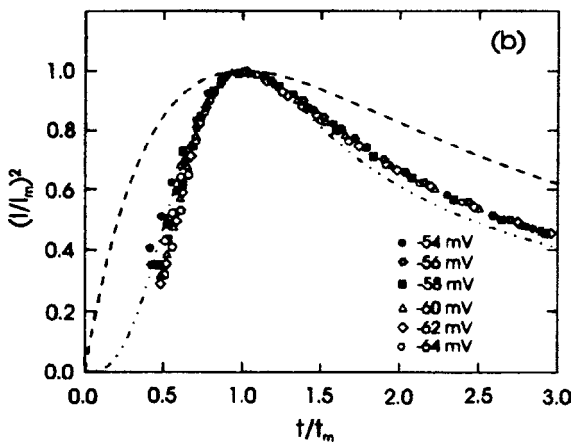


Figure 16 Typical plot of dimensionless plating current $(I/I_m)^2$ vs. dimensionless time t/t_m.[38]

In the previous arguments, issues of mass transfer limitations, nucleation, and growth were connected with Cu deposition onto an initially planar substrate. In damascene technology, however, a key problem is deposition into submicron vias and trenches, and specifically filling completely such features with metal. In that case, additional aspects of mass transfer, diffusion, and uniformity come into play due to the length scale of the features. These issues will be elaborated on in more detail in Sec. 7.4.

3.3 PHYSICAL DEPOSITION METHODS FOR COPPER

Physical deposition methods are characterized by the property that Cu atoms themselves are the "precursor" species rather than molecules containing Cu atoms as in CVD. The traditional physical methods have been evaporation and sputter deposition (Fig. 17). Compared to CVD, a key difference is that Cu atoms, and metal atoms in general, are not really volatile. Instead, they are highly reactive and have a very high sticking coefficient on most any substrate. This points immediately to the filling of high-aspect-ratio features in the ILD as the major issue with physical deposition methods. Due to line-of-sight conditions and high atomic reactivity (i.e., essentially unity sticking coefficient), Cu atoms will tend to deposit preferentially near the top of a feature, where their flux is highest, leading to quick closure of the feature at the top and a keyhole below (Fig. 18, [54]) (see also[45]). Therefore, the features do not get filled completely, and the void inside the metal constitutes a reliability risk.

In sputter deposition for Al technology, this drawback can largely be overcome by increasing the substrate temperature, thus increasing the surface mobility of the deposited Al atoms. Features with modest aspect ratios can be filled using this method. But the same method cannot be carried over to the deposition of Cu, since this would require too high a substrate temperature. Another way by which the via-filling problem can be mitigated somewhat in sputter deposition is to apply re-sputtering to the substrate.[45] When the substrate is made into the cathode and is being sputtered itself, metal is removed preferentially from the top areas of the features, where there was extra deposition, and is redistributed generally inside the feature. By alternating between sputter deposition and re-sputtering, the filling of features can be improved.

With Cu, two other approaches have been shown to be feasible (Fig. 17). These rely on the Cu atoms being highly directional, impinging on the substrate primarily along the normal direction. One type of implementation of this principle has been realized in collimated or long-throw sputter deposition. Here features are filled with metal from the bottom up, as the deposition rate on the vertical sidewalls is greatly decreased relative to the bottom, horizontal surface of a feature. The other type of implementation is represented by ionized physical vapor deposition

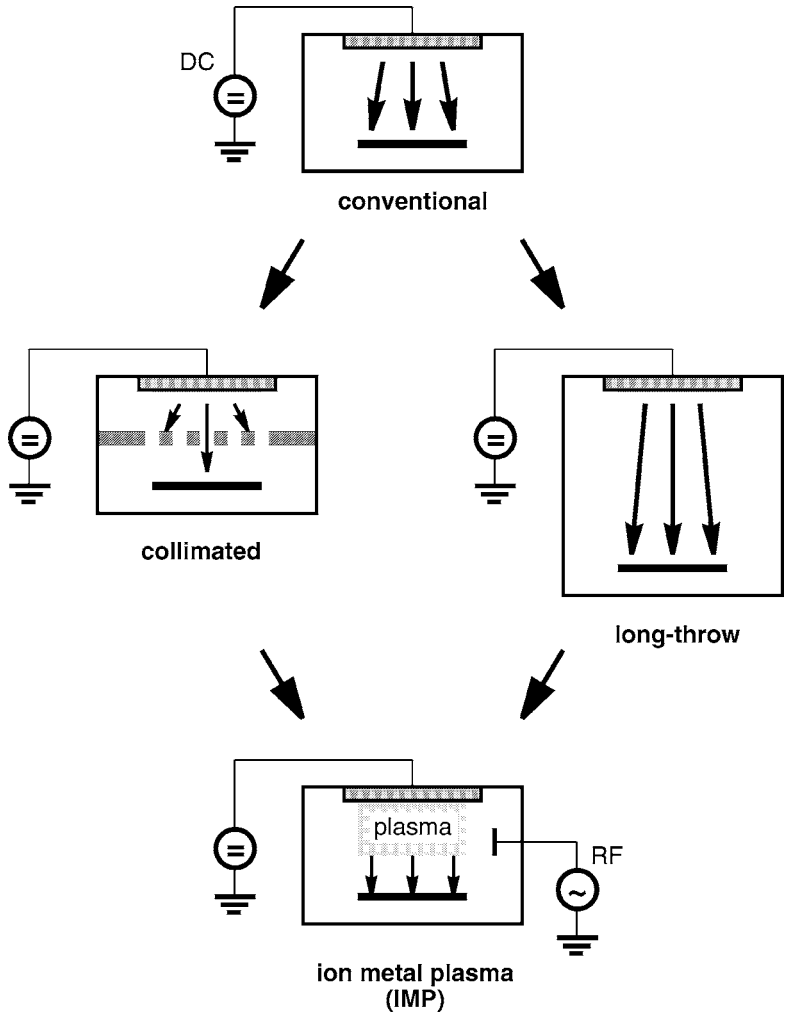


Figure 17 Experimental trends in physical vapor deposition (PVD) of metals.

(IPVD). This method again makes use of a form of re-sputtering, but in order to produce more conformal metal coverage and hence better via filling.

3.3.1 Collimated and long-throw sputter deposition

In collimated sputter deposition, a mechanical type of grid between the sputtering target and the substrate filters out metal atoms moving in off-normal directions and lets pass through only atoms moving more or less along the substrate normal

direction.[46,47] As mentioned above, this reduces deposition onto the sidewalls of features and the formation of overhangs at the top edges of features. The problem with the method is that it also reduces the overall deposition rate considerably, thus making the process rather slow. In addition, an unavoidable side effect of the filter action is deposition of atoms onto the filter itself. Therefore the transmission of the filter, and with it the deposition rate, decreases in the course of time.

In long-throw sputter deposition,[47–49] the effect of directionality is achieved by placing the sputtering target at a much larger distance from the wafer than in normal sputter deposition. This reduces the spread of incident angles of the atoms by reducing the effective size of the sputtering source, but in order to work as desired, the process must be maintained at a low enough pressure so that the metal atoms do not undergo any collisions on the way from the sputtering target to the substrate. The end effect, once again, is a reduced overall deposition rate.

The results of both collimated and long-throw sputter deposition can be interpreted in common terms, in the sense that they reduce the practical effective size of the source. Simulations have exemplified the effects of the feature aspect ratio and the target aspect ratio (source-to-substrate distance/source diameter) on via filling.[50]

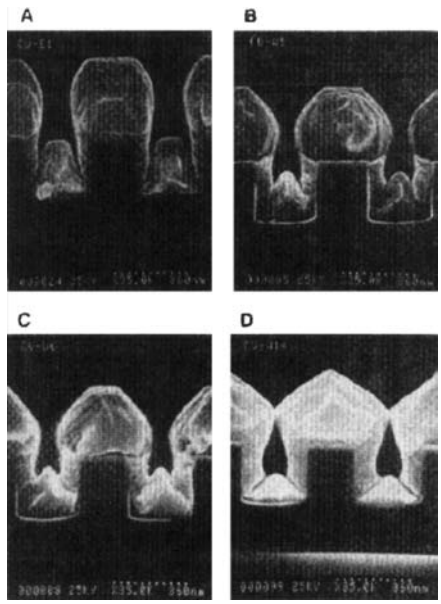


Figure 18 Formation of keyhole in metal when deposition is not conformal.[54] IPVD of Cu onto patterned SiO_2 (magnetron sputter deposition with post-ionization: magnetron power = 300 W, RF power = 1 keV, Ar pressure = 30 mTorr, deposition time = 24 min). Sample DC bias: a) −5 V, b) −20 V, c) −30 V, d) −50 V.

3.3.2 Ionized physical vapor deposition (IPVD)

In all variations of IPVD, the depositing species are not only directional but also carry extra kinetic energy beyond the normal thermal energy. This means that the approach combines aspects of species directionality and continuous re-sputtering, with the result that metal deposition into features is much more conformal, and via filling is improved greatly. This principle is illustrated in Fig. 19.

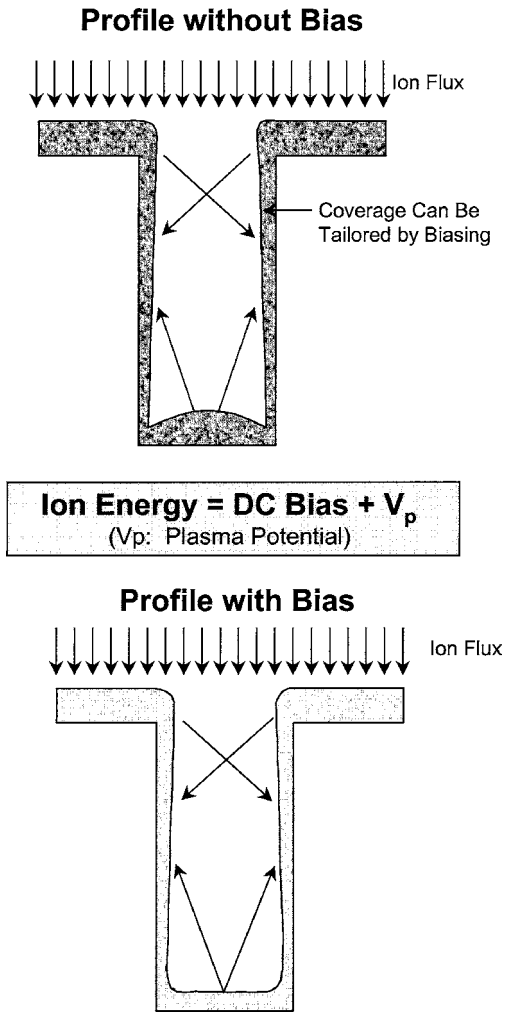


Figure 19 Metal deposition without and with wafer bias in ionized physical vapor deposition (IPVD).

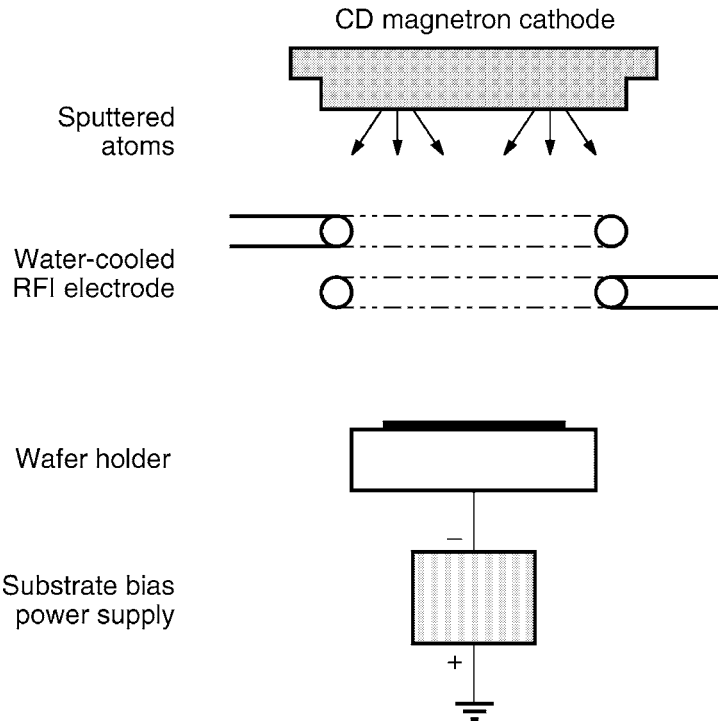


Figure 20 Experimental setup for magnetron sputter deposition with RF post-ionization.[54]

The earliest form of IPVD was termed partially ionized beam deposition (PIB). This involved thermal evaporation of metal atoms, followed by electron impact ionization of a small fraction of the evaporated species.[51,52] A potential bias of the order of 1 kV was applied between the source and the substrate, serving to impart directionality as well as substantial kinetic energy to the metal ions. This extra energy—a small fraction of the metal flux arriving at the substrate, was enough to prevent preferential deposition at the top of features and to allow successful filling of fairly high-aspect-ratio vias.

More recently, post-ionization of evaporated Cu atoms was achieved using an electron cyclotron resonance (ECR) discharge.[53] In this case, a large fraction of evaporated atoms ended up being ionized, so that in essence a Cu vapor plasma was being maintained. The potential bias between source and substrate was of the order of 50 V. Again, the net effect of the ionized metal flux to the substrate was much better via filling compared to conventional evaporation.

The most promising varieties of IPVD, at present, appear to be based on variations of magnetron sputter deposition which include some form of post-ionization.

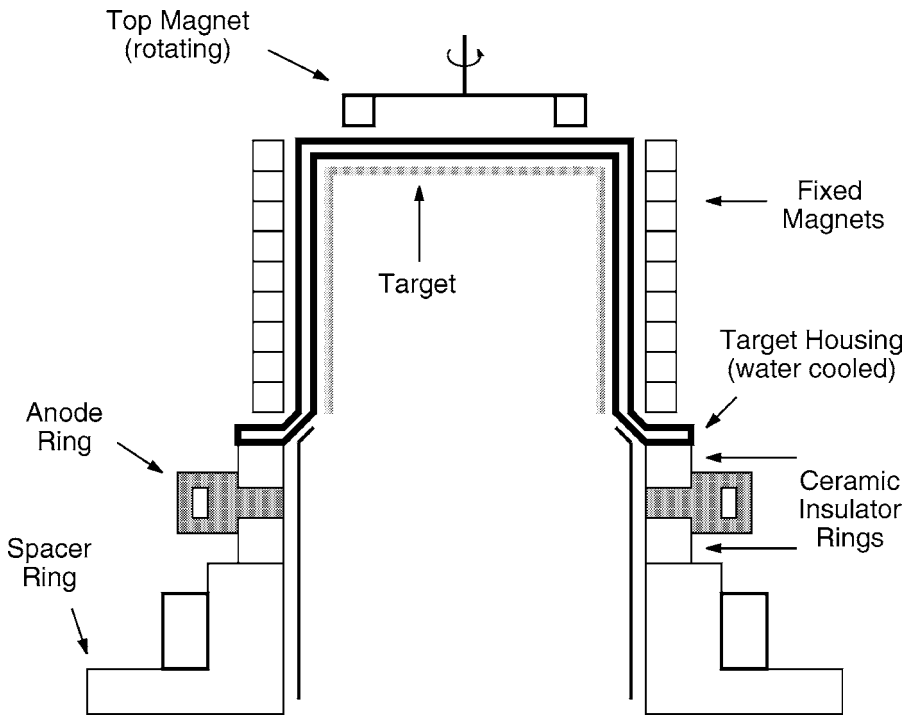


Figure 21 Experimental setup for hollow-cathode magnetron sputter deposition, redrawn schematically from [270].

The metal flux is generated from a magnetron target, and ionization of a fraction of these metal atoms is effected either by additional rf excitation[54–56,262] or by a special design of the magnetron source (e.g., a hollow-cathode magnetron).[57,58] The former situation has also been referred to as ion metal plasma (IMP) deposition, which has been developed and commercialized for a number of different applications.[263] An rf ionization setup is illustrated in Fig. 20 and a hollow-cathode magnetron setup in Fig. 21.

An example of results for Cu deposition with an rf ionization setup is given in Fig. 22.[54] Here the experimental conditions are chosen such that deposition at the bottoms of features is favored over deposition at the sidewalls. The extent to which this occurs depends on the gas pressure and the Cu ion energy at the substrate. The latter, in turn, is a function of the plasma potential and the substrate bias (see Fig. 19). Note that there is no overhang of Cu at the top, so that the features are filled very well. The main question with regard to IPVD of Cu is under what conditions and up to what aspect ratio features can be filled properly.

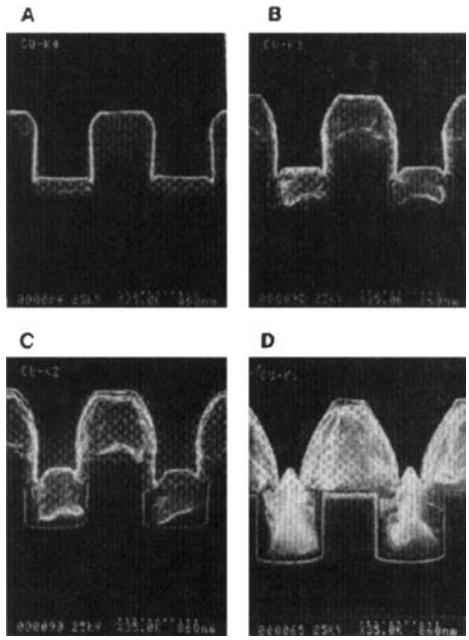


Figure 22 IPVD of Cu onto patterned SiO_2 (magnetron sputter deposition with post-ionization: magnetron power = 300 W, RF power = 1 keV, Ar pressure = 45 mTorr, sample DC bias = −12 V).[54] Scanning electron micrographs show time evolution of deposited film.

IPVD under conditions favoring conformal deposition has also been used successfully to deposit thin barrier layers.[57–59] This may well turn out to be one of the most important application of IPVD in practice (see Chapter 7 for additional information on this point).

4

COPPER PATTERNING

4.1 OVERVIEW

As we outlined in Sec. 3, there are two basic approaches to patterning for the purpose of creating multilevel interconnect structures. To put it in the simplest terms: The traditional, subtractive approach consists of patterning the metal by dry etching, filling the gaps in the metal pattern with ILD, and planarizing the ILD. The new damascene approach consists of patterning the ILD by dry etching, filling the features in the ILD with metal, and planarizing the metal by chemical-mechanical polishing (CMP). In this section, we will describe both approaches as they apply to Cu interconnect technology. The damascene approach is in the process of being adopted for mainstream applications with SiO_2 as the ILD, but new developments continue to be made with the subtractive approach.

4.2 SUBTRACTIVE COPPER PATTERNING

Here the key step is the fine-line patterning of Cu by anisotropic dry etching in a plasma, although some patterning of the ILD is involved as well. The dry etching of the Cu should be done to able to be done under conditions that are compatible with other processes and the materials present on the wafer. This presents unique difficulties with Cu, in contrast to Al. The major one of these difficulties is that common plasma chemistries yield reaction products with only marginal volatility. This fact can be appreciated by comparing the vapor pressures of potential etch products from typical halogen plasma chemistries. The following are estimates, based upon thermodynamic data,[60] for chlorinated products at room temperature:

Metal	Product	Vapor Pressure
Al	Al_2Cl_6	10^{-4} Torr
Cu	Cu_3Cl_3	10^{-8} Torr
	CuCl	~ 0

Products with other halogens tend to have lower vapor pressures yet. This implies that Cu plasma etching will require an elevated substrate temperature.

It should be noted that nonhalogen-based chemistries similar to those employed in CVD of Cu have been shown to form volatile Cu products at much

lower temperatures.[61,62] However, a dry etch process must not only yield volatile products at a useful rate, but it must allow, at the same time, for highly accurate pattern transfer. The non-halogen chemistries, relying on thermal processes, produce isotropic etching with rather poor pattern definition. On the other hand, sub-micron patterning requires highly anisotropic etching, which occurs only in the presence of ion bombardment of the substrate.[63] None of these chemistries have been implemented under those types of conditions.

The second difficulty with the subtractive patterning of Cu, which is a consequence of the high substrate temperature, relates to the masking technology used in the microlithography. Halogen plasmas present a rather aggressive environment at the substrate temperatures necessary, and normal photoresists are generally not stable enough under these conditions, so that nontraditional approaches to masking need to be sought.

Yet another issue following from the use of a halogen chemistry, and aggravated by high substrate temperature, is the potential corrosion of exposed metal by reaction by-products which were removed incompletely.

4.2.1 Reactive ion etching of copper

Reactive ion etching (RIE) refers to a reactor geometry in which the etching plasma is maintained as a parallel-plate, capacitively coupled rf discharge. The substrate is placed on the rf-driven electrode, which develops an induced dc bias potential and thus acts as the cathode. Hence the substrate is subject to bombardment by energetic ions from the plasma.[63]

It was realized early on that useful etch rates for Cu require a substrate temperature of about 200°C.[64] At lower temperatures, no etching occurs but rather a layer of Cu-chloride grows on top of the Cu film.[65] Schaible and Schwartz were able to obtain etch rates up to 500 nm/min in a CCl_4/Ar plasma.[64] Ashing of photoresist exposed to the etching plasma resulted in the formation of a thick black layer on the surface of the Cu. Therefore MgO was chosen as a hard mask. Etching was highly anisotropic under these conditions. With SiO_2 as a hard mask, etch by-products tended to attack the copper.

Later studies using BCl_3-based plasmas provided further details regarding the temperature dependence of the Cu etch rate and the etch mechanism in general.[66,67] The etch rate increases rapidly with the temperature at around 200°C but then levels off. This indicates that at higher temperatures the etch rate is limited by the supply of reactants, presumably Cl atoms, which depends strongly on the gas composition (Fig. 23). The addition of N_2 to BCl_3 is particularly effective in increasing the etch rate, in contrast to the addition of Ar. Optical emission spectroscopy confirms that the role of the N_2 is to enhance the production of Cl atoms in the plasma.[66,67] Although the etch selectivity of Cu relative to polymers is not

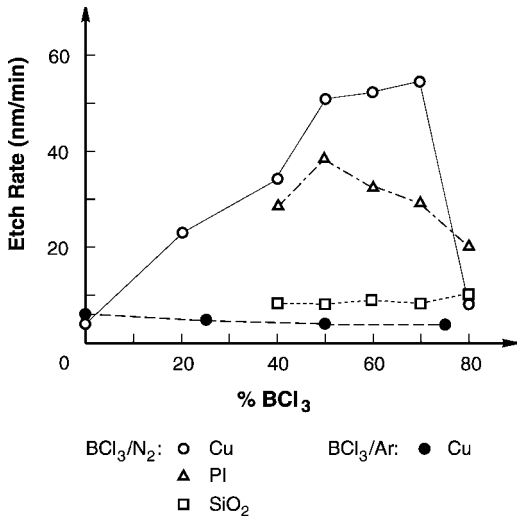


Figure 23 Etch rates in reactive ion etching (RIE) of Cu RIE vs. gas composition: pressure = 50 mTorr, DC bias = −300 V, wafer temperature = 250°C.[66]

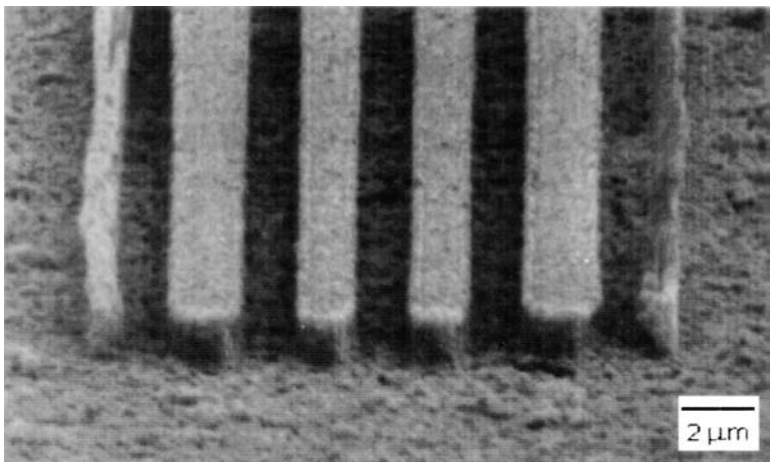


Figure 24 Pattern definition in Cu RIE using polyimide mask: flow rate ratio $BCl_3/N_2 = 50/50$, p = 50 mTorr, DC bias = −300 V, wafer temperature = 250°C.[66] Note the two narrow lines on both sides with a width of about 0.4 μm.

very large, sub-halfmicron anisotropic patterning can be achieved with a polymide mask that holds up well enough under exposure to the plasma at the elevated temperature (Fig. 24).

4.2.2 Etching of copper in high-density plasmas (MIE, ECR, ICP)

Even under optimum conditions, the etch rates attainable in RIE are rather low, typically less than 100 nm/min. Such rates are too small for economical single-wafer processing. The low etch rates can be attributed to correspondingly low plasma densities, i.e., low concentrations of ions and reactive neutral etchants. Various attempts have been made to obtain increased etch rates by using higher-density plasmas.

Magnetron ion etching (MIE), as an extension of parallel-plate RIE, represents one approach to enhancing the plasma density. A magnetron geometry is used for etching, whereby a magnetic field parallel to the electrodes is set up either by permanent magnets embedded inside the rf-driven electrode or placed near the counter-electrode, or by electromagnets outside the reactor (see for example[68]). This field forces the electrons to follow spiral paths along the magnetic filed lines. This effect confines electrons more strongly to the discharge volume than does a simple capacitive parallel-plate geometry, thus making the electrons more efficient in exciting and ionizing gaseous species.

With the MIE approach, Cu etch rates as high as 300 nm/min have been achieved in a $SiCl_4/N_2$ plasma.[67,69] Optical emission spectroscopy allowed the identification of chemical as well as physical etch products (CuCl vs. Cu) (Fig. 25).

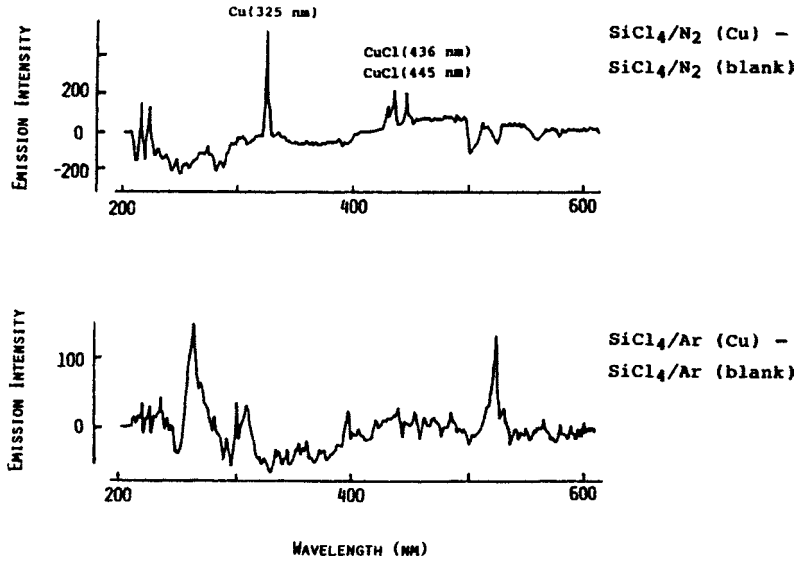


Figure 25 Optical emission spectra of $SiCl_4/N_2$ and $SiCl_4$/Ar plasmas in magnetron ion etching (MIE) of Cu.[69] Note reaction product CuCl with $SiCl_4/N_2$, but not with $SiCl_4$/Ar.

Moreover, the difference between plasmas with N_2 and with an Ar addition was again demonstrated, in that with a $SiCl_4$/Ar plasma no chemical etch products were observed (Fig. 25).

In another application of MIE, Cu was not only patterned anisotropically, but passivation of the sidewalls was achieved simultaneously in situ.[68] (Note that sidewall passivation is a general requirement in a technology employing subtractive patterning of Cu). The metal film was in fact a TiN/Cu/TiN stack, the mask was SiO_2, and the gas mixture contained $SiCl_4$, Cl_2, N_2, and NH_3. During the etching of the horizontal Cu surfaces, this particular plasma chemistry caused a film to be formed on the near-vertical sidewalls of the Cu profile (Fig. 26). This film presumably consisted of SiON and prevented the incorporation of Cl into the Cu.

An example of obtaining increased Cu etch rates has been reported using electron cyclotron resonance (ECR) etching.[70] In this work, Cu etch rates up to about 600 nm/min were obtained with an etch gas of Ar/Cl_2 at a typical composition of 1/2 and a substrate temperature of 200°C. Anisotropic features the size of several-microns were made using a photoresist mask. Post-etch, in situ cleaning in a H_2 plasma produced Cl-free etched surfaces showing no corrosion. Very recently, sub-halfmicron features have been fabricated using a chlorine-based process and a SiO_2 hard mask. Etch rates were also about 600 nm/min, but no process details were given.[256] Ye et al. also pointed out the importance of a proper post-etch treatment for the prevention of Cu corrosion.

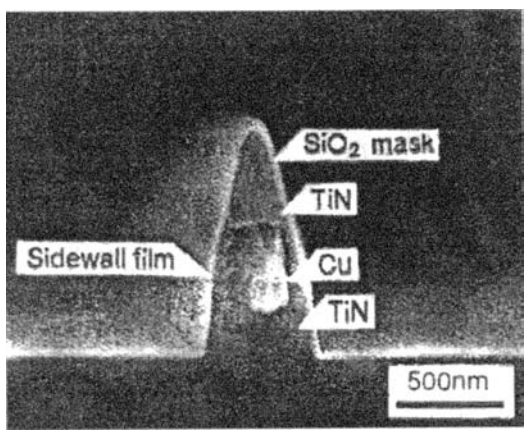


Figure 26 Cu pattern obtained with MIE using $SiCl_4/Cl_2/N_2/NH_3$ gas mixture:[68] Note in-situ passivation by film on sidewalls of Cu profile.

4.2.3 Radiation-enhanced RIE of copper

Even though etching of Cu with enhanced discharges has achieved markedly larger etch rates than conventional RIE, it still requires the same kind of elevated substrate temperature in order to ensure sufficient volatility of the etch reaction products. However, it turns out that if the Cu substrate is subject to additional radiation during etching, this temperature can be reduced substantially.

The effect of radiation-enhanced etching was first demonstrated using infrared (IR) radiation in a regular parallel-plate reactor[71] (see Fig. 27). A careful examination of the etch rate dependence on temperatures on one hand and on the IR radiation intensity on the other hand showed that the phenomenon is not thermal. Apparently, the radiation increases the volatility of surface etch products by photochemical excitation. This was related to the known strong IR-activity of solid CuCl.

Very recently, a similar effect has been reported in a reactor combining exposure of the Cu substrate to ultraviolet (UV) radiation with etching in a high-density, inductively coupled Cl_2/N_2 or Cl_2/Ar plasma.[72] The UV radiation lowered the activation energy for copper etching from 1.6 to 1.12 eV, thus enhancing CuCl desorption and making it possible to perform etching at low temperatures. An etch rate of about 300 nm/min was achieved even at room temperature. Since the etch

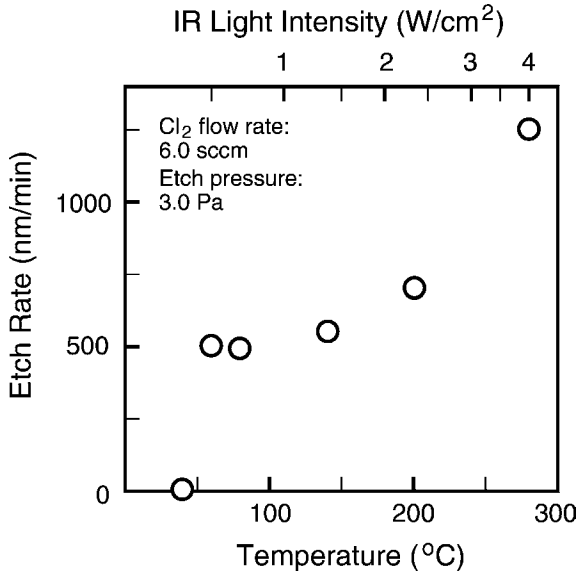


Figure 27 IR-enhanced reactive ion etching of Cu.[71] Sample temperature required for etching is much lower in the presence of IR radiation.

rate increased almost linearly with increasing ultraviolet light intensity, it was suggested that the enhanced etching was not a simple thermal process, but rather was promoted by photodesorption of CuCl due to the ultraviolet irradiation. The exact mechanism of how this occurs is not known at present. Furthermore, what remains to be seen is whether anisotropic patterning with these kinds of etch rates is possible under such radiation-enhanced conditions.

4.3 ADDITIVE COPPER PATTERNING BY CHEMICAL-MECHANICAL POLISHING (CMP)

In light of the difficulties in patterning Cu by subtractive dry etching, the damascene approach, as described in general terms in Chapter 2, has gained favor recently and is being implemented in production. It is part of the announced processes mentioned earlier[4–6] with Cu and SiO_2. It has also been used in a Cu/polyimide technology where the ILD is a three-layer Si_3N_4/BPDA-PDA/Si_3N_4 stack[73] and with Cu in combination with other polymer ILDs such as benzocyclobutene and parylene-n.[17,74–76]

The important process steps are detailed in Fig. 28 (see also Fig. 8). The interconnections, including contact vias and trenches connecting vias, are formed entirely in the ILD as an inlaid pattern by dry etching. A thin conformal barrier

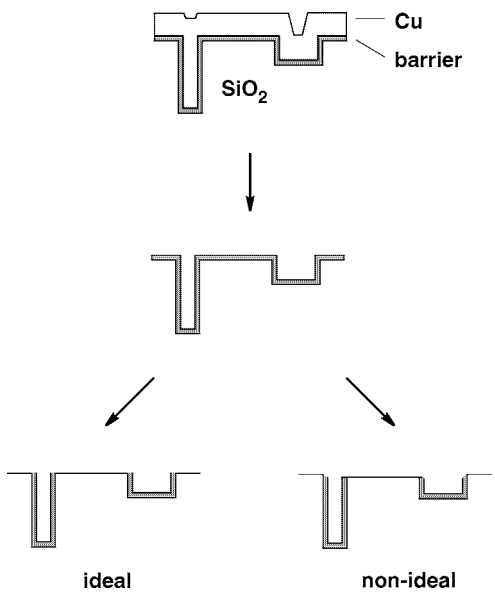


Figure 28 Principles of chemical-mechanical polishing (CMP) of Cu.

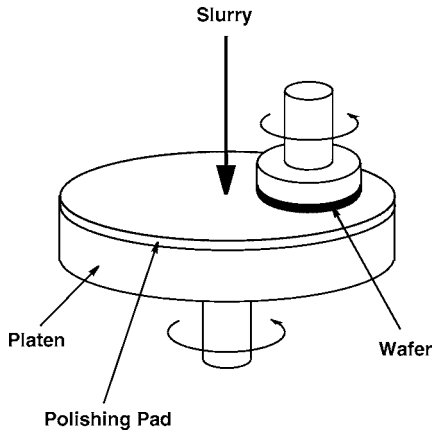


Figure 29 Schematic of experimental CMP setup.

layer is then deposited, and the features in the ILD are filled with Cu. Finally, the excess Cu and the horizontal portions of the barrier layer on top of the ILD are polished away by chemical-mechanical polishing (CMP) to yield a planar surface. A schematic of an experimental CMP setup is shown in Fig. 29. Note that the exposed top surfaces of the Cu connectors have to be covered with another barrier layer before the next ILD layer is deposited (Fig. 8).

The CMP technique makes use of a multi-component slurry consisting of an abrasive, acids or bases, surface modifiers, and a surfactant. The polishing is the result of the combined action of the mechanical abrasive, causing surface strain and damage, and the chemicals in the slurry dissolving strained surface material. In metal polishing, CMP is thought to remove areas of metal in direct contact with the pad (see Figs. 28 and 29), whereas other recessed areas not making such contact are passivated by the slurry.[77,78]

The material removal rate in CMP depends on many experimental variables, e.g., on slurry chemistry, slurry pH, nature of abrasive particles, polishing pad, polishing speed, pad pressure, etc. To a first approximation, the removal rate can be represented by Preston's equation as

$$(\Delta H/\Delta t) = K_p(L/A)(\Delta s/\Delta t), \tag{16}$$

where $\Delta H/\Delta t$ is the removal rate expressed in terms of the change in height of the material per unit time, L is the loading force applied over the entire surface with area A, $\Delta s/\Delta t$ is the speed of the pad relative to the sample, and K_p is Preston's coefficient. Equation (16) assumes that the removal rate is proportional to the applied pad pressure L/A and the relative pad speed.

Deviations from behavior as described by Preston's equation have been observed under a variety of circumstances, and corresponding modifications to the equation have been proposed. The removal rate is not always proportional to the relative pad speed.[79,80] Also, a threshold effect with respect to pressure has been noted where a measurable removal rate requires a certain minimum applied pressure, and where there is no removal at all below that threshold pressure.[81]

The main metals studied in CMP have been W, Al, and Cu. W and Al are the primary materials in Al interconnect technology, and their CMP behavior is relevant mostly to the extent that when the end point of the planarization of $SiO_2$is reached, some CMP of the metals will also take place. (However, see Refs. [82–84] for examples of CMP of W and Refs. [85,86] for CMP of Al).

The major difference between the CMP of Cu and the other two metals is how the acidity or alkalinity of the slurry affects the material removal. Cu forms oxides at pH > 7 but etches in acidic solutions, whereas W is passivated at pH < 4 and Al at pH between 4 and 8. Consequently, the two main slurry systems used for the CMP of Cu, NH_4OH-based and HNO_3-based, work differently. With NH_4OH, the high pH causes Cu-oxide to form, which gets abraided and then dissolved by the ammonia. With HNO_3, a corrosion inhibitor or an oxidizer added to the slurry passivates those parts of the Cu (i.e., the low parts) not in direct contact with the pad, whereas the high parts, in contact with the pad, are kept free of passivation and are etched by the slurry. Moreover, Cu oxides tend to be softer than Al or W oxides and thus provide less effective passivation.[76]

Many of the issues important in the removal of material by dry etching are also relevant in CMP. One of these issues is selectivity of removal rates. In the first step shown in Fig. 28, once the horizontal portions of the barrier layer are reached, two rather different materials need to be removed at the same rate. Hence, at this point no selectivity between the barrier and the metal would be desirable. As a result, two-step processes have been developed for the individual films. On the other hand, once the ILD is reached after the second step in Fig. 28, high selectivity for Cu and the barrier relative to the ILD is required, so that the barrier layer is completely removed everywhere on the ILD.

Another important issue in CMP is uniformity of material removal. To a certain extent the process is self-regulating in that high points on the substrate will experience a higher pad pressure and thus will be eroded more quickly [Eq. (9)]. Uniformity across the wafer is a function of the global uniformity of the pad pressure. This can be improved markedly using an air-pressure-backed carrier for the wafer, with additional corrective pressure applied mechanically along the wafer edge.[87]

An additional, closely related issue is illustrated in Fig. 28, namely the planarity of the polished substrate, which should be maintained locally between different materials and globally across the entire wafer. The non-ideal panel in Fig. 28

shows the phenomenon known as dishing, whereby inlaid metal areas are left non-planar. This can occur when the Cu and the ILD or the barrier are not removed at the same rate. For example, with an ammonia-based slurry, dishing of Cu on patterned wafers is strongly dependent on the width of the Cu lines but is only minimally dependent on the density of the Cu lines. The opposite is true for the removal of SiO_2 between Cu lines, which depends more strongly on pattern density than on the width of the Cu lines (Fig. 30).[88] On the other hand, with a fixed pattern density of 50%, the local oxide erosion is a function of the line width. Interestingly, for 1- and 10-μm wide oxide lines, the local erosion is less than for the field oxide, whereas for 50- and 100-μm wide oxide lines, it is more than for the field oxide.[255] Strong dishing versus pattern density and line width have also been reported for the CMP of Cu on polyimide in a nitric-acid-based slurry.[76] The addition of glycerol to increase the slurry viscosity reduced the dishing effect, pre-

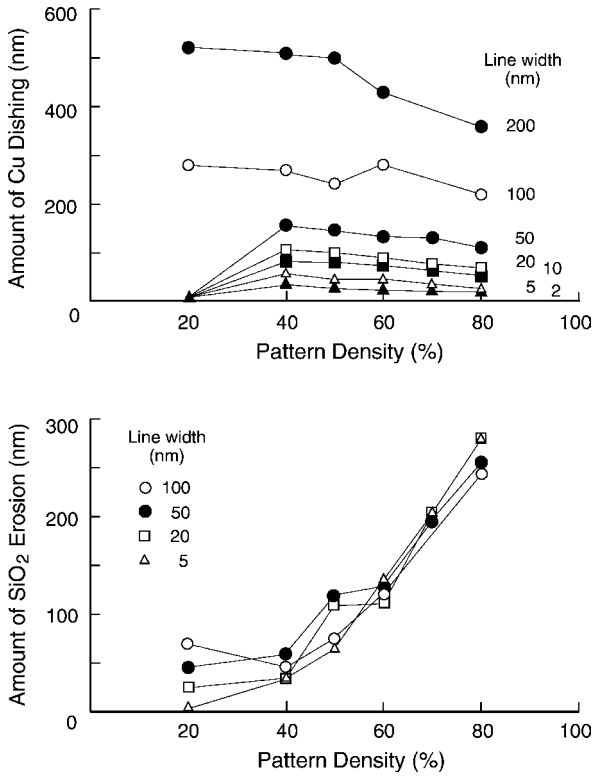


Figure 30 Metal dishing and ILD erosion vs. pattern density (redrawn from Ref. [88]). Cu lines of fixed width and varying density on 100 nm Ti on SiO_2. Initial Cu thickness of 2 μm.

sumably by reducing the motion of the abrasive particles.[76] Overall, dishing is less severe for smaller features and higher pattern density.

One of the most difficult problems in Cu CMP is monitoring material removal rates in real time, and especially end point detection [i.e., detecting the point when all the barrier material has been removed (Fig. 28)]. The reason for this is that the surface of the wafer being polished is not directly accessible to any probes. An indirect approach has been to follow the electric current to the driving motor. Because the frictional conditions between the pad and the wafer are strongly material dependent, a change in driving motor current can be detected when the polishing process reaches the interface between two materials. A method monitoring directly the edge of the wafer with a combination of different measurements has also been reported.[89] Very recently, an in-situ optical interferometric method has been implemented in a commercial polisher. A laser beam is directed at the wafer being polished through an opening in the platen and polishing pad. The method records the reflectance change upon removal of the metal film and is said to provide accurate real-time end-point detection.[254] End-point detection methods for CMP have been reviewed recently.[90]

Very recently, a new approach to Cu CMP has been proposed with an inverse geometry compared to the standard one shown in Fig. 29. The new approach has been termed PASCAL-CMP (for *pad-sca*nning local CMP).[245] It involves the rotating wafer facing up and a small oval pad polishing the wafer from the top. The pad position is scanned across the wafer, and high speed rotation of the pad at low pressure is said to be the key factor in suppressing Cu thinning by oxide erosion and achieving low Cu dishing.[245]

5

INTERLAYER DIELECTRICS

We now proceed to an examination of issues directly pertinent to the other component of an interconnect scheme, the interlayer dielectric (ILD). The first requirement for an ILD is a low dielectric constant k, but in our general discussion in Sec. 2.2 we have listed other materials properties that are necessary for a low-k ILD to be viable. Let us mention two specific areas of concern: mechanical stability and thermal conductivity of the ILD. In the context of low-k ILD candidates to replace SiO_2, one should keep in mind that polymers typically are much less strong than SiO_2 and less adherent to themselves or to other materials.[7] Furthermore, the thermal conductivity of polymers is typically a factor of 5 lower than that of SiO_2,[8] and the coefficient of thermal expansion (CTE) of polymers is typically an order of magnitude larger than that of Si.[7,91] Analogous differences in materials properties would apply to silicate-based materials with a lower density than SiO_2.

From our earlier discussion it is also clear that, ideally, the metal conductors should be surrounded completely by low-k ILD [Eqs. (4) and (5)]. If that cannot be realized, then substantial benefits can still be achieved if the spaces between high-aspect-ratio metal lines and vias are filled with low-k ILD.

A few possible architectures to implement these goals are illustrated schematically in Fig. 31, showing metal structures (two vias, a via with a metal line on top, and a metal line by itself) that may occur in different parts of the interconnect layer. In order to be specific, we take the layers shown to represent metal 1 and ILD 1, but the same principles apply to the upper levels of the interconnect scheme. Note that, for simplicity, barrier layers are not shown in Fig. 31. Also, the reader should review Figs. 5 and 6 for an abbreviated sequence of processing steps leading to the situations described in Fig. 31.

The first panel in Fig. 31, where the metal is embedded entirely in the ILD, depicts the ideal situation from the point of view of reducing all components of the RC delay, but it also presents the most difficulties in processing and integration. Specifically, in this case the low-k ILD must be able to withstand the stresses of planarization by CMP, and it must have sufficient thermal conductivity to allow dissipation of the heat from the Si substrate through the interconnect structure and the device package to the ambient. In the second panel of Fig. 31, the low-k ILD still surrounds the metal but has been capped by a layer of SiO_2. Here the SiO_2 reduces stresses on the ILD caused by CMP, and it also improves the thermal conductance in the vertical direction. The line-to-line capacitance would be nearly as

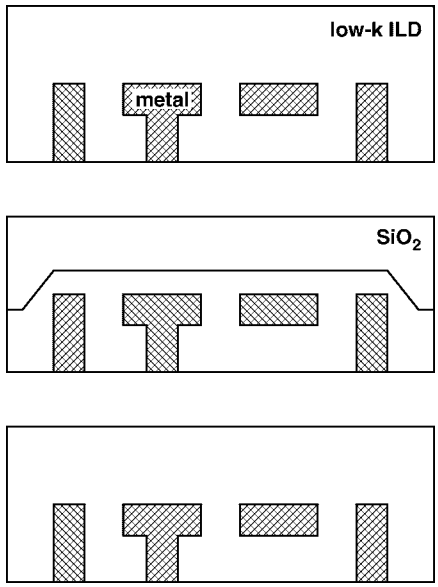


Figure 31 Low-*k* ILD architectures.

low as in the top panel, but the layer-to-layer capacitance would be increased somewhat. The third panel of Fig. 31 shows a situation where the low-*k* ILD is found only between metal features. This case would provide the greatest mechanical and thermal stability and ILD interfacial strength. At the same time, it would still bring about a substantial line-to-line capacitance reduction, but this would come at the cost of further increased vertical capacitance and increased process complexity (an additional etchback step to remove the low-*k* ILD outside of the metal lines).

Note that, in principle, the arguments above can be applied whether subtractive or damascene patterning has been employed in building these interconnect structures. However, in practice a particular structure may be realized more easily with one or the other approach. For example, with the damascene approach the most natural implementation would be the fully embedded case in the top panel of Fig. 31, whereas etchback would appear to be more readily compatible with the subtractive approach.

Below we will discuss various types of materials under investigation as low-*k* ILDs. We will follow the scheme outlined in Sec. 2.3, distinguishing two classes of materials (silicate-based and carbonaceous polymeric), and whether or not the materials are doped to a significant degree with other elements. We will begin with the deposition and the properties of these materials, and we will conclude the section with an examination of the patterning of ILDs for interconnect

structures, particularly as it relates to the damascene approach. We will reserve the discussion of specific interface issues between an ILD and Cu and/or a barrier material for Chapter 6 below.

5.1 SILICATE-BASED ILDS

5.1.1 Undoped Si oxides

5.1.1.1 Nanoporous silica

With this type of material, the low k is achieved by introducing porosity into what is fundamentally silicon dioxide.[10,92] The dielectric constant is reduced proportionately to the porosity (the volume fraction of pores) or, equivalently, increases proportionately to the density. The linear dependence of k on density is described well by an electrical parallel-circuit model.[92] This means that the dielectric constant can easily be tailored by proper processing for the corresponding material density.

The processing of nanoporous silica is similar to that of spin-on glasses. A liquid precursor film, typically based on tetraethoxy-silicate (TEOS), is spun onto the substrate and then subject to controlled gelation and drying. In the gelation step a continuous solid network is formed. Drying can be performed under supercritical conditions (in which case the resulting material is sometimes referred to as an aerogel) or by controlled solvent evaporation (in which case the resulting material is sometimes referred to as a xerogel). In either case, the main difficulty is to prevent the material from shrinking during the drying step so that cracking and delamination on a patterned wafer can be avoided. The best approach seems to be to permit shrinkage only before gelation and to fix the material density by the solvent concentration at the gel point.[92] The average pore size in the final material is roughly proportional to the inverse density. The pore size distribution depends on several process variables.

The two major issues with nanoporous silica are mechanical stability and water uptake. It is diffcult to maintain mechanical integrity if nanoporous silica is polished directly by CMP. However, a by-layer of nanoporous silica capped with dense CVD oxide (see Fig. 31) can be polished readily. Also, the CTE of nanoporous oxide is of the same magnitude as that of normal SiO_2, so that mechanical stresses induced by the thermal mismatch between the ILD and Si are comparable, but with the porous material having correspondingly lower strength to withstand those stresses. Water uptake needs to be prevented because water (really Si-OH groups) greatly increases the dielectric constant, thus obviating the benefits of porosity. Nanoporous silica films as deposited contain significant amounts of Si-OH groups because the large surface area from the pores presents numerous

adsorption sites for water molecules. In general, these adsorbed hydroxyl groups cannot be removed completely from the bulk of the film by a thermal treatment that is compatible with the devices already formed on the substrate. (Complete removal of the hydroxyl groups would require annealing at a very high temperature, which would also densify the material.) Surface treatments to make the nanoporous oxide film hydrophobic, based in particular on hexamethyldisilazane (HMDS), have been more succesful in controlling the OH content.[92]

Investigations into the integration of nanoporous silica with other elements of interconnect technologies such as Cu or Al wiring and CVD W via plugs are ongoing.[10] In one report two-level metal structures were fabricated with both Al and W plugs.[93] In another report, the material was used in filling spaces between Cu metal lines.[6] It should be noted, however, that the material may pose special challenges with regard to a diffusion barrier layer for copper since Cu diffuses much more rapidly through nanophase silica than through normal SiO_2.[94]

5.1.1.2 Silica with air gaps

Here the basic idea is to pattern the metal subtractively and then to coat the patterned metal with silicon oxide such that narrow spaces between metal lines are closed off on top and a large void is formed underneath (Fig. 32, [10]. See also Ref. [246]). This can be realized, for example, in an SiO_2 CVD process under highly non-conformal process conditions favoring deposition near the top of the

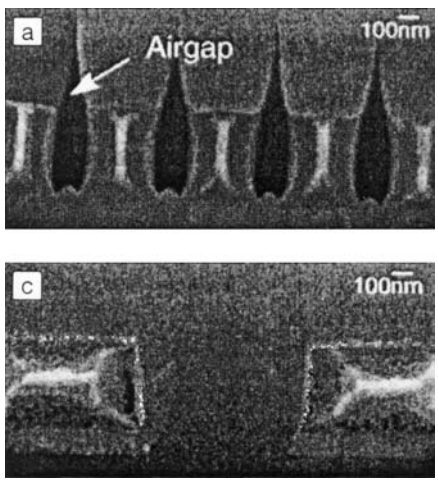


Figure 32 Air gap structure obtained in case of CVD SiO_2 onto patterned Al with narrow spaces between metal lines, panel (a).[10]

metal lines. (This is, of course, just the opposite of what one looks for when trying to fill spaces between metal lines completely with ILD.) The size of the void and the thickness of the oxide film on the sidewalls of the metal lines depend on the exact shape of the profile of the metal lines and on the aspect ratio of the spaces in-between (Fig. 32).

With interdigitated-comb test structures, this approach has been shown to yield substantial reductions in total capacitance while giving adequate ILD leakage current and breakdown voltage.[10] All of this is accomplished with well-known processing. From the point of view of maximizing interconnect performance, it is especially advantageous to let the air gaps extend above and below the space between metal lines.[246]

The main disadvantage of the air gaps is that when the spaces between metal lines are closed off on top, a seam is formed in the oxide ILD extending upward above the gap. This seam may cause problems with the lithography for the following interconnect layer by acting as an (unwanted) alignment mark.

It should be noted that with air gaps formed as described above, the major part of the space between metal lines is still taken up by oxide, and the actual air gap only occupies a relatively small fraction of the space. A related but rather different approach has been introduced recently in which most of the ILD between metal lines in a particular interconnect layer is replaced by air or gas.[247,248] The initial ILD is a sacrificial carbonaceous layer, which is removed after the metal pattern has been formed. In one case,[247] this has been implemented with sputtered amorphous carbon and W as the metal in a typical damascene process. After the metal has been planarized down to the carbon, a thin oxide layer is deposited. The carbon is then removed via oxidation, by a thermal treatment in an oxygen ambient at 450°C. The oxygen diffuses in, and the reaction products diffuse out, through the oxide. In another case, the initial ILD was a rather labile polymer covered by oxide.[248] The polymer could be decomposed thermally, and again the reaction products diffused out through the oxide capping layer.

5.1.2 Doped Si oxides

In this category we will include materials with a basic Si-O chemistry but containing a substantial amount of another element such as H, C, or F. These can be considered dopants of the silicon oxide. We will keep in mind that most CVD Si-oxides contain a small amount of H as deposited, and that eliminating that hydrogen completely takes a thermal annealing treatment at a rather high temperature approaching conditions for the growth of thermal oxide. Doping of silicon oxides with B or P has been in use for some time but will not be discussed here since the purpose of that type of doping has been to lower the glass transition temperature, thus improving the oxide reflow properties and reducing compressive film stress.[95]

5.1.2.1 H-doped oxide: Hydrogen silsesquioxane

Hydrogen silsesquioxane (HSQ) is a spin-coated material with the chemical formula $(RSiO_{1.5})_n$ where R=H.[10,96–98] Thus we classify it as H-doped silicon oxide. The dielectric constant achieved with this type of material is in the range of 2.7–3.0 after thermal curing at around 400°C. For the stoichiometry given, various structures can be formed. An example, the so-called ladder structure, is shown in Fig. 33. In polyhedral structures the parameter n defined in the chemical formula above varies approximately between 3 and 8.

Given the chemical similarity of HSQ and nanoporous silica, it is not surprising that the materials share the same areas of concern. Mechanical stability is an issue with HSQ as well, particularly during CMP, and the same remedy of capping with CVD oxide has also been applied.[10] On the other hand, HSQ has the advantage of being somewhat more flexible mechanically than nanoporous silica. In addition, dielectric degradation of the HSQ may arise when Si-H bonds are being replaced by Si-O bonds, but this occurs not so much by adsorption of moisture but rather by reaction of the H in the HSQ with the ambient, e.g., during ashing of a photoresist in an oxygen plasma after vias have been etched in the HSQ, during wet stripping of a photoresist, during wet post-CMP cleaning, or simply during annealing at elevated temperatures in an oxygen-containing ambient. The degradation after patterning can be avoided if the sidewalls of the vias can be prevented from being exposed to the damaging ambient. One implementation of this idea has been demonstrated using TiN rather than a photoresist as a mask for via etching in the HSQ.[97] The TiN mask is left in place, thus protecting the top of the material, and then additional TiN is deposited conformally into the vias as a Cu diffusion barrier, thus protecting the via sidewalls. Employing electrolytic-ionized pure water in post-CMP cleaning also helps to reduce dielectric degradation of the HSQ.[97] In addition, HSQ stability has been reported to be improved by an unspecified ion implantation[98] or an F-ion implantation treatment.[99]

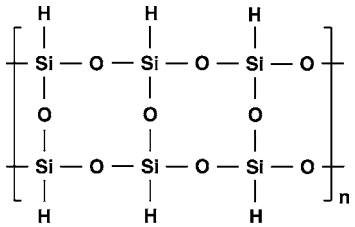


Figure 33 Ladder structure of hydrogen silsesquioxane (HSQ).

HSQ has been integrated successfully with multilevel Al/W metallization.[10,93] Its excellent planarization properties, electrical integrity, and low dielectric constant have also been taken advantage of in the fabrication of spiral inductors in a 0.5-μm BiCMOS technology.[100]

Very recently, initial characterization work on a new material called XKL from Dow Corning has been reported.[257] XKL is based on an HSG resin, using two solvents with different boiling points. This allows a controlled amount of porosity to be introduced into the HSG. At a porosity of 60%, a dielectric constant of 2.2 has been achieved. A one-level damascene test structure with Cu/TaN has been fabricated. A major issue with XKL, as with other porous materials, is mechanical strength and stability. A blanket XKL layer showed numerous defects after CMP, but no defects were observed after CMP of a patterned wafer.

5.1.2.2 F-doped oxide

This is material with composition SiO_xF_y. It is often abbreviated as FSG, for fluorinated silicate glass. Doping the silicon oxide with fluorine lowers the dielectric constant of the oxide to an extent that depends on the deposition method and conditions, and thus the film composition and structure.[101–105] Generally, the larger the F content, the lower the k.[95] The lowest k reported for FSG films has been 2.3.[103] However, films with high F content sometimes have stability problems. At this time a consensus is emerging that it is safe to use material with up to about 4 atomic % F in practical applications, giving a k of around 3.5,[104,105] but this limit may depend on the detailed structure of the films.

Fluorine in FSG can be determined quantitatively using the technique of nuclear reaction analysis (NRA), whereby the sample is irradiated with a proton beam and γ rays from the reaction $^{19}F(p,\alpha\gamma)^{16}O$ at 340 keV are recorded.[106] As the proton beam energy is varied, F atoms are sampled from a substrate depth at which the protons have slowed down to an energy of 340 keV. Hence, after calibration with materials of known F content, NRA yields quantitative F concentrations. NRA measurements have also been related to Fourier transform infrared spectroscopy (FTIR) data, which readily detects Si-F bonds in the glass.[106] A linear relationship between F from NRA and the Si-F absorption in FTIR has been established, which extends considerably beyond 4% of flourine content and is independent of the flourine precursor (C_2F_6 or NF_3), except at the very highest flow rates leading to unstable films.[101,102] In fact, it turns out that the Si-F/Si-O absorption ratio in FTIR is itself an almost quantitative measure of the F atomic fraction in the FSG (Fig. 34).[101,102]

Two types of chemistries have been used in the deposition of FSG. In the first one, an F-bearing precursor is added to a conventional plasma-enhanced CVD

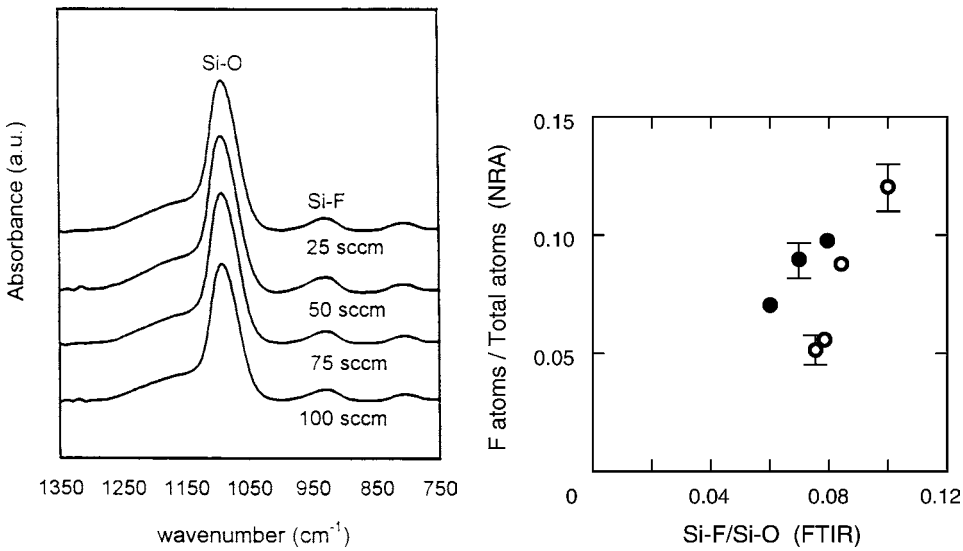


Figure 34 FTIR spectra and Si-F/Si-O bond ratio vs. fluorine concentration [F] in SiO_xF_y from nuclear reaction analysis (NRA).[102]

(PECVD) oxide process based on TEOS/O_2, typically in a parallel-plate reactor. The most common F-precursors are C_2F_6 and CF_4, but SF_6 and NF_3 have also been investigated. The second type of chemistry employs CVD from a high-density plasma (HDP) usually involving a SiH_4/O_2 process and SiF_4 or Si_2F_6 as the fluorine source.[107–109]

The physical reasons why F content lowers the dielectric constant of a silicon oxide are still being debated.[95] In FSG films made with the same type of process, increased F content is generally observed to be correlated with reduced film density. Thus it has been argued that film density is the main contributor to the dielectric constant.[110,111] However, FSG films with the same F content, but prepared by different process chemistries, may have different dielectric constants [102]. In a comparison of PECVD films from C_2H_6 and NF_3, it was found that k could be expressed as

$$k = 1 + (k_0 - 1)d/d_0 - \mathrm{a}k_0[\mathrm{F}]d/d_0, \tag{17}$$

where a is a suitable constant, k_0 is the dielectric constant of undoped oxide, [F] is the fluorine concentration in the FSG, and d and d_0 are the doped and undoped film densities.[101] The second term on the right side of Eq. (10) represents the contribution to k by the change in film density alone, whereas the third term on the right side of Eq. (10) is a measure of a structural, [F]-related contribution to the lower-

ing of k by the fluorine, possibly coming from electronic,[112] ionic polarization,[110] and orientational polarization effects.[113]

It is worth noting, too, that doping of silicon oxide with F brings additional benefits similar to those from doping with B and P [95]. Doping with F also improves the gap-filling properties of the oxide in the deposition for subtractive metal patterning processes, and it also reduces oxide film stress.

There have been a number of recent reports involving the chemical vapor deposition of FSG by means of a high-density plasma (HDP).[107–109,114–117]. In general, these works have made use of silicon fluorides as the fluorine source, as opposed to carbon fluorides, the rationale being that compounds with Si-F bonds already formed allow for easier incorporation of bound F into the silicate network. Of course, unbound F in the glass network presents a reliability hazard, as it is expected to be rather mobile and reactive.

The main problem areas in using FSG as a low-k ILD are fluorine outgassing, moisture absorption, and control of the metal/FSG interaction. A thermal annealing treatment reduces the F content and densifies the film,[95,104] but the actual amount of fluorine loss appears to depend on how the film was deposited. In one case, loss of F and the corresponding increase in k have been found to be fairly small even when the initial F content of the FSG was above 4 atomic %.[117] Some moisture is absorbed readily by FSG films. This leads to an increase of k, as water reacts with fluorine and Si-F bonds are replaced by Si-OH bond. Furthermore, the reacted F produces HF, which may etch the oxide. Fluorine loss and moisture absorption can be retarded significantly by capping the FSG with undoped oxide.[104] An alternative for reducing the susceptibility of the FSG to water absorption is treatment in an O_2 plasma, but this noticeably increases the dielectric constant.[118] Issues related to the reaction of F from the FSG with metal contact will be discussed in Sec. 6.2 on metal/ILD barriers.

5.1.2.3 C-doped oxide

Carbon is another dopant which can reduce the dielectric constant of silica. Carbon-doped silicon oxides have been synthesized along two different routes following a siloxane chemistry, with either a spin-on or a CVD process.

In analogy to HSQ, carbon-containing silsequioxanes are spin-on materials with the formula ($RSiO_{1.5}$) where R is a hydrocarbon group rather than simply H. Most often $R = CH_3$, in which case the material is referred to as methylsilsesquioxane, with the abbreviation MSQ (compare Figs. 33. and 35 for the structures of MSQ and HSQ).[96,98,119] Similar to HSQ, MSQ films attain a k of about 2.7 after proper curing, but the dielectric constant for MSQ is more stable in the ambient. Thanks to the methyl side groups in the crosslinked network, MSQ also exhibits considerably better thermal stability than HSQ.

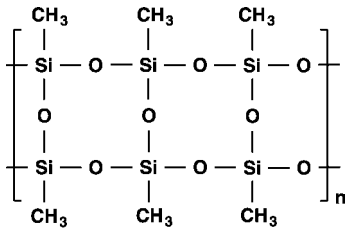


Figure 35 Molecular structure of methyl-silsesquioxane (MSQ).

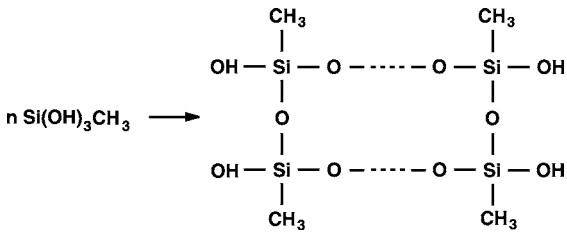


Figure 36 Siloxane polymerization reaction.

Siloxane materials have been made in a CVD process, primarily using the reaction of methyl-silanes with H_2O_2

$$\begin{aligned} CH_3\text{-}SiH_3 + H_2O_2 &\rightarrow CH_3\text{-}Si(OH)_3 + \text{by-products} \\ CH_3\text{-}Si(OH)_3 &\rightarrow CH_3\text{-}SiO_x + H_2O, \end{aligned} \tag{18}$$

and yielding films with $k = 2.8$–3.0.[120,121] See Fig. 36 for a schematic of the polymerization reaction, and also note the similarity to MSQ (Fig. 35). The polymerization reaction is slow enough so that the liquid-like deposited material flows quite easily to yield self-planarization. In the Flowfill process, an additional proprietary carbon dopant material is utilized.[120]

The main properties of C-containing siloxanes can be summarized as follows: k decreases as C content increases. The materials are thermally stable to about 450°C. Moisture absorption is negligible, k is stable over time, and 0.1-μm gaps with a 4:1 aspect ratio have been filled. The lowest reported k of 2.75 was reached using a mixture of mono- and di-methylsilane as Si precusor.[121]

Further reductions of k down to around 2.3 have been achieved by making porous siloxane materials.[122–124] In one case, this was accomplished by adding a sacrificial filler, substituted norborene polymer (NB) containing triethoxysilyl

groups, to a commercially available spin-on MSQ.[122] After curing, the NB was decomposed at 400°C, leaving behind 70 nm closed pores in the MSQ. This reduced k from 3.1 to 2.7. Furthermore, siloxane-like films have been deposited by a PECVD process using hexamethyldisiloxane monomer as the organic Si source, and an O_2 inductively coupled plasma as a remote oxygen radical source. Deposition at room temperature yielded a film with $k = 2.6$, and deposition at 200°C a film with $k = 3.3$. The glass transition temperature was higher than 400°C.[123] In yet another approach, copolymers from MSQ and other alkyl (trisiloxysilyl) units have produced films with a lowered k after the labile alkyl groups were removed thermally by baking at 450–500°C.[124] Only the trifluoropropyl group worked well, however, giving material with pores in the 1 nm range, whereas cyanoethyl, phenethyl and propyl groups led to material with collapsed pores. Using trifluoropropyl, films with $k = 2.3$ were obtained.

Furusawa et al.[258] have come out with a recent report on a silicon oxycarbide material (SiOC), deposited by CVD from methyltriethoxysilane in a parallel-plate reactor. They fabricated Cu-plug and Cu-wire test structures and obtained a k of 3.3. Their SiOC material turned out to be three times as strong as plain organosilicates and even stronger than oxide-capped organosilicates. Demolliens et al.,[259] using a similar SiOC material but also incorporating air gaps, achieved an effective k of about 2. Their approach was to first form a Cu/SiO_2-SiN damascene structure, then to remove the SiO_2-SiN dielectric, and finally to deposit PECVD SiOC under non-conformal conditions. The air gaps between the Cu lines were particularly effective at a small pitch. A 55% reduction of total capacitance compared to an SiO_2 structure was observed.

A related material, which can also be classified as a C-containing silicon oxide, has been introduced by Applied Materials under the name of Black Diamond.[267,268] This material is deposited in a PECVD process near room temperature, using the same organo-silane precursors, but gaseous oxidants such as O_2 are used rather than H_2O_2. The resulting films have a composition similar to SiO_2, combining silsesquioxane-type porosity with low-carbon concentration. A dielectric constant of around 2.7 can be achieved.[267] Feasibility of Black Diamond to be extended down to $k < 2.5$ has been demonstrated recently.[269] The physical properties of Black Diamond are also quite similar to those of SiO_2, including the mechanical strength, adhesion, and the ability to withstand CMP. The glass transition temperature of Black Diamond is well above 450°C.[268] The deposition of Black Diamond is generally run under conditions favoring gaseous reactants with high sticking probability. This results in poor step coverage and gap filling compared to the organo-silane and H_2O_2-deposited films. Therefore, Black Diamond is suitable for use as an intermetal dielectric only in a damascene scheme.[267,268]

5.2 ORGANIC POLYMER-BASED ILDS

A large number of carbon-based polymers[91,119] and inorganic-organic hybrid materials[96] have been under investigation for use as low-k ILDs. In this section we will focus on a few examples which appear to be of the highest current and future interest. They will be classified into two groups, according to whether or not they contain fluorine. Several non-fluorinated polymers have shown promise with a k considerably lower than SiO_2 or even FSG. Furthermore, as in the case of silicate materials, doping an organic polymer with fluorine tends to reduce its dielectric constant.

5.2.1 Non-fluorinated organic polymers

5.2.1.1 Parylene-n [poly(p-xylylene)]

The monomer shown in Fig. 37 is an example of a vapor-deposited low-k polymer.[10,125] The process involves vaporization of the di-p-xylylene dimer at around 150°C, cracking at 680°C to form two reactive monomers, and finally condensation and polymerization on the substrate surface. Deposition is very conformal, but the deposition rates are rather slow: < 10 nm/min at room temperature, and of the order of 100 nm/min with the substrate cooled to -20°C.[125]

The k of parylene-n is 2.6–2.7. The thermal stability is dependent on the oxygen content of the ambient. In nitrogen, parylene-n films begin to dissociate at around 420°C, with a weight loss of 5% in 30 minutes. Even a small oxygen content of the order of 1% reduces the temperature stability considerably.[125] This sensitivity to oxygen exposure at an elevated temperature is a feature (and a problem) shared by most hydrocarbon polymer ILDs.

Dual-damascene test structures with parylene-n and copper have been fabricated.[126,127] Efforts at integrating parylene-n into complete interconnect technologies are on-going.[10] Attempts have also been made at increasing the thermal stability of parylene-n, while maintaining or even improving its dielectric constant, by forming a copolymer of it with species such as chloro-p-xylylene or perfluorooctyl methacrylate.[128]

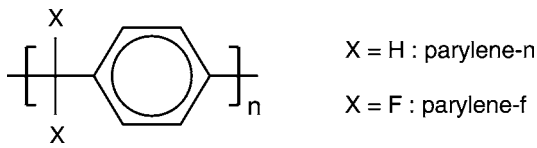


Figure 37 Molecular structures of parylenes.

A new type of low-*k* polymer closely related to parylene-n is polynaphatalene.[125] It has the molecular formula -$[C_{10}H_6]_n$-, with the monomer containing two benzene rings rather than just one, as does parylene-n. Polynaphatalene films have better thermal stability than parylene-n, but they also suffer from rather low deposition rates.

5.2.1.2 Benzocyclobutene (BCB, Cyclotene 501)

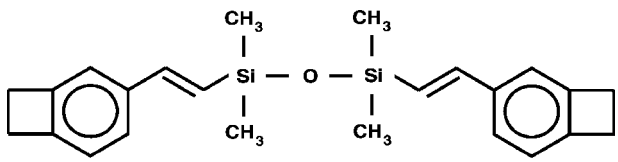
Benzocyclobutene is a spin-on copolymer of divinylsiloxane and *bis*-benzocyclobutene (DVS-BCB, or short BCB)[119,129,130] developed by Dow Chemical. The corresponding monomer is shown in Fig. 38. BCB is a thermoset material because the monomers crosslink upon curing. No moisture is evolved during curing, and since the functional groups of the BCB molecule are hydrophobic, moisture uptake after curing is very low. Planarization behavior is excellent.

A fully cured BCB film has an isotropic dielectric constant of 2.7. The main disadvantage of the material is that its thermal stability is somewhat low, with a glass transition temperature T_g of 350°C and a weight loss of 1% after 1 hour at 350°C in an oxygen-free ambient.[119,129] Again the stability is considerably lower in the presence of oxygen.

Damascene test structures have been fabricated and evaluated with BCB and Cu.[75,127] A complete interconnection process has also been reported where two levels of Al metallization were integrated with a top Cu level deposited by CVD into a dual-damascene structure BCB and patterned by CMP.[17]

5.2.1.3 FLARE 2.0

FLARE 2.0 is a commercial spin-on material from the class of poly(arylene ethers) developed by Allied-Signal.[119,131] Its chemical structure is illustrated schematically in Fig. 39. FLARE 2.0 is almost fully polymerized in solution and evolves no water upon final curing. This gives the material a very good shelf life.



DVS-BCB monomer

Figure 38 Molecular structure of DVS-BCB.

FLARE 2.0 has excellent gap-filling properties, since it is able to fill spaces less than 0.2 μm wide. The thermal stability of the cured films is good, with a $T_g >$ 450°C and isothermal weight loss of $< 0.8\%$ at 450°C for one hour in a nitrogen ambient. The dielectric constant is 2.84. Other processing details and materials properties have been described more fully in the literature.[131]

5.2.1.4 SiLK

A commercial spin-on aromatic hydrocarbon polymer from Dow Chemical, SiLK has a dielectric constant k of around 2.65, good gap fill and mechanical properties, and thermal stability to about 450°C.[249] SiLK has been used to fill spaces between metal lines in Al/W/SiO_2 test structures, but without electrical characterization other than via resistance measurements.[250] SiLK/Cu self- and nonself-aligned via test structures have also been reported.[260]

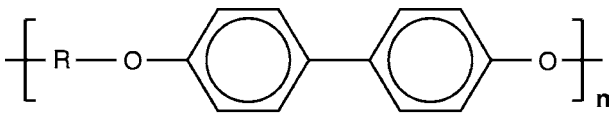
5.2.2 Fluorinated organic polymers

A number of the nonfluorinated polymers under investigation as ILDs have fluorinated counterparts. By comparison, the fluorinated varieties typically have a lower k, improved thermal stability, but also greater problems with respect to interface stability and adhesion than their non-fluorinated relatives.

5.2.2.1 Parylene-f [poly(tetrafluoro-*p*-xylylene)]

Parylene-f is another vapor-deposited low-k material (see Fig. 37).[10,125] The processing is similar to the one for parylene-n, except that the dimer cracking temperature is a little higher (~720°C), and the polymerization temperature has to be < -15°C.[125] Deposition is rather slow but also very conformal so that gaps with an aspect ratio of 6^{10} or even 10^{125} have been filled.

The dielectric constant obtained with parylene-f is 2.3. Temperature stability is again dependent on the oxygen content of the ambient. In a nitrogen atmosphere,



FLARE 2.0 : Poly (aryl ether)

Figure 39 Molecular structure of FLARE 2.0.

parylene-f begins to dissociate at around 500°C.[125] The main integration challenge with the material is its poor adhesion properties.

The benefits of using parylene-f have been demonstrated in a double-level Al metal capacitance test structure with 0.4-μm lines and spaces and an aspect ratio of 3. Using an etchback process, parylene-f was placed into the spaces between the metal lines, bordered on top and at the bottom by CVD oxide, in a manner indicated in the bottom panel on Fig. 31. This resulted in a 26% reduction in capacitance compared to CVD oxide as the ILD. If an 0.10-μm oxide liner between the metal lines was used in conjunction with the parylene-f, the capacitance reduction still was 22%.[10]

Films said to be very similar in structure to parylene-f have been deposited very recently using a plasma-enhanced CVD process and a Ar/1,4-bis-trifluoromethylbenzene gas mixture.[251]. The films have a dielectric constant between 2 and 2.6 and are reported to be stable to above 400°C if deposited at 300°C.

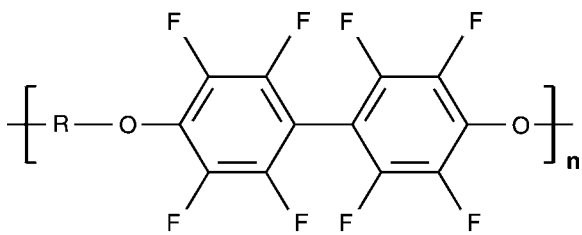
5.2.2.2 Perfluoro-cyclobutane (PFCB)

PFCB is another ILD material developed by Dow Chemical with a k of 2.24.[119,132] Its thermal properties are improved relative to those of BCB, in that the T_g of PFCB is 380°C. In addition, thickness loss is negligible at 350°C and becomes noticeable only at a processing temperature of 425°C.

The main problem with PFCB appears to be controlling the reactivity of F with the adjacent metal (see Sec. 6.3).

5.2.2.3 FLARE 1.0 and 1.51

Introduced by Allied-Signal,[133] FLARE 1.0 and 1.51 are two examples of fluorinated poly(arylene ethers). See Fig. 40 for the general chemical structure. Note



FLARE 1.0 : Fluorinated poly (aryl ether)

Figure 40 Molecular structure of FLARE 1.0.

that these materials have a lower k but also a decreased thermal stability compared to the non-fluorinated analogue.[131,133]

The original fluorinated material, FLARE 1.0, had a dielectric constant of about 2.4 and a T_g of about 260°C. With an improved formulation, FLARE 1.51, a dielectric constant of about 2.6 and a T_g of > 350°C were achieved.[133]

5.2.2.4 Fluorinated amorphous carbon (a-C:F)

Various fluorinated amorphous carbon films have been prepared by low-temperature PECVD methods, using different mixtures of fluorocarbon and hydrocarbon gases.[134–138] At this time these types of films are not very well characterized structurally, but it is clear that their properties depend on the fluorine and hydrogen content and on the extent of cross-linking achieved.

Dielectric constants as low as 2.1 have been reported for films as deposited (at a substrate temperature of 50–90°C). However, these films typically had marginal thermal stability, showing a substantial loss in thickness after annealing at 300°C.[135,136] Annealing stabilized the film properties, presumably by increasing cross-linking, but this was accompanied by an increase in k from 2.1 to 2.7. Incorporation of 10% nitrogen yielded films with a k of 2.4 and improved thermal stability, in the sense that annealing at 300°C did not change the value of k.[136] Further process optimization has produced films stable to 400°C with a k of around 2.5.[137,138]

Test structures similar to those described above for parylene-f have also been realized with a-C:F. Under the proper process conditions, 0.35-μm wide spaces with an aspect ratio of about 2.5 between Al lines could be filled with a-C:F. A three-level metal structure with a-C:F between the Al lines of the first two metal levels was shown.[134]

5.2.2.5 Teflon (PTFE)

Teflon represents the polymer with the lowest known dielectric constant, k being as low as 2.0.[125] It is not straightforward to deposit Teflon films with common methods. DuPont has produced a Teflon-like spin-on material called Teflon-AF 1600, which consists of a copolymer of tetrafluoroethylene and another fluorinated species. At this time, the resulting films have rather poor thermal and mechanical stability and poor adhesion to metals. Further process improvements continue being pursued. Significant improvements in film properties have been reported when using direct liquid injection in combination with UV-light-assisted rapid isothermal annealing.[139]

5.3 PATTERNING OF ILDS

We close the chapter on ILDs with a brief overview of ILD patterning by dry plasma etching. (For a review of dry etching covering all classes of materials important in microelectronics manufacturing, the reader may consult Ref. [63] for an example.) First we will outline some considerations relevant to plasma etching and fine-line patterning in general, and to the damascene approach in particular. This will set the stage for a somewhat more detailed, but certainly not exhaustive, discussion of issues important for etching the two classes of ILD materials of interest, silicate-based and organic polymeric, and for creating dual-damascene structures in them.

5.3.1 Overview

The primary purpose of plasma etching is to remove material from the substrate by a dry process. The plasma serves as the medium providing the necessary reactants. These must combine with the substrate in order to produce volatile products from *all* the different substrate atoms. The part of the process taking place on the substrate surface may be considered to consist of three consecutive steps: adsorption of reactants, followed by surface reaction, and finally desorption or removal of etch products. The slowest of these steps usually determines the overall etch rate. Of course, reactants also have to be transported to the substrate, and products need to be removed from the reactor, but these two gas-phase steps are rarely rate-limiting.

It should be kept in mind that an etching plasma represents a complex environment in which many chemical reactions occur, involving a large number of reactive species. Consequently, all reactants created in the plasma may not be beneficial for the desired etch reaction. For example, certain side reactions may compete with the real etchant in the adsorption step or produce involatile surface species. Also, for a given plasma chemistry, etching often competes with deposition, and the relative importance of the two components depends on the exact process conditions. On the other hand, a concurrent deposition reaction may in fact be critical to achieving *selective* removal of substrate material, i.e., preferential removal of one material relative to all others exposed to the plasma.

In order to achieve fine-line patterning, etching must be *anisotropic*. To this end, the experimental conditions are generally chosen such that the substrate is subject to ion bombardment in the substrate-normal direction, in addition to being exposed to neutral reactants. Ion bombardment enables anisotropic etching, i.e., the etching of structures with vertical sidewalls, by either promoting the reaction of neutral species or by maintaining a clean and reactive surface in those regions of the substrate accessible to the ions. In addition, energetic ions may act as chemical reactants themselves. The mechanisms by which ion bombardment enhances an

etch reaction depend on the substrate material, the plasma chemistry used, and the details of the experimental set-up and the process conditions.[63]

Creating fine-line patterns of the sort shown in Figs. 5–8 needed for interconnect structures involves creating first the desired pattern by lithographic means in a sacrificial masking layer deposited on top of the substrate. The pattern in the masking layer is then transferred by ansiotropic etching into the underlying substrate layer. Finally, the masking layer is removed. Materials for masking layers have traditionally been photoresists, i.e., photosensitive organic polymers.

These arguments suggests a number of issues which will figure prominently in the *fine-line patterning of ILDs* in general, and in the fabrication of *dual-damascene structures* for multilevel Cu interconnections in particular. First, whereas for the patterning of silicate-based ILDs one may expect to be able to proceed along lines familiar from the dry etching of silicon dioxide, in the case of organic polymer ILDs the interlayer dielectric is basically the same type of material as the traditional mask. Therefore, a normal plasma for etching the organic ILD will also erode the masking layer. This may pose serious problems for high-accuracy pattern transfer to the ILD. Thus a new approach to masking technology may be necessary in this case. Second, making a dual-damascene structure in the ILD, i.e., an inlaid pattern of trenches connecting vias, involves two masking and two pattern transfer steps in series in the same material. Again, this situation is somewhat unusual, and the question arises whether the order of these steps matters with regard to both the lithography and the pattern transfer. Third, in the patterning of vias (or contacts), deep structures with large aspect ratios need to be created. In this circumstance, the etch rate is often found to depend on the aspect ratio and therefore may vary with etch time. This puts special constraints on the etching process in terms of process control, as explained further below. Fourth, after the via etch is completed, it must be possible to make good electrical contact, at the bottom of the deep vias, between the underlying substrate layer and the next layer of metal deposited into the newly-formed via. This means that a process for cleaning of the bottoms of the vias has to be devised, which in itself is not a trivial task.

5.3.2 Patterning of silicate-based ILDs

Most processes for patterning a silicate material are based on etching silicon dioxide in a fluorocarbon plasma such as CF_4 or CHF_3 with the sample biased at a negative potential.[63] The combined exposure to neutral radical reactants and bombardment by energetic ions yields volatile products according to such generalized (non-stoichiometric) reactions as

$$\begin{aligned} CF_x + SiO_2 &\rightarrow SiF_x + CO_2, CO \\ CHF_x + SiO_2 &\rightarrow SiF_x + CO_2, CO, H_2O, \end{aligned} \tag{19}$$

where $x = 0$ to 3 for CF_4 and 0 to 2 for CHF_3. In simplified terms, C and F from the fluorocarbons serve to volatilize the O and Si from the oxide, respectively. (Other products, such as SiOF and $SiOF_2$, are also observed, depending on the plasma conditions.) Everything else being equal, the etch rate will generally be higher for a larger F/C ratio in the etching plasma. Excess carbon in the plasma will have the effect of slowing down or inhibiting the etching.

Note that ion bombardment of the substrate is essential in that no etching takes place with neutral reactants alone. Moreover, the chemical reactivity of the ions themselves contributes significantly to the overall etching. Note also an example of a possible undesirable side reaction, as mentioned above, in that CF_2 is a polymeric precursor and may form a polymer film according to

$$n\mathrm{CF_2} \rightarrow \text{-}[\mathrm{CF_2}]_n\text{-}. \tag{20}$$

This reaction can take place on the substrate as well as on the reactor walls. In the first instance, on the photoresist mask it would facilitate high etch selectivity, but on the oxide it would compete with the etching. In the second instance, it could lead to reproducibility and contamination problems for the process.

In traditional reactive ion etching (RIE) in a parallel-plate reactor, the degree of ionization and dissociation of the plasma is typically of the order of 10^{-4} to 10^{-3}; therefore, the plasma density is not very high. In that case species such as CF_3 and CF_2 are most prevalent.[63] More recently, high density plasmas are being used for etching, such as electron cyclotron resonance (ECR) or inductively coupled plasmas (ICP).[140,141] In these kinds of plasmas there is a much higher degree of dissociation (typically of the order of 10^{-2} to 10^{-1}), favoring CF_x species with smaller x. How to adjust the fluorocarbon plasma chemistry for optimal etch anisotropy and selectivity in these cases is under active investigation.[142] New etch gases are also being examined, for example C_4F_8 [140] or C_3F_7H and iodofluorocarbons.[143]

As already indicated, one of the most critical steps of the patterning of ILDs is the etching of contact holes with large aspect ratios. In this situation, the etch rate is often observed to be a function of the aspect ratio. In fact, the etch rate may either increase or decrease with increasing aspect ratio.[144] This means that the etch rate inside the via is time-dependent. The mechanisms as to how aspect-ratio-dependent etching comes about are still being debated, but it is clear that the relative fluxes of the different reactive species on top of the substrate and at the bottom of the via, and how these fluxes change as the via becomes deeper, play an important role. Moreover, in steady state the silicon dioxide surface being etched is covered by a very thin fluorocarbon film. The nature and thickness of this film

on top of the oxide and at the bottom of a via may be different, and the film in the via may change during the course of etching.[141,145] A build-up of carbon at the bottom of a via has been noted.[145]

Given that in doped silicon oxide low-*k* ILDs, the dopants (C, F, H) are species also present in the etching plasma, the effect of the doping on the etch process can be understood to first order on the basis of the general chemical arguments given above. F-doped silicon dioxide (FSG) tends to etch a little faster than undoped silicon dioxide,[146,147] because the F from the oxide assists in volatilizing the substrate and in effect increases the F/C ratio of the etchant. By contrast, H- and C-doped oxides tend to etch slower than undoped oxide, unless the etching plasma contains excess fluorine.[147] This behavior can be understood by keeping in mind that H and C from the oxide in effect decrease the F/C ratio of the etchant. Overall, though, the doped oxides do not present fundamentally new problems with regard to the fine-line patterning.

5.3.3 Patterning of organic polymeric ILDs

The dry etching of polymers is governed by the production of CO and CO_2 from carbon in the polymer. This can generally be achieved in an oxygen-based plasma. Again, ion bombardment of the substrate is necessary for anisotropic etching. The main reactants are O atoms and O_2^+ ions (possibly also O^+ in high-density plasmas).[63] No special problems with respect to material removal are encountered if the polymer ILD contains only C, H, F, N, etc., as do for example parylene-n and parylene-f.[148]

An interesting problem does come up, however, when the polymer contains Si, as do for example BCB[130,149–151] and Si-containing polynorbornenes.[152] A pure oxygen plasma is unsuitable for etching these kinds of materials because the oxygen reacts with the Si in the polymer to form etch-resistant Si-oxides. The general remedy is to add some F-containing species such as CF_4 or SF_6 to the plasma, so that the fluorine removes the silicon. The composition of the etching gas needs to be optimized properly. If the F-content of the etchant is too low, a rough etched surface with Si residues may result. On the other hand, if the F-content is too high in a CF_4-O_2 plasma, the overall etch rate decreases.[149,151] In an SF_6-based plasma, the etch rate is highest with pure SF_6 rather than an SF_6-O_2 mixture, and the pure SF_6 plasma gives very smooth BCB surfaces.[252]

Additional complications arise in the fine-line patterning of polymer ILDs. These are due to the fact that a photoresist, the traditional masking layer in the pattern transfer step, is the same type of material as the ILD; therefore both the photoresist and ILD are removed at a comparable rate in a typical etching plasma. As a practical consequence, the profile of the feature etched into the polymer often

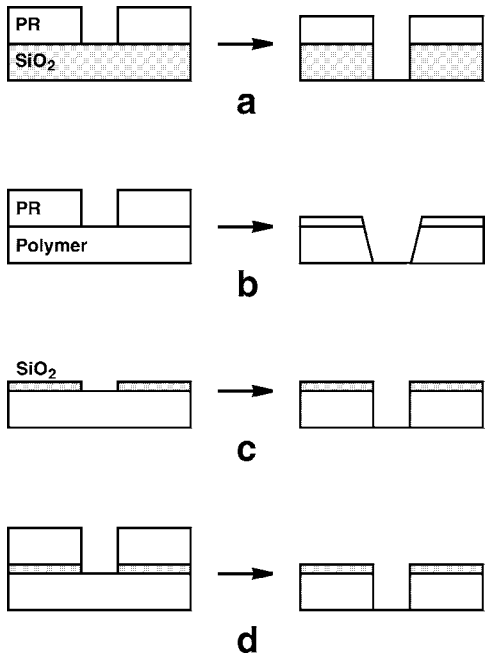


Figure 41 Fine-line patterning of ILDs: a) traditional approach with SiO_2 ILD; b) traditional approach with polymer ILD; c) single-level hard mask with polymer ILD; dual-level mask with polymer ILD.

shows degradation, as illustrated schematically in Fig. 41b, even if the etch process is highly anisotropic in principle. Note that in the patterning of silicon oxides, it is in general quite straightforward to achieve adequate etch selectivity between the photoresist mask and the oxide, and thus good accuracy in the pattern transfer (Fig. 41a).

By contrast, in etching a polymer with an oxygen plasma, a high selectivity is achieved with respect to silicon oxide; therefore, it would seem natural to use silicon oxide as a mask in the patterning of a polymer ILD (see Fig. 41c). However, in practice it turns out that in this case there is often sputtering of Si or Si oxide from the hard mask, or the bottom of the feature during overetching, and redeposition of this sputtered material onto the polymer. This occurs especially inside a via and tends to render the patterning unreliable[148–150] (cf. Fig. 42). The best general approach seems to be to use a two-layer mask, with photoresist on top of a thin layer of silicon oxide or nitride.[148–150]. The pattern is first imaged and developed in the photoresist, then "developed" into the oxide or nitride by plasma etching. In the subsequent pattern transfer into the polymer ILD, the intermediate silicon oxide layer serves to maintain the dimensional accuracy although during almost the

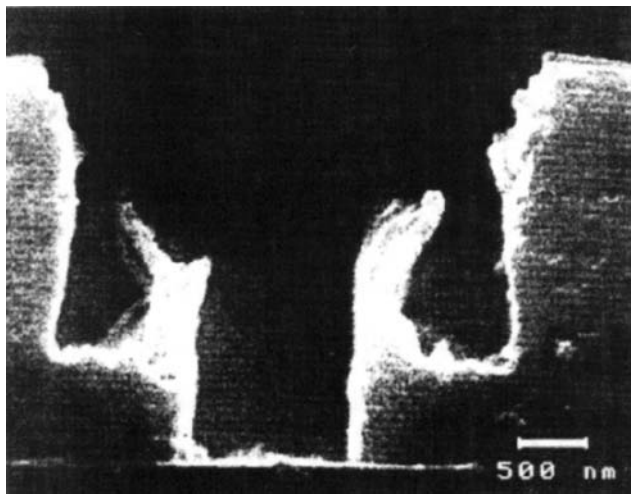


Figure 42 Fine-line patterning of parylene-n ILD using single level Si-oxide hardmask:[148] Via first, with overetch of trench completion. Note redeposition of mask material and/or Si from substrate onto via sidewalls.

entire process only polymer is exposed to the oxygen plasma. It is advantageous to tailor the etch recipe such that by the time patterning of the ILD is finished, the layer of photoresist has also been removed (Fig. 41d). The remaining silicon oxide layer may be left in place as part of the ILD without compromising its performance significantly.

5.3.4 Etching dual-damascene structures into the ILD

In forming a metal wiring layer by the damascene method, vias inside of trenches connecting the vias must be etched into the ILD (Fig. 6). This requires two masking/etching steps: one for the vias and one for the trenches. In principle, these two steps can be performed in either order, i.e., via first or trench first (Fig. 7). In both cases, this two-step process presents several new patterning issues, some independent of the ILD used and thus generic, and some peculiar to polymer ILDs.

A generic difficulty is caused by the fact that, regardless of the order of the steps, for one of the two masking layers the substrate is not flat. If the vias are formed first, then the photoresist (PR) for the second masking step planarizes the substrate as a whole and fills the vias. Hence the PR inside the vias is much thicker than in the trench regions outside the vias. Then, in the second lithography step, if the PR exposure time is chosen such that the trench regions receive the proper illumination dose, the PR inside the vias ends up being underexposed and is incompletely developed. This may leave PR residue in the vias, which will impede

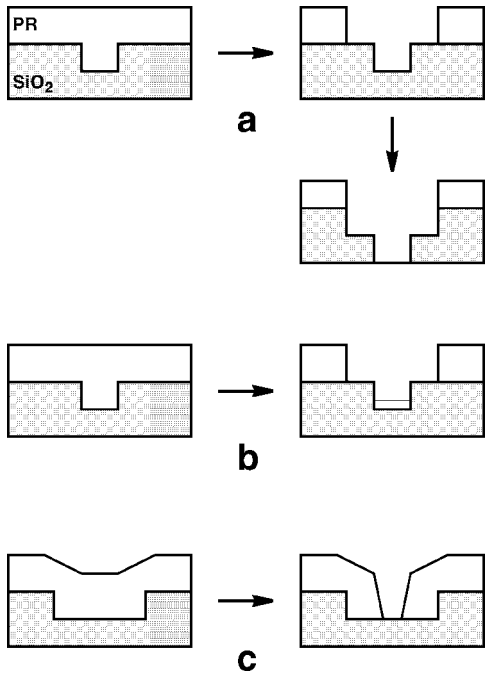


Figure 43 Lithography issues in fabrication of dual-damascene structures: a) via first: ideal case; b) via first: underexposed photoresist inside via; c) trench first: non-planar photoresist for via exposure.

the etching of the ILD in the second step (Fig. 43b). The etch rate in the vias may be substantially less than in the trench regions, or in the worst case of polymer residue in oxide vias, the vias may not get etched at all. (Keep in mind that high etch selectivity between ILD and PR is necessary for achieving accurate patterning of the trenches themselves.) If one tries to insure complete development of the PR in the vias by using a longer exposure, the PR in the field regions will be overexposed and the lithographic resolution may be compromised. On the other hand, if the trenches are formed first, then the lithography for the vias must be done on a non-planar PR layer. This again may have an adverse effect on the accuracy of the patterning overall and the lithography in particular, since imaging the vias, with the smallest dimensions of all features, generally constitutes the most critical step in the lithographic process (Fig. 43c).

These problems are compounded when the ILD is a polymer because, as we mentioned above, each of the two masking levels for dual-damascene structures generally requires two layers (PR on top of hard mask).[150] This makes the entire process that much more complex. In Fig. 44 we give a simplified illustration of one possible process flow, in which the vias are formed first, but again trench

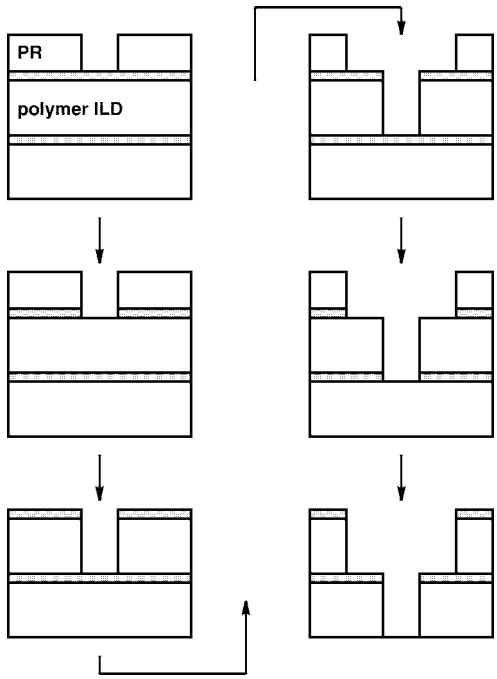


Figure 44 Process flow for dual-damascene structure with polymer ILD. Note two hard masks.

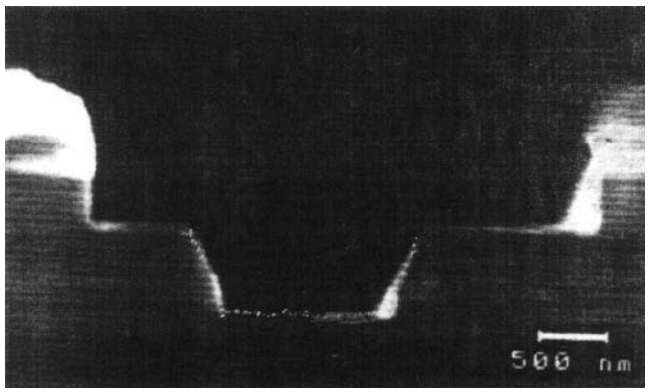


Figure 45 Example of dual-damascene structure etched into BCB.[149] Sidewalls of via are slightly tapered.

first is also feasible. Fig. 45 shows an example of a dual-damascene structure realized in BCB as the ILD.[150] Additional variants for the etch process sequence and associated integration issues have been discussed in more detail elsewhere.[75,153]

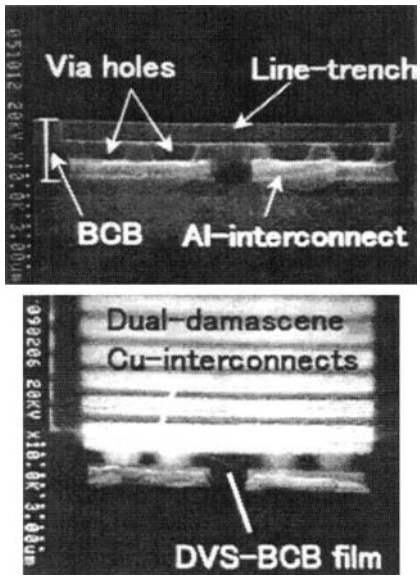


Figure 46 Dual-damascene BCB structure filled with Cu.[17]

Process development and optimization for creating dual-damascene structures in polymer ILDs is ongoing. Moreover, although we have emphasized the complexities with respect to accurate patterning, let us point out that there has been at least one report, using BCB as the ILD and Cu as the metal, in which a dual-damascene structure was fabricated with a singel-level photoresist mask only (Fig. 46).[17] It is also interesting to note that although etching dual-damascene structures into silicon oxide ILD is more straightforward in principle than into a polymer, it has been found that a more complex layer involving thin intermediate (silicon nitride) hardmasks of the sort shown in Fig. 44 gives improved pattern definition even with an oxide ILD.[154] A general discussion of challenges in etching low-*k* ILDs has been given recently.[253]

5.3.5 Via cleaning

The final step in the patterning of dual-damascene structures is the cleaning of the bottoms of the vias before deposition of the next metal or barrier layer. This is to assure good electrical contact between the two neighboring metal layers. If we assume that the via in the upper ILD ends on Cu in the layer below, then a clean contact area in the via relies on complete removal of the ILD and on a conductive Cu surface. The details of how this can be achieved depend on whether the ILD is oxide or polymer.

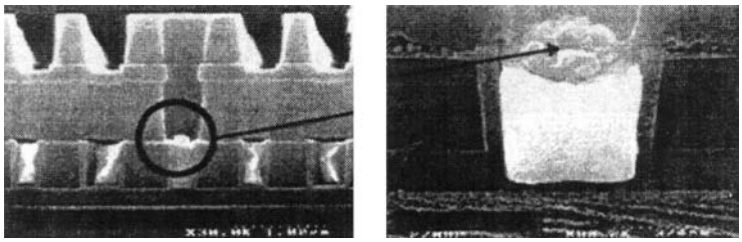


Figure 47 Etch residue inside via hole etched into SiLK polymer ILD.[155]

For a silicate ILD, the deposition of the silicon oxide onto unprotected Cu leads to the formation of a thin layer of Cu-oxide, which can be removed by a hydrogen plasma treatment (see Sec. 7.2 below). But additionally, the etching of the via in a fluorocarbon plasma and the subsequent ashing of the photoresist tend to leave a polymeric residual film, possibly with some Cu mixed in, which may be difficult to clean. (For an example see Fig. 47 and Ref. [155].) Various approaches to dealing with this problem are under investigation, including wet chemical methods,[156,157] dry gaseous methods,[157] and H_2 plasma cleaning.[158] For example, it has been found that dilute HF removes Cu-polymer residue and CuO, but not Cu_2O. The latter requires a gas-based method using hexafluoroacetylacetone.[156] Also, the best recipe for removing the residual polymer film remaining on the oxide after etching is different for the field oxide areas and for the bottoms of the vias.[156] This is evidently a consequence of the different compositions of those films.[141,145] Of course, this reflects the fact noted above that the composition of the impinging gas flux, and thus the etch mechanism, is expected to be different on top of the substrate and at the bottom of a via.

For a polymer ILD, the via etching step itself, in an oxygen-based plasma, will introduce some oxidation of the Cu because the Cu will be exposed to the plasma near the endpoint of the etching. Also, if removal of remaining photoresist by plasma ashing is necessary, this may again cause the formation of residue in the via and oxidation of the copper. Dilute HF has been used for cleaning vias in BCB.[75] Other wet chemical cleaning methods based on proprietary agents are being evaluated and are said to look promising.[155] An intermediate silicon nitride hardmask between the Cu and the polymer ILD acts as an etch stop[75,155] and not only protects the Cu but also facilitates via cleaning.[155]

5.3.6 Planarization of low-k ILDs by CMP

Planarization of undoped silicon dioxide is a mature field and has been treated extensively elsewhere.[159] Therefore, it will not be discussed here. Issues specific

to the CMP of low-*k* dielectrics have been outlined recently.[160] The details of the behavior in CMP, of course, depend on the nature of the dielectric, but from the view point of process integration it is also important in which context a particular materials is used, e.g., whether its application will be with Al or Cu metallization.

There have been very few reports regarding the CMP of doped silicate glasses and how these materials differ in their CMP characteristics from undoped oxide. Part of the reason for this is that in many present applications, doped oxides are capped by a layer of undoped oxide and thus are not polished directly.[10] In a recent paper, CMP of FSG has been used in conjuntion with an unspecified metal/barrier system.[161] It has also been reported that FSG does not withstand exposure to conventional CMP slurries and post-CMP cleaning chemicals as well as undoped oxide.[162] Planarization of porous silicates by CMP may well turn out to be rather difficult because of the low mechanical strength of the material. But again, this difficulty may be circumvented by using a normal oxide cap.[10,163,164]

Planarization of polymer ILDs by CMP is in the early stages of development. One important issue in the direct CMP of polymers is their softness, which tends to lead to scratching due to the mechanical abrasion. Let us also point out that the CMP of polymers is not only rather different from that of silicon oxides in terms of slurry chemistry, abrasives, etc., but there are even substantial differences between individual polymers. For example, the optimal polishing slurry for parylene-n is not the same as for BCB.[165] Also under investigation is the CMP of poly(arylene) ethers,[166,167] siloxane spin-on glasses,[168] and fluorinated amorphous carbon.[169]

On the other hand, the CMP of polymers may not be a critical problem, at least in the short run. First, polymer ILDs presumably are sufficiently planar as deposited and do not need planarization. Also, a metal or metal nitride diffusion barrier will always be used between the polymer ILD and Cu. Therefore, the barrier would act as a polishing stop in the CMP of Cu and prevent the polymer from being subject to direct CMP, unless at the very end of the process the barrier itself is also removed by CMP. Alternatively, it may be possible to remove the barrier in the field regions by means other than CMP, e.g., by dry etching. Hence the main issue would be the adhesion and stability of the barrier-ILD interface.

Moreover, it has been suggested that few manufacturers will be willing to take the reliability risk of depositing the diffusion barrier directly onto the polymer ILD [160]. With a silicon oxide or silicon nitride capping layer between the diffusion barrier and the Cu, one can simplify the process complexities while incurring only a minor penalty in terms of degraded ILD performance (i.e., increased effective *k*). By dealing separately with the polymer/capping layer and capping layer/barrier interfaces, one can reduce the materials variables for the former and benefit from barrier and Cu/SiO_2 process technology know-how for the latter.

6

CU/ILD BARRIERS

The benefits of an interconnect technology depend on the properties of the metal and the ILD, as we outlined in Chapter 2. However, the practical feasibility of a certain metal/ILD combination ultimately rests to a large extent on the characteristics of the interface between the metal and ILD. Unless this interface is strong and remains stable over time, the reliability of the circuit, and thus its usefulness, may be compromised.

As an aside, let us remark that interfaces are not only critical for the interconnect structure but also play a key role in and on the active devices, for example in the first-level metal contact areas to source and drain, in the gate contacts, etc. Consideration of those kinds of interface issues is outside the scope of the present book. The interested reader may find further information in Refs. [7,73,170].

The use of Cu as the metal, either with SiO_2 or a low-*k* dielectric as the ILD, presents a unique challenge primarily because the Cu/ILD interface is in general much less strong than the corresponding Al/ILD interface. In fact, a major reason for the success of Si technology to date has been the stability of the interface in the workhorse metallization scheme of Al and SiO_2.

In the context of metal/ILD interface issues, three properties of copper are especially important and pose a much greater problem than with aluminum.

(1) Cu adheres poorly to most ILD materials because it does not interact strongly with them,
(2) Cu oxidizes easily, and its oxidation is not self-limiting,
(3) Cu diffuses readily through undoped SiO_2.

Cu is of course an extremely undesirable impurity in Si, as it forms a generation/recombination center for free charge carriers. In addition, Cu reacts readily at low temperature with most metals and metal silicides.[170] All of these points may be regarded as reliability hazards in the use of Cu. It should also be mentioned, however, that in one respect Cu has a definite advantage over Al: it is generally agreed now that resistance to electromigration is greatly improved in Cu compared to Al.[3]

With respect to how Cu diffuses readily through undoped SiO_2, note that the diffusion behavior of Cu depends on the type of oxide (thermal, PEVCD), and that silicon oxynitride, and even more so silicon nitride, are more resistant to Cu diffusion than silicon oxide.[171] The data on Cu diffusion through low-*k* ILDs such

as doped SiO_2 and polymers are incomplete at this time, but it is likely that Cu diffusion will be a serious problem there, too. Consequently, Cu must be used with a thin interlayer film between it and the ILD. This additional layer must correct the three problematic properties of Cu mentioned above; it must provide the "glue" to insure good metal/ILD adhesion, it must protect the Cu from oxidation, and it must act as a barrier for the diffusion of Cu into the ILD.

Moreover, it has become apparent recently that if the ILD contains fluorine, then the barrier must perform a fourth function, namely to prevent the diffusion of F into the metal. Recent data indicate, however, that this may end up being more of a concern with Al than with Cu, since the reactivity of these two metals towards F is rather different, as will be explained below.

Whether the film of a single material will be able to fulfill all these requirements in a given situation is uncertain. Our general discussion on manufacturing damascene structures in Sec. 2.4 suggests that two different materials may be used anyway, one as a liner in the inlaid vias and trenches, and another one, typically SiN, on top of the planarized metal (Fig. 8). It is also becoming evident that the optimal barrier will be specific to a particular Cu/ILD (or metal/ILD) combination rather than just being dependent on the metal itself.

Yet another constraint on the diffusion barrier arises from electrical considerations. Given the low electrical resistivity of copper, the barrier material will by necessity have a much higher resistivity than the Cu itself. Hence the barrier must be thin enough so as not have a negative impact on the via resistance and the overall electrical conduction properties of the metal wiring. At the same time, the barrier must be thick enough to prevent the diffusion of copper. As the widths of metal lines, and thus barrier thicknesses, are continually being decreased, in parallel to the downscaling of feature sizes, the demands on the barrier stability are becoming ever more stringent.

The arguments above suggest that transition metals and their nitrides should be good candidates for a Cu/ILD barrier due to their high melting point, their chemical inertness, and their relatively low electrical resistivity.[170,172–174] Very recently, transition metal-silicon-nitrides have also been proposed as barrier materials.[175] It should be emphasized at this point that although it may be possible to discern general trends in barrier behavior between different materials, the details in the behavior of a specific type of material depend on many variables such as the deposition method, the precise composition, the crystalline structure and texture, the nature of the built-in defects, other aspects of the microstructure, the thermal annealing history, etc. With regard to transition metal nitrides, the deposition methods investigated include reactive sputtering, plasma nitridation of the metal, ionized physical vapor deposition, and chemical vapor deposition.

Analytical methods for determining Cu diffusion, or the absence thereof, often monitor either changes in the Cu itself, e.g., its electrical resistivity, or changes

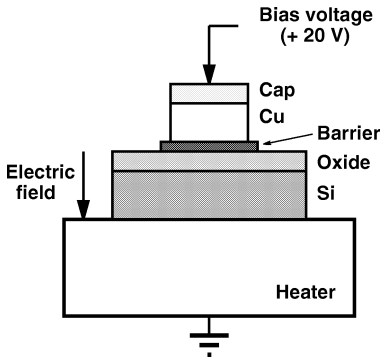


Figure 48 C-V and BTS test structure.

in a suitable test structure, e.g., in a Cu/barrier/ILD/Si capacitor, as indicated by shifts in the the capacitance-vs-voltage characteristic (C-V) or the leakage current through the ILD (Fig. 48). Other methods, such as structural characterization and different varieties of compositional depth profiling, have also been employed. These compositional methods include sputter depth profiling using secondary ion mass spectrometry (SIMS) or x-ray photoelectron spectroscopy (XPS). Diffusion of Cu is initiated either by normal thermal annealing or by bias temperature stress (BTS), in which case diffusion occurs in the presence of a strong electric field across the ILD (Fig. 48).

It should be mentioned here that the barrier layer affects the structure and properties of the Cu grown on top of it. For example, significant differences in the crystallographic texture of the Cu have been noted as a function of the nature and structure of the barrier layer[176] (see Secs. 7.3 and 7.4 below). This observation is significant with regard to reliability, since Cu films with stronger (111) texture showed longer median times to failure in electromigration tests.[176]

A variety of materials have also been investigated as barriers for Cu diffusion when deposited directly on Si rather than on an ILD. Let us point out, however, that in our further discussion we will focus primarily on the behavior of materials as diffusion barriers for Cu on SiO_2 and other ILDs. That is, we will proceed with the implicit assumption that this is the most critical property, and adhesion and passivation can be controlled adequately in the process. However, for the sake of putting these results in proper perspective, we will also include some examples where Cu and the barrier were deposited onto Si. The study of diffusion barriers has a considerable history in connection with Al metallization, where the main objective is to prevent diffusion of Al into the Si contact areas. This work has been summarized in Ref. [7].

6.1 Cu/UNDOPED-SiO_2 BARRIERS

The barrier materials under closest examination to date for this metal/ILD combination are Ti/TiN, Ta and TaN. Ti/TiN was used in two of the Cu processes.[5,6] (In the third announced Cu process, the barrier was not specified.[4]) Other authors have favored TaN[177,178] (see Sec. 7.3 below). In a comparison of PVD Ti, TiN, Ti/TiN, Ta, and TaN barriers, based on thermal annealing of MOS capacitors, it was concluded that the most stable system was Ti/TiN, followed by TiN by itself, and that Ta and TaN were significantly less stable than TiN.[179] It is not clear, however, whether one materials system is preferable in principal over another, given the significant variations in properties within a given system as a function of the deposition method. This is evident, for example, when comparing a metal nitride obtained either from nitridation of deposited metal, from reactive sputter deposition, or from CVD. On the other hand, there appears to be general agreement that for a common barrier thickness, a metal nitride has better barrier properties than the corresponding pure metal.[177–180] But then, perhaps what should be compared is barriers with different thicknesses and the same electrical resistivity, since the latter is the benchmark from the point of view of electrical performance.

The importance of the details of the deposition method and its effect on barrier properties is highlighted in studies involving CVD of nominally the same metal nitrides but using different metal-organic precursors.[173,174,181] For example, in the CVD of TaN it was shown that a strong metal-nitrogen bond in the precursor is preserved during deposition, yielding low-resistivity films of cubic structure with good barrier properties.[173,174] Similarly, better TiN barrier films were obtained from the decomposition of a nitrogen-containing precursor than from the reaction of $TiCl_4$ with NH_3.[182]

Other metal nitrides such as MoN and WN are also being investigated.[172–176] In annealing tests, W_2N was found to be stable to 600°C, as compared to TaN which was stable to 700°C.[183] Additional materials under examination include TaC, which was found to be stable under annealing to 600°C,[182] WSiN/WSi_x,[183] Nb/NbN_x,[172] and Cr/CrN_x.[172,184]

A different approach to forming a diffusion barrier for Cu has been proposed, whereby the transition metal to form the nitride is first deposited with the Cu as an alloy, then driven thermally to the surface of the Cu and finally reacted with a nitrogen-containing ambient.[170] The main question in this approach is whether the remaining Cu, which may still contain some of the transition metal after annealing, has a low enough resisitivity. This latter problem can be largely avoided if a Cu-Al or Cu-Mg alloy is used,[185–187] because the concentration of those elements can be kept low enough so that the resistivity of the Cu is not adversely affected. The Al or Mg on top of the Cu are made to react with oxygen in order to form a passivating oxide. This oxide film prevents oxidation of the Cu itself and also

inhibits Cu diffusion, but whether it is adequate as a diffusion barrier remains to be determined.

6.2 Cu/DOPED-SiO_2 BARRIERS

The only system of this type for which some data are available at present is the Cu-FSG system. In one study,[188] the FSG was deposited onto p-Si with 5-nm of thermal oxide, and Cu was deposited either directly onto FSG or with a PVD Ti or TiN barrier in-between. On the Cu/FSG samples, thermal annealing (10 hours at 500°C) and BTS measurements (3 MV/cm at 250°C) indicated that Cu diffusion into the FSG was markedly reduced compared to undoped oxide. In addition, no diffusion of F into the Cu was detected. With a 5-nm Ti barrier, substantial diffusion of F into the Ti, and build-up of F in the Ti, was noticed. The amount of F detected in TiN was almost an order of magnitude lower than in Ti.

In another study using Ta and TaN as a barrier between Cu and FSG, depth profiling with NRA showed no F in the barriers or in the Cu.[189] (Cu diffusion into the barrier and the FSG was not examined there). By contrast, for TaN between Al and FSG, and to a somewhat lesser extent also for Ta between Al and FSG, fairly rapid diffusion of F through the barrier was observed.[190] In addition, F diffused rapidly through the Al itself to its top surface.[189–191] TiN between Al and FSG acts as a sacrificial barrier with respect to fluorine diffusion,[188] just as it does between Cu and FSG.[188] When Al is deposited onto FSG, fluorine again diffuses rapidly to the top metal surface and reacts there to form an Al-oxyfluoride, but there is very little reaction at the Al/FSG interface.[191]

The very strong reactivity and F diffusion from FSG into Al can be mitigated noticeably by a treatment of the FSG in a fluorocarbon/oxygen plasma before deposition of the Al.[190] Under optimal, slightly etching, process conditions, F diffusion into Al is reduced by a factor of two. However, some process conditions also lead to an increase in the dielectric constant of the FSG. The mechanism at work here is presumably that the slight etch depletes some of the F at the FSG surface and replaces it with carbon.

When using a Cu-Al alloy as a self-passivating Cu material,[186] it is interesting to note that for Cu-1%Al in contact with FSG, diffusion of F through the metal is very rapid, even at room temperature, and results in a large build-up of F on top of the metal film.[190] This type of fluorine build-up produces a poorly conducting metal surface layer, which may be very hard to clean off, giving rise to contact resistance problems when the next metal layer is deposited.

These observations lead to the conclusion that F apparently has a very low affinity for and reactivity with pure Cu, whereas Cu-1%Al and Al are quite reactive towards fluorine. This in turn has a significant impact on the behavior of the barrier with respect to diffusion of F from the FSG into the metal, in the sense that it is Cu

as much as the barrier itself which determines the diffusion of fluorine. However, the behavior of barriers with respect to diffusion of both copper and fluorine clearly merits further study.

For other types of doped oxides as well as for porous oxide, there have not been any published studies yet on the properties of potential Cu diffusion barriers. Preliminary work on the diffusion of Ta and Cu into porous Si oxide indicates that the behavior is a strong function of the ambient in which the diffusion takes place.[192]

6.3 Cu/POLYMER BARRIERS

The studies of the diffusion of Cu into polymers, and suitable barriers to prevent this diffusion and assure strong adhesion, are less well developed than for the Cu/SiO_2 system. Moreover, it is likely that in comparison to SiO_2, the larger number of potential polymer ILD materials will bring with it a much wider range of Cu/barrier/ILD phenomena.

Cu is known to adhere poorly to non-fluorinated polymers such as polyimide.[73] Transition metals such as Ta and Cr can act as adhesion layers, whereby Ta yields a somewhat stronger bond to the polymer than Cr. No evidence for reaction between Cu/Ta or diffusion of Cu into Ta was observed after annealing at 500°C for one hour. The metal/polymer interaction is strong enough to withstand Cu CMP for fabricating damascene structures. PECVD Si_3N_4 is a good insulating barrier on top of Cu, and it also provides a strong bond between different layers of polyimide.[73]

Adhesion issues are compounded for Cu on fluorinated polymers such as Teflon (PTFE) and tetrafluoroethylene-hexafluoropropylene copolymer (FEP),[193] Teflon 1600[194,195] and FLARE 1.0.[196,197] Again Cu is generally not reactive towards the polymer, but potential barrier metals are very reactive and cause a rather weak and brittle bond to appear at the barrier/polymer interface. The strength of this bond does depend on the nature of the polymer, being stronger for FEP than for PTFE.[193] The nature of the metal/polymer interaction has been examined with XPS. For Cu on FLARE 1.0, no Cu-F bonding is observed, whereas Ti on FLARE 1.0 causes defluorination with subsequent formation of Ti-C, Ti-O, and Ti-F bonds.[196]

An increase in the barrier/polymer bond strength can be achieved if bonds other than metal-F can be promoted at the interface. This can be realized by a plasma treatment of the fluorinated polymer before metal deposition.[194,196–198] For the direct deposition of Cu onto Teflon, Shi et al. found[194] that treatment in a H_2 plasma was most efficient in eliminating fluorine, whereas treatment in an O_2 or N_2 plasma increased the adhesion of the Cu, presumably because some Cu-O and Cu-N bonding occurs at the interface. On the other hand, Du et al.[197] found no reactivity for Cu on FLARE 1.0 as deposited or treated in O_2, N_2, or Ar plasmas.

Ar plasma treatment of parylene-f before deposition of Ta leads to a reduction of the Ta-F interaction and an increase of the Ta-C interaction at the interface.[198]

Very little has been reported yet regarding the characterization of Cu/polymer ILD interactions in terms of Cu diffusion and electrical performance. In one investigation, the behavior of a poly-arylene-ether (Low-*k* 2000 PAE, Schumacher), a fluorinated polyimide (FPI-136M, DuPont), and BCB (Cyclotene 5021, Dow) under bias temperature stress was examined.[199] These experiments were performed on metal/ILD capacitor test structures in N_2 at 150-275°C and electric fields of 0.1–1.0 MV/cm for one hour. The ILDs were sandwiched between 50-nm oxide layers to prevent electron/hole injection from the gate and to provide a stable interface at the Si substrate. The main results were that Cu^+ ions drift much more easily into PAE and FPI than into BCB and that a 75-nm thick silicon nitride layer can prevent this drift.

7

CURRENT PRACTICE

7.1 OVERVIEW

In previous chapters we gave a broad general discussion of the steps for producing copper damascene interconnect structures with the aim of putting related issues in perspective. Now we will revisit some of these issues and highlight details of the practice preferred at present in implementing this type of process in production. Figure 49 outlines the essential steps of the process sequence.

The individual steps we will focus on specifically are the precleaning of the metal inside vias before barrier deposition, deposition of an adhesion/diffusion barrier for Cu, and Cu deposition itself. The latter will include deposition of a Cu seed layer for ECP either by IMP or by CVD, and damascene filling by ECP or CVD. We will not examine any further the patterning of the dielectric and the planarization of the metal, although in both areas process optimization is on-going. This applies in particular to the formation of dual-damascene structures in the ILD, as aspect ratios become larger in SiO_2, and as ILDs with lower k are being introduced. Also note that the examples we will give involve mostly Cu with undoped SiO_2 as an ILD. This is the present stage of production, whereas the use of low-k ILDs is in the development phase. We will close this chapter with an outlook on future directions.

7.2 PRECLEAN

As pointed out earlier, at the end of the via formation, the Cu in the underlying metal layer will be exposed to an oxidizing atmosphere. This will cause formation of copper oxide (Cu_xO), which must be removed prior to the following barrier/metal deposition to assure low via resistance.

One common method for Cu_xO removal is by physical sputtering with Ar^+ ions although, as is always the case with physical sputtering, the products are not really volatile, which may pose problems in cleaning deep features by redepositing sputtered material onto the sidewall.

Another method to remove copper oxide is by reactive preclean with a hydrogen plasma.[200] Note that reduction of copper oxide by molecular hydrogen is

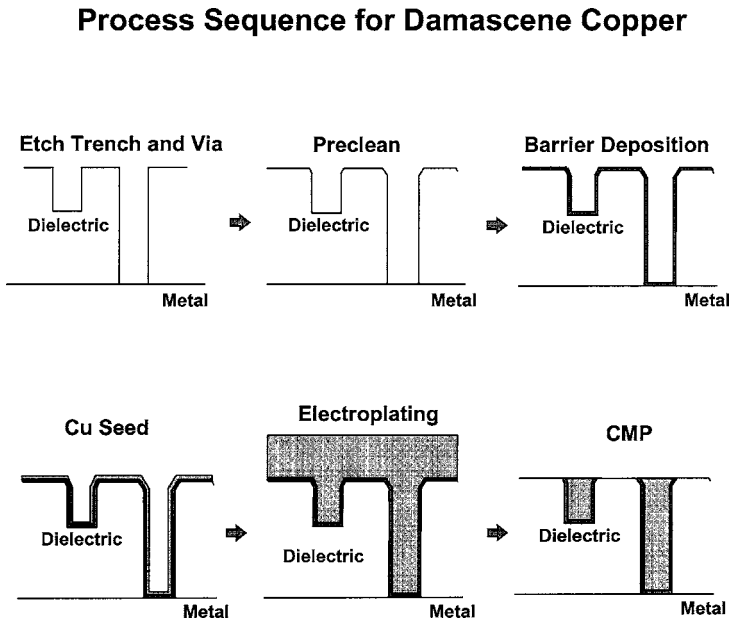


Figure 49 Process sequence for fabricating Cu damascene interconnect structure.

favored only weakly, but reduction by atomic hydrogen is favored strongly, on thermodynamic grounds:[201]

$$\begin{array}{lcll} Cu_2O + H_2 & \rightarrow & 2\,Cu + H_2O\,(gas) & \Delta G = -67\ kJ/mole \\ CuO\ + H_2 & \rightarrow & Cu + H_2O\,(gas) & -79 \\ Cu_2O + 2\,H & \rightarrow & 2\,Cu + H_2O\,(gas) & -501 \\ CuO\ + 2\,H & \rightarrow & Cu + H_2O\,(gas) & -514. \end{array} \tag{21}$$

In (21) ΔG denotes the Gibbs free energy of reaction. Reduction of mixed Cu oxides should behave similarly. Thus, given that the plasma functions here as a source of H atoms, the reaction at the Cu_xO/Cu interface is expected to be rapid and limited only by diffusional transport of H atoms.

A versatile process for etch residue and Cu_xO removal is an Ar plasma etch followed by a reactive preclean which combines the physical actions (sputtering by Ar^+ ions) and the chemical actions (reduction of Cu_xO by H atoms).[200] The sputtering by Ar^+ ions assists in the removal of reaction products and also allows to introduce tapering of the top corners in the ILD features (Fig. 49). The latter can be used to tailor the via/trench profile in order to facilitate conformal barrier coating and better via filling by the copper. The tapering of the top corners of the

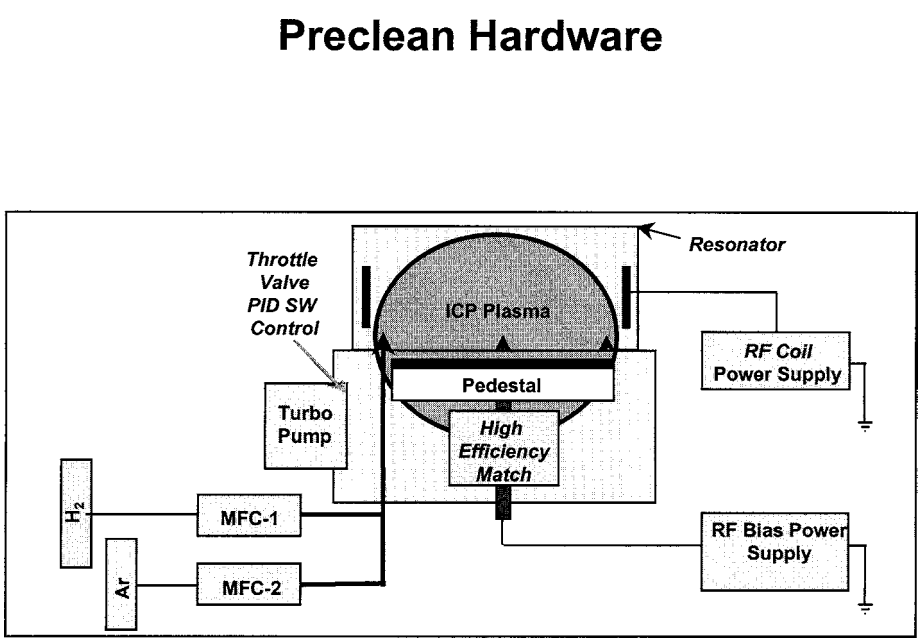


Figure 50 Example of reactor used for precleaning.

SiO_2 is due to the well-known maximum in the sputtering yield as a function of the incident angle of the ions (Ref. [7], Chapter 1).

A typical reactor used for precleaning is illustrated in Fig. 50. It can be operated in single mode (H_2 or Ar, alone) or in dual mode (Ar and H_2 sequentially). It also allows for independent control of the plasma power (plasma density) and the wafer bias (ion bombardment at the wafer).

An example of the effect of an H_2 plasma preclean on copper oxide is shown in Fig. 51. The sample was ECP Cu which had been polished by CMP, exposed to Si nitride barrier etch chemistry, precleaned and then capped with a 25-nm Cu layer. Fig. 51 displays secondary ion mass spectrometry (SIMS) analysis of sample depth profiles taken after various periods of precleaning treatment. The gradual reduction of the oxygen peak from Cu_xO by almost two orders of magnitude is apparent.

The H_2 plasma preclean process is applicable in principle to high aspect ratio structures and to low-*k* ILDs. However, it should be pointed out that the above data were taken on a blanket substrate. In addition, via cleaning may be more difficult if the material at the bottom of the vias is something more complex than Cu_xO, as was discussed in Sec. 5.3.5.

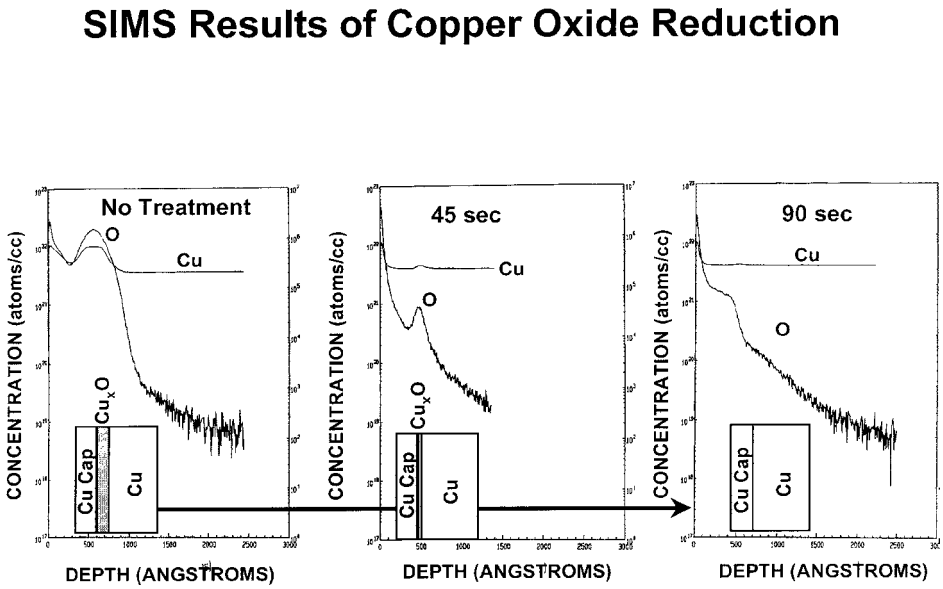


Figure 51 Time-lapsed SIMS depth profiles showing Cu_xO reduction by hydrogen preclean.

7.3 BARRIER LAYERS

In Chapter 6 we gave a general discussion of requirements on a barrier layer between Cu and the ILD. To recap, the barrier must prevent Cu diffusion into the ILD and must assure mechanical stability (good adhesion) between the Cu and ILD. Furthermore, a barrier layer must be thin, conformal, and with low electrical resistivity. Deposition should be at a low temperature, and producing few particles. The barrier must be compatible with CMP of Cu and with Cu deposition by electrochemical plating.

We also noted in Sec. 3.3 the advantages of using sputter deposition in combination with post-ionization, as realized with a hollow cathode magnetron[57,58] source or an ion metal plasma (IMP) source[202] (see Figs. 20–22). The main points of these setups are the increased plasma density, leading to a substantial fraction of the sputtered metal atoms being ionized, and the variable bias applied at the wafer. In an example of IPVD of Ta, up to 85% of the Ta flux was due to ions.[203] Somewhat lower but still significant ion fractions were achieved in the IPVD of TiN.[204]

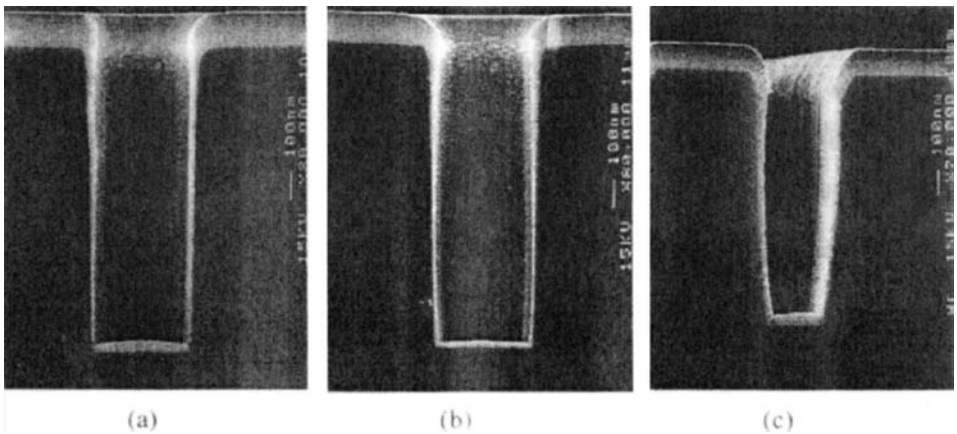


Figure 52 Effect of wafer bias on conformality of IMP-deposited TaN: a) via without bias; b) via with bias; c) trench with bias.[205]

The wafer bias, in conjunction with the gas pressure, allows one to modify the ion energy and the ion directionality at the substrate. These two factors determine how the ion fluxes deposit onto the bottoms and sidewalls of vias and trenches. A higher Ar ion flux at the bottom increases re-sputtering of deposited barrier material and therefore causes redistribution onto the sidewalls. At the same time, some preferential re-sputtering near the top corners occurs, similar to the tapering of ILD features mentioned above in Sec. 7.2 on precleaning. Both effects tend to promote more conformal coating of the via/trench with barrier material (Fig. 19). A vivid example is shown in Figs. 52 and 53 for a Ta-nitride barrier.[205] In Fig. 52 one can see the improved barrier conformality in an entire via when wafer bias is used (note the reduced barrier layer thickness at the bottom of the via). Fig. 53 shows a magnified comparison view of the Ta-nitride coverage around the bottom corners of vias with 0.25–0.3-μm width and 4–4.8 aspect ratio. Without wafer bias, the film thickness at the bottom of the trench is more than twice the thickness on the sidewall whereas with wafer bias the layer on the sidewall is even thicker than at the bottom.

The trade-off to be made between electrical and diffusion barrier properties is illustrated in Fig. 54 for Ta-nitride.[205,206] In Ref. [205], Ta-nitride was deposited by IMP on Si oxide for a test structure as shown earlier in Fig. 48, whereas in Ref. [206], Ta-nitride was deposited by DC magnetron sputtering onto Si. The deposition conditions strongly affect the material composition and microstructure. The process regime of choice is indicated by the N_2 flow yielding optimal barrier properties (amorphous Ta-nitride of approximate composition Ta_2N) and accept-

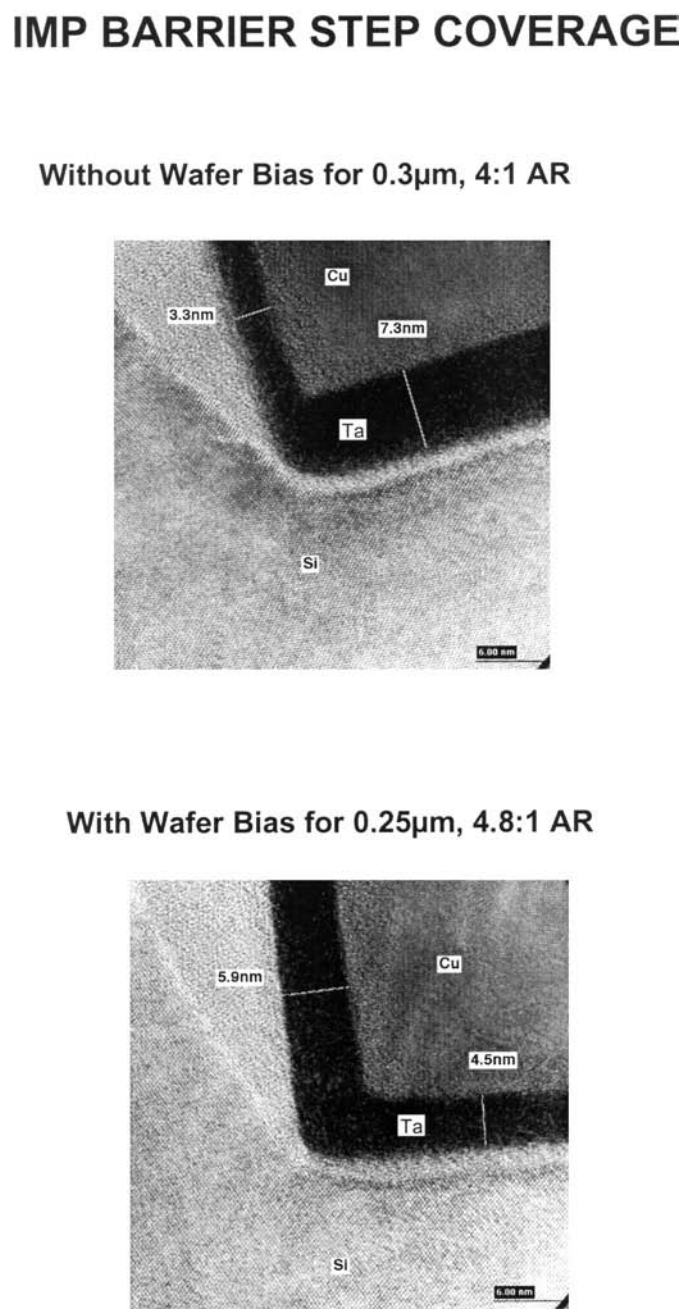


Figure 53 Effect of wafer bias on conformality of IMP-deposited TaN: bottom corner of trench.

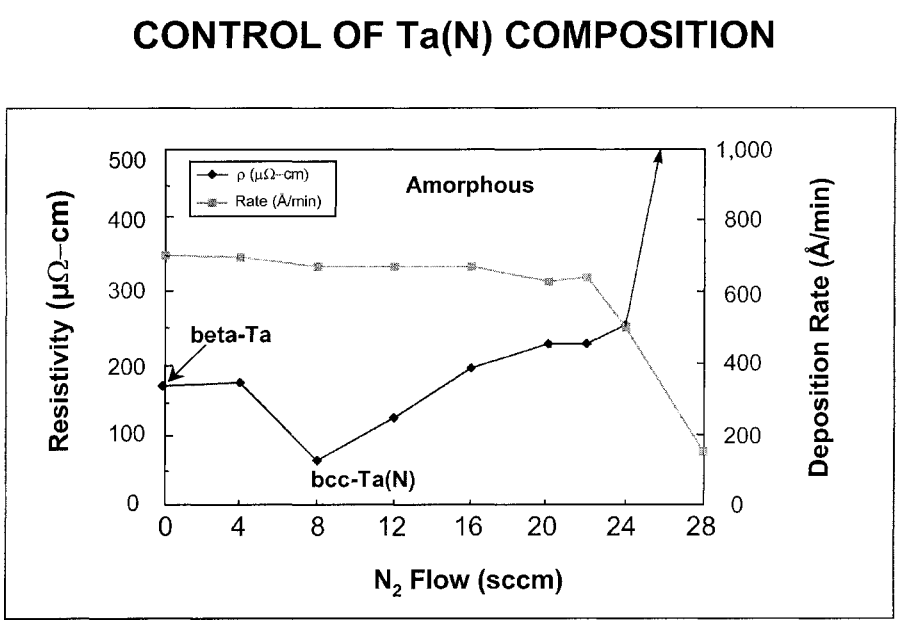


Figure 54 Properties of IMP-deposited TaN: Electrical resistivity and deposition rate vs. N_2 flow.

able electrical resistivity. In fact, the best Ta-nitride barrier has only a slightly higher resistivity than pure Ta (see below). On the other hand, the material with the lowest resitivity (bcc-Ta) contains only a small amount of N and turns out not to be a good barrier. When the stoichiometry of the Ta-nitride approaches TaN at the highest N_2 flow rates, the resistivity increases very rapidly.

Electrical test results for the performance of different IMP-deposited materials as Cu diffusion barriers are shown in Figs. 55 and 56. Figure 55 presents a general example of leakage current versus time through a capacitor test structure (see Fig. 48) under bias temperature stress (BTS) conditions (electrical field of 2 MV/cm across the oxide ILD, temperature of 275°C). Failure is identified with a leakage current of 10^{-4} A. 20 capacitors were tested in each case, and the cumulative probability distribution of the time to failure is plotted in Fig. 56. Ta-nitride (with the amorphous structure noted above) is clearly the best diffusion barrier, followed by Ta, and then by PVD TiN. These findings are consistent with recent results combining C-V and BTS measurements[206] and with earlier results involving the thermal annealing of Cu/barrier/Si[207,208] and Cu/barrier/silicon oxide samples.[209]

Ta and Ta-nitride also exhibit different surface morphologies (Fig. 57). Atomic force microscopy (AFM) reveals that for a fixed film thickness of 25 nm of

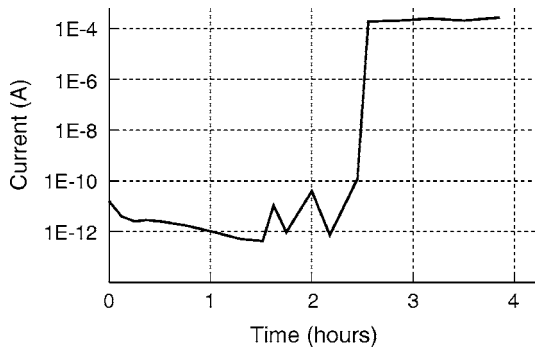


Figure 55 Typical leakage current through test capacitor vs. time.

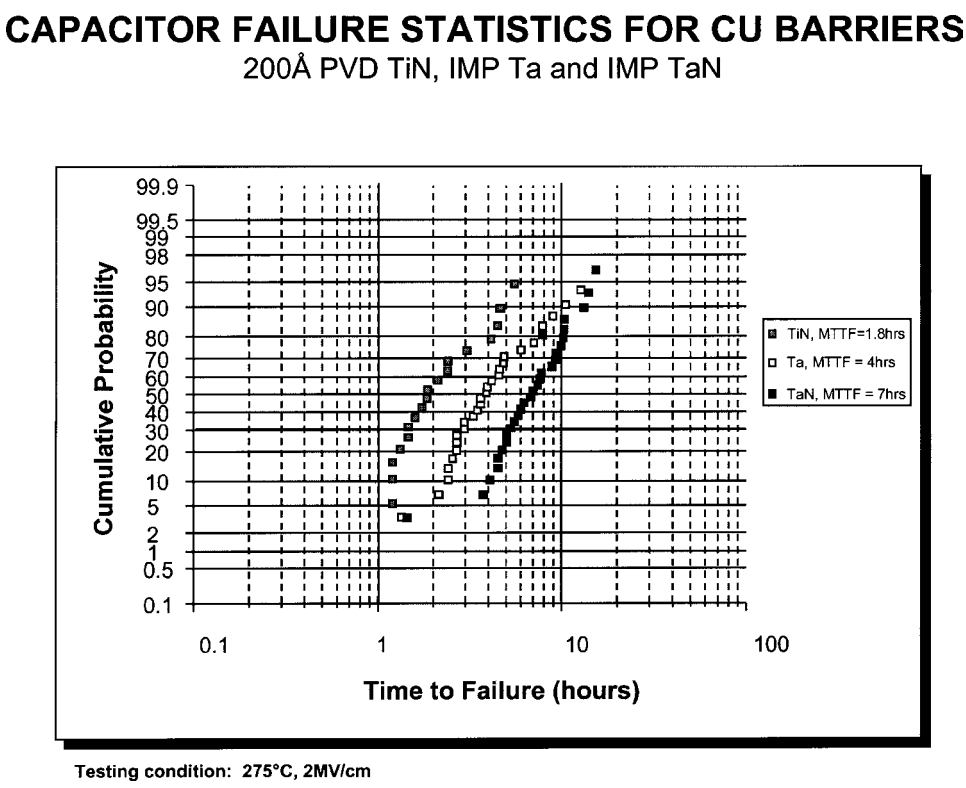


Figure 56 Mean times to failure for 20 nm TiN, Ta, and TaN barriers in bias temperature stress (BTS) tests. Test conditions: 275°C, 2 MV/cm.

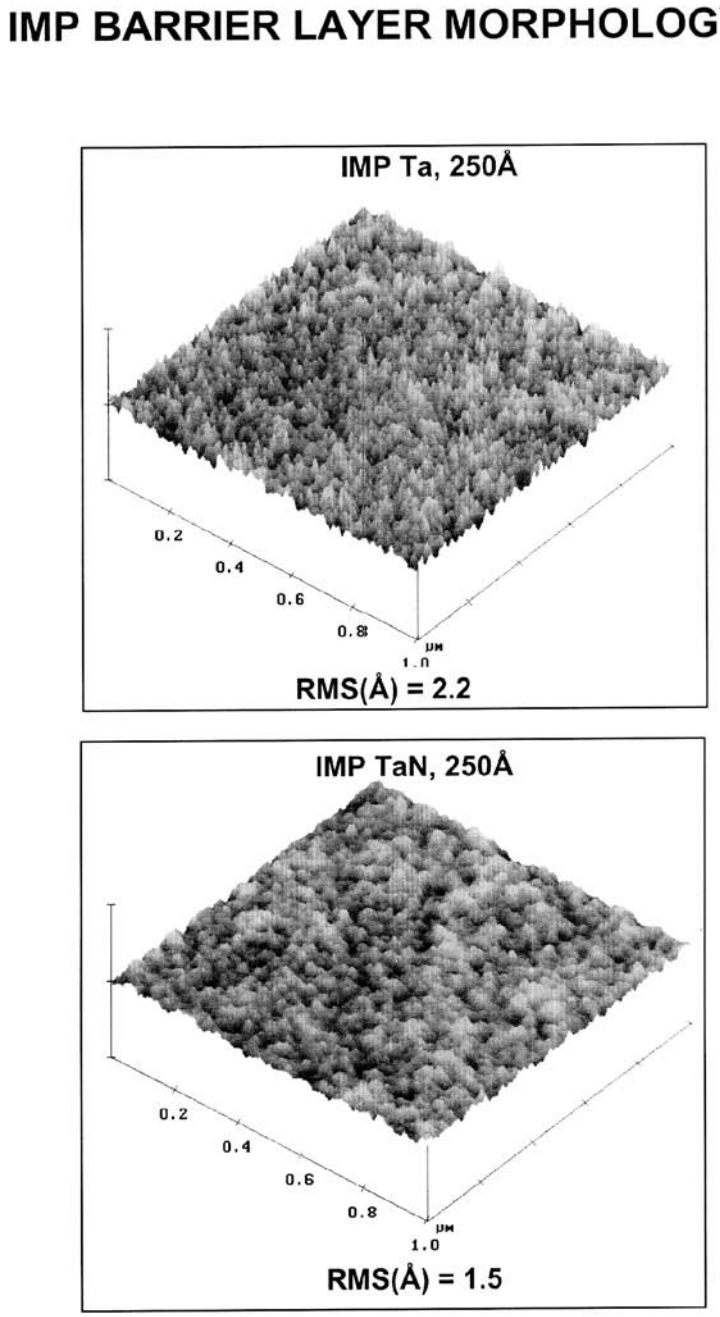


Figure 57 Atomic force microscope (AFM) measurements of surface morphology of IMP Ta and TaN.

IMP-deposited Ta or Ta-nitride, the Ta-nitride is smoother than the Ta. This morphology plays an important role in how the Cu seed layer, and subsequently the Cu metallization, grows on top of the barrier, as will be explained further in the following section. The advantages of the individual Ta and TaN film properties have been incorporated into a Ta/TaN/Ta graded structure which has been demonstrated to have better electromigration resistance.[267]

7.4 COPPER FILL METHODS

Electroplating is the Cu deposition method widely adopted in the industry for implementing Cu interconnect technology. However, there have been recent developments in Cu CVD as well.

In the context of the damascene approach to patterning, deposition of Cu by ECP must be able to fill vias and trenches with metal without voids. An important point to note is that Cu electroplated directly onto any one of the barrier materials discussed above generally leads to a poorly adhering film,[210] although efforts are underway to find plating conditions which will circumvent this problem. Successful electroplating of Cu requires that a Cu seed layer be deposited first by a method other than ECP, providing good adhesion to both the barrier and the ECP Cu. The Cu seed layer must also be conformal and smooth, or else it may give rise to voids in the ECP Cu film.[210,211] In addition, the seed layer must have low resistivity, optimal crystalline orientation, and low contamination. The overall structure and texture of the seed layer has a strong influence on the microstructure of the ECP Cu film.

The preferred method for depositing the Cu seed layer is IMP at present. This produces conformal films as shown in Fig. 58. Also note that the same benefit of improved conformality accrues here from biasing the sample, as was described above for the barrier deposition.[205] It is important to keep the temperature low in this process. Elevated temperature leads to increased de-wetting of the Cu and yields significant cluster growth rather than a smooth seed layer (Fig. 59). This can impede the formation of a continuous film in the subsequent Cu ECP and can give rise to voids in the Cu film. These problems have led to the incorporation of subzero-degree cooling hardware which is used to further lower the wafer temperature (Fig. 59).

The crystallographic texture of the Cu seed layer is influenced strongly by the underlying barrier layer, as is illustrated in Fig. 60. This texture, in turn, determines the microstructure of the ECP Cu deposited onto the seed layer.[212] Note that a (111) orientation of the Cu is generally preferred because it tends to give the most reliable films.

Turning now to the deposition of Cu by ECP, specifically for the purpose of trench and via filling in damascene structures, let us note that the general charac-

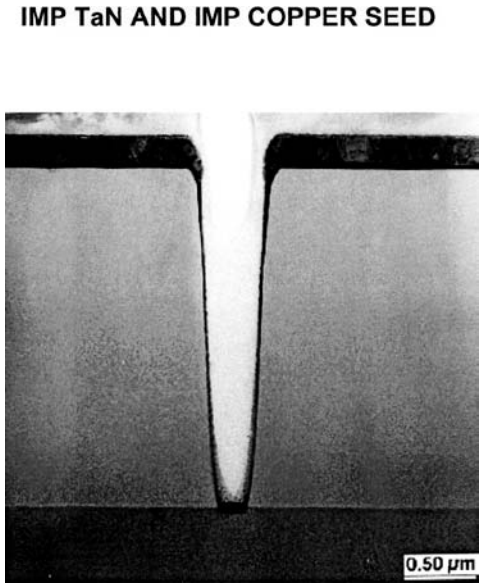


Figure 58 TaN barrier/Cu seed layer deposition by IMP.

teristics of the ECP process were described above in Sec. 3.2.2. The main points to keep in mind are that the uniformity of the deposit depends on the state of the seed layer and on diffusional mass transport and the electric current distribution on the feature scale. Modeling shows that convection is not important on the feature scale.[213]

Practical ECP baths typically contain not only the pure plating electrolyte solution as such but also certain proprietary organic additives,[211,214] traditionally referred to as brighteners and levelers. The role of these additives will be examined shortly. Let us point out first here that because of these organics, there was a concern in the early stages of the application of Cu ECP to IC manufacturing that some of these compounds might find their way into the Cu. Such impurities could be expected to increase the electrical resistivity of Cu, thus reducing its advantage relative to Al. However, these concerns have turned out to be unfounded. As Fig. 61[268] demonstrates, the resistivity of electroplated Cu is comparable to that of sputtered Cu as deposited, and annealing brings the resistivity close to the bulk value for Cu. This, in turn, indicates that there is minimal incorporation of impurities into the ECP Cu.

With the proper seed layer, it is possible to fill completely features with quite high aspect ratio.[211,214] An example of filled trenches is shown in Fig. 62. Filling has been demonstrated up to an aspect ratio of about five if the plating bath contains the appropriate additives.[211] Without additives, plating is generally non-uniform

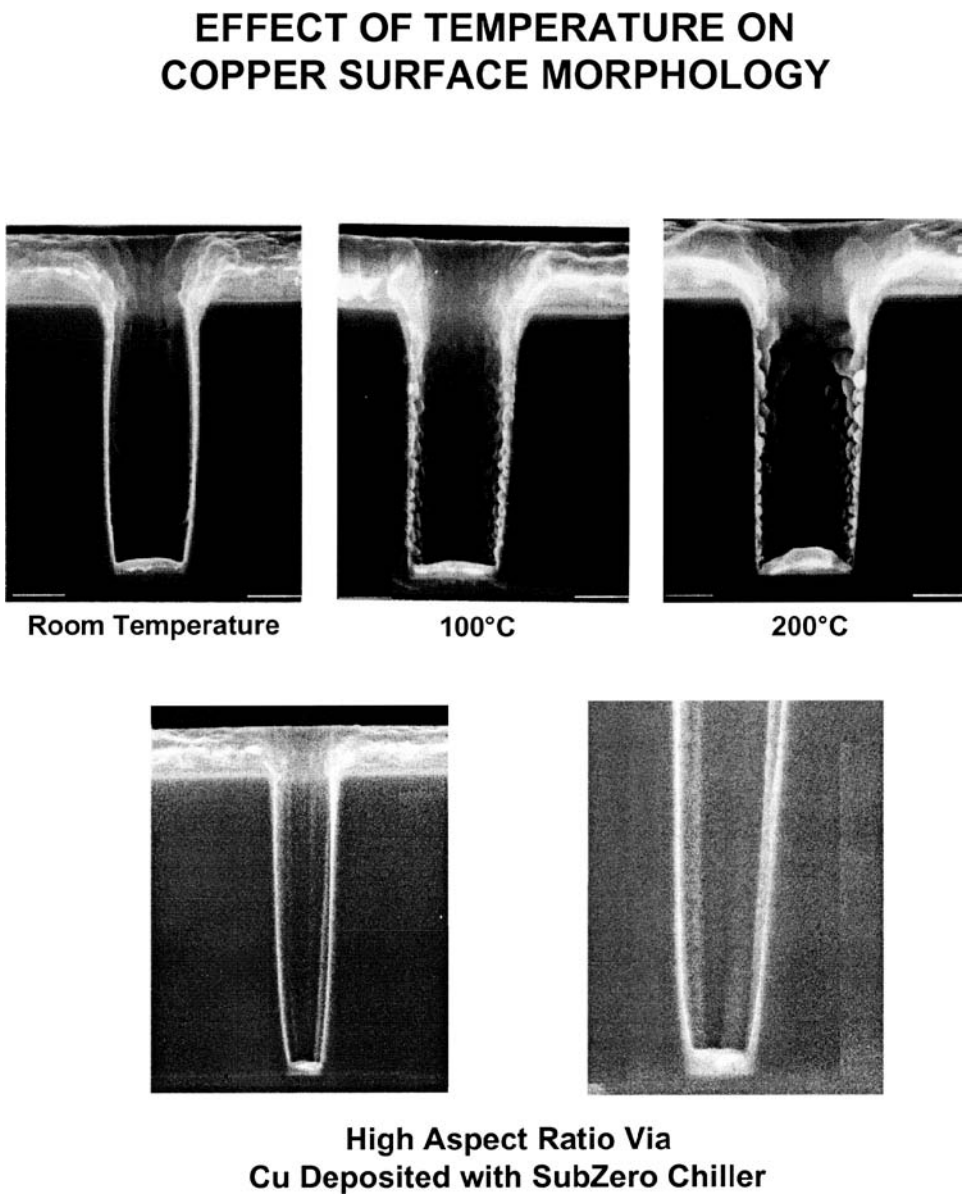


Figure 59 Effect of wafer temperature on surface morphology of Cu deposited into vias by IMP. Note use of subzero-degree chiller for lower temperature.

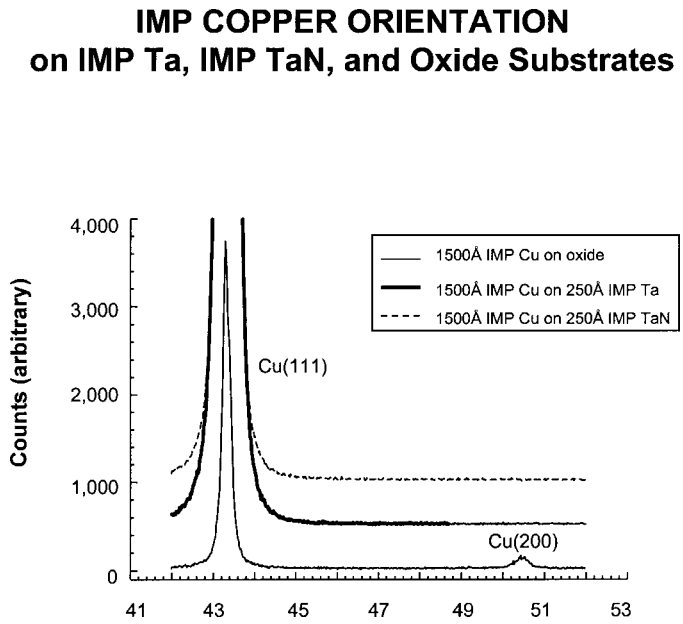


Figure 60 Crystallographic texture of IMP Cu.

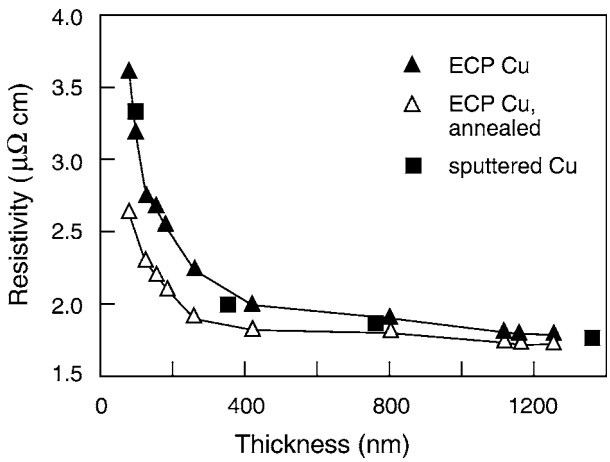


Figure 61 Electrical resistivity of sputtered and electroplated Cu.[268]

inside a trench and produces the highest deposition rate near the top corners of the feature.[210,211] As in normal sputter deposition, this causes the trench to be pinched off at the top, such that a void is left inside the trench. Voids may extend all the

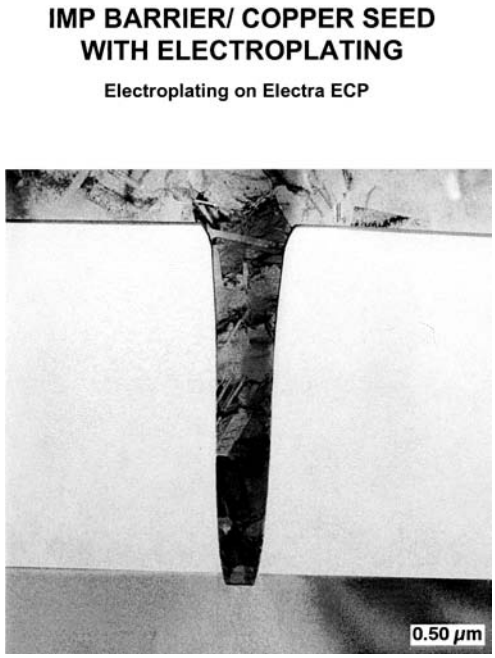


Figure 62 Grain structure of Cu electroplated into vias. Note excellent via filling and large Cu grains.

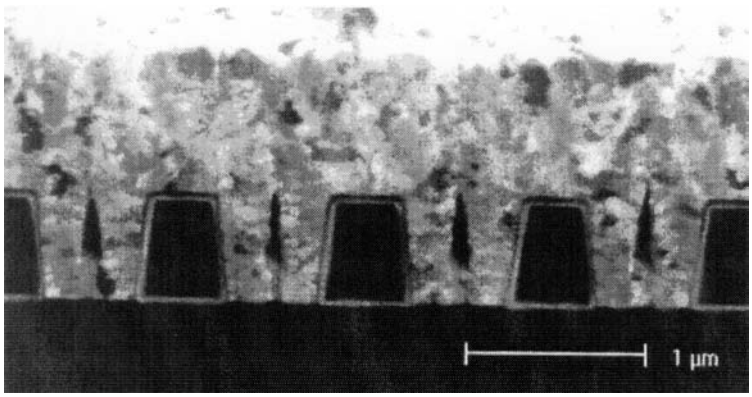


Figure 63 Voids formed in trenches when electroplating Cu under non-conformal conditions.[210]

way up a trench if the aspect ratio is not too large (Fig. 63),[210] or they may be confined to the bottom of the trench.[211] Such voids generally cannot be removed by annealing after ECP.

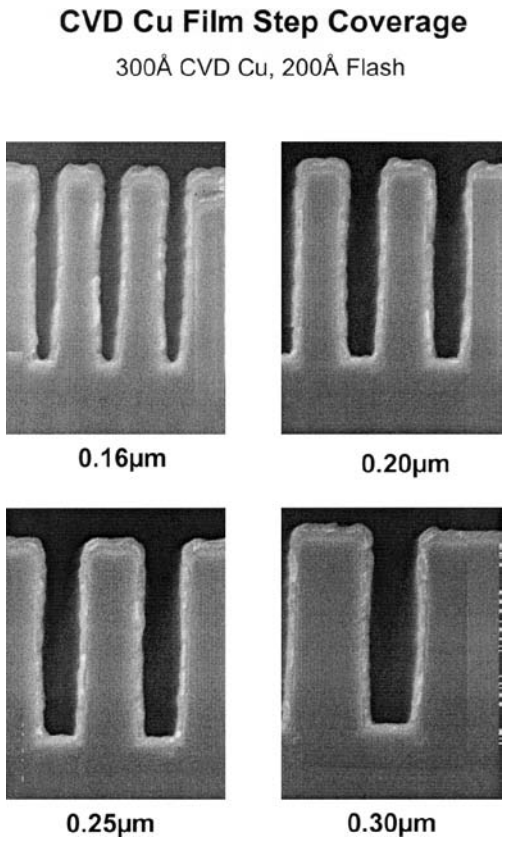


Figure 64 Step coverage achieved in chemical vapor deposition of Cu.

One of the essential roles of the organic additives is to facilitate the complete filling of vias and trenches with Cu. Under optimal conditions, features in fact are filled "from the bottom up" without leaving a void.[211] This comes about because inside a feature, the deposition rate is much larger at the bottom than on the sidewalls. How this occurs is still under investigation. It is thought that a major function of the organic additives is to inhibit deposition. Since they are present in the plating bath at very low concentration, they may be depleted significantly inside a high-aspect-ratio feature because of mass transfer limitations.[213] Therefore, their inhibiting action would be largest near the top of a feature and diminish gradually deeper into the feature.

The organic additives also have a large and surprising influence on the microstructure of the electroplated Cu. With additives, Cu films are reflective and fine-grained as deposited. After deposition, the Cu recrystallizes *at room tempera-*

Figure 65 Via fill achieved in chemical vapor deposition of Cu.

ture over a period of hours to days or weeks to form quite large grains (see Fig. 62 and also Refs. [214–216]). The phenomenon is sometimes also referred to as room temperature self-annealing. This grain growth is the reason for the observed reduction in resistivity.[214] The effect has been known for some time in the literature[217] but has been taken advantage of only recently, in connection with the ECP of Cu for producing interconnects.

The room temperature recrystallization of ECP Cu has been investigated in terms of its dependence on the sample geometry and the plating bath characteristics. For example, with trenches of fixed 0.5-µm width, the recrystallization is faster when the trenches are closer together. Also, the recrystallization appears to start at the upper corners of a trench.[215,216] As an explanation, it has been suggested that higher local stress and a higher local dislocation density at these top corners initiate the recrystallization.[215,216] In addition, the kinetics of recrystallization depend on the concentration of the additives. For deposition without additives, no recrystallization is observed.[214,216] The rate of recrystallization increases upon addition of additives, and there is a concentration of additives at which the transformation takes place fastest.[214] The current density and the plating bath temperature during deposition also have an effect on the recrystallization kinetics.[214]

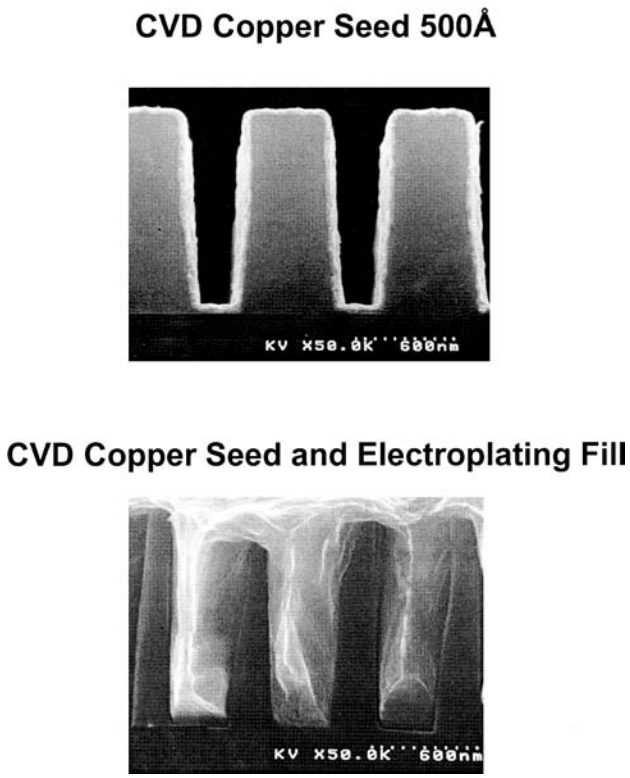


Figure 66 Cu seed layer deposition by CVD and subsequent trench filling by Cu ECP.

Work on Cu CVD is also ongoing, both for trench and via filling and for the deposition of ECP seed layers. The most widely used process is the one involving the precursor CupraSelect,[22] which is a trade name for (hfac)Cu^{I}(tmvs) where hfac stands for hexafluoroacetylacetonate and tmvs for trimethylvinylsilane (see Sec. 3.2.1 and Fig. 12). Key parameters for the deposition rate are the wafer temperature and the precursor flow rate. Typically, the deposition rate increases with increasing temperature and flow rate. Cu coverage can be highly conformal, even into 0.16-μm wide trenches with an aspect ratio of about 9:1 (Fig. 64). In a similar vein, it is also possible to achieve excellent via filling (Fig. 65). Moreover, the high conformality of the deposited films is useful in the formation of Cu seed layers for Cu electroplating (Fig. 66). A key inhibitor to implementing CVD Cu is the poor adhesion property to the underlying barrier layer. Another area of concern is the electromigration properties of the finer-grained material in comparison with electroplated Cu.[265]

7.5 FUTURE DIRECTIONS

Intense work in all areas related to Cu interconnections continues, with a view to push the technology towards ever smaller features sizes and ever larger numbers of interconnect layers. In this final section, we will touch upon some recent developments pointing to the future, especially in the areas of Cu deposition methods, low-*k* dielectrics, and barrier materials.

We note that even though at this point electroplating of Cu has emerged as the preferred deposition method, at least in the short term, the ultimate limitation of Cu ECP has not been determined yet, particularly regarding trench and via filling capability. One limiting factor may be that in the traditional DC plating approach, deposition is sometimes not completely conformal, producing a slightly thicker layer at the top of a feature.[211] This increases the possibility of forming a void inside the trench or via. It is unclear whether this effect can be obviated by tailoring the intial profile of the feature, e.g., by rounding off the top corners (see Fig. 62). On the other hand, the reverse-pulse plating approach appears promising in circumventing the problem.[41,211,218] The idea is, by pulsing with forward and reversed voltage, to alternate between electrochemical deposition and removal. This should improve film conformality because removal during the reverse-bias periods should be faster at precisely those locations where during forward bias deposition was faster. Pulse plating could also be used to alter the balance between mass transfer and current density effects compared to the steady state DC plating situation.

Another point requiring further elucidation is the influence of organic additives in Cu ECP. We pointed out above their marked effect on the microstructure of the deposited Cu films, in particular how they control the room temperature recrystallization (see also[219–222]). The mechanism of how this occurs is unclear at present. An in-situ TEM study suggests that impurities impede normal grain growth and that grains growing abnormally during recrystallization reject impurities.[221] Additives may also affect the texture of the films, which in turn may depend on the feature geometry and on the underlying barrier layer. A stronger (111) texture has been linked to improved electromigration resistance.[219]

A question closely related to the limits of Cu ECP and also to the IPVD of metal layers is at what point, and for what purpose, Cu CVD will be needed. At present, one advantage of Cu CVD over ECP is the more uniform conformality over the bottom and sidewalls of features. This may become significant at very high aspect ratios. Developments in Cu CVD include optimization of processes using common precursors such as $Cu^{II}(hfac)_2$ and hydrogen[223] and $(hfac)Cu^{I}(tmvs)$.[224,225]. New precursors of the form $(hfac)Cu^{I}(L)$ are also being evaluated.[226] On the other hand, new developments in Cu PVD involve using a self-ionized plasma (SIP) to improve step coverage.[266]

In the interlayer dielectric area, the deposition of a porous (poly-arylether) polymer with a dielectric constant k of about 1.8 has been described recently.[227] There have also been several recent reports on the plasma-enhanced CVD of fluorinated amorphous carbon from precursors of the form C_xF_y or C_xF_yH[228–230] or fluorinated aromatics.[251] The area of fluorinated amorphous carbon ILDs has been reviewed recently.[231] Furthermore, the interaction of fluorinated ILDs with Cu and barrier materials has received continued interest, specifically Cu/SiOF and Cu/W-N/SiOF[232] and Ta-N/*a*-C:F.[233] W-N was found to retard the interdiffusion of Cu into the SiOF and F into the Cu.[232] At the Ta-N/*a*-C:F, a strong interaction occurs, which manifests itself as defluorination of the *a*-C:F by the Ta-N accompanied by formation of TaF.[233] This could present a long-term stability problem for this system.

The development of new barrier materials and CVD deposition processes for barrier deposition has seen very significant activity. The goal in both cases is to relax barrier thickness requirements and to assure entirely conformal deposition even into very high aspect ratio features. Among the emerging materials are W-N deposited by CVD,[182,234,235] transition metal nitrides containing Si, for example WSiN,[183,236] TaSiN,[238] TiSiN,[175,236,237] and WBN.[236] Very recently, Ta stuffed with CeO_2 has been proposed as a barrier material.[239] The CeO_2 is said to occupy grain boundaries in the Ta, thus inhibiting diffusion through the metal. CVD processes for the more traditional metal nitrides are also under examination, including TiN[181,237] and TaN.[173,240,241]

The framework for implementing Cu and undoped SiO_2 (USG) in an integrated process technology can be seen from the reports mentioned in Chapter 1.[4–6] A new approach along the same lines, focusing on abrasive-free CMP of Cu has been presented recently by Yamaguchi et al.[261] In this process, W plugs were used for metal level 1, Cu with single damascene for metal levels 2–5, and Al for metal levels 6 and 7. The removal of the Cu/TiN metallization was done in two steps: an abrasive-free Cu CMP step which removes Cu only chemically, followed by a more conventional CMP step for removal of the barrier. This two-step combination allowed to minimize erosion and dishing and to eliminate residues from the W plugs. Post-CMP wet cleaning was also done in an abrasive-free manner.

In two recent papers from IBM, future developments combining Cu and a low-*k* dielectric have been outlined. In the first paper [4b], the integration of F-doped oxide (FSG) with Cu in a 0.18-μm technology has been described. Particular attention was paid to optimizing the deposition of the FSG for stable adhesion to the silicon nitride barrier layer and for stress control to minimize stress-induced voiding. The deposited FSG had a dielectric constant of 3.75. In order to maximize reliability, a dual FSG/USG dielectric layer was used, with the FSG extending to 20% below the bottom level of the trench. This architecture resulted in an improvement of about 6.5% in total capacitance compared to a USG dielectric. The process

is going to be incorporated in the Power4 microprocessor in combination with SOI front end technology for a total performance improvement of 40%.

In the second paper [4c], the integration of dual-damascene Cu with SiLK as the ILD for the 0.13-μm technology node has been demonstrated. For the pattering of the polymer ILD, a bi-layer hard mask without an embedded etch stop was chosen. The standard liner/seed deposition and Cu plating processes were found to be compatible with the organic ILD. Compared to Cu/USG, the Cu/SiLK system yielded an improvement in the normalized wire delay of 30%.

In summary, it seems fair to state that in all the different areas which are part of Cu interconnect technology, there is still ample room for process improvement and materials optimization along the lines described. This will, of course, be necessary in order to meet the demands of the continued decrease in device feature size and the increase in circuit complexity. On the other hand, new challenges in manufacturing may well emerge, since this process development will occur concurrently with the movement of the microelectronics industry from 200- to 300-mm wafer size.

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